

# 54F/74F181

## 4-Bit Arithmetic Logic Unit

### General Description

The 'F181 is a 4-bit Arithmetic logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations. It is 40% faster than the Schottky ALU and only consumes 30% as much power.

### Features

- Full lookahead for high-speed arithmetic operation on long words
- Guaranteed 4000V minimum ESD protection

**Ordering Code:** See Section 11

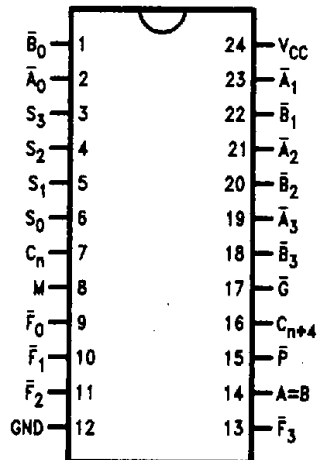
Commercial	Military	Package Number	Package Description
74F181PC		N24A	24-Lead (0.600" Wide) Molded Dual-In-Line
74F181SPC		N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
	54F181DM (Note 2)	J24A	24-Lead Ceramic Dual-In-Line
	54F181SDM (Note 2)	J24F	24-Lead (0.300") Ceramic Dual-In-Line
74F181SC (Note 1)		M24B	24-Lead (0.300") Molded Small Outline, JEDEC
	54F181FM (Note 2)	W24C	24-Lead Cerpack
	54F181LM (Note 2)	E28A	24-Lead Ceramic Leadless Chip Carrier, Type C

**Note 1:** Devices also available in 13" reel. Use suffix = SCX.

**Note 2:** Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

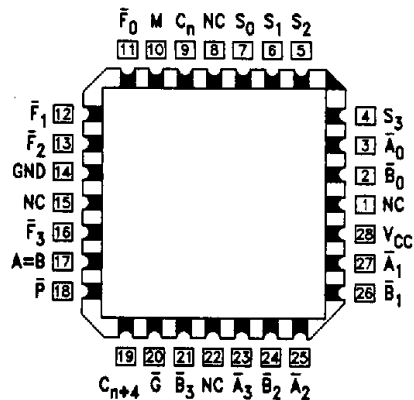
### Connection Diagrams

Pin Assignment  
for DIP, SOIC and Flatpak



TL/F/9491-1

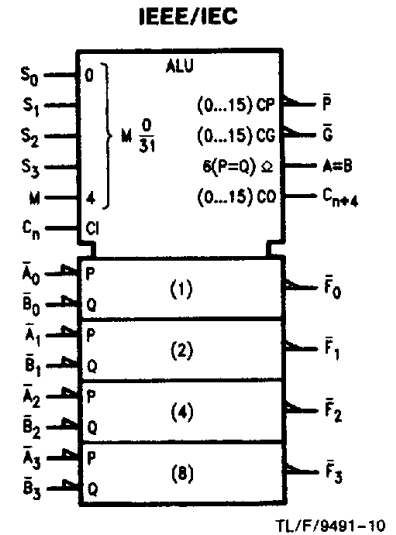
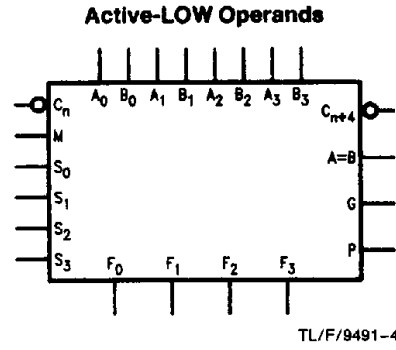
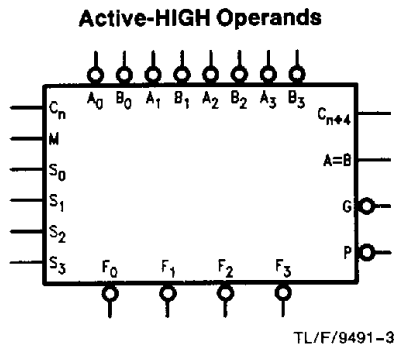
Pin Assignment  
for LCC



TL/F/9491-2

7

## Logic Symbols



### Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\bar{A}_0-\bar{A}_3$	A Operand Inputs (Active LOW)	1.0/3.0	20 $\mu$ A / -1.8 mA
$\bar{B}_0-\bar{B}_3$	B Operand Inputs (Active LOW)	1.0/3.0	20 $\mu$ A / -1.8 mA
$S_0-S_3$	Function Select Inputs	1.0/4.0	20 $\mu$ A / -2.4 mA
M	Mode Control Input	1.0/1.0	20 $\mu$ A / -0.6 mA
$C_n$	Carry Input	1.0/5.0	20 $\mu$ A / -3.0 mA
$\bar{F}_0-\bar{F}_3$	Function Outputs (Active LOW)	50/33.3	-1 mA / 20 mA
A = B	Comparator Output	OC*/33.3	* / 20 mA
$\bar{G}$	Carry Generate Output (Active LOW)	50/33.3	-1 mA / 20 mA
$\bar{P}$	Carry Propagate Output (Active LOW)	50/33.3	-1 mA / 20 mA
$C_{n+4}$	Carry Output	50/33.3	-1 mA / 20 mA

\*OC-Open Collector

## Functional Description

The 'F181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs ( $S_0-S_3$ ) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on Active HIGH or Active LOW operands. The Function Table lists these operations.

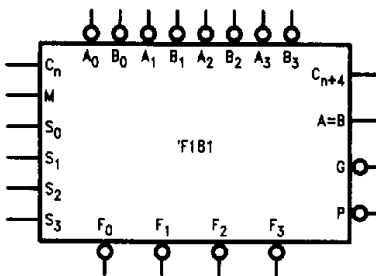
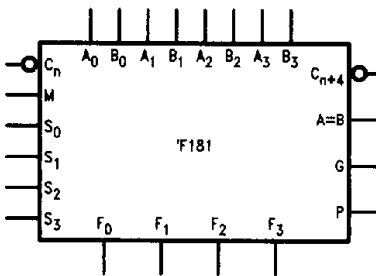
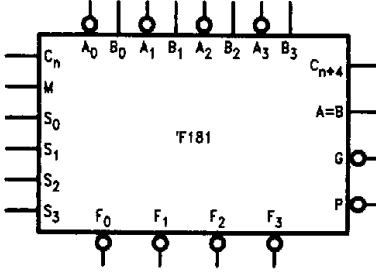
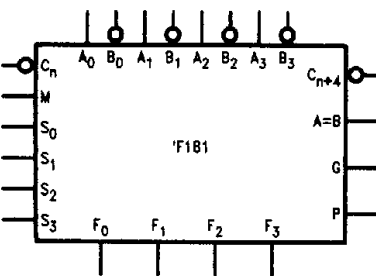
When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the  $C_{n+4}$  output, or for carry lookahead between packages using the signals  $\bar{P}$  (Carry Propagate) and  $\bar{G}$  (Carry Generate). In the Add mode,  $\bar{P}$  indicates that  $\bar{F}$  is 15 or more, while  $\bar{G}$  indicates that  $\bar{F}$  is 16 or more. In the Subtract mode  $\bar{P}$  indicates that  $\bar{F}$  is zero or less, while  $\bar{G}$  indicates that  $\bar{F}$  is less than zero.  $\bar{P}$  and  $\bar{G}$  are not affected by carry in. When speed requirements are not stringent, the 'F181 can be used in a simple Ripple Carry mode by connecting the Carry output ( $C_{n+4}$ ) signal to the Carry input ( $C_n$ ) of the next unit. For high speed operation the device is used in conjunction with a carry lookahead circuit. One carry lookahead package is required for

each group of four 'F181 devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.

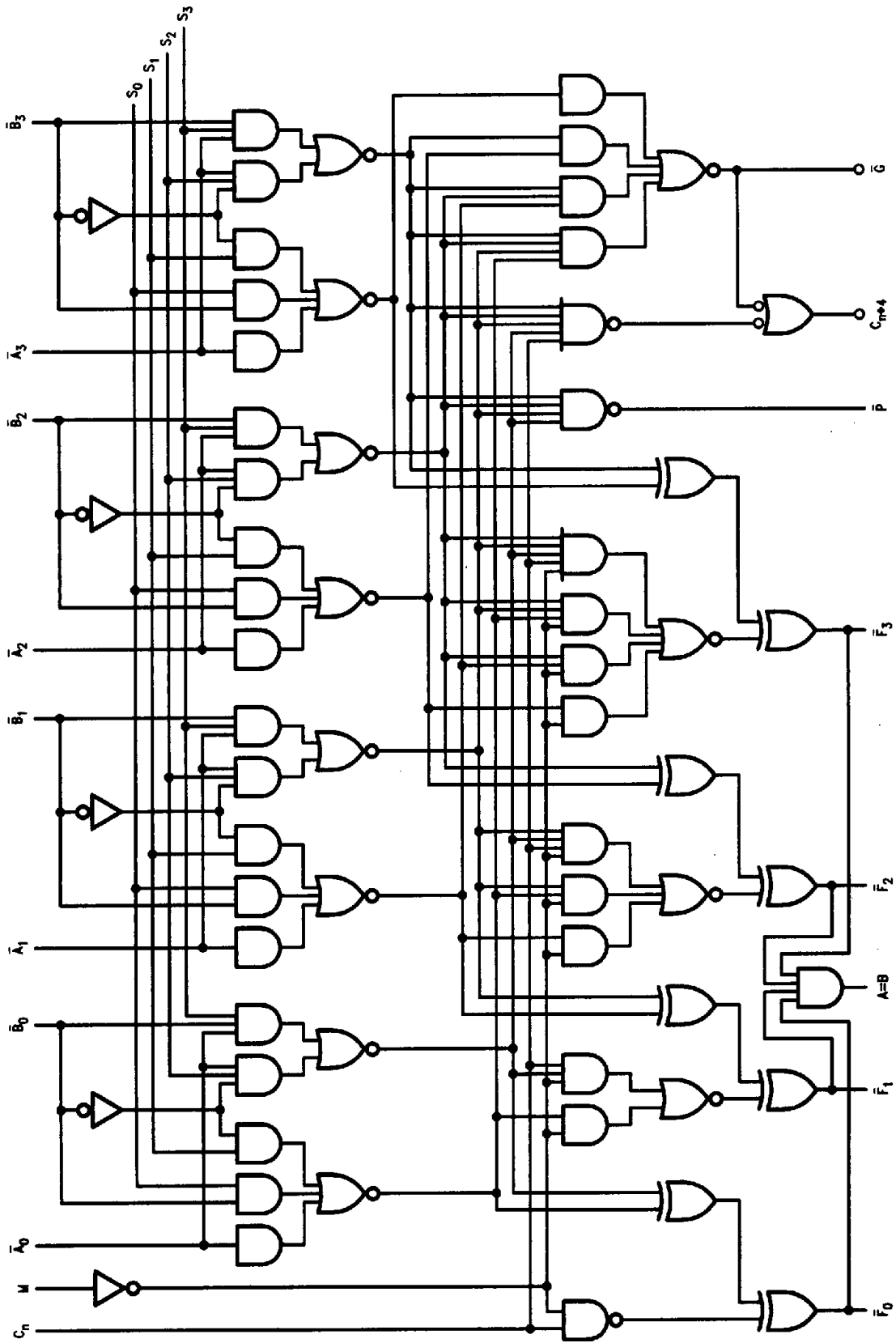
The A = B output from the device goes HIGH when all four  $\bar{F}$  outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the Subtract mode. The A = B output is open collector and can be wired AND with other A = B outputs to give a comparison for more than four bits. The A = B signal can also be used with the  $C_{n+4}$  signal to indicate  $A > B$  and  $A < B$ .

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHLH generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow. As indicated, this device can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

'F181 Operation Table

	S <sub>0</sub>	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	Logic (M = H)	Arithmetic (M = L, C <sub>0</sub> = Inactive)	Arithmetic (M = L, C <sub>0</sub> = Active)
 <p>a. All Input Data Inverted</p>	L	L	L	L	$\bar{A}$	A minus 1	A
	H	L	L	L	$\bar{A} \cdot \bar{B}$	A • B minus 1	A • B
	L	L	L	L	$\bar{A} + \bar{B}$	A • $\bar{B}$ minus 1	A • $\bar{B}$
	H	H	L	L	Logic "1"	minus 1 (2s comp.)	Zero
	L	L	H	L	$\overline{A + B}$	A plus (A + $\bar{B}$ )	A plus (A + $\bar{B}$ ) plus 1
	H	L	H	L	$\bar{B}$	A • B plus (A + $\bar{B}$ )	A • B plus (A + $\bar{B}$ ) plus 1
	L	H	H	L	$A \oplus \bar{B}$	A minus B minus 1	A minus B
	H	H	H	L	A + $\bar{B}$	A + $\bar{B}$	A + $\bar{B}$ plus 1
	L	L	L	H	$\bar{A} \cdot B$	A plus (A + B)	A plus (A + B) plus 1
	H	L	L	H	A $\oplus$ B	A plus B	A plus B plus 1
 <p>b. All Input Data True</p>	L	L	L	L	$\bar{A}$	A	A plus 1
	H	L	L	L	$\bar{A} + \bar{B}$	A + B	A + B plus 1
	L	H	L	L	$\bar{A} \cdot B$	A + $\bar{B}$	A + $\bar{B}$ plus 1
	H	H	L	L	Logic "0"	minus 1 (2s comp.)	Zero
	L	L	H	L	$\bar{A} \cdot \bar{B}$	A plus (A • $\bar{B}$ )	A plus A • $\bar{B}$ plus 1
	H	L	H	L	$\bar{B}$	A • $\bar{B}$ plus (A + B)	A • B plus (A + B) plus 1
	L	H	H	L	A $\oplus$ B	A minus B minus 1	A minus B
	H	H	H	L	A • $\bar{B}$	A • $\bar{B}$ minus 1	A • $\bar{B}$
	L	L	L	H	$\bar{A} + B$	A plus A • B	A plus A • B plus 1
	H	L	L	H	$\bar{A} \oplus \bar{B}$	A plus B	A plus B plus 1
 <p>c. A Input Data Inverted; B Input Data True</p>	L	L	L	L	$\bar{A}$	A minus 1	A
	H	L	L	L	$\bar{A} + \bar{B}$	A • $\bar{B}$ minus 1	A • B
	L	H	L	L	$\bar{A} \cdot \bar{B}$	A • B minus 1	A • B
	H	H	L	L	Logic "1"	minus 1 (2s comp.)	Zero
	L	L	H	L	$\bar{A} \cdot B$	A plus (A + B)	A plus (A + B) plus 1
	H	L	H	L	B	A • $\bar{B}$ plus (A + B)	A • $\bar{B}$ plus (A + B) plus 1
	L	H	H	L	A $\oplus$ B	A plus B	A plus B plus 1
	H	H	H	L	A + B	A + B	A + B plus 1
	L	L	L	H	$\overline{A + B}$	A plus (A + $\bar{B}$ )	A plus (A + $\bar{B}$ ) plus 1
	H	L	L	H	$\overline{A \oplus \bar{B}}$	A minus B minus 1	A minus B
 <p>d. A Input Data True; B Input Data Inverted</p>	L	L	L	L	$\bar{A}$	A	A plus 1
	H	L	L	L	$\bar{A} \cdot B$	A + $\bar{B}$	A + $\bar{B}$ plus 1
	L	H	L	L	$\bar{A} + \bar{B}$	A + B	A + B plus 1
	H	H	L	L	Logic "0"	minus 1 (2s comp.)	Zero
	L	L	H	L	$\bar{A} + B$	A plus A • B	A plus A • B plus 1
	H	L	H	L	B	A • B plus (A + $\bar{B}$ )	A • $\bar{B}$ plus (A + B) plus 1
	L	H	H	L	$\bar{A} \oplus \bar{B}$	A plus B	A plus B plus 1
	H	H	H	L	A • B	A • B minus 1	A • B
	L	L	L	H	$\bar{A} \cdot \bar{B}$	A plus A • $\bar{B}$	A plus A • $\bar{B}$ plus 1
	H	L	L	H	A $\oplus$ B	A minus B minus 1	A minus B

# Logic Diagram



TL/F/9491-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	-0.5V to V <sub>CC</sub>
Standard Output	-0.5V to +5.5V
TRI-STATE® Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)  
ESD Last Passing Voltage (Min) 4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.5 2.7		V	Min	I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.5 0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub> ( $\bar{F}_n, \bar{G}, \bar{P}, C_{n+4}$ )
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6 -1.8 -2.4 -3.0	mA	Max	V <sub>IN</sub> = 0.5V (M) V <sub>IN</sub> = 0.5V ( $\bar{A}_0, \bar{A}_1, \bar{A}_3, \bar{B}_0, \bar{B}_1, \bar{B}_3$ ) V <sub>IN</sub> = 0.5V (S <sub>n</sub> , $\bar{A}_2, \bar{B}_2$ ) V <sub>IN</sub> = 0.5V (C <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150	mA	Max	V <sub>OUT</sub> = 0V ( $\bar{F}_n, \bar{G}, \bar{P}, C_{n+4}$ )
I <sub>OHC</sub>	Open Collector, Output OFF Leakage Test			250	μA	Min	V <sub>O</sub> = V <sub>CC</sub> (A = B)
I <sub>CCH</sub>	Power Supply Current		43	65.0	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		43	65.0	mA	Max	V <sub>O</sub> = LOW

**AC Electrical Characteristics:** See Section 2 for Waveforms and Load Configurations

Symbol	Parameter		74F			54F		74F		Units	Fig. No.
			T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
			Path	Mode	Min	Typ	Max	Min	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay C <sub>n</sub> to C <sub>n+4</sub>		3.0	6.4	8.5	3.0	10.0	3.0	9.5	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Ā or B̄ to C <sub>n+4</sub>	Sum	5.0	10.0	13.0	5.0	15.5	5.0	14.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Ā or B̄ to C <sub>n+4</sub>	Dif	4.0	9.4	12.0	3.5	16.5	4.0	13.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay C <sub>n</sub> to F̄	Any	5.0	10.8	14.0	5.0	17.0	5.0	15.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay C <sub>n</sub> to F̄	Any	5.0	10.0	13.0	4.0	15.0	5.0	14.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay C <sub>n</sub> to F̄	Any	3.0	6.7	8.5	2.5	16.0	3.0	9.5	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay C <sub>n</sub> to F̄	Any	3.0	6.5	8.5	2.5	12.0	3.0	9.5	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Ā or B̄ or C̄	Sum	3.0	5.7	7.5	2.5	9.0	3.0	8.5	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Ā or B̄ or C̄	Sum	3.0	5.8	7.5	2.5	9.5	3.0	8.5	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Ā or B̄ to C̄	Dif	3.0	6.5	8.5	2.5	11.5	3.0	9.5	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Ā or B̄ to C̄	Dif	3.0	7.3	9.5	2.5	11.0	3.0	10.5	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Ā or B̄ to P̄	Sum	3.0	5.0	7.0	2.5	8.5	3.0	8.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Ā or B̄ to P̄	Sum	3.0	5.5	7.5	3.0	9.5	3.0	8.5	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Ā or B̄ to P̄	Dif	3.0	5.8	7.5	2.5	11.0	3.0	8.5	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Ā or B̄ to P̄	Dif	4.0	6.5	8.5	3.0	11.0	4.0	9.5	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Ā <sub>i</sub> or B̄ <sub>i</sub> to F̄ <sub>i</sub>	Sum	3.0	7.0	9.0	3.0	14.5	3.0	10.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Ā <sub>i</sub> or B̄ <sub>i</sub> to F̄ <sub>i</sub>	Sum	3.0	7.2	10.0	3.0	14.5	3.0	10.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Ā <sub>i</sub> or B̄ <sub>i</sub> to F̄ <sub>i</sub>	Dif	3.0	8.2	11.0	3.0	17.5	3.0	12.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Ā <sub>i</sub> or B̄ <sub>i</sub> to F̄ <sub>i</sub>	Dif	3.0	5.0	11.0	3.0	14.5	3.0	12.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Any Ā or B̄ to Any F̄	Sum	4.0	8.0	10.5	3.5	16.5	4.0	11.5	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Any Ā or B̄ to Any F̄	Sum	4.0	7.8	10.0	4.0	13.5	4.0	11.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Any Ā or B̄ to Any F̄	Dif	4.5	9.4	12.0	3.5	17.5	4.5	13.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Any Ā or B̄ to Any F̄	Dif	3.5	9.4	12.0	3.0	14.0	3.5	13.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Ā or B̄ to F̄	Logic	4.0	6.0	9.0	3.5	14.5	4.0	10.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Ā or B̄ to F̄	Logic	4.0	6.0	10.0	3.0	15.5	4.0	11.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Ā or B̄ to A = B	Dif	11.0	18.5	27.0	8.0	35.0	11.0	29.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Ā or B̄ to A = B	Dif	6.0	9.8	12.5	5.5	21.0	6.0	13.5	ns	2-3