National Semiconductor

54F/74F181
4-Bit Arithmetic Logic Unit

General Description

The 'F181 is a 4-bit Arithmetic logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations. It is 40% faster than the Schottky ALU and only consumes 30% as much power.

Features

- Full lookahead for high-speed arithmetic operation on long words
- Guaranteed 4000V minimum ESD protection

Ordering Code: See Section 11

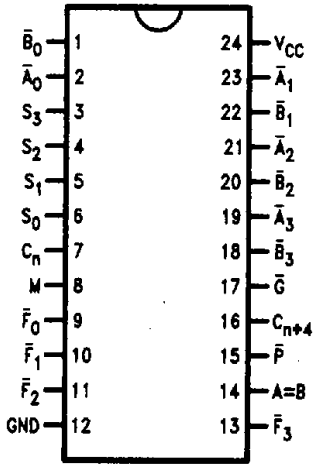
Commercial	Military	Package Number	Package Description
74F181PC		N24A	24-Lead (0.600" Wide) Molded Dual-In-Line
74F181SPC		N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
	54F181DM (Note 2)	J24A	24-Lead Ceramic Dual-In-Line
	54F181SDM (Note 2)	J24F	24-Lead (0.300") Ceramic Dual-In-Line
74F181SC (Note 1)		M24B	24-Lead (0.300") Molded Small Outline, JEDEC
	54F181FM (Note 2)	W24C	24-Lead Cerpack
	54F181LM (Note 2)	E28A	24-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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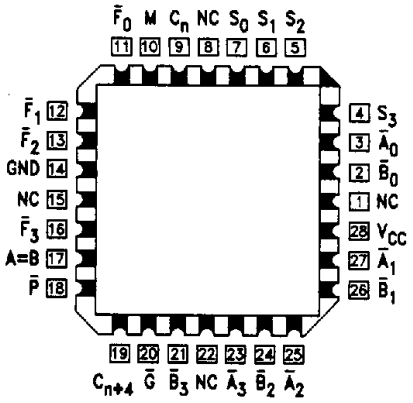
Pin Assignment for LCC



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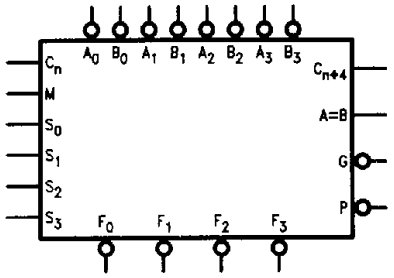
Logic Symbols

Active-HIGH Operands



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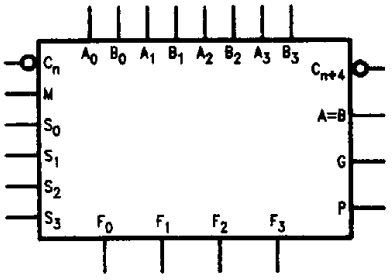
Active-LOW Operands



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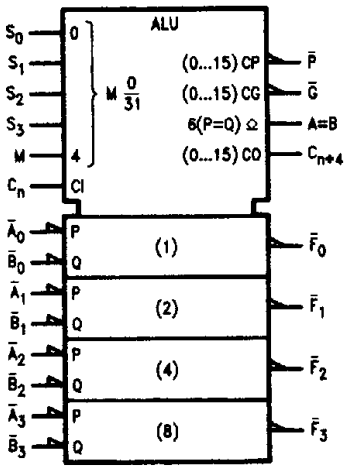
IEEE/IEC



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Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\overline{A}_0$–$\overline{A}_3$	A Operand Inputs (Active LOW)	1.0/3.0	20 μA/−1.8 mA
$\overline{B}_0$–$\overline{B}_3$	B Operand Inputs (Active LOW)	1.0/3.0	20 μA/−1.8 mA
S_0–S_3	Function Select Inputs	1.0/4.0	20 μA/−2.4 mA
M	Mode Control Input	1.0/1.0	20 μA/−0.6 mA
C_n	Carry Input	1.0/5.0	20 μA/−3.0 mA
$\overline{F}_0$–$\overline{F}_3$	Function Outputs (Active LOW)	50/33.3	−1 mA/20 mA
A = B	Comparator Output	OC*/33.3	*/20 mA
$\overline{G}$	Carry Generate Output (Active LOW)	50/33.3	−1 mA/20 mA
$\overline{P}$	Carry Propagate Output (Active LOW)	50/33.3	−1 mA/20 mA
C_{n+4}	Carry Output	50/33.3	−1 mA/20 mA

*OC-Open Collector

Functional Description

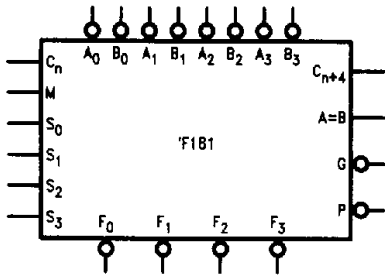
The 'F181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S_0–S_3) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on Active HIGH or Active LOW operands. The Function Table lists these operations.

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). In the Add mode, $\overline{P}$ indicates that $\overline{F}$ is 15 or more, while $\overline{G}$ indicates that $\overline{F}$ is 16 or more. In the Subtract mode $\overline{P}$ indicates that $\overline{F}$ is zero or less, while $\overline{G}$ indicates that $\overline{F}$ is less than zero. $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, the 'F181 can be used in a simple Ripple Carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For high speed operation the device is used in conjunction with a carry lookahead circuit. One carry lookahead package is required for each group of four 'F181 devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A=B output from the device goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the Subtract mode. The A=B output is open collector and can be wired AND with other A=B outputs to give a comparison for more than four bits. The A=B signal can also be used with the C_{n+4} signal to indicate A>B and A<B.

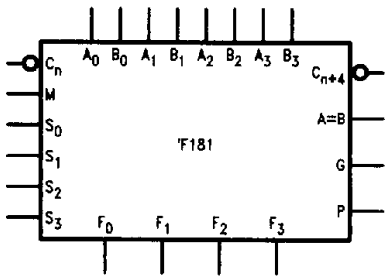
The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow. As indicated, this device can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

'F181 Operation Table



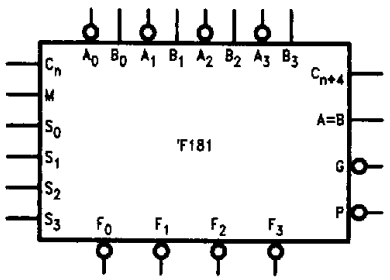
a. All Input Data Inverted

S_0	S_1	S_2	S_3	Logic (M = H)	Arithmetic (M = L, C_0 = Inactive)	Arithmetic (M = L, C_0 = Active)
L	L	L	L	$\overline{A}$	A minus 1	A
H	L	L	L	$\overline{A} \bullet \overline{B}$	A • B minus 1	A • B
L	H	L	L	$\overline{A} + B$	A • $\overline{B}$ minus 1	A • $\overline{B}$
H	H	L	L	Logic "1"	minus 1 (2s comp.)	Zero
L	L	H	L	$\overline{A + B}$	A plus (A + $\overline{B}$)	A plus (A + $\overline{B}$) plus 1
H	L	H	L	$\overline{B}$	A • B plus (A + $\overline{B}$)	A • B plus (A + $\overline{B}$) plus 1
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1	A minus B
H	H	H	L	$A + \overline{B}$	A + $\overline{B}$	A + $\overline{B}$ plus 1
L	L	L	H	$\overline{A} \bullet B$	A plus (A + B)	A plus (A + B plus 1
H	L	L	H	$A \oplus B$	A plus B	A plus B plus 1
L	H	L	H	B	A • $\overline{B}$ plus (A + B)	A • $\overline{B}$ plus (A + B) plus 1
H	H	L	H	A + B	A + B	A + B plus 1
L	L	H	H	Logic "0"	A plus A (2 × A)	A plus A (2 × A) plus 1
H	L	H	H	A • $\overline{B}$	A plus A • B	A plus A • B plus 1
L	H	H	H	A • B	A plus A • $\overline{B}$	A plus A • $\overline{B}$ plus 1
H	H	H	H	A	A	A plus 1



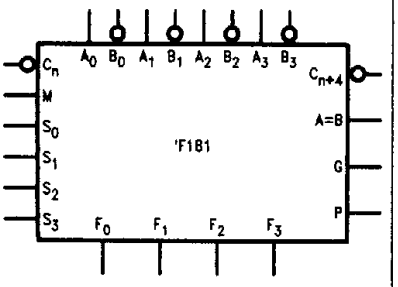
b. All Input Data True

S_0	S_1	S_2	S_3	Logic (M = H)	Arithmetic (M = L, C_0 = Inactive)	Arithmetic (M = L, C_0 = Active)
L	L	L	L	$\overline{A}$	A	A plus 1
H	L	L	L	$\overline{A + B}$	A + B	A + B plus 1
L	H	L	L	$\overline{A} \bullet B$	A + $\overline{B}$	A + $\overline{B}$ plus 1
H	H	L	L	Logic "0"	minus 1 (2s comp.)	Zero
L	L	H	L	$\overline{A} \bullet \overline{B}$	A plus (A • $\overline{B}$)	A plus A • $\overline{B}$ plus 1
H	L	H	L	$\overline{B}$	A • $\overline{B}$ plus (A + B)	A • B plus (A + B) plus 1
L	H	H	L	$A \oplus B$	A minus B minus 1	A minus B
H	H	H	L	$A \bullet \overline{B}$	A • $\overline{B}$ minus 1	A • $\overline{B}$
L	L	L	H	$\overline{A} + B$	A plus A • B	A plus A • B plus 1
H	L	L	H	$\overline{A \oplus B}$	A plus B	A plus B plus 1
L	H	L	H	B	A • B plus (A + $\overline{B}$)	A • B plus (A + $\overline{B}$) plus 1
H	H	L	H	A • B	A • B minus 1	A • B
L	L	H	H	Logic "1"	A plus A (2 × A)	A plus A (2 × A) plus 1
H	L	H	H	A + $\overline{B}$	A plus (A + B)	A plus (A + B) plus 1
L	H	H	H	A + B	A plus (A + $\overline{B}$)	A plus (A + $\overline{B}$) plus 1
H	H	H	H	A	A minus 1	A



c. A Input Data Inverted; B Input Data True

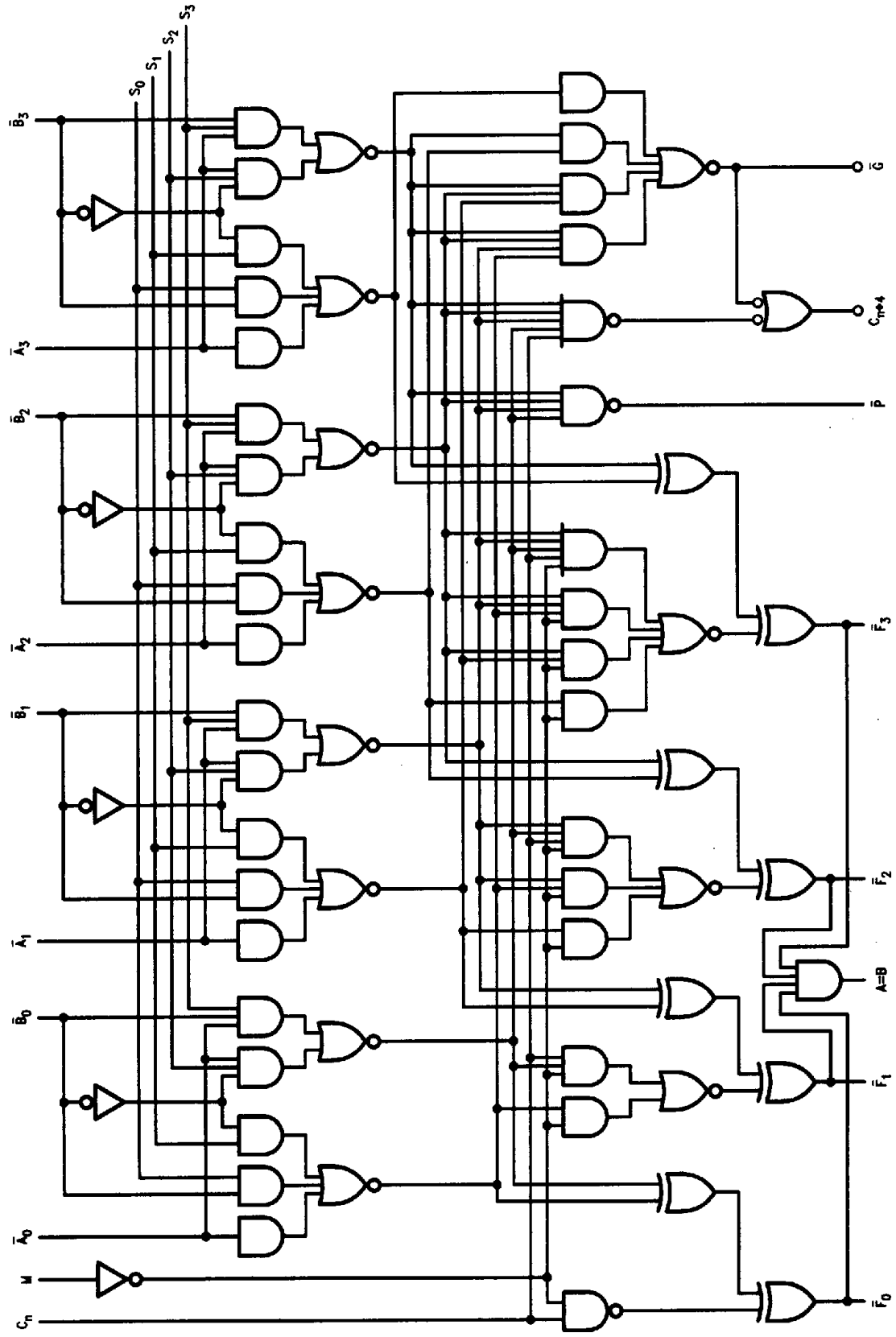
S_0	S_1	S_2	S_3	Logic (M = H)	Arithmetic (M = L, C_0 = Inactive)	Arithmetic (M = L, C_0 = Active)
L	L	L	L	$\overline{A}$	A minus 1	A
H	L	L	L	$\overline{A} + B$	A • $\overline{B}$ minus 1	A • B
L	H	L	L	$\overline{A} \bullet \overline{B}$	A • B minus 1	A • B
H	H	L	L	Logic "1"	minus 1 (2s comp.)	Zero
L	L	H	L	$\overline{A} \bullet B$	A plus (A + B)	A plus (A + B) plus 1
H	L	H	L	B	A • $\overline{B}$ plus (A + B)	A • $\overline{B}$ plus (A + B) plus 1
L	H	H	L	$A \oplus B$	A plus B	A plus B plus 1
H	H	H	L	A + B	A + B	A + B plus 1
L	L	L	H	$\overline{A + B}$	A plus (A + $\overline{B}$)	A plus (A + $\overline{B}$) plus 1
H	L	L	H	$\overline{A \oplus B}$	A minus B minus 1	A minus B
L	H	L	H	$\overline{B}$	A • B plus (A + $\overline{B}$)	A • B plus (A + $\overline{B}$) plus 1
H	H	L	H	$A + \overline{B}$	A + $\overline{B}$	A + $\overline{B}$ plus 1
L	L	H	H	Logic "0"	A plus A (2 × A)	A plus A (2 × A) plus 1
H	L	H	H	A • B	A plus A • $\overline{B}$	A plus A • $\overline{B}$ plus 1
L	H	H	H	A • $\overline{B}$	A plus A • B	A plus A • B plus 1
H	H	H	H	A	A	A plus 1



d. A Input Data True; B Input Date Inverted

S_0	S_1	S_2	S_3	Logic (M = H)	Arithmetic (M = L, C_0 = Inactive)	Arithmetic (M = L, C_0 = Active)
L	L	L	L	$\overline{A}$	A	A plus 1
H	L	L	L	$\overline{A} \bullet B$	A + $\overline{B}$	A + $\overline{B}$ plus 1
L	H	L	L	$\overline{A + B}$	A + B	A + B plus 1
H	H	L	L	Logic "0"	minus 1 (2s comp.)	Zero
L	L	H	L	$\overline{A} + B$	A plus A • B	A plus A • B plus 1
H	L	H	L	B	A • B plus (A + $\overline{B}$)	A • $\overline{B}$ plus (A + B) plus 1
L	H	H	L	$\overline{A \oplus B}$	A plus B	A plus B plus 1
H	H	H	L	A • B	A • B minus 1	A • B
L	L	L	H	$\overline{A} \bullet \overline{B}$	A plus A • $\overline{B}$	A plus A • B plus 1
H	L	L	H	$A \oplus B$	A minus B minus 1	A minus B
L	H	L	H	$\overline{B}$	A • $\overline{B}$ plus (A + B)	A • $\overline{B}$ plus (A + B) plus 1
H	H	L	H	A • $\overline{B}$	A • $\overline{B}$ minus 1	A • $\overline{B}$
L	L	H	H	Logic "1"	A plus A (2 × A)	A plus A (2 × A) plus 1
H	L	H	H	A + B	A plus (A + $\overline{B}$)	A plus (A + $\overline{B}$) plus 1
L	H	H	H	A + $\overline{B}$	A plus (A + B)	A plus (A + B) plus 1
H	H	H	H	A	A minus 1	A

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE® Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
		74F 10% V_{CC}			0.5			I_{OL} = 20 mA
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	V_{IN} = 2.7V
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	V_{IN} = 7.0V
		74F			7.0			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	V_{OUT} = V_{CC} ($\overline{F}_n$, $\overline{G}$, $\overline{P}$, C_{n+4})
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (M)
					−1.8			V_{IN} = 0.5V ($\overline{A}_0$, $\overline{A}_1$, $\overline{A}_3$, $\overline{B}_0$, $\overline{B}_1$, $\overline{B}_3$)
					−2.4			V_{IN} = 0.5V (S_n, $\overline{A}_2$, $\overline{B}_2$)
					−3.0			V_{IN} = 0.5V (C_n)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V ($\overline{F}_n$, $\overline{G}$, $\overline{P}$, C_{n+4})
I_{OHC}	Open Collector, Output OFF Leakage Test				250	μA	Min	V_O = V_{CC} (A = B)
I_{CCH}	Power Supply Current			43	65.0	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			43	65.0	mA	Max	V_O = LOW

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter		74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$			54F $T_A, V_{CC} = Mil$ $C_L = 50\ pF$		74F $T_A, V_{CC} = Com$ $C_L = 50\ pF$		Units	Fig. No.
	Path	Mode	Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay		3.0	6.4	8.5	3.0	10.0	3.0	9.5	ns	2–3
t_{PHL}	C_n to C_{n+4}		3.0	6.1	8.0	3.0	9.5	3.0	9.0		
t_{PLH}	Propagation Delay		5.0	10.0	13.0	5.0	15.5	5.0	14.0	ns	2–3
t_{PHL}	$\overline{A}$ or $\overline{B}$ to C_{n+4}	Sum	4.0	9.4	12.0	3.5	16.5	4.0	13.0		
t_{PLH}	Propagation Delay		5.0	10.8	14.0	5.0	17.0	5.0	15.0	ns	2–3
t_{PHL}	$\overline{A}$ or $\overline{B}$ to C_{n+4}	Dif	5.0	10.0	13.0	4.0	15.0	5.0	14.0		
t_{PLH}	Propagation Delay		3.0	6.7	8.5	2.5	16.0	3.0	9.5	ns	2–3
t_{PHL}	C_n to $\overline{F}$	Any	3.0	6.5	8.5	2.5	12.0	3.0	9.5		
t_{PLH}	Propagation Delay		3.0	5.7	7.5	2.5	9.0	3.0	8.5	ns	2–3
t_{PHL}	$\overline{A}$ or $\overline{B}$ or $\overline{G}$	Sum	3.0	5.8	7.5	2.5	9.5	3.0	8.5		
t_{PLH}	Propagation Delay		3.0	6.5	8.5	2.5	11.5	3.0	9.5	ns	2–3
t_{PHL}	$\overline{A}$ or $\overline{B}$ to $\overline{G}$	Dif	3.0	7.3	9.5	2.5	11.0	3.0	10.5		
t_{PLH}	Propagation Delay		3.0	5.0	7.0	2.5	8.5	3.0	8.0	ns	2–3
t_{PHL}	$\overline{A}$ or $\overline{B}$ to $\overline{P}$	Sum	3.0	5.5	7.5	3.0	9.5	3.0	8.5		
t_{PLH}	Propagation Delay		3.0	5.8	7.5	2.5	11.0	3.0	8.5	ns	2–3
t_{PHL}	$\overline{A}$ or $\overline{B}$ to $\overline{P}$	Dif	4.0	6.5	8.5	3.0	11.0	4.0	9.5		
t_{PLH}	Propagation Delay		3.0	7.0	9.0	3.0	14.5	3.0	10.0	ns	2–3
t_{PHL}	$\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Sum	3.0	7.2	10.0	3.0	14.5	3.0	10.0		
t_{PLH}	Propagation Delay		3.0	8.2	11.0	3.0	17.5	3.0	12.0	ns	2–3
t_{PHL}	$\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Dif	3.0	5.0	11.0	3.0	14.5	3.0	12.0		
t_{PLH}	Propagation Delay		4.0	8.0	10.5	3.5	16.5	4.0	11.5	ns	2–3
t_{PHL}	Any $\overline{A}$ or $\overline{B}$ to Any $\overline{F}$	Sum	4.0	7.8	10.0	4.0	13.5	4.0	11.0		
t_{PLH}	Propagation Delay		4.5	9.4	12.0	3.5	17.5	4.5	13.0	ns	2–3
t_{PHL}	Any $\overline{A}$ or $\overline{B}$ to Any $\overline{F}$	Dif	3.5	9.4	12.0	3.0	14.0	3.5	13.0		
t_{PLH}	Propagation Delay		4.0	6.0	9.0	3.5	14.5	4.0	10.0	ns	2–3
t_{PHL}	$\overline{A}$ or $\overline{B}$ to $\overline{F}$	Logic	4.0	6.0	10.0	3.0	15.5	4.0	11.0		
t_{PLH}	Propagation Delay		11.0	18.5	27.0	8.0	35.0	11.0	29.0	ns	2–3
t_{PHL}	$\overline{A}$ or $\overline{B}$ to A = B	Dif	6.0	9.8	12.5	5.5	21.0	6.0	13.5		