

**40V COMPLEMENTARY PAIR ENHANCEMENT MODE MOSFET**

**Product Summary**

Device	V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub> max T <sub>A</sub> = 25°C (Notes 3 & 5)
Q1	40V	45mΩ @ V <sub>GS</sub> = 10V	5.5A
		60mΩ @ V <sub>GS</sub> = 4.5V	4.2A
Q2	-40V	45mΩ @ V <sub>GS</sub> = -10V	-5.8A
		60mΩ @ V <sub>GS</sub> = -4.5V	-4.2A

**Description and Applications**

This MOSFET has been designed to ensure that R<sub>DS(on)</sub> of N and P channel FET are matched to minimize losses in both arms of the bridge. The DMC4040SSD is optimized for use in 3 phases brushless DC motor circuits (BLDC), CCFL backlighting.

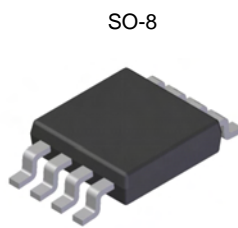
- 3 phases BLDC motor
- CCFL backlighting

**Features and Benefits**

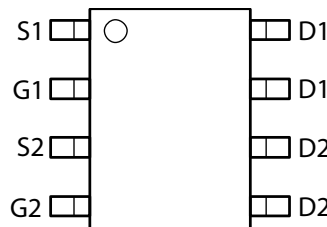
- Matched N & P R<sub>DS(on)</sub> - Minimizes power losses
- Fast switching – Minimizes switching losses
- Dual device – Reduces PCB area
- "Green" component and RoHS compliant (Note 1)
- Qualified to AEC-Q101 Standards for High Reliability

**Mechanical Data**

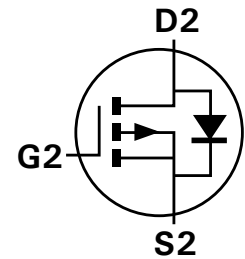
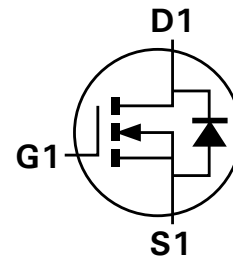
- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0 (Note 1)
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Matte Tin annealed over Copper lead frame. Solderable per MIL-STD-202, Method 208
- Weight: 0.074 grams (approximate)



Top View



Top View



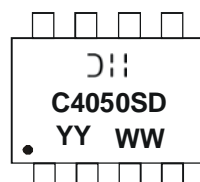
Equivalent Circuit

**Ordering Information** (Note 1)

Product	Marking	Reel size (inches)	Tape width (mm)	Quantity per reel
DMC4050SSD-13	C4050SD	13	12	2,500

Notes: 1. Diodes, Inc. defines "Green" products as those which are RoHS compliant and contain no halogens or antimony compounds; further information about Diodes Inc.'s "Green" Policy can be found on our website. For packaging details, go to our website.

**Marking Information**



D = Manufacturer's Marking  
 C4050SD = Product Type Marking Code  
 YYWW = Date Code Marking  
 YY = Year (ex: 10 = 2010)  
 WW = Week (01 - 53)

**Maximum Ratings** @ $T_A = 25^\circ\text{C}$  unless otherwise specified

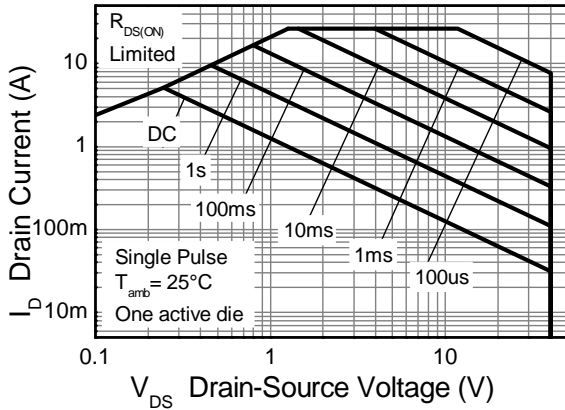
Characteristic			Symbol	N-Channel - Q1	P-Channel - Q2	Units
Drain-Source Voltage			$V_{DSS}$	40	-40	V
Gate-Source Voltage			$V_{GSS}$	$\pm 20$	$\pm 20$	
Continuous Drain Current	$V_{GS} = 10\text{V}$	(Notes 3 & 5)	$I_D$	5.8	-5.8	A
		$T_A = 70^\circ\text{C}$ (Notes 3 & 5)		4.38	-4.52	
		(Notes 2 & 5)		4.2	-4.2	
		(Notes 2 & 6)		5.3	-5.3	
Pulsed Drain Current	$V_{GS} = 10\text{V}$	(Notes 4 & 5)	$I_{DM}$	24.1	-24.9	
Continuous Source Current (Body diode)			$I_S$	2.5	-2.5	
Pulsed Source Current (Body diode)			$I_{SM}$	24.1	-24.9	

**Thermal Characteristics** @ $T_A = 25^\circ\text{C}$  unless otherwise specified

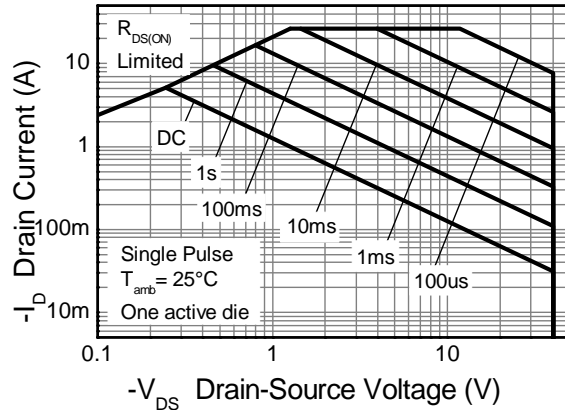
Characteristic		Symbol	N-Channel - Q1	P-Channel - Q2	Unit
Power Dissipation Linear Derating Factor	(Notes 2 & 5)	$P_D$	1.25		W mW/ $^\circ\text{C}$
			10		
	(Notes 2 & 6)		1.8		
	(Notes 3 & 5)		14.3		
Thermal Resistance, Junction to Ambient	(Notes 2 & 5)	$R_{\theta JA}$	2.14		$^\circ\text{C}/\text{W}$
	(Notes 2 & 6)		17.2		
	(Notes 3 & 5)		100		
			70		
Thermal Resistance, Junction to Lead	(Notes 3 & 5)	$R_{\theta JL}$	58		
Operating and Storage Temperature Range		$T_J, T_{STG}$	-55 to +150		$^\circ\text{C}$

- Notes:
2. For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
  3. Same as note (2), except the device is measured at  $t \leq 10$  sec.
  4. Same as note (2), except the device is pulsed with  $D = 0.02$  and pulse width 300 $\mu\text{s}$ .
  5. For a dual device with one active die.
  6. For a device with two active die running at equal power.
  7. Thermal resistance from junction to solder-point (at the end of the drain lead).

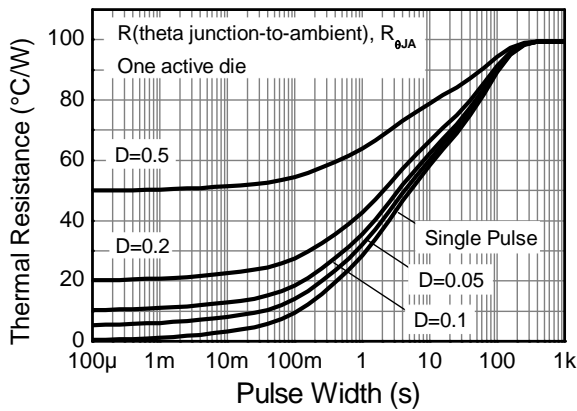
**Thermal Characteristics**



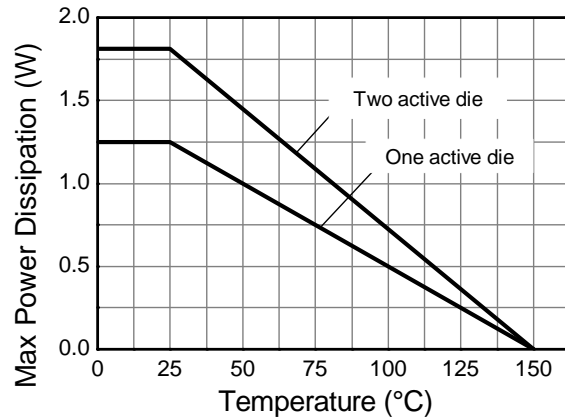
**N-channel Safe Operating Area**



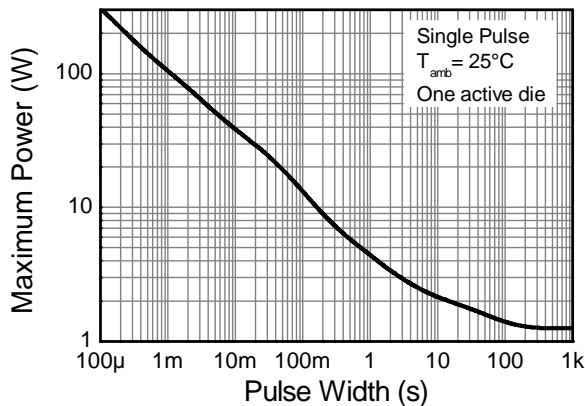
**P-channel Safe Operating Area**



**Transient Thermal Impedance**



**Derating Curve**



**Pulse Power Dissipation**

**Electrical Characteristics N-CHANNEL** @T<sub>A</sub> = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 8)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	40	-	-	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
Zero Gate Voltage Drain Current T <sub>J</sub> = 25°C	I <sub>DSS</sub>	-	-	1.0	μA	V <sub>DS</sub> = 40V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	-	-	±100	nA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 8)</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	0.8	1.3	1.8	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	-	20	45	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 3A
			33	60		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 3A
Forward Transfer Admittance	Y <sub>fs</sub>	-	12.6	-	S	V <sub>DS</sub> = 5V, I <sub>D</sub> = 3A
Diode Forward Voltage (Note 8)	V <sub>SD</sub>	-	0.7	1.0	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 1A
<b>DYNAMIC CHARACTERISTICS (Note 9)</b>						
Input Capacitance	C <sub>iss</sub>	-	1790.8	-	pF	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V, f = 1.0MHz
Output Capacitance	C <sub>oss</sub>	-	160.6	-	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>	-	120.5	-	pF	
Gate Resistance	R <sub>g</sub>	-	1.03	-	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1MHz
Total Gate Charge	Q <sub>g</sub>	-	37.56	-	nC	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 20V, I <sub>D</sub> = 3A
Gate-Source Charge	Q <sub>gs</sub>	-	7.8	-	nC	
Gate-Drain Charge	Q <sub>gd</sub>	-	6.6	-	nC	
Turn-On Delay Time	t <sub>D(on)</sub>	-	8.08	-	ns	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 20V, I <sub>D</sub> = 3A
Turn-On Rise Time	t <sub>r</sub>	-	15.14	-	ns	
Turn-Off Delay Time	t <sub>D(off)</sub>	-	24.29	-	ns	
Turn-Off Fall Time	t <sub>f</sub>	-	5.27	-	ns	
			-	-		

Notes: 8. Short duration pulse test used to minimize self-heating effect.  
9. Guaranteed by design. Not subject to production testing.

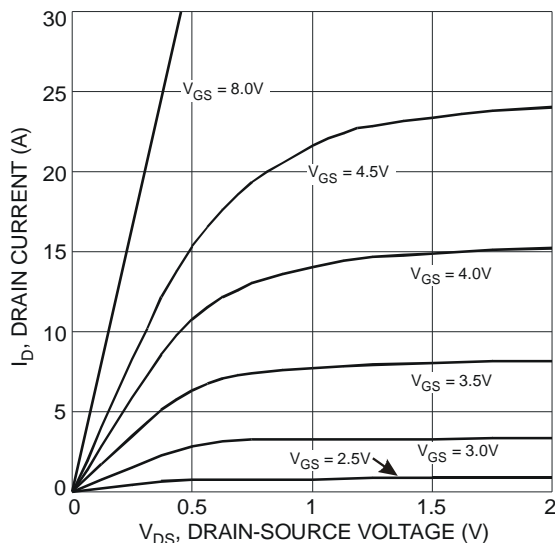


Fig. 1 Typical Output Characteristic

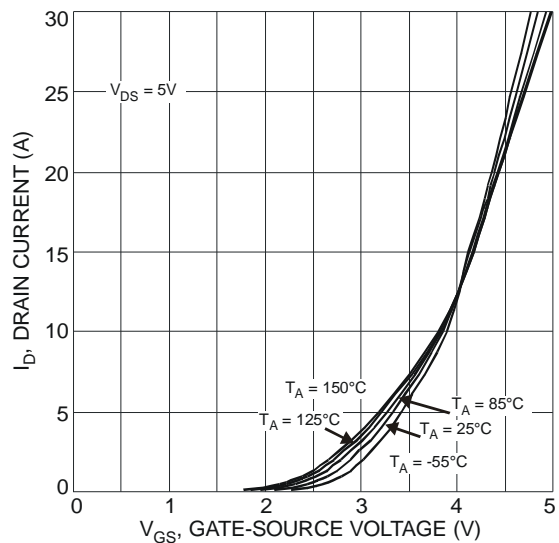


Fig. 2 Typical Transfer Characteristic

**DMC4050SSD**

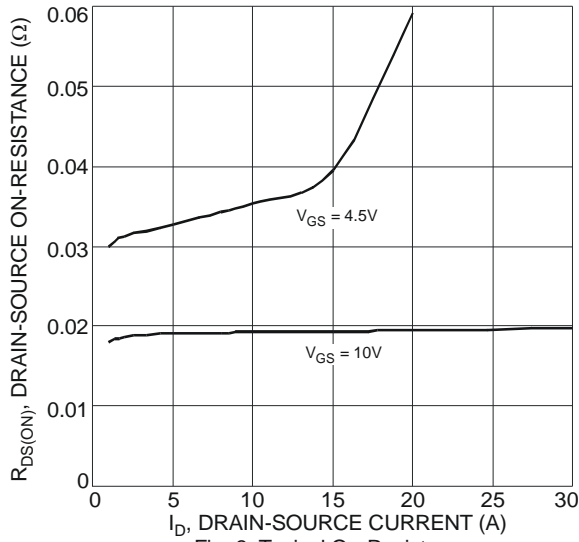


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

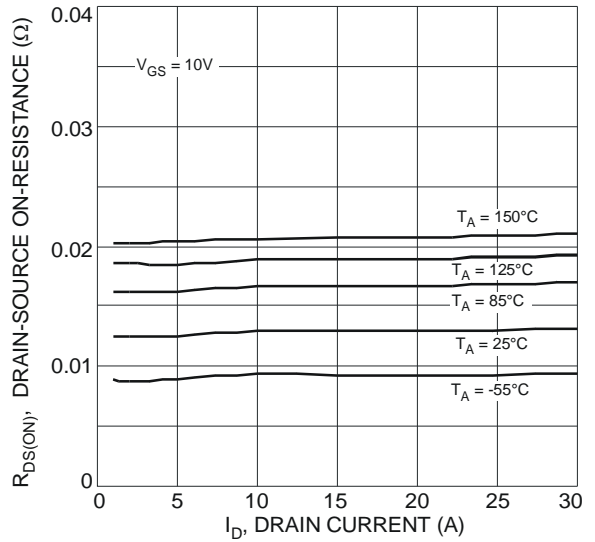


Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

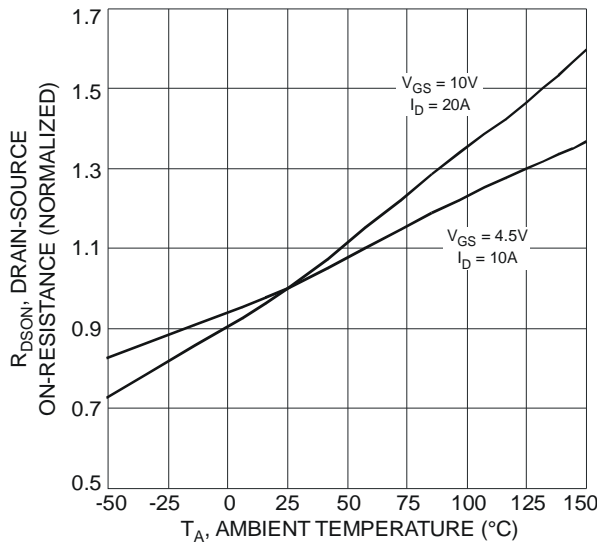


Fig. 5 On-Resistance Variation with Temperature

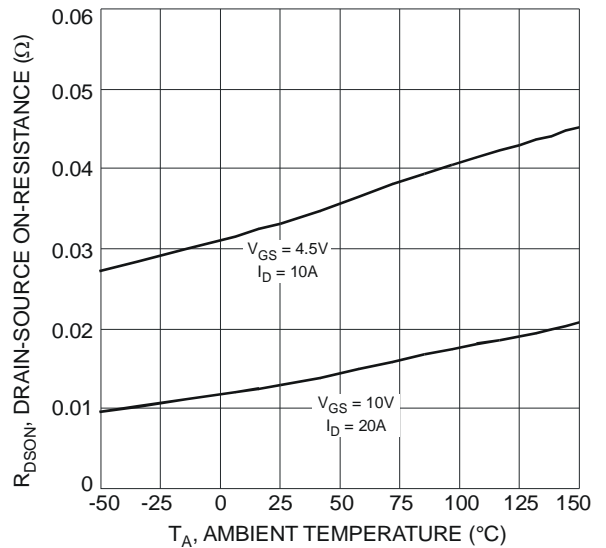


Fig. 6 On-Resistance Variation with Temperature

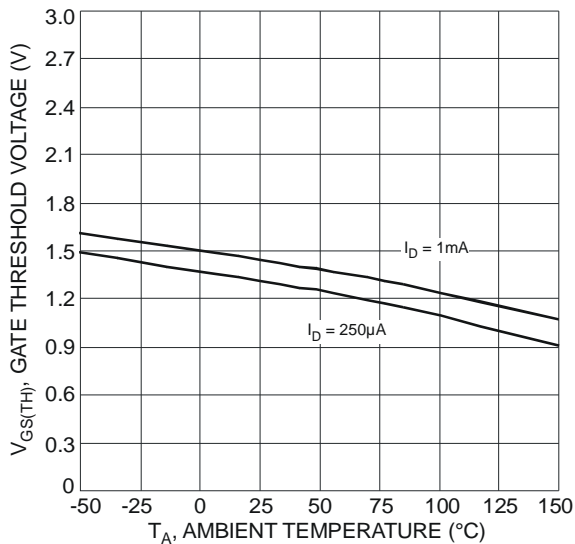


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

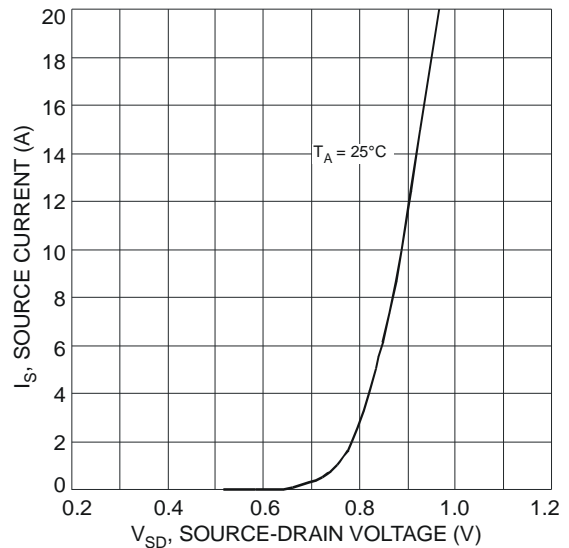


Fig. 8 Diode Forward Voltage vs. Current

**DMC4050SSD**

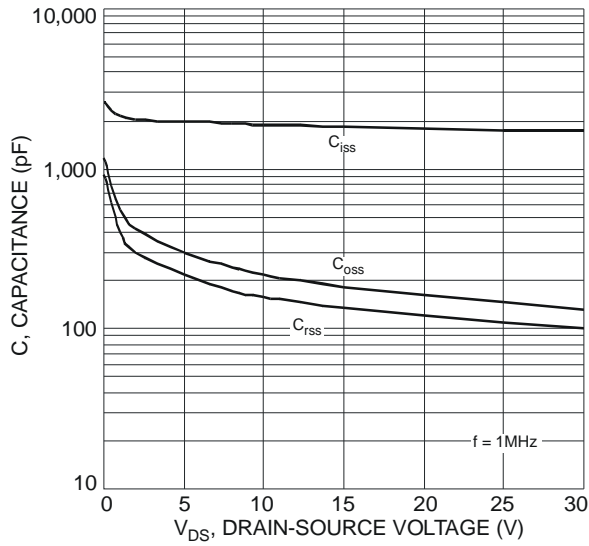


Fig. 9 Typical Total Capacitance

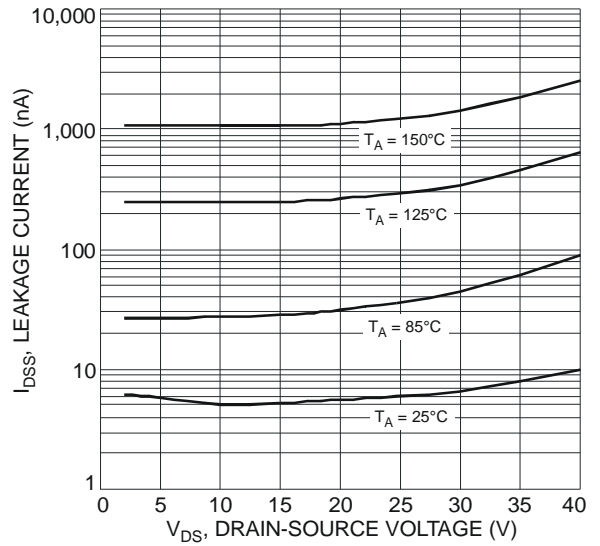


Fig. 10 Typical Leakage Current vs. Drain-Source Voltage

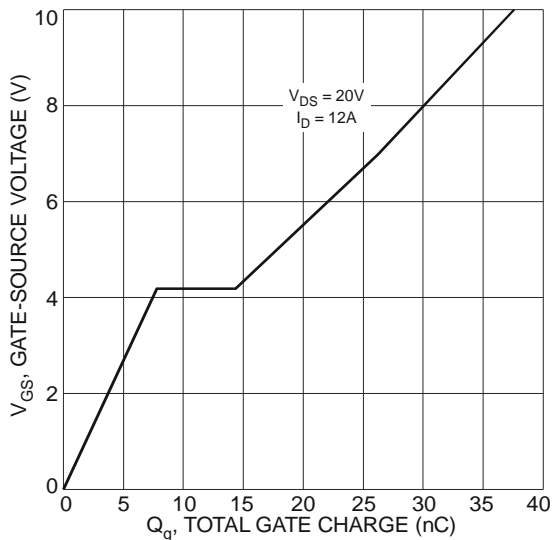


Fig. 11 Gate-Charge Characteristics

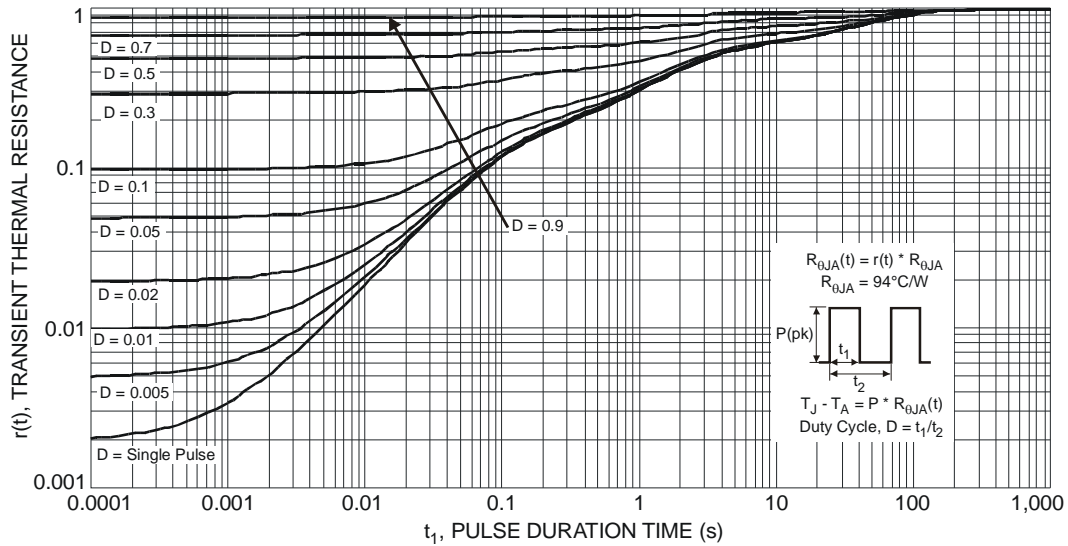


Fig. 12 Transient Thermal Response

**Electrical Characteristics P-CHANNEL** @ $T_A = 25^\circ\text{C}$  unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 8)</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	-40	-	-	V	$V_{GS} = 0V, I_D = -250\mu A$
Zero Gate Voltage Drain Current $T_J = 25^\circ\text{C}$	$I_{DSS}$	-	-	-1.0	$\mu A$	$V_{DS} = -40V, V_{GS} = 0V$
Gate-Source Leakage	$I_{GSS}$	-	-	$\pm 100$	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
<b>ON CHARACTERISTICS (Note 8)</b>						
Gate Threshold Voltage	$V_{GS(th)}$	-0.8	-1.3	-1.8	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
Static Drain-Source On-Resistance	$R_{DS(on)}$	-	28 30	45 60	m $\Omega$	$V_{GS} = -10V, I_D = -3A$ $V_{GS} = -4.5V, I_D = -3A$
Forward Transfer Admittance	$ Y_{fs} $	-	16.6	-	S	$V_{DS} = -5V, I_D = -3A$
Diode Forward Voltage (Note 8)	$V_{SD}$	-	-0.7	-1.0	V	$V_{GS} = 0V, I_S = -1A$
<b>DYNAMIC CHARACTERISTICS (Note 9)</b>						
Input Capacitance	$C_{iss}$	-	1643.17	-	pF	$V_{DS} = -20V, V_{GS} = 0V,$ $f = 1.0\text{MHz}$
Output Capacitance	$C_{oss}$	-	179.13	-	pF	
Reverse Transfer Capacitance	$C_{rss}$	-	127.82	-	pF	
Gate Resistance	$R_g$	-	6.43	-	$\Omega$	$V_{DS} = 0V, V_{GS} = 0V, f = 1\text{MHz}$
Total Gate Charge	$Q_g$	-	33.66	-	nC	$V_{GS} = -10V, V_{DS} = -20V,$ $I_D = -3A$
Gate-Source Charge	$Q_{gs}$	-	5.54	-	nC	
Gate-Drain Charge	$Q_{gd}$	-	7.30	-	nC	
Turn-On Delay Time	$t_{D(on)}$	-	6.85	-	ns	$V_{GS} = -10V, V_{DS} = -20V,$ $I_D = -3A$
Turn-On Rise Time	$t_r$	-	14.72	-	ns	
Turn-Off Delay Time	$t_{D(off)}$	-	53.65	-	ns	
Turn-Off Fall Time	$t_f$	-	30.86	-	ns	

Notes: 8. Short duration pulse test used to minimize self-heating effect.  
9. Guaranteed by design. Not subject to production testing.

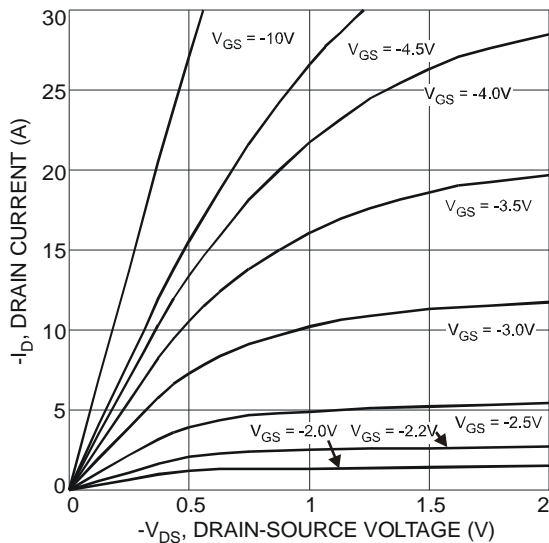


Fig. 13 Typical Output Characteristic

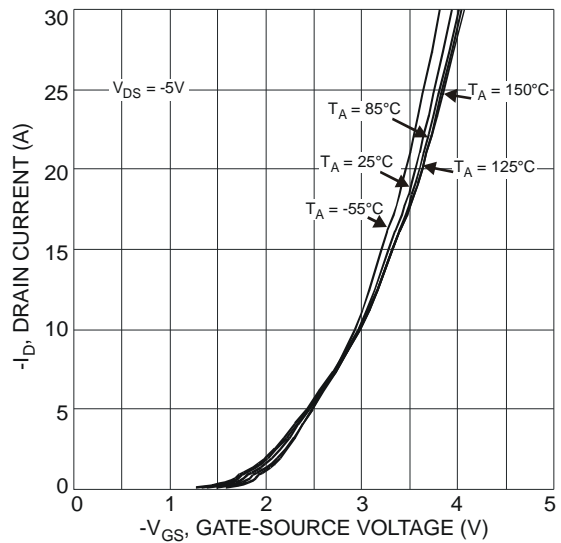


Fig. 14 Typical Transfer Characteristic

**DMC4050SSD**

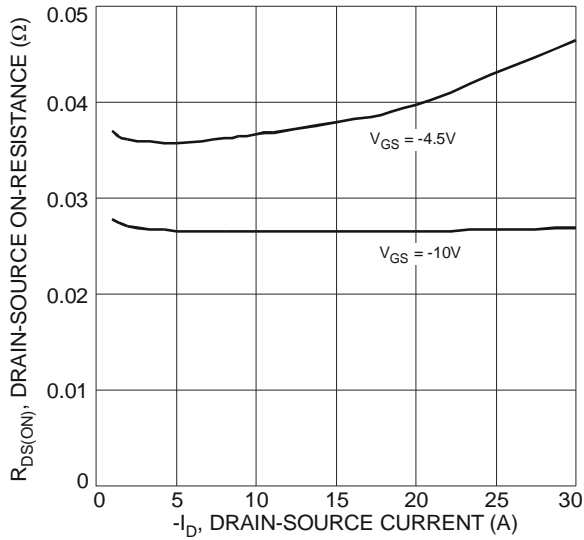


Fig. 15 Typical On-Resistance vs. Drain Current and Gate Voltage

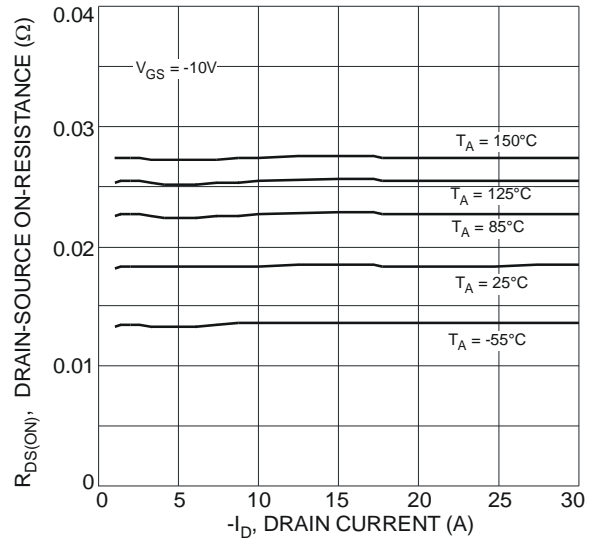


Fig. 16 Typical On-Resistance vs. Drain Current and Temperature

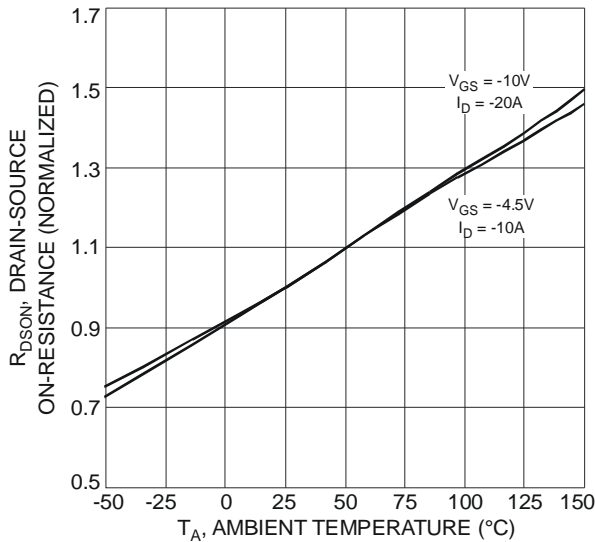


Fig. 17 On-Resistance Variation with Temperature

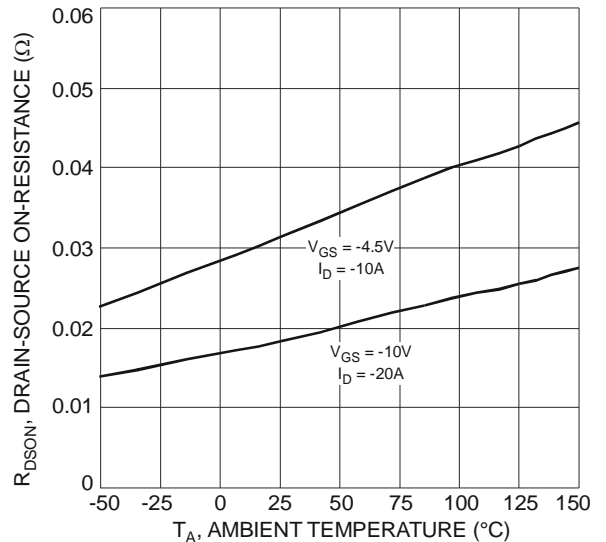


Fig. 18 On-Resistance Variation with Temperature

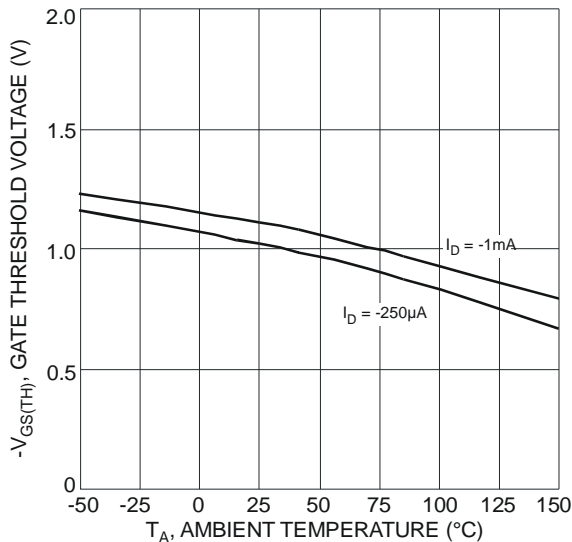


Fig. 19 Gate Threshold Variation vs. Ambient Temperature

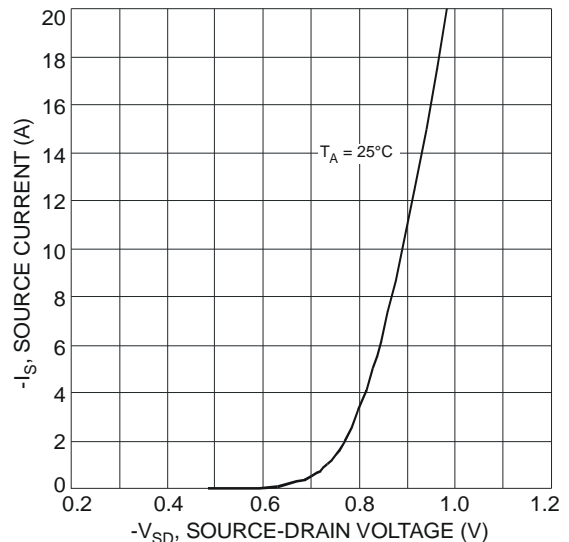


Fig. 20 Diode Forward Voltage vs. Current



**DMC4050SSD**

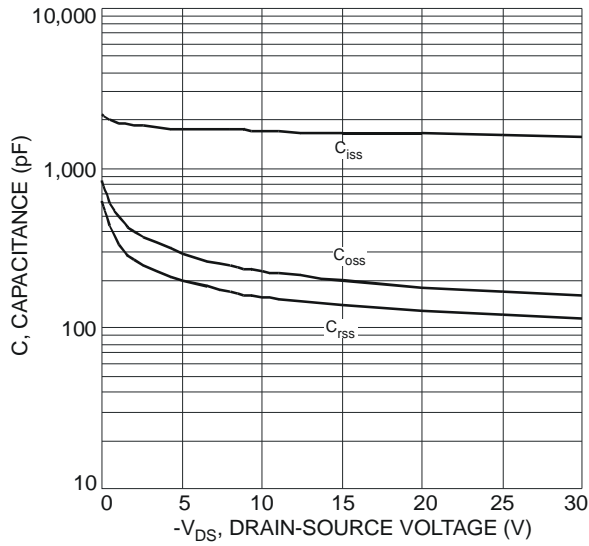


Fig. 21 Typical Total Capacitance

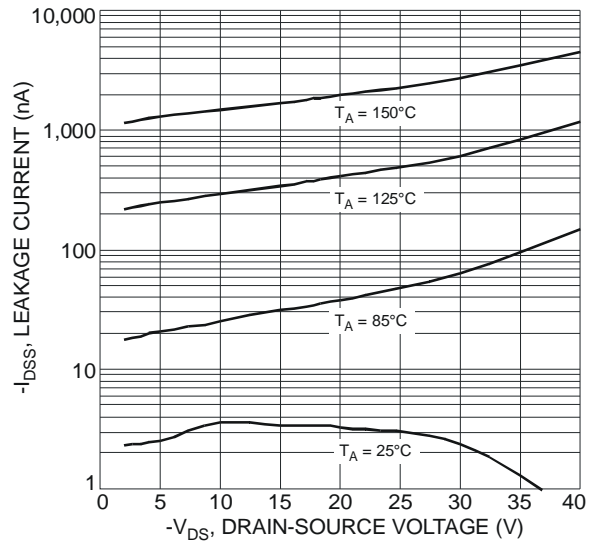


Fig. 22 Typical Leakage Current vs. Drain-Source Voltage

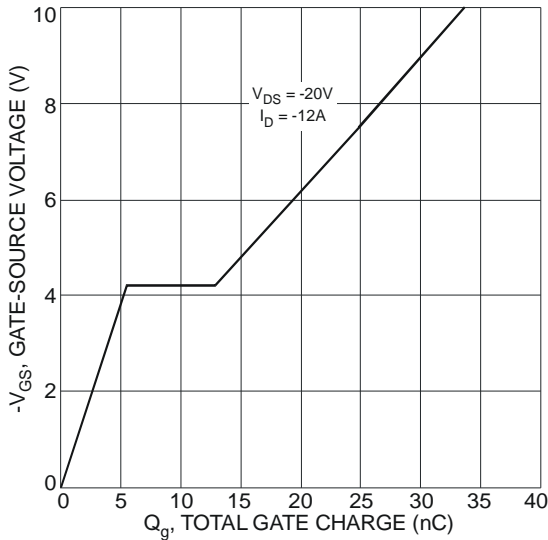


Fig. 23 Gate-Charge Characteristics

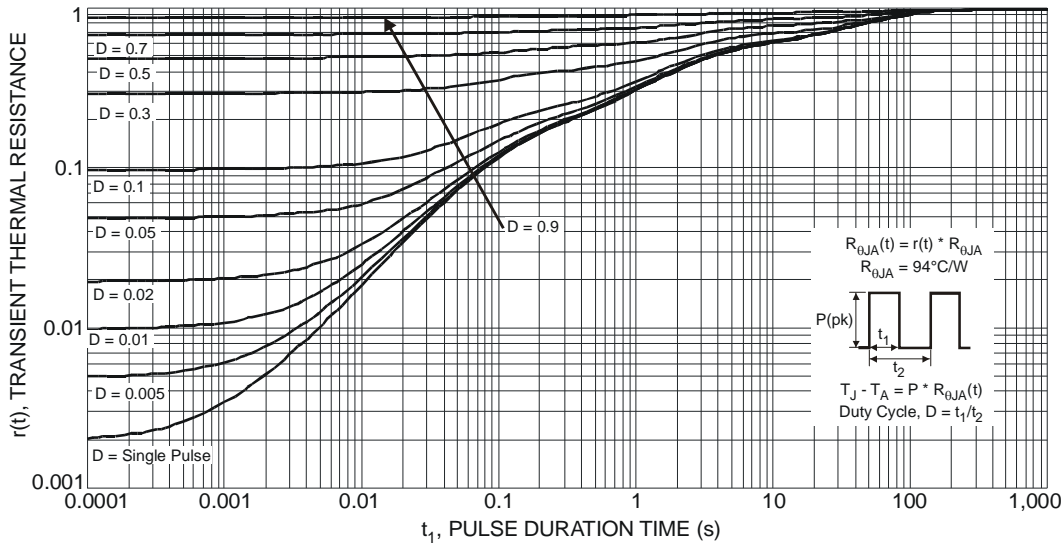
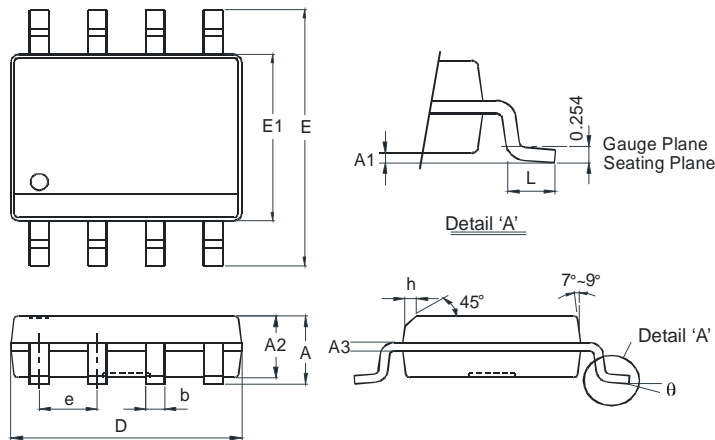


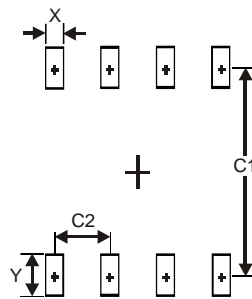
Fig. 24 Transient Thermal Response

**Package Outline Dimensions**



SO-8		
Dim	Min	Max
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

**Suggested Pad Layout**



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

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