IA3222/23 DAA CHIPSET WITH ANALOG INTERFACE

Features

- Programmable worldwide telecom compliance with one hardware build
- V.92 (56 kb/s) performance
- Virtually unlimited high-voltage isolation
- Highly-competitive BOM cost
- Lowest pin count chipset
- High common-mode RF immunity
- Continuous dc and audio snooping with >5 MΩ Tip to Ring
- Parallel pick-up, line-in-use, ring, and "911" detection
- –86 dBm receiver noise floor
- +6.5 dBm transmit power
- 120 dB Caller ID common-mode rejection at 120 Hz

Applications

- Low-cost fax-engine DAA retrofits
- Point-of-sale terminals
- Metering devices
- Alarm systems
- PBX FXO/IP telephony
- Cordless telephones
- Speaker phones

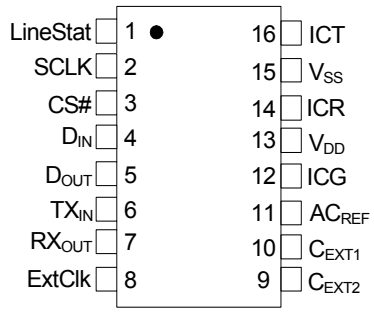
Description

The IA3222 and IA3223 integrated V.92 (56K) capable direct access arrangement (DAA) chipset is suitable for worldwide telephone line interface requirements. The patented isolation bridge technology eliminates the need for usual telecom isolation components, such as transformers or optocouplers. Innovative techniques reduce the number of discrete components, reducing overall solution cost.

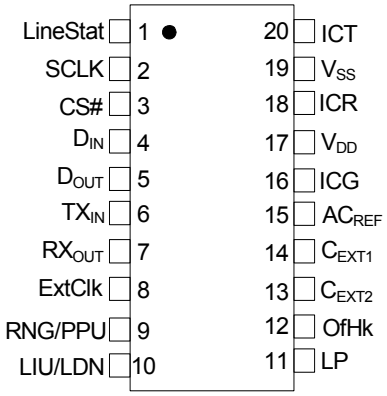
The chipset can be programmed by software to pass PTT certification worldwide. The integrated V.92 DAA offers an easy-to-use analog interface with an internal or external dc reference for seamlessly interfacing to a variety of systems. It allows easy building-block integration where audio codecs are either separate or integrated into DSPs. It is also ideal for non-modem systems requiring isolated DAAs, such as alarm systems, VoIP, and PBX FXO interfaces.

Pin Assignments

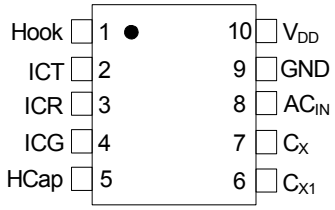
16-Pin QSOP (IA3223)



20-Pin QSOP (IA3223A)

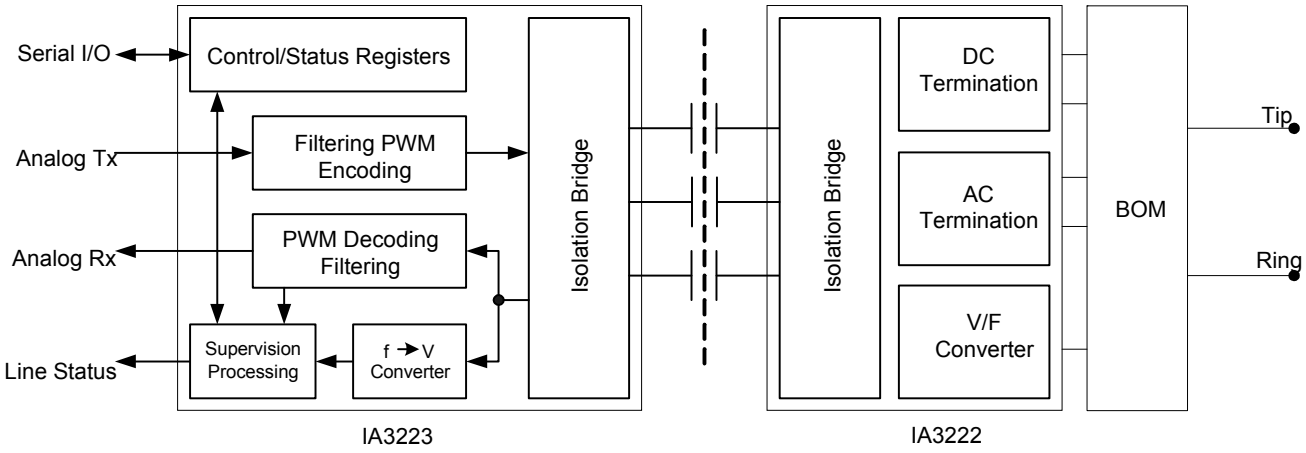


10-Pin MSOP (IA3222B)



U.S. Patent # 7,031,458
U.S. Patent # 7,139,391

Functional Block Diagram



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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
	Operating temperature	–25		85	°C
V_{DD}	Power-supply voltage	3.0	3.3	3.6	V
V_{IL}	Logic-low input voltage	0	—	35	% V_{DD}
V_{IH}	Logic-high input voltage	65	—	100	% V_{DD}
V_{ACREF}	Optional AC_{REF} pin reference voltage*	1.2	—	1.8	V
	AC reference capacitor (pin left open)*	—	100	—	nF
C1	External capacitor #1	—	10	—	nF
C2	External capacitor #2	—	220	—	nF
	RX_{OUT} load resistance	2	—	—	kΩ
	RX_{OUT} load capacitance	—	—	200	pF
	Loop current	20	—	120	mA
	Loop current, degraded performance	14	—	130	mA
	Line voltage for Caller ID power	15	—	70	V
	Internal sampling rate based on external clock	57.6	—	83.333	kHz
tck	Serial clock period	25	—	—	ns
tcssuf	Chip Select fall to clock rising edge setup time	12	—	—	ns
tcssur	Chip Select rise to clock rising edge setup time	12	—	—	ns
tcsh	Chip Select rise or fall to clock rising edge hold time	8	—	—	ns
tdisu	Data in to clock rising edge setup time	12	—	—	ns
tdih	Data in to clock rising edge hold time	8	—	—	ns
	IA3222 power derating over 25 °C ambient	—	6	—	mW/ °C

***Note:** The ACREF pin may be left open, in which case this internal bias voltage needs to be decoupled to the audio ground by means of a 100 nF capacitor. Refer to Table 3, “DC Characteristics,” on page 6 for more information on driving the ACREF pin. Also refer to “5.5. Interfacing Examples” for alternate ways of driving the ACREF pin.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units
Junction operating and storage temperature	–40	150	°C
ESD (human body model)	—	2	kV
Power-supply voltage	–0.5	7	V
Voltage at any pin	–0.5	V_{DD} + 0.5	V
Current at any input or output (System Side)	–100	100	mA
Loop Current (IA3222)	—	150	mA

Table 3. DC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Logic input current		–10	—	10	µA
Logic input hysteresis		—	240	—	mV
Logic output low voltage	I_{OL} = –4 mA	—	—	0.4	V
Logic output high voltage	I_{OH} = 4 mA	0.8	—	—	V_{DD}
Ring-detection threshold	RTH[1:0] = 00	10	—	20	V_{RMS}
	RTH[1:0] = 01	12.5	—	25	V_{RMS}
	RTH[1:0] = 10	15	—	30	V_{RMS}
	RTH[1:0] = 11	20	—	40	V_{RMS}
Voltage at AC_{REF} pin	Pin left open	1.42	1.50	1.58	V
AC_{REF} input resistance	Small signal	42	60	78	kΩ
AC_{REF} input current	Sink or source	—	10	—	µA
Pull-down resistance	ExtClk, OfHk inputs, V = 0.65 V_{DD}	80	—	300	kΩ
Pull-up resistance	LineStat open-drain output, V = 0.35 V_{DD}	80	—	300	kΩ
Power supply current	Off hook, internal clock	—	7.9	—	mA
	Off hook, external clock	—	6.2	—	mA
	On hook	—	3.4	—	mA
	Power down, no external clock	—	2	—	µA
Loop-current sensor gain	Normal headroom, TBR21 mode	—	0.95	—	mV/mA
	All other headroom and impedance modes	—	1.15	—	mV/mA

Table 4. AC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
tcdo	Clock falling edge to Data Out valid from driven or floating state*	—	12	20	ns
tcsdf	Chip Select disabled to Data Out floating*	—	12	20	ns
	Internal sampling rate based on internal clock	67.2	73.4	82.8	kHz
***Note:** Load = 50 pF					

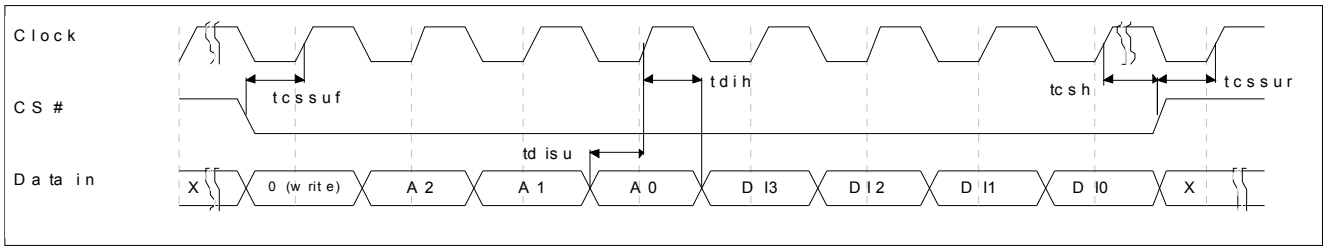


Figure 1. Serial Interface Write-Cycle Timing Diagram (Data Output Pin Floating)

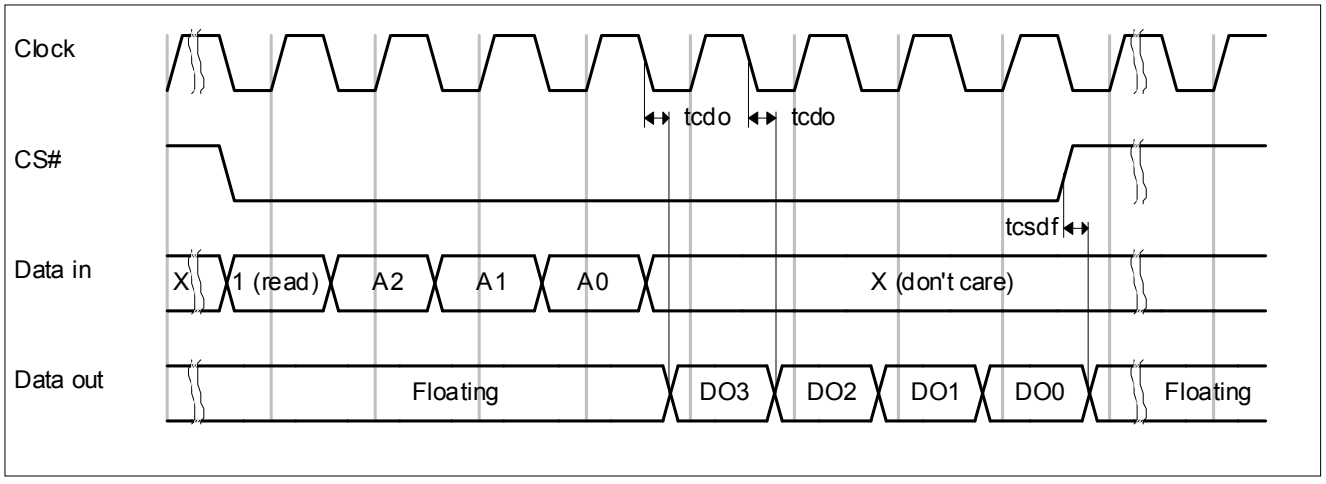


Figure 2. Serial Interface Read-Cycle Timing Diagram

Table 5. Off-Hook Receiver Performance

Parameter	Conditions	Min.	Typ.	Max.	Unit
Idle channel noise referred to Tip and Ring	300–3400 Hz, 600 Ω, internal clock	—	–85	—	dBm
Total harmonic distortion	1 kHz, –7 dBm, normal or high headroom	—	–76	—	dB
Gain from Tip and Ring to RX_{OUT} pin	1 kHz (symmetrical around AC_{REF}), high headroom	—	–3	—	dB
Gain from Tip and Ring to RX_{OUT} pin	1 kHz (symmetrical around AC_{REF}), other headrooms	—	0	—	dB
Receiver power headroom	Sine wave, high headroom, referenced to 600 Ω	0	—	—	dBm
	Sine wave, normal headroom, referenced to 600 Ω	–3	—	—	dBm
	Sine wave, low headroom, referenced to 600 Ω	–3	—	—	dBm
	Sine wave, lowest headroom, referenced to 600 Ω	–5	—	—	dBm
Maximum level at RX_{OUT} pin	1 kHz (symmetrical around AC_{REF})	—	1.55	—	V_{PP}
Power-supply induced noise referred to Tip and Ring	1 kHz, 100 mV_{PP} at V_{DD}, high headroom	—	–84	—	dBV
	1 kHz, 100 mV_{PP} at V_{DD}, other headrooms	—	–87	—	dBV
	f > 3400 Hz, dc coupled, high headroom	—	–66	—	dBV
	f > 3400 Hz, dc coupled, other headrooms	—	–69	—	dBV
Longitudinal balance	f = 1000 Hz	—	99	—	dB
Longitudinal balance	f = 3000 Hz	—	93	—	dB

Table 6. On-Hook Receiver (Caller ID) Performance at 48 V_{DC}

Parameter	Conditions	Min	Typ	Max	Unit
Caller ID noise referred to Tip and Ring	400–3000 Hz, internal clock	—	–48	—	dBV
Caller ID distortion	1 kHz, 100 mV_{RMS}, normal or high headroom	—	–37	—	dB
Caller ID gain, Tip and Ring to AC_{REF}	1 kHz, high gain setting	—	0.5	—	dB
	1 kHz, low gain setting	—	–4.5	—	dB
Maximum level at Tip and Ring	1 kHz, high gain setting	—	–3	—	dBm
	1 kHz, low gain setting	—	+3	—	dBm
Maximum level at Rx pin	1 kHz, high or low gain setting	—	1.55	—	V_{PP}
Power-supply induced noise referred to Tip and Ring	1 kHz, 100 mV_{PP} at V_{DD}, high gain setting	—	–55	—	dBV
	1 kHz, 100 mV_{PP} at V_{DD}, low gain setting	—	–50	—	dBV
Common-mode rejection	120 Hz	120	—	—	dB

Table 7. Transmitter Performance

Parameter	Conditions	Min.	Typ.	Max.	Unit
Idle channel noise referred to Tip and Ring	300–3400 Hz, 600 Ω, internal clock	—	–82	—	dBm
Total harmonic distortion	1 kHz, 3 dB below clipping level, normal or high headroom	—	–78	—	dB
Gain from TX_{IN} pin to Tip and Ring	1 kHz, 600 Ω, referenced to AC_{REF}, high headroom	—	9	—	dB
	1 kHz, 600 Ω, referenced to AC_{REF}, other headrooms	—	6	—	dB
Part-to-part gain variation at 1 kHz, 600 Ω mode, normal headroom	Transmitter gain	—	0.5	—	±dB
	Product of transmitter gain times receiver gain	—	0.5	—	±dB
Transmitter power headroom, sine wave*	LP[5:4] = 00, 600 Ω load	6.5	—	—	dBm
	LP[5:4] = 00, 900 Ω load	5.5	—	—	dBV
	LP[5:4] = 01, 600 Ω load	3	—	—	dBm
	LP[5:4] = 01, 900 Ω load	2	—	—	dBV
	LP[5:4] = 01, Australia or TBR21 load	2	—	—	dBV
	LP[5:4] = 01, New Zealand load	1	—	—	dBV
	LP[5:4] = 10, 600 Ω load, 400–3400 Hz	–5	—	—	dBm
	LP[5:4] = 10, 600 Ω load with bootstrap, 400–3400 Hz	–1	—	—	dBm
	LP[5:4] = 11, 600 Ω load, 400–3400 Hz	–9	—	—	dBm
	LP[5:4] = 11, 600 Ω load with bootstrap, 400–3400 Hz	–3	—	—	dBm
	LP[5:4] = 11, 600 Ω load with bootstrap, DTMF tones	–1	—	—	dBm
TX_{IN} pin input resistance		35	50	65	kΩ
Input common-mode rejection, defined as: $(V(TX_{IN}) + V(AC_{REF})) / 2$	300–3400 Hz, dc-coupled	—	40	—	dB
	f > 3400 Hz, dc-coupled	40	—	—	dB
Power-supply-induced noise referred to Tip and Ring (SGAIN = 0)	1 kHz, 100 mV_{PP} at V_{DD}, high headroom	—	–86	—	dBV
	1 kHz, 100 mV_{PP} at V_{DD}, other headrooms	—	–89	—	dBV
	f > 3400 Hz, dc-coupled, high headroom	–56	—	—	dBV
	f > 3400 Hz, dc-coupled, other headrooms	–59	—	—	dBV
Longitudinal balance	f = 1000 Hz or f = 3000 Hz	90	—	—	dB

***Note:** The bootstrap circuit shown in the application circuit (R18, C16, and Q6) is optional. Its function is to increase the transmit headroom voltage at the low and lowest headroom settings. Those settings should be used only when the dc voltage needs to be minimized for low-voltage countries, such as Japan, Malaysia, etc.

Table 8. Line-Side Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Self-regulated supply voltage		—	2.47	—	V
Current protection threshold		130	170	210	mA
On-hook voltage-protection threshold		110	145	210	V
Temperature-shutdown threshold	Loop current = 130 mA	136	146	156	°C
On-hook dc resistance, Tip to Ring	5.6 MΩ voltage-sensing resistors	5	—	—	MΩ
Ringer equivalent load		—	—	0.1	REN
Return loss at 1 kHz (typical) or 300–3400 Hz (minimum)	600 Ω impedance mode and reference load	20	30	—	dB
	600 Ω + 1 µF impedance mode and reference load	20	30	—	dB
	900 Ω impedance mode and reference load	20	30	—	dB
	900 Ω + 1 µF impedance mode and reference load	20	30	—	dB
	Australia impedance mode and reference load	17	27	—	dB
	New Zealand impedance mode and reference load	20	26	—	dB
	TBR21 impedance mode and reference load	17	27	—	dB
Echo return loss, ITU-T G.122 method	600 Ω impedance mode and reference load	20	30	—	dB
	600 Ω + 1 µF impedance mode and reference load	20	30	—	dB
	900 Ω impedance mode and reference load	20	30	—	dB
	900 Ω + 1 µF impedance mode and reference load	20	28	—	dB
	Australia impedance mode and reference load	20	25	—	dB
	New Zealand impedance mode and reference load	20	26	—	dB
	TBR21 impedance mode and reference load	20	25	—	dB

Table 8. Line-Side Characteristics (Continued)

Parameter	Conditions	Min	Typ	Max	Unit
Transhybrid distortion referred to line	600 Ω load, –10 dBm signal, normal or high headroom	—	–91	—	dBm
Tip-Ring voltage	I_{DD} = 20 mA, no current limit, lowest headroom	—	5.85	6	V
	I_{DD} = 20 mA, no current limit, low headroom	—	6.4	7	V
	I_{DD} = 20 mA, no current limit, normal headroom	—	7.8	9	V
	I_{DD} = 20 mA, no current limit, high headroom	—	9	10	V
	I_{DD} = 42 mA, TBR21 current limit, normal headroom	—	—	14.5	V
	I_{DD} = 50 mA, TBR21 current limit, normal headroom	—	—	40	V
Loop-current limit	TBR21 legacy mode, 50 V, 230 Ω feed	—	—	60	mA

2. Typical Performance Characteristics

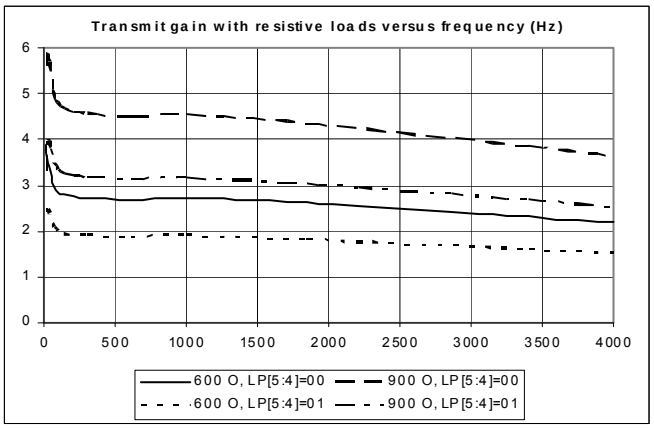


Figure 3. Transmit Gain with Resistive Loads

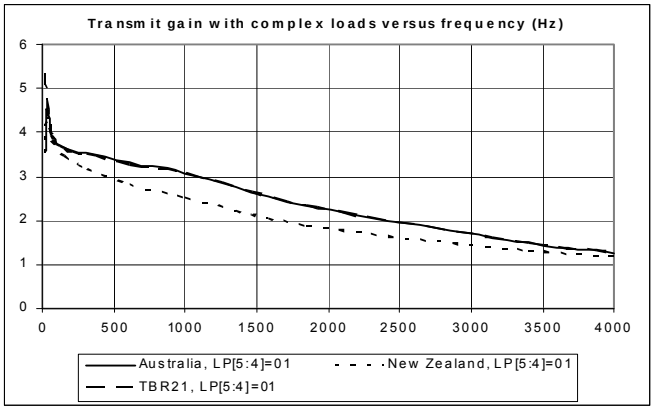


Figure 6. Transmit Gain with Complex Loads

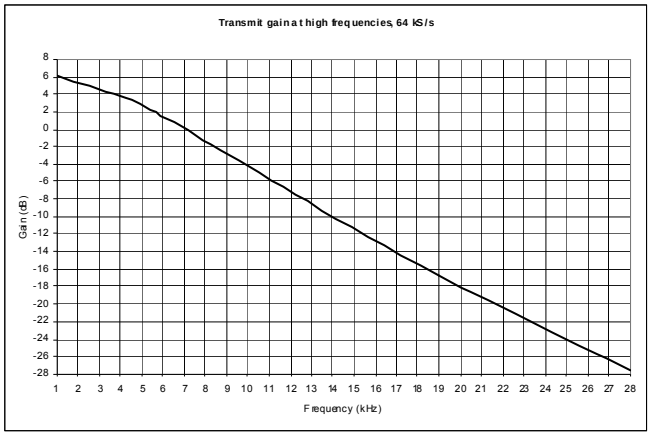


Figure 4. Transmit Gain at High Frequencies (600 Ω)

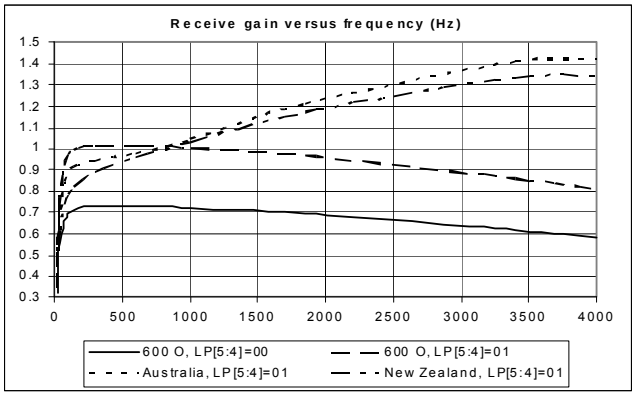


Figure 7. Receive Gain versus Frequency

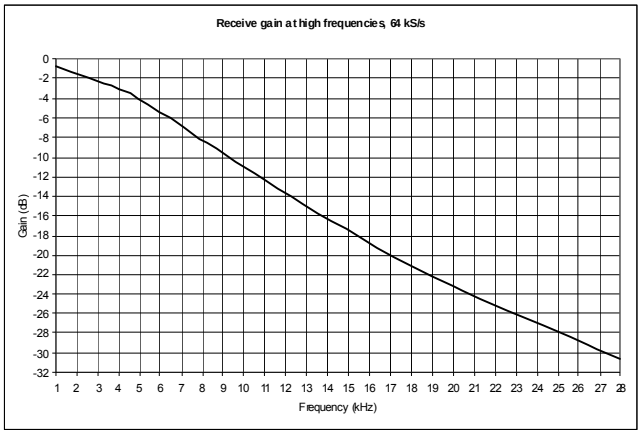


Figure 5. Receive Gain at High Frequencies (600 W)

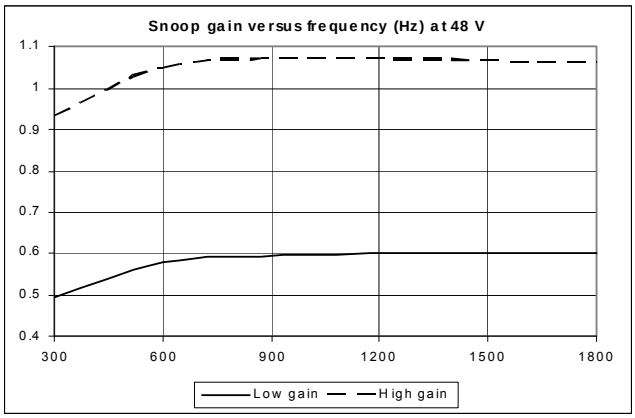


Figure 8. Snoop Gain versus Frequency

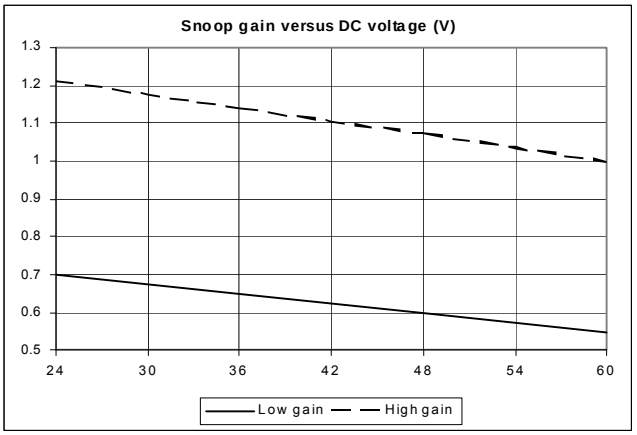


Figure 9. Snoop Gain vs. Line DC Voltage

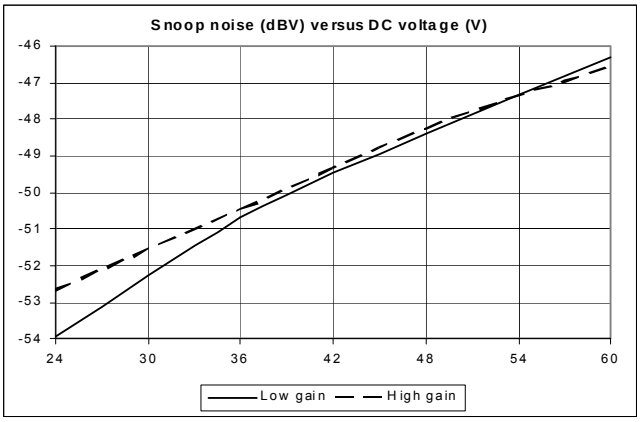


Figure 12. Snoop Noise vs. Line DC Voltage

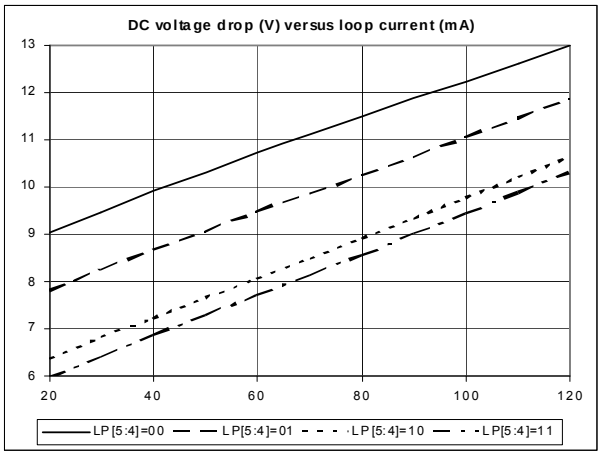


Figure 10. DC Voltage vs. Current, No Regulation

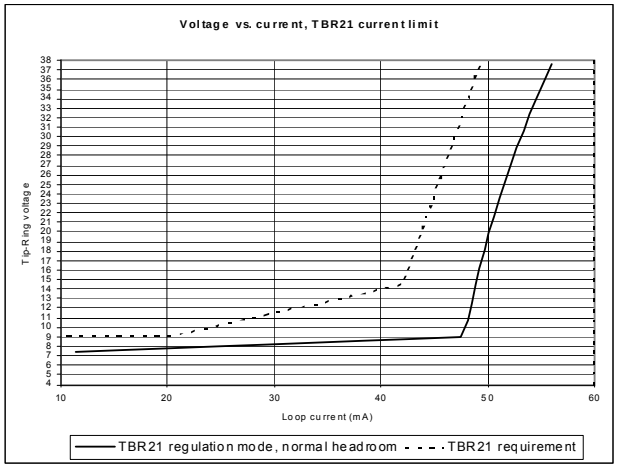


Figure 13. DC Voltage vs. Current, TBR21 Regulation

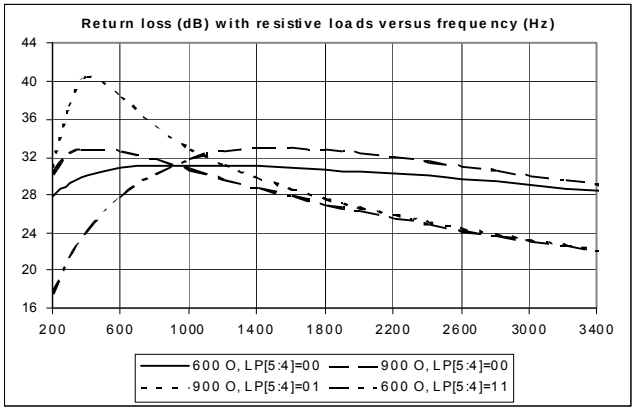


Figure 11. Return Loss for Resistive Modes

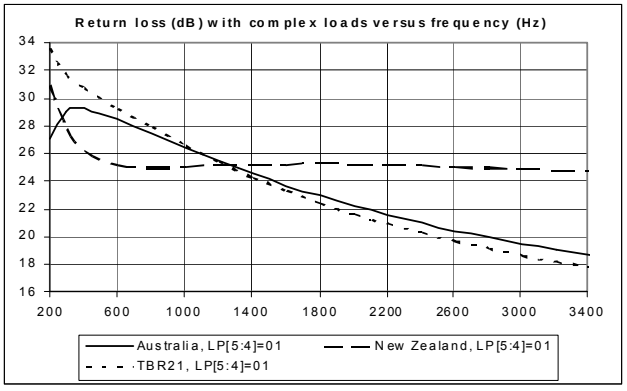


Figure 14. Return Loss for Complex Modes

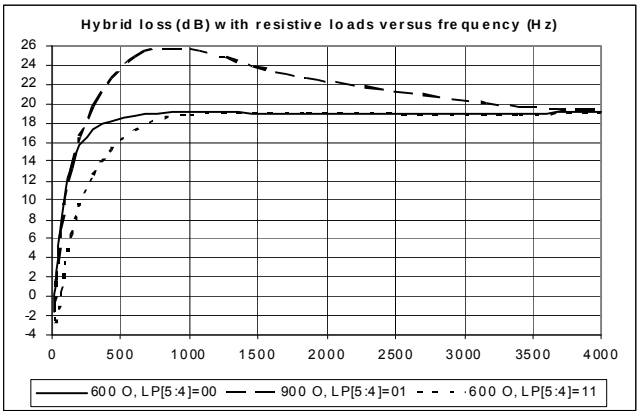


Figure 15. Transhybrid Loss for Resistive Modes

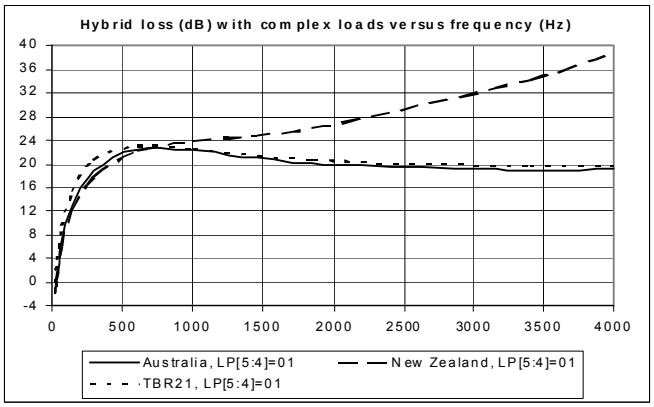


Figure 18. Transhybrid Loss for Complex Modes

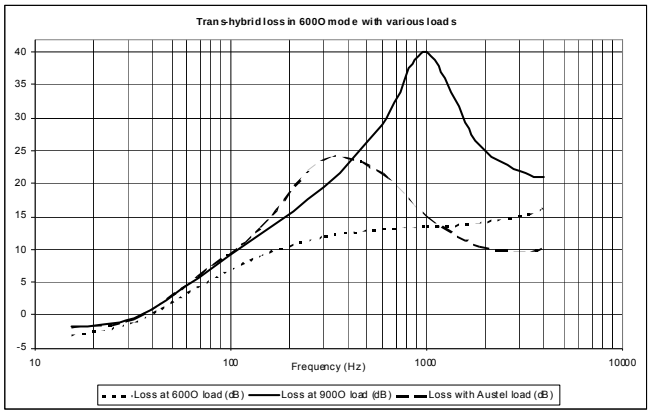


Figure 16. Transhybrid Loss in 600 Ω Mode with Various Loads

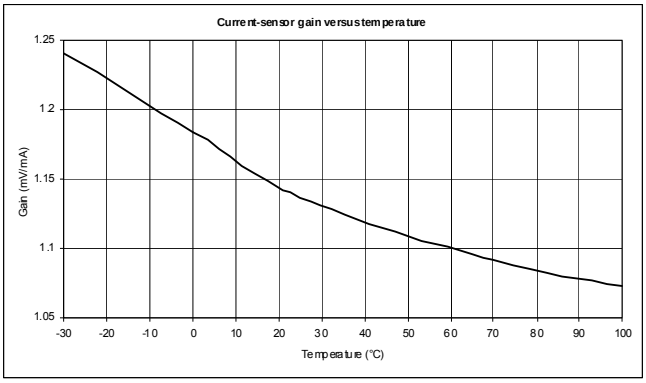


Figure 19. Current Sensor Gain vs. Temperatures

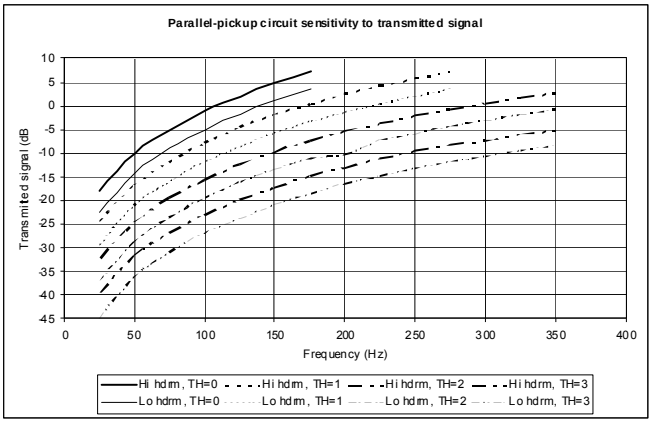


Figure 17. Parallel Pickup Sensitivity to Transmitted Signals

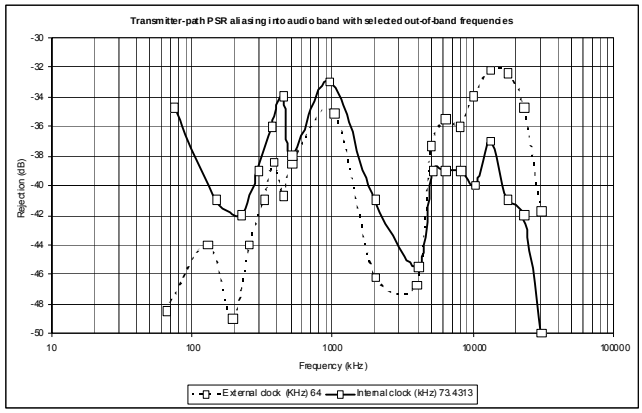


Figure 20. Transmitter-Path PSR Aliasing into Audio Band with Selected Out-of-Band Frequencies

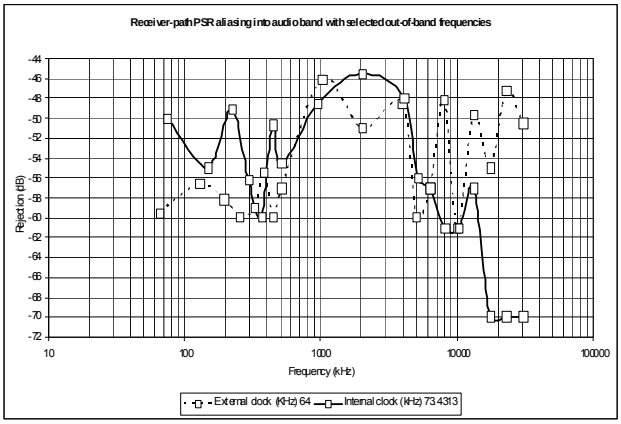


Figure 21. Receiver Path PSR Aliasing into Audio Band with Selected Out-of-Band Frequencies

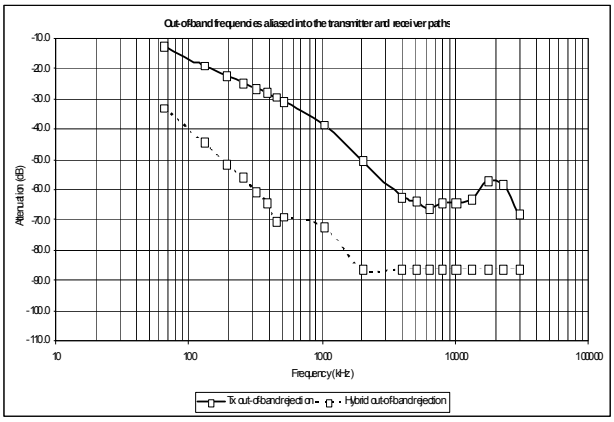


Figure 24. Aliasing into Audio Band (Signals at Selected Out-of-Band Frequencies Injected into TX Pin)

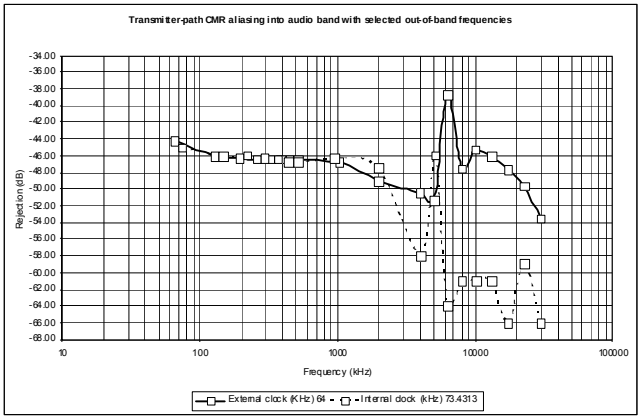


Figure 22. Transmitter-Path CMR Aliasing into Audio Band with Selected Out-of-Band Frequencies

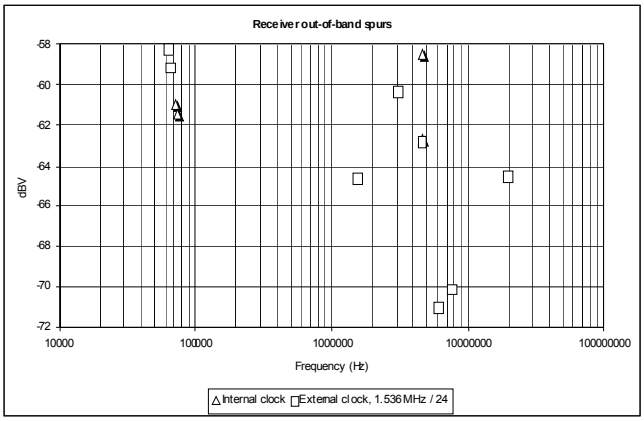


Figure 25. Receiver Out-of-Band Spurs

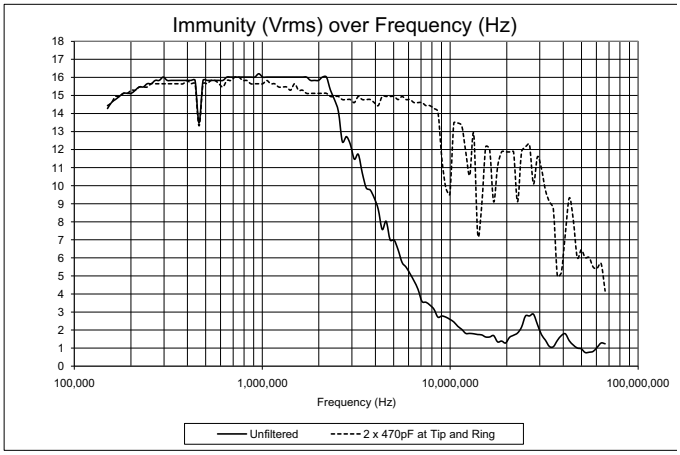


Figure 23. Immunity (Vrms) Over Frequency (Hz)

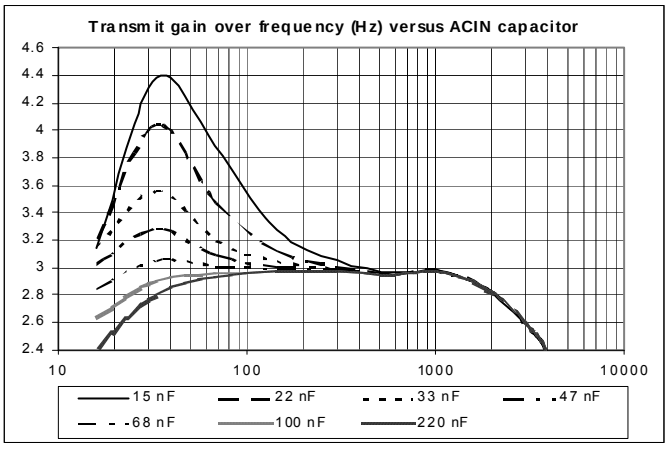


Figure 26. Transmit Gain vs. ACIN Capacitor

3. Applications

3.1. IA3222B for Worldwide Telecom Compliance

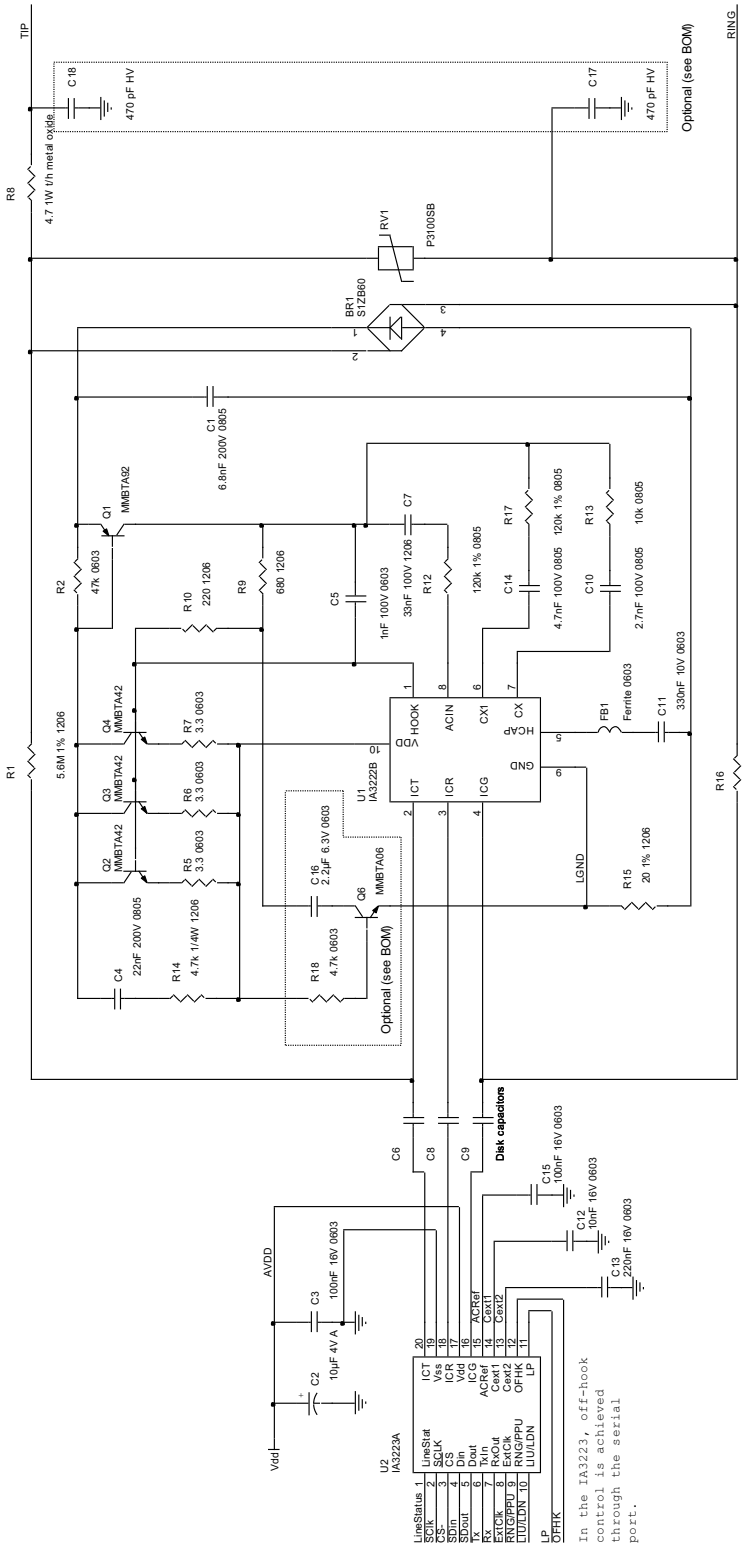


Figure 27. IA3222B Application Schematic

3.2. Bill of Materials

Table 9. IA3222/23 Bill of Materials

Qty	Ref	Part	Part #	Mfr
1	BR1	Rectifier bridge 400 V	S1ZB60	Shindengen
1	C1	6.8 nF 200 V 0805	MCCI682K2NR	SMEC
1	C2	10 µF 4 V	EEE-1CA100SR	Panasonic
2	C3, C15	100 nF 16 V 0603	C0603X7R160-104MNP	Venkel
1	C4	22 nF 200 V 0805	C0805X7R201-223KNP	Venkel
1	C5	1 nF 100 V 0603	C0603X7R101-102MNP	Venkel
3	C6, C8, C9	isolation bridge capacitors, drawn on PCB		
1	C7	33 nF 100 V 1206	C1206X7R101-333KNP	Venkel
1	C11	330 nF 10 V 0603[1]	C0603X7R100-334KNP	Venkel
1	C12	10 nF 16 V 0603	C0603X7R160-103MNP	Venkel
1	C13	220 nF 16 V 0603	C0603X7R160-224MNP	Venkel
1	Q1	PNP, 100 mA, 300 V, SOT23-BEC	MMBTA92LT1	On Semi
3	Q2, Q3, Q4	NPN, 200mA, 300V, SOT23-BEC[2,3]	MMBTA42LT1	On Semi
1	RV1	Sidactor, 275 V, D0-214AA	P3100SBL	Littelfuse
2	R1, R16	5.6 M Ω 1% 1206	CR1206-8W-5904FT	Venkel
1	R2	47 kΩ 0603	CR0603-16W-473JT	Venkel
3	R5, R6, R7	3.3 Ω 0603[2,3]	CR0603-16W-3R3JT	Venkel
1	R9	680 Ω 1206	CR1206-8W-681JT	Venkel

Notes:

1. For optimal audio performance, C11 (0.33 uF & V>=10) should be an aluminum electrolytic capacitor with the positive end connected to HCAP through FB1. This is due to micro phonic noise that can be generated by a ceramic cap when the PCB is less than the typical 0.062” thickness and there are vibration sources in the application. EKMG500ELLR33ME11D is an appropriate alternative in this case.
2. If the loop current is never more than 60 mA, Q4 and R7 may be omitted, and R5 and R6 may be 2.2 Ω.
3. Do not replace Q2, Q3, Q4, R5, R6, and R7 with a single transistor of PZTA42 type. Power transistors with a higher gain-bandwidth product may be used, but often they are not cost-effective. Refer to the component discussion for more details.
4. C10 and C14 need to be NPO if V.90 modem performance is required. Otherwise, it is more cost-effective to use X7R ceramic capacitors. Refer to “7.3. Line-Side Programming Registers” to determine whether C10 or C14 is required.

Table 9. IA3222/23 Bill of Materials (Continued)

Qty	Ref	Part	Part #	Mfr
1	R10	220 Ω 1206	CR1206-8W-221JT	Venkel
1	R12	120 kΩ 1% 0805	CR0805-10W-1203FT	Venkel
1	R14	4.7 kΩ 1206	CR1206-8W-472JT	Venkel
1	R15	20 Ω 1% 1206	CR1206-8W-20R0FT	Venkel
2	U1, U2	DAA chipset	IA3222B, IA3223A	Silicon Labs
Option	C16	2.2 µF 6.3 V 0603 (only if more signal headroom is needed at the low or lowest headroom setting)	C0603X7R6R3-225KNP	Venkel
Option	Q6	MMBTA06 (only if more signal headroom is needed at the low or lowest headroom setting)	MMBTA06LT1	On Semi
Option	R18	4.7 kΩ 0603 (only if more signal headroom is needed at the low or lowest headroom setting)	CR0603-16W-472JT	Venkel
Option	R8	4.7 Ω through-hole metal-oxide or other fusible resistor (only for UL 60950 or equivalent requirement)	ERX-1SJ4R7A	Panasonic
Option	C10	2.7 nF 100V 0805 (Use only if C_X is required.)[4]	C0805X7R101-272KNP	Venkel
Option	R13	10 kΩ 0805 (Use only if C_X is required.)[4]	CR0805-10W-103JT	Venkel
Option	C14	4.7 nF 100 V 0805 (Use only if C_{X1} is required)[4]	C0805X7R101-472MNP	Venkel
Option	R17	120 kΩ 1% 0805 (Use only if C_{X1} is required.)[4]	CR0805-10W-1203FT	Venkel
Option	FB1	Ferrite bead, 0603, 600 Ω at 100 MHz (required for EN 55024 and equivalent immunity requirements)	BK1608H-S601-T	Taiyo Yuden
Option	C17,C18	470 pF (required for EN 55024 and equivalent immunity requirements; voltage rating depends on safety requirements)	CS85-B2GA471KYNS	TDK

Notes:

1. For optimal audio performance, C11 (0.33 uF & V>=10) should be an aluminum electrolytic capacitor with the positive end connected to HCAP through FB1. This is due to micro phonic noise that can be generated by a ceramic cap when the PCB is less than the typical 0.062" thickness and there are vibration sources in the application. EKMG500ELLR33ME11D is an appropriate alternative in this case.
2. If the loop current is never more than 60 mA, Q4 and R7 may be omitted, and R5 and R6 may be 2.2 Ω.
3. Do not replace Q2, Q3, Q4, R5, R6, and R7 with a single transistor of PZTA42 type. Power transistors with a higher gain-bandwidth product may be used, but often they are not cost-effective. Refer to the component discussion for more details.
4. C10 and C14 need to be NPO if V.90 modem performance is required. Otherwise, it is more cost-effective to use X7R ceramic capacitors. Refer to "7.3. Line-Side Programming Registers" to determine whether C10 or C14 is required.

3.3. Application Schematic (Legacy TBR21 Current-Limit Support)

TBR21 current limiting is no longer required in Europe but may still be required for certain countries, e.g. Algeria, Bahrain, Croatia, Estonia, Ghana, Ivory Coast, Lebanon, Morocco, and Turkey. This application circuit is also suitable for all other countries.

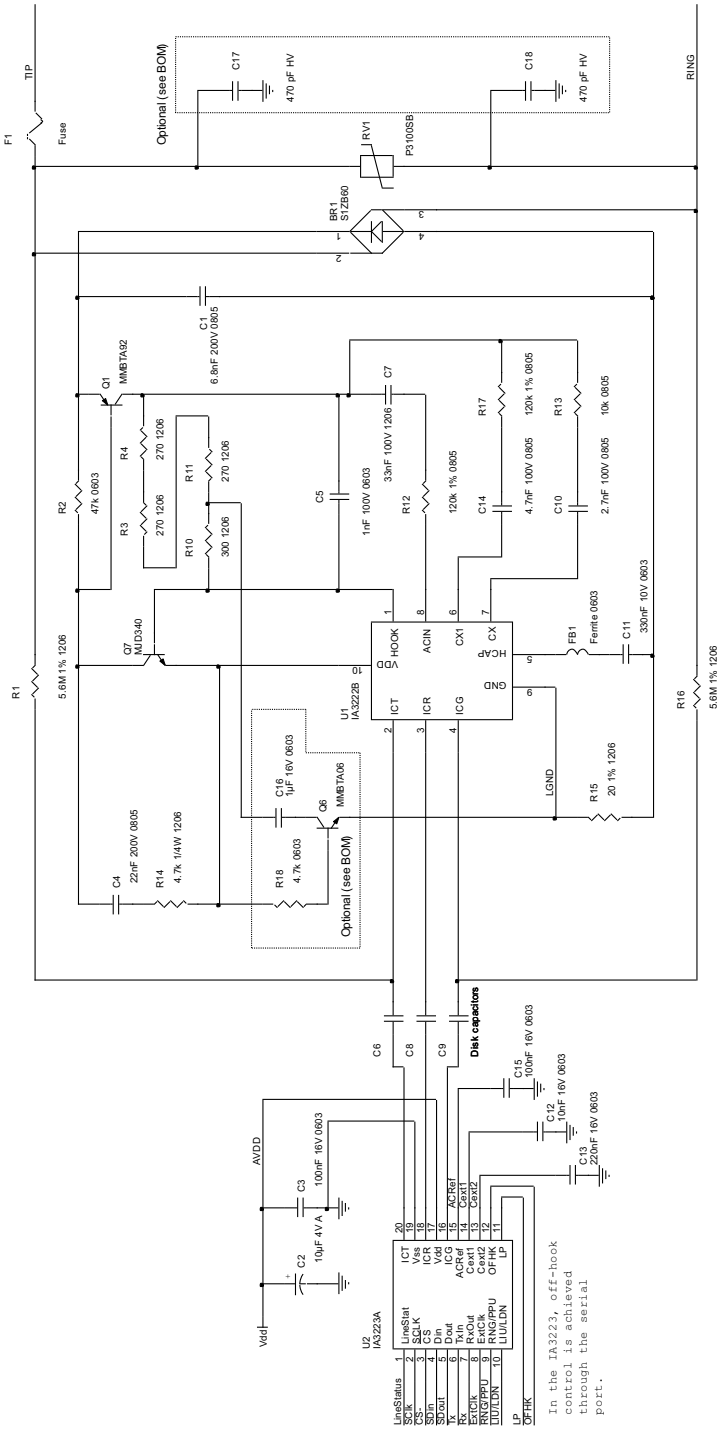


Figure 28. Legacy TBR21 Current-Limit Support Application Schematic

3.4. Bill of Materials (Legacy TBR21 Current-Limit Support)

Table 10. Legacy TBR21 Current-Limit Support Bill of Materials

Qty	Ref	Part	Part #	Mfr
1	BR1	Rectifier bridge 400 V	S1ZB60	Shindengen
1	C1	6.8 nF 200 V 0805	MCCI682K2NR	SMEC
1	C2	10 µF 4 V	EEE-1CA100SR	Panasonic
2	C3, C15	100 nF 16 V 0603	C0603X7R160-104MNP	Venkel
1	C4	22 nF 200 V 0805	C0805X7R201-223KNP	Venkel
1	C5	1 nF 100 V 0603	C0603X7R101-102MNP	Venkel
3	C6, C8, C9	isolation bridge capacitors, drawn on PCB		
1	C7	33 nF 100 V 1206	C1206X7R101-333KNP	Venkel
1	C11	330 nF 10 V 0603[1]	C0603X7R100-334KNP	Venkel
1	C12	10 nF 16 V 0603	C0603X7R160-103MNP	Venkel
1	C13	220 nF 16 V 0603	C0603X7R160-224MNP	Venkel
1	Q1	PNP, 100 mA, 300V, SOT23-BEC	MMBTA92LT1	On Semi
1	Q7	NPN, 300 V, D-PAK	MJD340	Fairchild
1	RV1	Sidactor, 275 V, DO-214AA	P3100SBL	Littelfuse
2	R1, R16	5.6 MΩ 1% 1206	CR1206-8W-5904FT	Venkel
1	R2	47 kΩ 0603	CR0603-16W-473JT	Venkel
3	R3, R4, R11	270 Ω 1206	CR1206-8W-271JT	Venkel
1	R10	300 Ω 1206	CR1206-8W-301JT	Venkel
1	R12	120 kΩ 1% 0805	CR0805-10W-1203FT	Venkel
1	R14	4.7 kΩ 1206	CR1206-8W-472JT	Venkel

Notes:

1. For optimal audio performance, C11 (0.33 uF & V>=10) should be an aluminum electrolytic capacitor with the positive end connected to HCAP through FB1. This is due to micro phonic noise that can be generated by a ceramic cap when the PCB is less than the typical 0.062” thickness and there are vibration sources in the application. United Chemi-Con EKMG500ELLR33ME11D is an appropriate alternative in this case.
2. C10 and C14 need to be NPO if V.90 modem performance is required. Otherwise, it is more cost effective to use X7R ceramic capacitors. Refer to “7.3. Line-Side Programming Registers” to determine whether C10 or C14 is required.

Table 10. Legacy TBR21 Current-Limit Support Bill of Materials (Continued)

Qty	Ref	Part	Part #	Mfr
1	R15	20 Ω 1% 1206	CR1206-8W-20R0FT	Venkel
2	U1, U2	DAA Chipset	IA3222B, IA3223A	Siicon Labs
Option	C16	1 µF 16 V 0603 (only if more signal headroom is needed at the low or lowest headroom setting)	C0603X7R160-105KNP	Venkel
Option	Q6	MMBTA06 (only if more signal headroom is needed at the low or lowest headroom setting)	MMBTA06LT1	On Semi
Option	R18	4.7 kΩ 0603 (only if more signal headroom is needed at the low or lowest headroom setting)	CR0603-16W-472JT	Venkel
Option	F1	Fuse (only for UL 60950 or equivalent requirement)		
Option	C10	2.7 nF 100 V 0805 (Use only if C_X is required)[2]	C0805X7R101-272KNP	Venkel
Option	R13	10 kΩ 0805 (Use only if C_X is required.)[2]	CR0805-10W-103JT	Venkel
Option	C14	4.7 nF 100 V 0805 (Use only if C_{X1} is required.)[2]	C0805X7R101-472MNP	Venkel
Option	R17	120 kΩ 1% 0805 (Use only if C_{X1} is required.)[2]	CR0805-10W-1203FT	Venkel
Option	FB1	Ferrite bead, 0603, 600 Ω at 100 MHz (required for EN 55024 and equivalent immunity requirements)	BK1608HS601-T	Taiyo Yuden
Option	C17,C18	470 pF (required for EN 55024 and equivalent immunity requirements; voltage rating depends on safety requirements)	CS85-B2GA471KYNS	TDK

Notes:

1. For optimal audio performance, C11 (0.33 uF & V>=10) should be an aluminum electrolytic capacitor with the positive end connected to HCAP through FB1. This is due to micro phonic noise that can be generated by a ceramic cap when the PCB is less than the typical 0.062” thickness and there are vibration sources in the application. United Chemi-Con EKMG500ELLR33ME11D is an appropriate alternative in this case.
2. C10 and C14 need to be NPO if V.90 modem performance is required. Otherwise, it is more cost effective to use X7R ceramic capacitors. Refer to “7.3. Line-Side Programming Registers” to determine whether C10 or C14 is required.

4. Overview

The chipset provides a low-cost, worldwide-compliant telephone line interface. Due to its high level of integration, only a few external components are required for operation. Its patented isolation bridge technology eliminates the need for costly and bulky transformers yet still ensures a high level of isolation between the phone line and the system side.

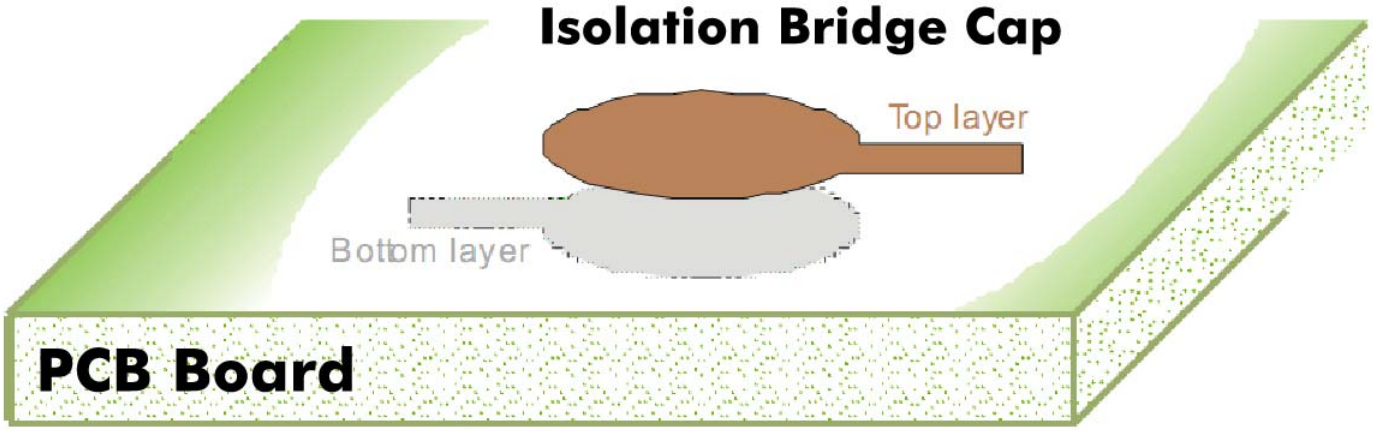
4.1. Analog Interface

The DAA is easily interfaced using single-ended transmitters and receivers. An extra input pin can be used to set the dc reference, thus facilitating an interface with or without coupling capacitors. Refer to the applications section below for more details.

4.2. Isolation Barrier

In most cases, equipment meant to be connected to the Public Switch Telephone Network must comply with specific safety requirements, including the implementation of a high-voltage isolation barrier between the telephone line side and the system side. Various standards require the isolation barrier to withstand from 1000 to 3000VAC. The chipset implements a high-voltage isolation barrier between the IA3223 codec and its IA3222 line-side device by means of its patented isolation bridge technology. Where typical designs use costly transformers or optocouplers, isolation bridge reduces the total bill of materials cost by embedding high-voltage capacitors in the PCB. This unique technique allows for virtually zero-cost capacitors.

PCB board material, thickness, trace width, and pad dimensions determine the capacitance achieved by this technique. The IA3222/IA3223 requires three 0.7 pF (nominal) capacitors and is designed to operate over the wide variations seen in standard PCB materials.



The application requires three PCB capacitors whose diameters range typically from 140 to 190 mils depending on the thickness of the board.

4.3. International Compliance

The chipset can be programmed to meet the variety of telecommunication requirements and standards worldwide through the serial loading of two registers.

4.4. Serial Interface

The IA3222/IA3223 can be programmed using a simple asynchronous serial protocol independent of the audio path.

When $\overline{CS}$ is low (active), the first clock rising edge latches the read or write command. The next three clock edges latch a three-bit register address. The next four clock rising edges serially shift a four-bit data word in, or the next four clock falling edges serially shift a four-bit data word out, depending on the status of the read/write command. Refer to the timing diagrams in the specification section for more details on the serial interface.

4.5. International Programming Sequence

International programming options are loaded into the system side and updated to the line side upon any of the following events:

- Register loading if the line side is in the off-hook state
- When the line side is made to go off hook
- When the line side recovers from a line interruption

4.6. Hook Switch Control

The DAA is set to on-hook or off-hook by writing the OFH bit in the control register through the serial interface or through the use of the OFHK pin if using the IA3223A (QSOP-20).

4.7. Line Overload Protection

The chipset provides a built-in line-overload protection circuit to protect the IA3222 line-side device from unusual telephone line conditions, which can result in excessive voltage or current conditions. If the IA3222 senses an excessive line voltage (about 100 V) when on-hook, it will not go off-hook even when an off-hook state is set in the control register. If the IA3222 senses an excessive loop current (about 170 mA) when off-hook, it will immediately go on-hook. This results in oscillation since, in this case, the IA3222 still sees an off-hook command and, therefore, keeps trying to go back off-hook. While a fault condition exists, the LD status bit is high.

4.8. DC Termination (Voltage Drop vs. Loop Current)

The chipset offers four main dc termination modes and current-limiting support specific for legacy TBR21 countries. Since TBR21 has been superseded by ES 203 021, European countries no longer require on-current limiting. The four main dc termination modes ensure that any country's I/V curve requirement can be met. The maximum transmit level is different for each setting.

Legacy TBR21 (current limiting) support is possible but not recommended since so few countries require it and the standard has been superseded. In order to meet TBR21 current limiting requirements, a DAA needs to dissipate 2 W safely. In the IA3222/3223 application, about half of this power is dissipated in R3, R4, R10, and R11, and the other half in the NPN transistor.

4.9. AC Termination (Line Impedance Matching)

The chipset offers several different ac terminations selectable through the serial port. These ac terminations can be combined with any dc termination selected to address a country's loop interface requirements.

4.10. DTMF Dialing

DTMF dialing is controlled by the host, and only a few parameters in the IA3223, such as the gain and maximum transmission level, need to be set prior to dialing.

4.11. Pulse Dialing

Pulse dialing is accomplished by going on-hook and off-hook repeatedly to generate make and break pulses. It is the host's responsibility to implement the timing related to pulse dialing, such as make/break times and ratio, inter-digit pause, and pulses per second. The IA3222 meets international "spark quenching" requirements.

4.12. Caller ID

When the device is on-hook, the Caller ID audio signal is available at the receiver output pin of the IA3223. This function is achieved while maintaining the high on-hook impedance required by telecom regulations. The gain can be set high (0 dB) for normal operation or low (–6 dB) for DTMF monitoring.

4.13. Power-Down Mode

In order to reduce power consumption, it is possible to set the IA3223 to power-down mode. In this state, the device will not go off-hook or monitor the line.

5. Functional Description

5.1. Component Discussion

The application schematic shown in Figure 27 on page 17 is intended as a high-density surface-mount solution. When using through-hole components, some changes may be possible in the design.

The main hook switch is composed of three parallel NPN transistors (Q2–Q4) and three emitter ballasting resistors (R5–R7). This structure is necessary when using low-cost, generic 300 V transistors in order to keep these transistors out of their quasi-saturation region at high loop currents.

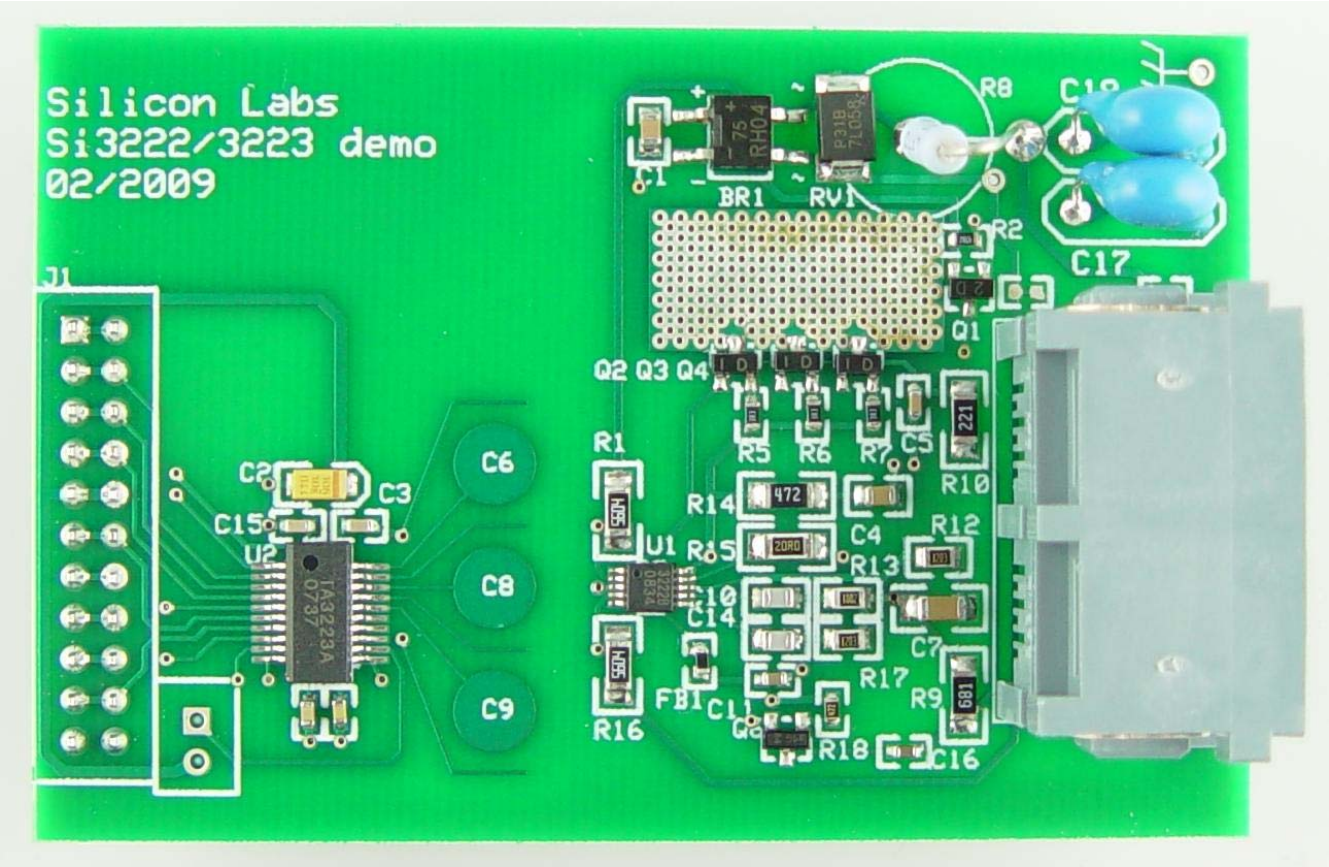


Figure 29. IA3222/3223 Evaluation Board

5.2. Sample Layout

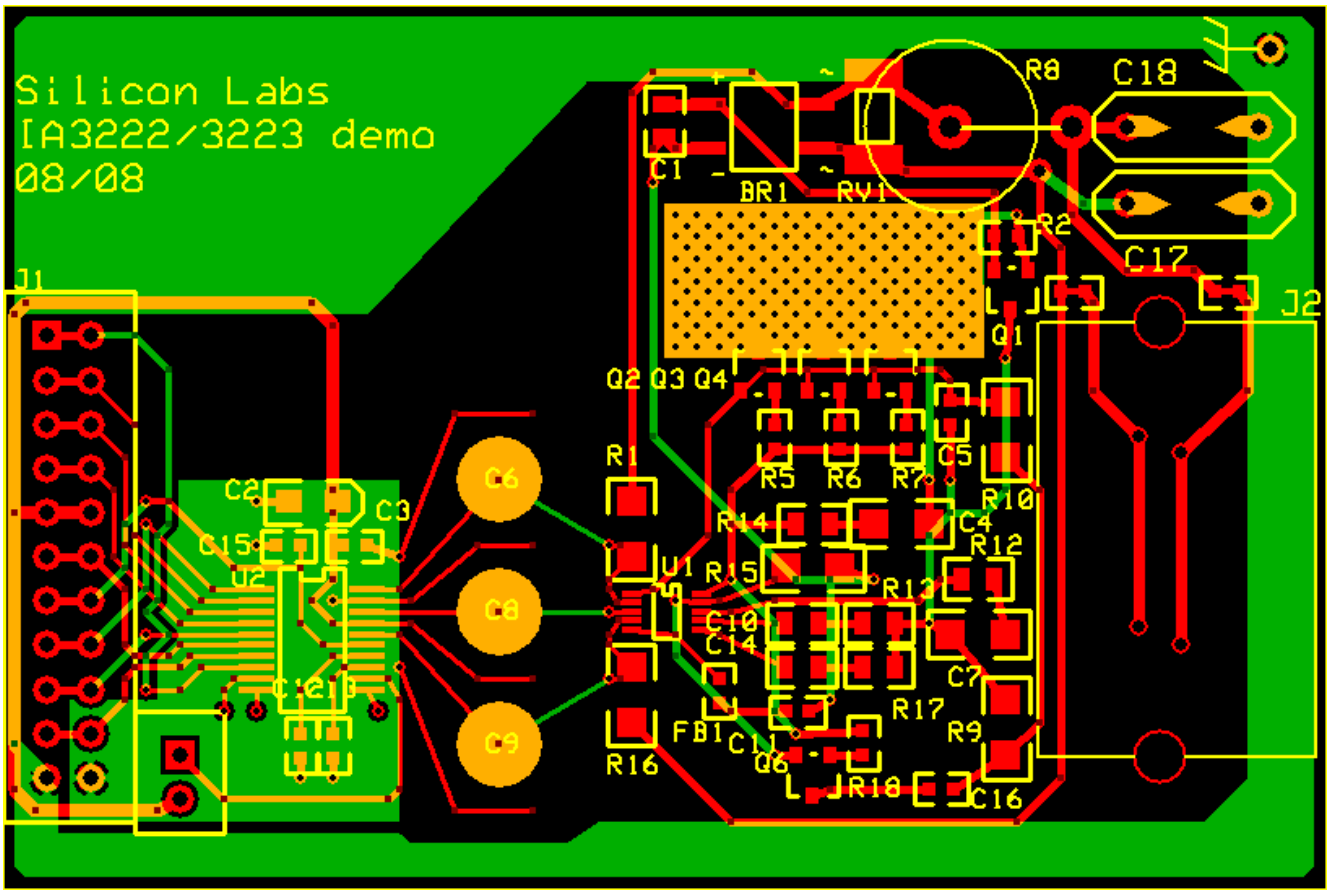


Figure 30. IA3222/3223 Evaluation Board Layout

5.3. Layout Guidelines

- Minimize trace lengths between U1, R1, and R15.
- Disc capacitors and their connecting traces should be drawn exactly as shown, with 4.95 mm (195 mils) diameters, 2.5 mm (98.5 mils) spacing and 10 mil traces in between on the system side only. All dimensions must match. This assumes a standard board thickness (0.062") and FR-4 material. Contact Silicon Labs for other board thicknesses or materials.
- Carefully observe the required creepage distance (surface distance over isolation) for surge rating. There must be at least 2.5 mm (98.5 mils) between any line-side conductive trace and any system-side conductive trace, including the mounting holes if they are electrically connected. Because of PCB manufacturing tolerances, the minimum drawn distances should be about 2% larger, or 2.55 mm (100.5 mils). It is a good practice to designate a "preferred arc path" between the Tip and Ring lines and the chassis, e.g. at the RJ-11 connector, by drawing those at the minimum required distance, while all other spacings between Line Side and System Side are drawn lightly larger, e.g. 2.8 mm (110 mils).
- Put no metal markings in the area of the disk capacitors. This must be watched closely, since PCB manufacturers routinely add markings wherever they find it convenient, possibly shortening the creepage distance.
- Place a ground plane under U2 and all capacitors connected directly to it as shown in the sample layout. Note the separation between chassis ground and system ground.
- Q2, Q3, and Q4 should be laid out with plenty of extra copper on both sides of the board with thermal vias in order to facilitate heat dissipation. Provide details, such as copper area, via density, etc.

5.4. Interfacing the IA3223

The simplified block diagrams in Figures 31, 32, and 33 show a single-ended interface to the A/D and D/A. The analog interface consists of three pins:

- TX—audio input
- RX—audio output
- ACREF—AC voltage reference

There are two ways to interface to the A/D and D/A: dc coupling and ac coupling.

5.4.1. DC Coupling

All three pins, TX, RX, and ACREF, are connected to the codec directly. The ACREF pin has a weak internal buffer (see Table 3, “DC Characteristics,” on page 6), which can easily be overdriven with an external reference. The external reference voltage must be in the 1.2 to 1.8 V range. Connecting the codec's ac reference to the ACREF pin will ensure good common-mode rejection.

One of the advantages of dc coupling is an alternative way for the host processor to detect parallel pick-up (PPU). PPU may be detected using the LINESTAT pin, as described in the next section. The alternative way is to monitor the dc offset at the RX pin. (Line-Side programming bit LP1 must be set to zero.) The dc loop current is added to the RX signal as a dc offset with a gain of about 1 mV/mA. Applying a digital low-pass filter to the RX channel audio enables the detection of a drop in the dc loop current, thus indicating a PPU event.

5.4.2. AC Coupling

All three pins, TX, RX, and ACREF, may also be connected to the codec using coupling capacitors. For the ACREF pin, a capacitor of at least 100 nF is recommended. All coupling capacitors should be selected so that they will not cause any significant attenuation at low frequencies (taking input resistances into account). The TX pin is internally biased at 1.5 V.

5.5. Interfacing Examples

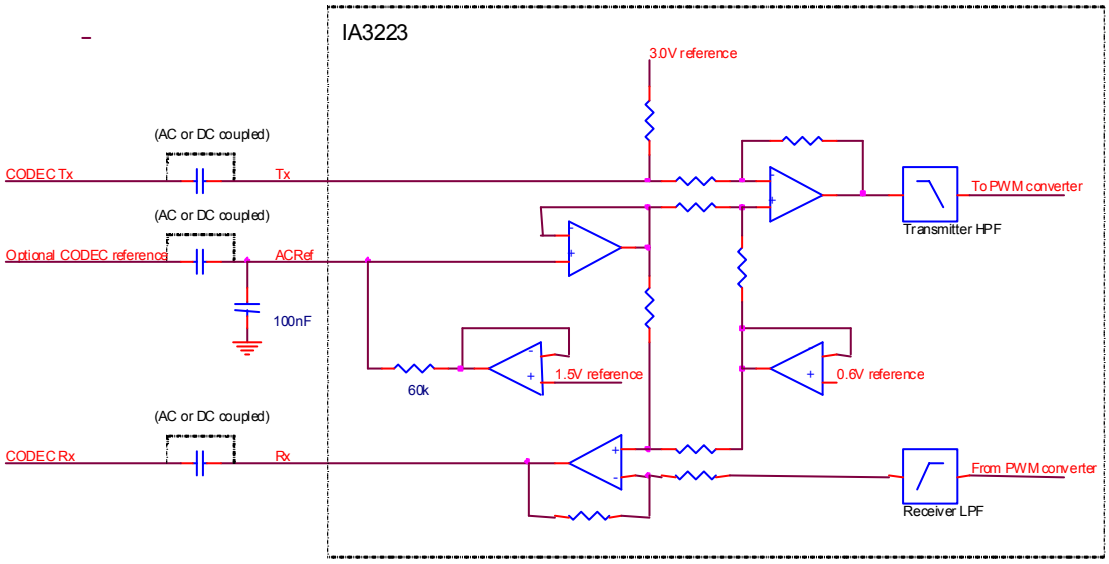


Figure 31. Single-Ended Interface

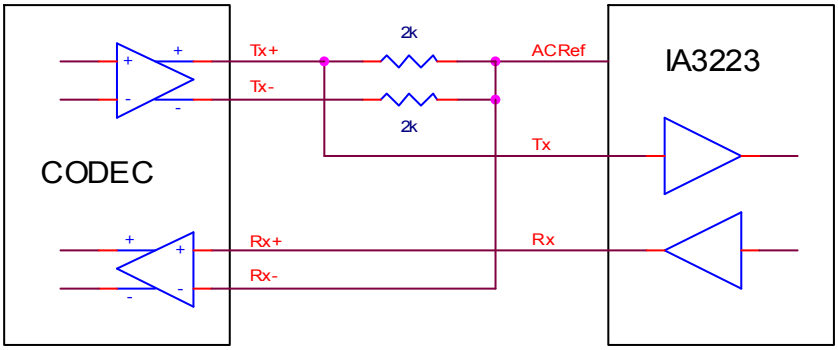


Figure 32. Differential interface (Without Reference)

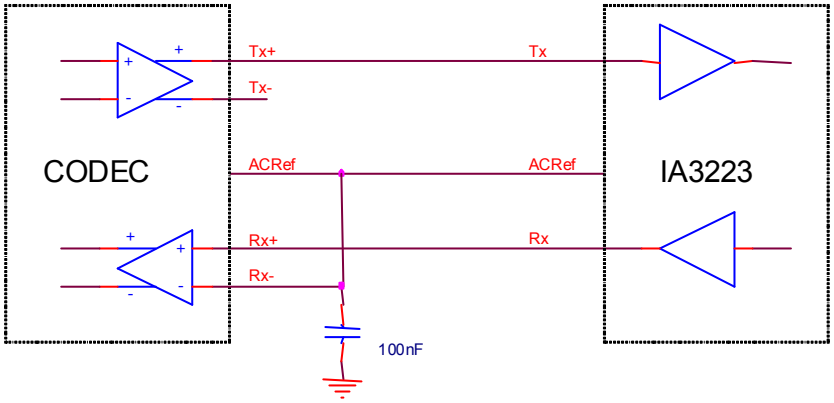


Figure 33. Differential Interface (With Reference)

6. Line Monitoring

6.1. On-Hook Line Status Theory of Operation

The IA3222/3223 chipset was designed to provide ac and dc information about the telephone line and allow intelligent line management and automatic telephone devices to share the line with human-controlled applications. Automatic DAA applications may be found in set-top boxes, alarm systems, fax machines, meter readers, remote-diagnostic modems, answering machines, VoIP boxes, etc. A key feature of the IA3223 is the LineStat pin, which can be programmed to generate an interrupt if the line status changes either while in the on-hook or off-hook state. This reduces the need for continuous polling of the line-status bits.

In the on-hook state, the IA3222 Line Side chip converts the line voltage to a frequency at the rate of 2 kHz per volt. The voltage-to-frequency converter (V-to-f) operating range is from ±3 to over ±150 V. This frequency is sent as pulses across the capacitor isolation barrier. The pulse duty cycle contains line-polarity information. The V-to-f converter's signal is sufficient to allow the IA3223 System Side to decode all dc line voltage, ring signals, line reversals, and audio information (Caller ID, DTMF, and other tone monitoring). While monitoring the line in the on-hook state, the Line Side is greater than 5 MΩ dc resistance. This allows continuous monitoring while exceeding regulatory minimum idle-line resistance requirements.

The IA3223 System Side chip receives the frequency-encoded voltage information and converts it back to a continuous representation of the line voltage. The voltage difference between the ac pin and the CExt2 pin is about 1/200th of the line voltage. The dc source resistance of CExt2 is about 75 kΩ. Measuring this voltage requires a high impedance (>10 MΩ) to prevent excessive loading.

CExt1 is part of a gyrator circuit that separates the large dc line voltage from the low-level ac voltage; so, the line audio signal may be amplified without excessive offset. CExt1 sets the low-frequency corner on this gyrator. With CE x t1 = 10 nF, the –3 dB corner is around 240 Hz, and the slope is 6 dB per octave. The upper-frequency corner is around 4 kHz set by internal RC values and rolls off at approximately 18 dB per octave.

In the on-hook state, CExt2 filters the line voltage analog with a time constant of CExt2 times 75 kΩ, for separating the ac ring signal from the dc line voltage. With a CExt2 of 220 nF, the corner frequency is about 10 Hz. The ring-detection circuit compares the voltage on CExt2 with an internal unfiltered signal. If the CE x t2 voltage exceeds one of the four programmable thresholds in one direction, a ring-detection condition occurs. This produces a standard half-wave ring-detection signal that works similarly to a standard opto-isolator ring-detection circuit.

In addition to ring detection, the other on-hook functions are line-polarity (LP) detection, line-in-use detection (LIU), and line-activity (LACT) detection. The LIU detector measures whether the line voltage exceeds one of four programmed voltage levels. The LACT detector output is activated if the line voltage changes by more than 10 to 20 V, thus acting like a sensitive full-wave ring detector. All of these signals can be read from IA3223 registers. Depending on the setting of the LSR bit, either the ring-detection signal or the LACT signal can be output to the LineStat (line status) pin.

6.2. Ringing

The IA3223 supports conventional ring-detection algorithms that produce an on-off digital output when the ac ring signal exceeds a preset threshold. The period between cycles is measured by the host to within 1–2 ms to qualify ring signals and differentiate them from other line signals, such as on/off-hook transients, dial pulses, and test signals sent by the telephone company. The ring-detection state is presented on the RNG bit and may optionally be multiplexed to the LineStat pin. The width of the ring-detection pulse is always at least 20% of the ring period for sine-wave ring signals.

Many regulatory ring requirements have disappeared in the last fifteen years, and the use of pulse dialing has also decreased. Years ago, when telephone companies were monopolies, 10 V_{RMS} signals were sent down telephone lines in order to determine how many ringer loads were present. Although this probably no longer occurs, conventional wisdom is that ring detectors should not trip below 10 V_{RMS}. Many country-specific regulations and EIA/TIA recommendations still support this requirement.

The most common spurious ring detection is due to pulse dialing. Most countries use 10 pulses per second (pps) for pulse dialing. Japan uses both 10 and 20 pps. The simple way to prevent spurious ring detection from dial pulses is to set a sufficiently high ring-detection threshold.

In countries that have strong ring signals, setting one of the upper two thresholds (22.5 or 30 V_{RMS}) will prevent ring detection of most dial pulses. The first pulse may still be detected because the initial dial pulse or off-hook transient may present a large signal to the ring-detection circuit. Subsequent dial pulses will fall below the ring threshold as the dc-averaging circuit centers the ac waveform. This problem can be seen with all conventional ring detectors. This is why ring-detection algorithms always need to qualify at least two ring cycles by ensuring they fall within the time limits that correspond to the ring frequency.

In some countries, such as the UK and Australia, low ring thresholds are desired. Rather than setting ring threshold, period, and number of valid cycles for every country, it is simpler to divide the whole world into a few separate ring qualification groups. Valid ring signals are between 15 and 68 Hz. Ring cadences are usually less than 2 seconds on but may be on as little as 0.2 seconds for distinctive ringing. If a 1 ms period resolution is available, and assuming a tolerance of ±10% ±1 ms, the valid period range is 12 to 74 ms. These period limits screen out 10 pps but not 20 pps pulse dialers. An example of two ring qualifier groups would be:

- Set lowest ring threshold (15 V_{RMS}), qualify ring period 12 to 74 ms, require at least two to three valid periods in a row (disqualify if any period falls outside this range). This works worldwide except for 20 pps pulse dialing.
- For strong ringer countries (e.g., North America and Japan), use the same criteria, but set the ring threshold to 30 V_{RMS}.

Line reversal (LR), line in use (LIU), or line activity (LACT) may also be used for ring detection in limited circumstances. Line reversal is probably safe in high-ringer-threshold countries and would reject 20 pps dial pulses effectively. In low-ringer-threshold countries, it may not reliably detect weak ring signals since the ringer signal typically rides on top of the dc line voltage. If the ringer ac peaks are less than the line voltage, line reversal will not occur.

LACT and LIU will almost always be triggered on any ring signal, but qualifying the ring frequency is a problem because both detectors may produce more than one pulse per ring period. Although LACT is a sensitive full-wave ring detector, full-wave ring detectors are less accurate with period because ring signals can be asymmetric either because of origination or because of loading. In addition, the LACT detector is not as precise as the ring detector. Its threshold may vary from 10 to 20 V peak.

Another ring-detection scheme makes use of the snoop audio output available at the RxOut pin. If the –6 dB snoop gain is set (SGAIN bit set to zero) and if the CExt1 corner is placed correctly, the ring signal will be available in the snoop audio path with sufficient attenuation to avoid clipping. A CExt1 of 10 nF will work well for typical 20 Hz ring signals. If the ring signal is expected to be around 50 Hz, CExt1 should be reduced to 4.7 nF. This will increase the –3 dB high-pass corner of the snoop audio path to about 700 Hz, which is normally acceptable for Caller ID signals.

6.3. Line Reversal

On-hook line reversal (not to be confused with off-hook loop current reversal) occurs in some countries instead of the first ring cadence before the Caller ID message. Line reversal may also be used for other signaling. Typically, many DAAs with line-reversal detection capability can only detect the transient and not the actual line polarity, making it difficult to differentiate a line reversal from an off-hook transient. The IA3223 has a true line-polarity detector. Line polarity is directly sensed in the IA3222 Line-Side chip, and this information is sent across the isolation barrier to the IA3223 System-Side chip. Line polarity reversal may take up to 50 ms. Through this transition, all three detectors, Line In Use, Line Activity, and Ring, may be triggered. A line reversal can be qualified by determining if the change in polarity is stable for 50 to 100 ms.

6.4. Line Activity

The LACT detector can be programmed to drive the LineStat interrupt pin. This avoids the need for continuous polling of either the LP (line polarity) or RNG (ring detection) bit. LACT detects 10 to 20 V changes in either direction, also triggering on any ring, line reversal, or hook status change. When a LineStat interrupt occurs, the system polls the RNG, LP, and LIU bits and applies qualification algorithms for about 100 ms or until line activity stops.

6.5. Line in Use and Line Disconnect

The LIU detector is a dc line-voltage threshold detector. One of four levels (~2.5, 15, 22.5, and 30 V) can be selected. Unfortunately, line-in-use status is ambiguous for voltages between 12 V and 19 V. Central Office lines and short-range digital loop carrier systems always provide at least 21 V of on-hook voltage. Some PBXs and VoIP boxes may supply less. Telephone devices will generally work with less than 12 V at a loop current of 20–30 mA. Users sometimes add in-line Zener devices (available at Radio Shack®) in series with answering machines in order to improve parallel-pickup disconnect performance. These in-line Zener devices increase the answering machine's off hook voltage by 6 to 8 V, often pushing the total off-hook voltage above 15 V. On short loops with 60 mA capability, some telephone devices may drop over 12 V when off hook. European telephone devices with TBR-21 current limiting may even exceed 32 V when off hook on short lines.

For most situations, the 15 V LIU threshold setting should be the default. A simple technique to reduce ambiguity is to use both LIU and snoop audio detection. A more sophisticated method is to have the system learn normal on and off hook voltages by stepping through the LIU levels of 15, 22.5 and 30 V while using the snoop circuit to monitor audio.

The 2.5 V threshold setting is intended to differentiate a disconnected line (not plugged in) from a powered line without attempting to distinguish on hook from off hook. A disconnected line may create erratic 2.5 V and line-reversal detection. Generally, a valid line is present only if the voltage is stable above 3 V and not reversing. If it is below 2 V or reversing, the line should be considered disconnected. Off-hook loop-current reversal (if available on a trunk) occurs only after dialing to indicate far party answer (toll call).

6.6. The LineStat Pin as Interrupt (On Hook)

The LineStat pin is an active-low interrupt output. Because it has an open-drain output with a weak internal pull-up resistor, it can be wire-ORed with other interrupts in the system. When LineStat is active, the system must determine the cause of the interrupt based on history and the state of the DAA. Table 11 suggests criteria for qualifying the interrupt when the DAA is on-hook.

Table 11. Interrupt Qualifying Criteria (On-Hook)

LSR Required Setting	Possible Cause of Interrupt	Criterion
High	Ringing	Expected ring cadence both at LineStat pin and at RNG bit
Low	Line reversal	LP bit changed compared to before interrupt, stable for 100 ms
	Line in use	LIU bit high if previously low, stable for 100 ms
	Line no longer in use	LIU bit low if previously high, stable for 100 ms
	Line activity	No ring cadence or change in LP or LIU bits

6.7. Audio Snooping

The snoop circuit does not have the same audio performance as the off-hook receiver path, but it is adequate for Caller ID decoding and line monitoring. Snoop audio recovers from all high voltage line signals in less than 10 ms and is continuously present. Besides Caller ID, snooping can be used to monitor the line for call logging or used for voice/fax steering. If a fax calling tone or a specific DTMF sequence is detected, the DAA may be instructed to seize the line. Since DTMF signals normally have higher amplitude than Caller ID signals, a –6 dB gain setting exists for the snoop path (SGAIN set to zero), which allows monitoring of up to 4 VPP signals without clipping.

6.8. Theory of Operation- Off-Hook Line Status

In the off-hook state, the same gyrator circuit that is used for on-hook line-status monitoring is reconfigured to filter audio signals from the line-current change circuit (parallel-pickup detector) so that changes in loop current can be measured without spurious parallel-pickup signals from normal audio. Capacitor CExt2 with an internal 1.2 MΩ resistor forms a large time constant that stores the average dc value of the received signal. This dc value is compared with short-term changes to detect loop current drops caused by a parallel phone on the line going off-hook. Sensitivity to parallel pickup is also affected by the IA3222 Line-Side's holding and ac-input capacitor values. There are four levels of parallel-pickup sensitivity programmed by register bits LTH0 and LTH1. Each setting is about twice as sensitive as the previous. When a parallel-pickup event occurs, it causes a temporary active state both at the PPU (Parallel Pick Up) bit and at the LineStat pin.

6.9. Line Drop

Line drop or wink is a complete drop in loop current from the Central Office switch, usually indicating call disconnect or call waiting depending on the duration of the drop. Drops over 500 ms indicate disconnect, while shorter drops indicate call waiting. Consequently, it is important to time the duration of line drops with at least 10 ms resolution. Line drop is detected by the IA3223 System Side and flagged as the LD (Line Drop) status bit when the IA3222 Line Side receives insufficient loop current to keep it operational (less than 10 mA).

6.10. Parallel Pickup

Generally, the primary reason for parallel-pickup detection is to allow automatic telephone devices (set-top box modems, fax machines, etc.) to drop the line if a parallel telephone device attempts to dial. When a parallel telephone device goes off-hook, the loop current into the IA3222 Line Side decreases. The parallel-pickup circuit detects the low-frequency (less than 100 Hz) transients associated with a parallel pickup or hang up. To prevent spurious detects due to large, low-frequency audio signals, the parallel-pickup circuit attenuates audio-band signals. At the most sensitive setting, the parallel-pickup circuit will spuriously detect maximum amplitude voice and DTMF signals but not modem signals. Parallel pickup dI/dt may be very low either because the parallel phone has a high off-hook voltage relative to Line Side IC or because the parallel phone holding circuit (electronic inductor) may turn on slowly. The parallel-pickup circuit must, therefore, be very sensitive.

In a modem or fax application, lower parallel-pickup sensitivity can be set when dialing DTMF tones to prevent a spurious detection. A higher sensitivity can then be set after dialing. Typically, a –10 dBm modem signal transmitted from the DAA will not trigger the parallel-pickup detector on its most sensitive setting. One method for setting the levels is to raise the sensitivity until spurious detects occur and then reducing the sensitivity by one step. Each step has about a 6 dB difference in sensitivity.

Because the transmit-to-receive transhybrid return loss is poor at frequencies below 100 Hz, it is important that there be no low-frequency transients in the transmitted audio signal to prevent spurious parallel-pickup detections. Modem software can create low-frequency settling transients when switching modes, typically during training or DTMF dialing. These may cause spurious parallel-pickup detections. If adjusting the modem software is not possible, another solution is to put a low-frequency blocking capacitor in the transmit path.

6.11. The LineStat Pin as Interrupt (Off Hook)

In the off-hook state, the LineStat pin behaves in a way similar to the on-hook state. Table 12 suggests criteria for qualifying the interrupt when the DAA is off hook.

Table 12. Interrupt Qualifying Criteria (Off-Hook)

LSR Required Setting	Possible Cause of Interrupt	Criterion
High	Line drop	LD bit high
	Loop-current reversal	LP bit changed compared to before interrupt
	Parallel pickup	PPU bit high

6.12. Measuring Loop-Current Changes through the Received Audio Signal

The Line Side senses line-current information and encodes it for the System Side as a dc offset superimposed onto the received audio data. Since modem DSP algorithms routinely remove low-frequency components from the incoming data stream, dc offset is not a problem, but it needs to be taken into account in headroom calculations.

The current sensor has considerable dc offset, which needs to be calibrated to obtain good current-sensor performance. This is achieved by adding a dc component to the transmitted data proportional to the received dc offset using the following algorithm:

- Disable the current sensor by setting bit LP1 in the Line-Side LSB programming register. This cancels the dc component due to the loop current itself and leaves the current sensor's offset component as dc offset in the received data stream.
- Add a small amount (20 to 50 mV) of dc offset to the outgoing data and note the amount of change in dc offset in the incoming data. The ratio of incoming to outgoing dc offset changes is the dc-offset correction factor, for which the sign must be retained.
- Add a dc offset to all transmitted data equal to the received dc offset divided by the dc-offset correction factor, based on the desired dc reference for the received signal. This is normally the same voltage as that of the ACREF pin.
- Enable the current sensor. The loop current can now be read as incoming-data dc offset from the dc reference voltage. The sensitivity of the current sensor is approximately 1.25 mV of dc offset for every 1 mA of loop current. Note that both the dc-offset correction factor and the gain change with the line-side termination impedance setting.

6.13. Surges, Isolation, and EMC

Among the three regulatory domains that DAAs must comply with (telecom, safety and EMC), safety and EMC tend to be highly intertwined. Designing for regulatory approval can sometimes compromise field reliability of DAAs. Historically, the dominant cause for field failures of modems or other DAA-based telephone products has been electrical overstress from the telephone line due to lightning, ESD, or incompatibility with digital PBX lines. The failures are both metallic (differential) and longitudinal (common mode). Metallic failures are evidenced by damage to components on the line side while longitudinal failures usually damage the drivers or receivers on either side of the isolation barrier. Overdesigning for surge immunity can add as much as a dollar in costly surge components compared to what is necessary to pass required regulatory testing or withstand field stresses. Even minimal surge and regulatory isolation components may be the most expensive non-IC components in the DAA Bill of Materials. Moreover, contrary to expectation, more robust surge components may actually make the DAA less robust overall.

For regulatory, functional and safety reasons, DAAs provide isolation and protection against excessive voltages and currents. The classic example of inherent isolation is the standard telephone, which is not connected to the ac mains. Answering machines and cordless telephones are completely insulated despite being powered by the mains because two-prong transformer wall supplies provide the safety isolation. Products that have a third prong safety ground on the power plug almost always use a DAA for the loop interface. If a product has a conductive chassis or has other electrical connections, it will need a DAA to interface to the telephone line. Examples in this group are alarm systems, set-top boxes, fax machines, remote meter readers, etc.

6.14. Lightning Surges

Lightning rarely strikes the phone line directly. Lightning surges typically couple into the telephone line via several different mechanisms. Lightning can strike the high-voltage distribution lines on the same pole as the phone line. The strike may deliver a brief 1 kA pulse down a hundred meters or more of power line before arcing to ground through the nearest power-distribution lightning arrestor. Since the strike current runs parallel to the telephone lines, its very high dI/dt induces a large common-mode voltage in the parallel phone cable. Although the twisted-pair phone cable has a conductive sheath around it that is grounded periodically, its effectiveness is limited by its own return inductance and resistance through the ground path. The power lines and the telephone cable form a very low impedance pulse transformer that couples the lightning surge as a common-mode (longitudinal) transient to the phone line. The net effect is that several kV of longitudinal transients can be put on the telephone line for any lightning strike on the power line that runs above the same telephone lines.

Another coupling method for lightning is via ground-return bounce. Since the lightning strike must return to ground (and especially if the ground is resistive), the local voltage at the ground return may bounce by thousands of volts for several tens of microseconds. If the local ground is at the switch end of the telephone line, this will induce a common-mode transient toward the CPE end of several kV. Conversely, if the strike ground return is local to the CPE, it will make the local ground bounce by several kV relative to the telephone switch end that may be miles away. Either mechanism generates a longitudinal transient of several kV between the telephone line and the local ground.

These transients are the reason why telephone lines all have primary lightning arrestors to local ground at the PSTN (Public Switched Telephone Network) network access port. Normally, there is one primary arrestor on each side of the telephone line to a local ground, typically a clamp on a water pipe or ground stake. These arrestors trigger in the 300 to 600 V range. Common arrestors are 6-mil carbon gaps, gas tubes, MOVs (Metal Oxide Varistors), or semiconductor breakover diodes. The carbon gaps and gas-tube arrestors are slow and may take several µs to trigger, allowing up to several kV for a few µs. Typically, the arrestors can withstand at least a 100 A surge for a standard lightning surge pulse of several hundred µs. The resistance of the telephone line limits the current. Typical 26-gauge twisted-pair cable has a resistance of 40 Ω per kft. Surge suppressors either have breakover characteristics where their forward voltages drop to a few volts when triggered but need at least 100 mA to keep them conductive, or they have Zener voltage clamp characteristics. Voltage clamps (MOVs are the common example) need to absorb many Joules of energy without damage (1 kV x 100 A x 100 µs = 10 J). With the breakover diode, the peak current may be several times higher because it provides little blocking voltage, but it dissipates less than 1/100th of the energy of voltage clamp because of its low forward voltage. The bulk of the surge energy is dissipated down the series resistance of the telephone line.

Metallic (differential) surges arise from the longitudinal lightning surges causing either the asymmetric triggering of the primary arrestors, or arcing of only one side of the line to ground (if only one primary arrestor is functioning). To protect against metallic surges, a DAA uses a surge suppressor that clamps the differential voltage to prevent damage. Good solutions provide surge immunity for both on-hook and off-hook DAA states. Protecting the off-hook state requires some form of current limiting to protect the off-hook path during the surge. Breakover diodes generally work better since they collapse the surge voltage, thus reducing the energy dissipated in the off-hook circuit over 100 times. MOVs can be used for surges, but because of their nearly two-to-one spread between minimum and maximum clamp voltages, the hook switch must be capable of withstanding much higher peak voltages than with breakover diodes. In addition, the hook circuit must turn itself off (blanking) during the surge in order to prevent excess dissipation.

Because the primary arrestors are not typically in a mutually triggered pair (unlike some gas tubes) during a common mode high voltage transient, one arrestor will always fire before the other. Ironically, on a telephone product with a breakover secondary surge protection diode between tip and ring, this can lead to overstress of the diode especially if the primary arrestors have a breakover characteristic (carbon gap, gas tube, or semiconductor breakover diode). The reason for this is that, once a primary arrestor triggers on one side of the line, the longitudinal surge becomes metallic. This triggers the secondary breakover diode in the telephone product. At that point, the other primary arrestor will not trigger at all, since there is now a low-voltage path around it through the secondary protector and back through the first primary protector that fired. In this situation, the breakover diode sees the same current as the primary arrestor. Typically, for this mechanism to occur, both primary and secondary surge protectors need to have break-over characteristics.

There are several remedies to prevent this. One is to insert a resistance of about 5 Ω in series with Tip and Ring but before the breakover diode. The added resistance increases the voltage drop sufficiently to ensure that the second primary arrestor triggers on large current transients. Small transients can be absorbed by the breakover diode. If a resistor is used, it must be capable of withstanding the worse-case surge. If it has suitable fuse characteristics and is flame proof, it can be used as an inexpensive slow-blow fuse for protection against line cross. Another remedy is to use a larger secondary breakover diode.

Experience shows that a DAA that survives an FCC part 68 Type-B surge provides good field immunity against most lightning surges over the life of the product. This surge specifies a 1 kV peak produced by discharging a 20 µF source capacitor with about 40 Ω of resistance for limiting current. Into a break-over diode, this produces a peak current of about 25 A. Several vendors produce breakover diodes rated to survive this test.

Although the designer can use more robust components to survive an FCC part 68 Type-A surge, (800 V, 100 A),

the added expense is probably not warranted. Furthermore, a Type-A surge only requires a safe failure mode, not continued product operation. Generally, lightning surges that produce differential surges of 100 A are likely to cause extensive damage to a wide variety of electrical devices in the house. As pointed out earlier, the telephone line resistance limits the peak current. Long lines will tend to have higher-voltage and more numerous surges, but the increased resistance helps limit the surge current.

Much of the observed lightning damage to DAAs would not occur if the primary arrestors always were in place and properly grounded. Unfortunately, ground connections at the network-access point may get disconnected due to building construction. The ground is often not reconnected because the telephone line works fine without it. The surge arrestors may also be damaged and not replaced, or the network-access port may be removed and not replaced. Even a properly installed ground stake in a dry climate may fail if the soil dries out, thus causing a high-impedance return path to ground.

6.15. ESD Surges

Arcing across the isolation barrier is the more serious DAA failure that arises when the primary arrestor protection is defective. Longitudinal voltages need to rise above 2 to 3 kV before arcing occurs. Lower voltages usually don't arc since most DAAs are designed to withstand transients of at least 1.5 kV and the continuous application of 1 kV_{RMS}. Even though longitudinal transients above 5 kV may be rare, electrostatic (ESD) transients can easily exceed 10 or 15 kV. A telephone product that includes a DAA might be struck by an ESD event and not have an adequate ground return. The resulting ESD event may then arc across the isolation barrier. For example, a user might be installing a fax machine at home and then plug the telephone line before plugging the power cord. If an ESD transient strikes while the fax machine is unplugged, the DAA might be damaged due to arcing across its isolation.

There are several remedies for the ESD event. One is to use common-mode, high-voltage EMI capacitors between the chassis ground and the phone line. These are typically installed for EMI radiation and susceptibility reduction. If these are around 470 pF, they will divide the voltage of an ESD transient by as much as ten times. Since these capacitors must meet the telephone-line isolation requirements, they will naturally withstand the divided voltage.

The IA3222/3223 chipset does not need these costly EMI capacitors because of the high RF impedance of the isolation capacitors. These capacitors achieve an effective breakdown voltage in the tens of kV at only the cost of the PCB area they occupy. In practice, excessive common-mode voltage will arc across the surface of the board. If the DAA designer doesn't select a preferred path for common-mode arcing, the surge will find its own path with consequent damage. A preferred arc path would normally be between either Tip or Ring and the chassis ground of the telephone product. The desired arc gap should be both shorter and more pointed than any other potential arc path. If part of the arc gap is on the circuit board, it is important that the ends not have insulating silkscreen over them. For most worldwide applications, the gap should be at least 2.5 mm. This means that the other creepage (surface distance) distances should be at least 3 mm.

6.16. Overvoltage Surges

The IA3222 Line Side has a smart power-limiting hook control circuit that prevents damage to the hook switch; either during high-voltage surges or even if continuous high voltage is present on the line. The chip senses both line voltage and line current. If the line voltage exceeds 100 V or the loop current exceeds 170 mA, the hook switch turns off to prevent excessive power dissipation in the main hook transistors. This prevents thermal overstress damage as might occur during ringing peaks, from any surge voltage, or by connecting the DAA to a digital PBX supply with no current limit.

The digital PBX issue has been a major return rate problem on modem DAAs especially for laptop computers. Digital PBX phone systems normally provide 24 to 50 V to power smart phones. This power may be current limited to 1 A or even more, only to prevent a fire hazard. Some systems provide power, control, and audio digital signaling down the normal Tip and Ring pair. If a regular telephone device is plugged into these lines, it may damage the DAA since normal DAAs only expect up to 120 mA of loop current.

6.17. Power-Line Cross

A power-line cross is a fault condition that occurs when a power line is connected to the phone line. This is usually due to a downed power line. All DAAs provide isolation protection against common-mode power line cross, but may not provide protection against differential line cross (full power applied between Tip and Ring). Most regulatory standards only require protection against common-mode power line ac voltages and not differential power line voltages. Line crosses are much rarer events than lightning surges.

A line cross can occur from the user side or from the telephone system side. If the chassis of a telephone product somehow gets shorted to one side of the ac power line, the DAA isolation protects telephone-company technicians and equipment from excessive voltages and power. From the telephone system side, a line cross might occur if a power line falls across the telephone line shorting to one side of the line. Power-line cross is different than lightning surges because of its longer duration. This makes it much more dangerous even though it is less likely to occur than a lightning surge. Failure can occur either from isolation breakdown or from excessive voltage between Tip and Ring, which can create a fire hazard in the DAA.

A power-line cross may start out as a longitudinal high-voltage event but may quickly turn into a metallic event. When a power line gets connected to one side or the other of the telephone line, it may cause the primary surge suppressor to trigger, which, in turn, burns open, leaving the ac mains on one side of the phone line. Then, if the telephone device goes off hook, or, if the breakover diode triggers, the other primary arrestor may trigger and create a path directly through the DAA for the ac power line. In this scenario, there may be very little telephone line resistance in the current loop to limit the current. The result is a destructive failure of the DAA. It may burst into flames due to the continuous flow of energy into the DAA surge suppressor, which is normally not capable of continuous currents above 1 A.

Safe differential line-crossing failure, when required, only means that the product needs to fail safely on a line cross, i.e. not burst into flames during the test. Designing a DAA to survive a line cross is possible but at a significant cost. The simple method is to use an expensive 600 VAC PTC (Positive Temperature Coefficient) resetable fuse or a slow fusible link. Fast-blow fuses will likely get blown by lightning transients and are, therefore, not recommended. There also exist special (and costly) telecom fuses that will survive a 25 A peak Type B surge but will blow on a differential line cross event. Another solution is to use a 5 to 10 Ω, 1 to 2 W, flame-proof metal-oxide resistor for a fusible link. With some testing and care, this cheaper solution will withstand the Type B surge but safely blow on a line-crossing event. This also has the advantage of limiting the surge current that results from asymmetrical firing of the primary lightning arrestors. Any fusible link needs to be flame proof and physically separate from the PC board since the UL 1459 test ramps the ac voltage slowly up to 600 VAC to allow components to generate heat and possibly start a fire, rather than just blow apart. If a component, such as a metal oxide resistor, begins to glow and is lying flat on the PC board, it will carbonize the PC board material, which may lead to conductive tracking (carbonized insulator becoming conductive) and possibly fire.

6.18. Common-Mode Noise from the Mains Supply

A hidden common-mode noise issue arises from the absence of the third (green) wire safety ground in home ac power wiring. In the U.S., third-wire grounds and three-prong ac outlets were not installed extensively until the mid-1950s and were not required by code until the early 1960s. Europe and other countries have similar histories. Thus, in older homes, third-wire grounds are missing in some or all rooms, even if three-prong sockets are present. When computer equipment with switching supplies is plugged into such an outlet, up to half of the ac mains voltage can be measured on the chassis ground relative to real earth ground (or the telephone) line. The reason is that most computer switching supplies have pi network power-line EMI filters that have RF decoupling capacitors in the nF range tied between live, neutral, and ground. If the third-wire ground is not actually grounded, the capacitors in the filter create a divider between live and neutral with the third-wire ground. It is possible to get a slight electrical shock from a computer chassis just from this effect. More significantly, it creates a very large common-mode noise voltage between the phone line (in effect a ground connection) and the local, ungrounded ground wiring.

This large ac common-mode voltage sometimes causes overload problems on resistor-capacitor isolated Caller ID circuits. The IA3222 does not have this issue since it is completely isolated. Even with otherwise isolated DAAs, EMI immunity capacitors, if mismatched, can introduce noise on the telephone line, especially if large ac line transients are present. For example, if two 470 pF EMI capacitors are mismatched by 5%, the 23.5 pF unbalance has an impedance of 2.3 MΩ at 3 kHz. Against a typical line impedance of 600 Ω, this represents 72 dB of

common-mode balance. If the power line has 20 V audio-band transients and the third wire ground is disconnected, this results in 10 V at the chassis and will inject about 2.6 mV of audio noise on the phone line, enough to disrupt most high-speed (V.90, V.34, V.32) modem communication. For this reason, EMI bypass capacitors, when they are necessary, should be of the lowest value necessary to reduce EMI to the desired level.

The power-distribution system can generate common-mode induction transients that arise from power-distribution switching or heavy-duty loads (industrial motors, etc.). Generally, these induction events are mostly a source of common-mode noise and do not produce voltages high enough to cause damage.

6.19. EMC

An advantage of the IA3222/3223 chipset is that many applications do not require the usual telephone-line EMC suppression components. The 2 pF total value of the isolation capacitors presents significant impedance at VHF and UHF radiating frequencies. At 300 MHz, 2 pF has a reactive impedance of 265 Ω, comparable to that of ferrite beads.

If higher levels of RF suppression are required, adding EMI shunt capacitors between each side of the line to the chassis will be more effective than adding ferrite beads. To minimize the need for EMI shunt capacitors, the line side area should be minimized and placed as close as possible to the phone line connector. Extending the chassis ground on each line side (while still maintaining minimum isolation creepage) will act as an RF shield. If board area is available, the EMI line capacitors can be fabricated like the PCB isolation capacitors by using the upper and lower PCB layers. Matched 10 pF capacitors on each side of the line to the chassis would attenuate line RF by about 20 dB.

6.20. RF Susceptibility

For DAAs, large common-mode RF signals below 2 MHz can be a serious source of interference. In particular, AM radio-band transmitters in the 500 kHz to 1.6 MHz range are common large-signal RF sources in urban areas. Although the field strength for AM radio is typically no more than other urban signals (TV, FM, two-way radio, cell phones, etc.), the twisted-pair telephone line from the pole plus the unshielded telephone line in the building makes an excellent long-wave antenna since neither of these are shielded like the multi-pair cable on the pole. Because of the long wavelengths in this band (150 to 600 m), a quarter-wave long wire antenna has a large RF capture area, providing up to a hundred times higher common-mode signal levels than the field strength per meter.

The IA3222/3223 chipset achieves very high common-mode RF immunity. This results from the combination of very low isolation capacitance and internal filtering. Typically, RF immunity of the IA3222/3223 will be sufficient, and the DAA will perform quite well without any special RF suppression components. On the other hand, if immunity is desired to the level specified in EN 55024 or even to Brazil's more demanding Anexo a Resolução No 237, a pair of 470 pF high-voltage capacitors between Tip/Ring and the chassis ground is normally sufficient. In general, filtering components work both ways: any RF solution that works well for radiated signals will work well for susceptibility in the same frequency range.

6.21. Return Loss

Telephone devices transmit and receive bidirectionally down a twisted-pair line. All of the transmitted signal would be present on the receiver were it not for a cancellation circuit called a hybrid or a two-to-four-wire hybrid. A hybrid works by canceling the actual echo back from the line with the expected transmitted reflection. If the actual line impedance and drive impedance is identical, the echo cancellation will be complete. In practice, the line impedance varies significantly with the length of the line and with the presence of bridged taps (parallel open-circuit twisted pair stubs) so that echo cancellation varies with the frequency of the transmitted signal and with the line.

The standard measure of the cancellation of the hybrid balance is return loss. This is a measure of the reflection from the transmit path back to the receive path in terms of loss (attenuation) normalized to levels on the telephone line and expressed in dB. The higher the loss, the lower the reflection and the better the hybrid balance. For example, a 20 dB return loss at a given frequency indicates that the transmitted signal at the receiver will be 20 dB lower than if the same level of signal was received on the telephone line from an outside source. Return loss for a line and its terminating impedance can also be calculated if both impedances are known.

7. Registers

7.1. Register Map*

A2	A1	A0	Register	D3	D2	D1	D0
0	0	0	Control	OFH	LSR	SGAIN	PWD
0	0	1	Line Side programming MSB	LP5	LP4	LP3	LP2
0	1	0	Line Side programming LSB	LP1	LP0		REVID
0	1	1	Thresholds	LTH1	LTH0	RTH1	RTH0
1	0	0	Line status (read only)	RNG/PPU	LIU/LD	LACT	LP
1	0	1	Dividers		F2	F1	F0
1	1	X	Reserved				

***Note:** REVID is a read-only bit, hardwired to zero.

7.2. Control Register

Control Bit	Definition	Function when Low	Function when High	Reset State
OFH	Off-hook command	On hook	Off hook, ORed with OfHk pin	Low
LSR*	Line Status Ring	Line-Status pin reflects the state of the LACT status bit (inverted).	Line-Status pin reflects the state of the RNG/PPU status bit (inverted).	High
SGAIN	Select gain	Low-gain Caller ID Normal transmit gain	High-gain Caller ID Additional 6 dB of transmitter gain	Low
PWD	Power down	Normal operation	Device powered down	Low

***Note:** Refer to "6. Line Monitoring" on page 29 for a description of the Line-Status pin.

7.3. Line-Side Programming Registers

LP5	LP4	Setting
0	0	High transmit voltage headroom and dc voltage drop (reset state)
0	1	Normal transmit voltage headroom and dc voltage drop
1	0	Low transmit voltage headroom and dc voltage drop*
1	1	Lowest transmit voltage headroom and dc voltage drop*
***Note:** This mode is not allowed in 600 Ω + 1 µF or 900 Ω + 1 µF impedance mode.		

LP3	LP2	LP0	Setting	IA3222A	IA3222B	C_X Required? (IA3222B Only)	C_{X1} Required? (IA3222B Only)
0	0	0	600 Ω or 600 Ω + 2.16 µF	Yes	Yes		
0	0	1	600 Ω + 1 µF[1]		Yes		Yes
0	1	0	900 Ω		Yes		
0	1	1	900 Ω + 1 µF[1]		Yes		Yes
1	0	0	ES 203 021, Australia or China complex impedance		Yes	Yes	
1	0	1	New Zealand complex impedance		Yes	Yes	Yes
1	1	0	TBR21 complex impedance with current limit[2]		Yes	Yes	
1	1	1	Reserved				

Notes:
1. This mode is not allowed with low or lowest transmit voltage headroom.
2. When using LP[3,2,0]=110 you must use the application schematic in schematic 3.3 for Legacy TBR21 Current-Limit Support. Using this setting with the standard schematic in section 3.2 may result in circuit damage.

LP1 Setting: 0, current sensor enabled; 1, current sensor disabled (recommended when current sensor is not required)

The Line Side is programmed when any of the following conditions is fulfilled: (1) after going from on-hook to off-hook; (2) when the Line Side LSB programming register is updated by the user or (3) after recovering from a loop-current interruption (line drop).

7.4. Threshold Register

LTH1	LTH0	Line-in-Use Threshold (VDC)	Parallel-Pickup Threshold*
0	0	22.5 ±7.5 V (reset state)	0: least sensitive (reset state)
0	1	30 ±10 V	1
1	0	15 ±5 V	2
1	1	Line-disconnect detection (~2.5 V)	3: most sensitive

***Note:** The parallel-pickup threshold must be selected based on line usage and history. Depending on the application, selecting too sensitive a threshold may falsely detect a parallel pickup in the presence of large signals. Setting 0 or 1 is recommended for voice applications. Modem applications, where transmitted levels and frequency envelopes are well controlled, may benefit from using a more sensitive setting. Refer to Figure 17, which indicates the sensitivity of the detection circuit for signals of different frequencies for various settings. Note that the "high" headroom setting, (because of the reduced receiver gain), reduces the sensitivity of the parallel-pickup function by 3 dB. Each setting is approximately twice as sensitive as the previous setting.

RTH1	RTH0	No-Detection Ring Threshold (Vrms)	Ring Threshold (Vrms)
0	0	10 (reset state)	20 (reset state)
0	1	12.5	25
1	0	15	30
1	1	20	40

7.5. Line Status Register (Read Only)*

***Note:** Writing any value to this register will reset all registers to their default values.

Mnemonic	Definition	Applicability	Status When Bit is Low	Status When Bit is High
RNG[1]	Ring signal	On hook	Voltage below ring threshold	Voltage above ring threshold
PPU[1]	Parallel pickup	Off hook	No loop-current drop	Loop-current drop
LIU[1]	Line In Use	On hook	Voltage above LIU threshold	Voltage below LIU threshold
LD[1]	Line Drop	Off hook	Line active	Line disconnected or line fault
LACT[2]	Line activity	On hook	No change in line-in-use status	Change in line-in-use status
		Off hook	No parallel-pickup event	Parallel-pickup event
LP [Note 1]	Line polarity	On hook and off hook	Line reversed	Line direct

Notes:
1. This bit is multiplexed to a digital output pin of the IA3223A.
2. In the on-hook state, LACT will become high if the line voltage change is at least 10 to 20 V in either direction.

7.6. Divider Register

F2	F1	F0	Clock Mode	Minimum Input Frequency (MHz)	Maximum Input Frequency (MHz)
0	0	0	Internal (reset state)	0.0672 (internal)	0.0828 (internal)
0	0	1	External divided by 24	1.38	2.0
0	1	0	External divided by 32	1.84	2.667
0	1	1	External divided by 48	2.76	4.0
1	0	0	External divided by 64	3.68	5.333
1	0	1	External divided by 96	5.52	8.0
1	1	0	External divided by 128	7.37	10.667
1	1	1	External divided by 1	0.0576	0.08333

Notes:
1. Table represents clock frequencies typically used for PCM interface devices.
2. An external clock can be used to synchronize an external codec with the DAA in order to avoid aliasing.

8. Suggested Country Settings

Table 13. Suggested Country Settings

Country	LTH[1:0]	LP[3,2,0]	LP[5:4]	LP[5:4] (see remark)	Remark
Argentina	00	000	01		
Australia	10	100	01	11	For line-seizure state only
Belarus	00	000	01		
Brazil	10	000	10	11	When not transmitting only
Brunei	01	000	10		
Canada	01	000	01		
Chile	00	000	01		
China	01	000	10		
TBR21 Group*	01	110	01		
Egypt	01	100	10	11	When not transmitting only
FCC	01	000	01		
Germany	01	100	01		
Greece	01	100	01		
Hong Kong	01	000	01		
Hungary	00	000	10	11	When not transmitting only
India	01	000	01		
Indonesia	01 or 10	000	01		
Ireland	01	100	01		
Israel	01	100	01		
Japan	01	000	10	11	When not transmitting only
Jordan	01	000	01	11	When not transmitting only
Kazakhstan	00	000	01		
Malaysia	01	000	10	11	When not transmitting only
Mexico	01	000	01		
NewZealand	01	101	01		
Norway	01	100	01		
Pakistan	01	000	10	11	When not transmitting only

Table 13. Suggested Country Settings (Continued)

Poland	11	000	01		
Portugal	01	100	01		
Qatar	01	000	01		
Romania	10	000	10		
Russia	00	000	01		
Singapore	01	000	10		
Slovakia	01	100	10		
South Africa	10	000	01		
Spain	01	100	01		
Syria	00	000	10	11	When not transmitting only
Taiwan	01	000	01		
Thailand	01	000	10	11	When not transmitting only
Ukraine	00	000	01		

***Note:** When using LP[3,2,0]=110 you must use the application schematic in section 3.3 for Legacy TBR21 Current-Limit Support. Using this setting with the standard schematic in section 3.2 may result in circuit damage.

9. Pin Description—IA3223 System-Side QSOP-16

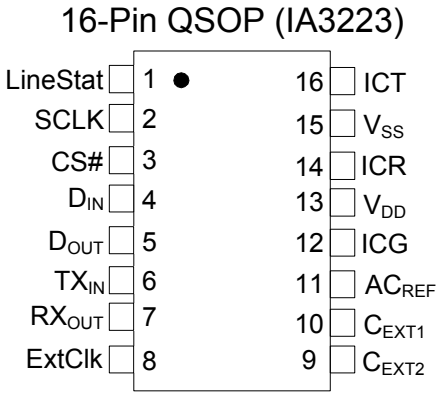


Figure 34. Pin Configuration

Table 14. IA3223 System Side Pin Definitions

Pin Number	Pin Name	Pin Type	Pin Function
1	LineStat	DO, PU	Line Status open-drain output*
2	SCLK	DI	Serial interface clock
3	$\overline{CS}$	DI	Serial interface chip select, active low with weak pull-down
4	D_{IN}	DI	Serial interface data in
5	D_{OUT}	DO	Serial interface data out
6	TX_{IN}	AI	DAA transmit input
7	RX_{OUT}	AO	DAA receive output
8	ExtClk	DI, PD	Optional external clock; this pin may be left open.
9	C_{EXT2}	AIO	External capacitor #2 connection
10	C_{EXT1}	AIO	External capacitor #1 connection
11	AC_{REF}	AI	DAA optional dc offset; this pin may be left open.
12	ICG	AIO	Line-Side isolation bridge interface reference ground
13	V_{DD}	S	Positive power supply
14	ICR	AI	Line-Side isolation bridge interface for receiver path
15	V_{SS}	S	System ground
16	ICT	AO	Line-Side isolation bridge interface for transmitter path
***Note:** Refer to the section on line monitoring for a description of the Line-Status pin.			

10. Pin Description—IA3223A System-Side QSOP-20

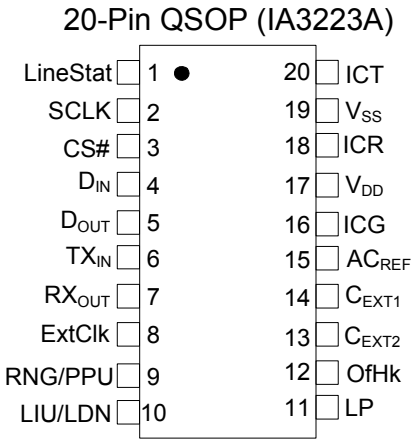


Figure 35. Pin Configuration

Table 15. IA3223A System Side Pin Definitions

Pin Number	Pin Name	Pin Type	Pin Function
1	LineStat	DO, PU	Line Status open-drain output*
2	SCLK	DI	Serial interface clock
3	$\overline{CS}$	DI	Serial interface chip select, active low with weak pull-down
4	D_{IN}	DI	Serial interface data in
5	D_{OUT}	DO	Serial interface data out
6	TX_{IN}	AI	DAA transmit input
7	RX_{OUT}	AO	DAA receive output
8	ExtClk	DI, PD	Optional external clock; this pin may be left open.
9	RNG/PPU	DO	Ring signal (on hook) or parallel pickup (off hook)
10	LIU/LD	DO	Line in use or disconnect (on hook) or line drop (off hook)
11	LP	DO	Line polarity (on hook and off hook)
12	OfHk	DI, PD	Off hook, active high, ORed with internal OFH control bit
13	C_{EXT2}	AIO	External capacitor #2 connection
14	C_{EXT1}	AIO	External capacitor #1 connection
15	AC_{REF}	AI	DAA optional dc offset; this pin may be left open.
16	ICG	AIO	Line-Side isolation bridge interface reference ground
17	V_{DD}	S	Positive power supply
18	ICR	AI	Line-Side isolation bridge interface for receiver path
19	V_{SS}	S	System ground
20	ICT	AO	Line-Side isolation bridge interface for transmitter path
***Note:** Refer to the section on line monitoring for a description of the Line-Status pin.			

11. Pin Description—IA3222B Line-Side MSOP-10

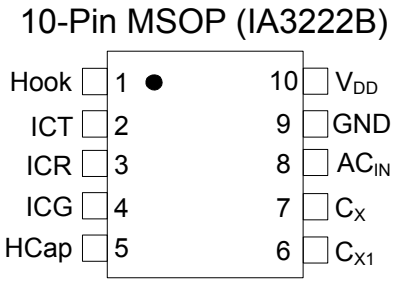


Figure 36. Pin Configuration

Table 16. IA3222B Line Side Pin Definitions

Pin Number	Pin Name	Pin Function
1	Hook	Hook-switch control
2	ICT	Line-Side isolation bridge interface for transmitter path
3	ICR	Line-Side isolation bridge interface for receiver path
4	ICG	Line-Side isolation bridge interface reference ground
5	HCap	Holding capacitor connection
6	C_{X1}	Termination-impedance capacitor
7	C_X	Termination-impedance capacitor
8	AC_{IN}	Receiver path sensing capacitor input
9	GND	Device ground
10	V_{DD}	Device supply, self regulated through hook-switch transistor

12. Ordering Guide

System-Side Devices			
Part Number*	**Package**	**RoHS Compliant?**	**Temperature Range**
IA3223-C-FU	QSOP-16	Yes	–25 to +85 °C
IA3223A-C-FU	QSOP-20	Yes	–25 to +85 °C
Line-Side Devices			
Part Number*	**Package**	**RoHS Compliant?**	**Temperature Range**
IA3222B-F-FT	MSOP-10	Yes	–25 to +85 °C
***Note:** Add an “R” to the end of the ordering part number to denote tape and reel packaging.			

13. Package Markings (Top Markings)

Codes for the IA3222-C-FU, IA3223A-C-FU, and IA3222B-F-FT top marks are as follows:

- YY = Current Year
- WW = Work Week
- R = Die Revision
- T...T = Trace Code

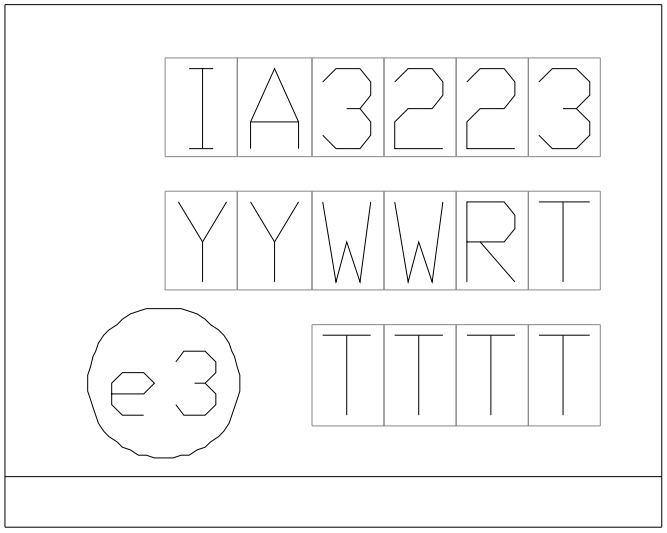


Figure 37. IA3223-C-FU Top Marking

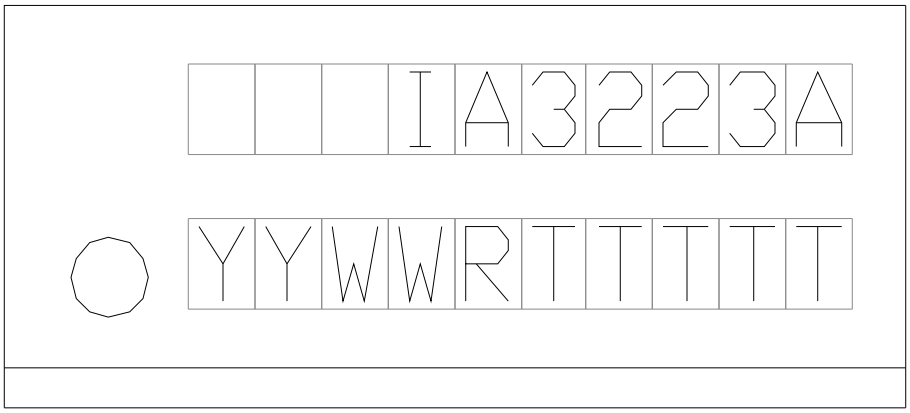


Figure 38. IA3223A-C-FU Top Marking

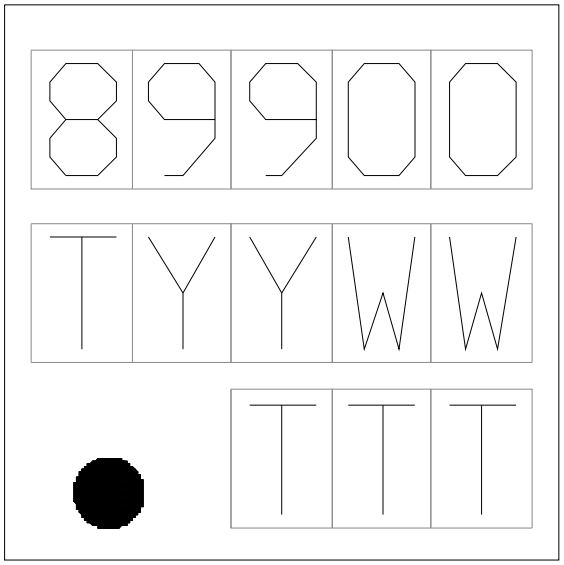
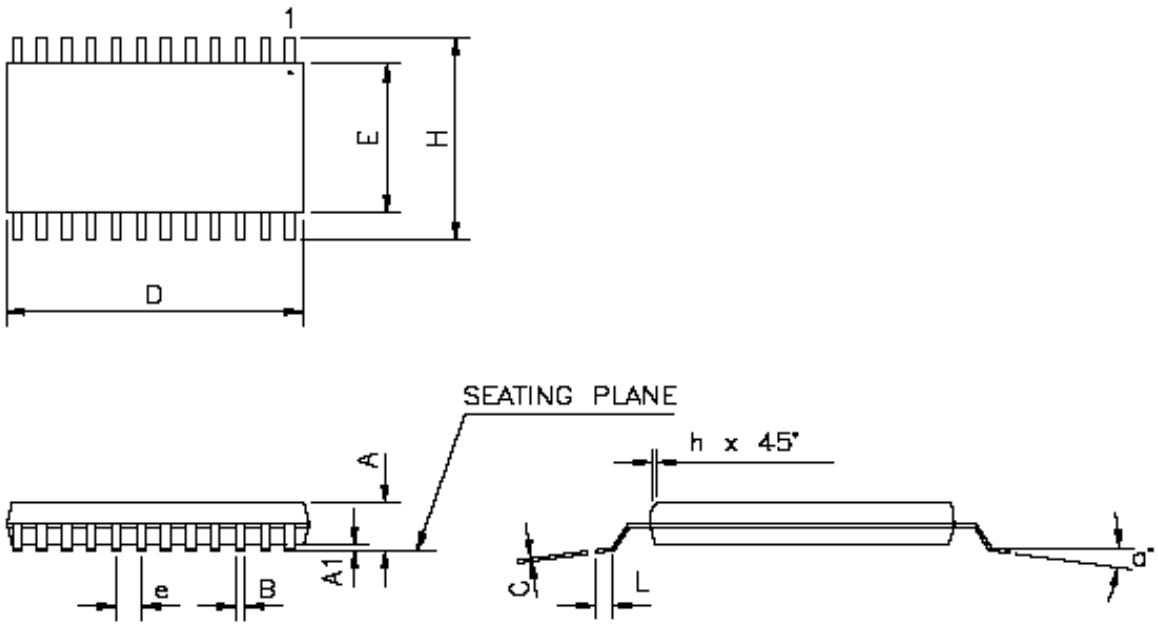


Figure 39. IA3222B-F-FT Top Marking

14. Package Outline: QSOP-16 and QSOP-20

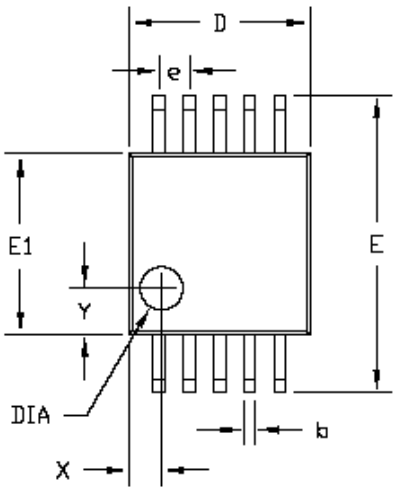


JEDEC #	MO-137AB		MO-137AD	
TYPE	16 LEAD		20 LEAD	
SYMBOL	Min	Max	Min	Max
A	0.060	0.068	0.060	0.068
A1	0.004	0.008	0.004	0.008
B	0.009	0.012	0.009	0.012
C	0.007	0.010	0.007	0.010
D	0.188	0.197	0.337	0.344
E	0.150	0.157	0.150	0.157
e	0.025 BSC		0.025 BSC	
H	0.230	0.244	0.230	0.244
h	0.010	0.016	0.010	0.016
L	0.016	0.035	0.016	0.035
α°	0°	8°	0°	8°

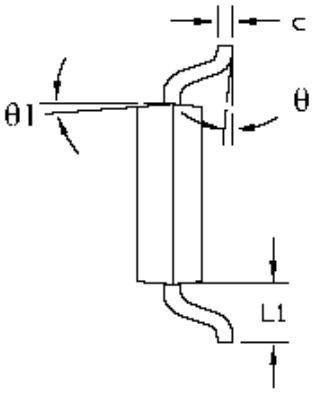
NOTES

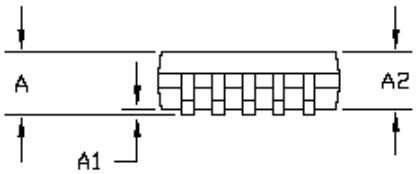
1. LEAD WIDTH AND LEAD THICKNESS EXCLUSIVE OF SOLDER PLATE
2. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASHES AND BURR DIMENSIONS
3. ALLOWABLE MOLD FLASH IS 5 MILS PER SIDE.
4. DIMENSIONS ARE GIVEN IN INCHES.
5. LEAD COPLANARITY IS 0.003 INCH MAX.

15. Package Outline: MSOP-10



TOP VIEW





SIDE VIEW

SYMBOL	INCHES		
	MIN	MAX	ACTUAL
A	0.036	0.043	0.038
A1	0.002	0.006	0.004
A2	0.032	0.037	0.034
b	0.007	0.010	0.008
c	0.003	0.009	0.006
D	0.116	0.120	0.118
E	0.190	0.198	0.194
E1	0.116	0.120	0.118
e	0.020		
L1	0.036	0.040	0.038
θ	0°	8°	5°
θ1	5°	10°	7°
DIA	ø0.028 depth=0.004		
X	0.017	0.025	0.021
Y	0.026	0.034	0.030

Document Change List

Revision 4.2 to Revision 5.0

- Updated from Integration Associates formatting to Silicon Laboratories
- Removed 8-pin IA3222A option
- Updated on-hook voltage-protection threshold specification
- Updated application schematics and BOM
- Added suggested country settings
- Added package top markings

NOTES:

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