



16-BIT 2:1 MUX/DEMUX SWITCH

IDT74FST163233

FEATURES:

- Bus switches provide zero delay paths
- Low switch on-resistance
- TTL-compatible input and output levels
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Hot insertion capability
- Very low power dissipation
- Available in SSOP and TSSOP packages

DESCRIPTION:

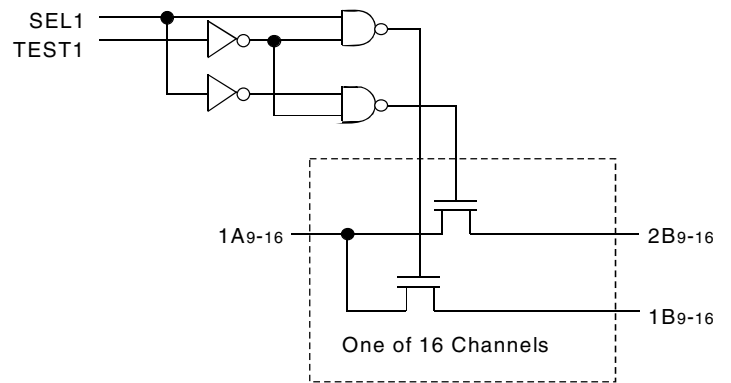
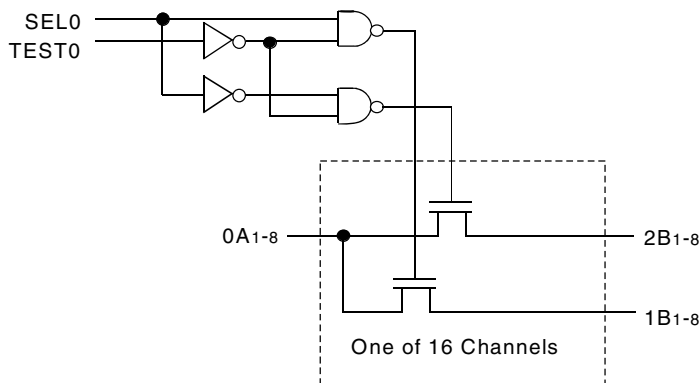
The FST163233 belongs to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. Thus they generate little or no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When the gate-to-source junction of this FET is adequately forward-biased the device conducts and the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off, therefore with no Vcc applied, the device has hot insertion capability.

The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

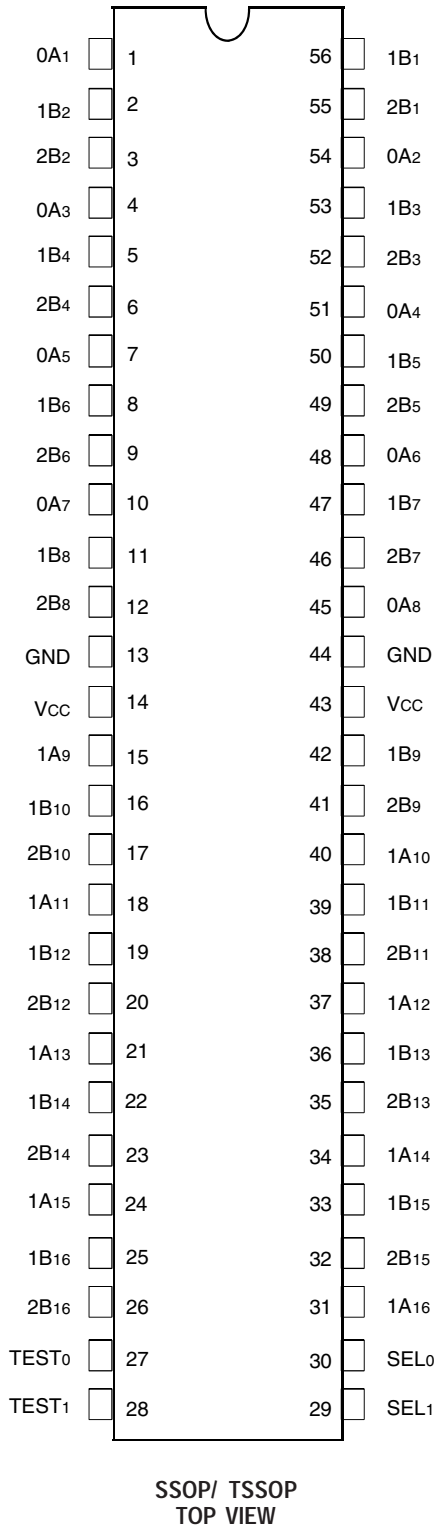
The FST163233 provides three 16-bit TTL-compatible ports that support 2:1 multiplexing. The SEL0,1 and TEST0,1 pins provide switch enable and mux select control as shown below.

The A port can be connected to port 1B or port 2B or both ports 1B and 2B.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7	V
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	Maximum Continuous Channel Current	128	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC}, Control, and Switch terminals.

CAPACITANCE⁽¹⁾

Symbol	Parameter	Conditions ⁽²⁾	Typ.	Unit	
C _{IN}	Control Input Capacitance		6	pF	
C _{I/O}	Switch Input/Output Capacitance	A Port	Switch Off	17	pF
		B Port	Switch Off	12	

NOTES:

- Capacitance is characterized but not tested.
- T_A = 25°C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V.

PIN DESCRIPTION

Pin Names	I/O	Description
A, 1B, 2B	I/O	Buses A, 1B, 2B
SEL _{0,1} TEST _{0,1}	I	Control Pins for MUX and Switch Enable Functions

FUNCTION TABLE⁽¹⁾

SEL ₀	TEST ₀	Description
L	L	0A to 1B
H	L	0A to 2B
X	H	0A to 1B and 0A to 2B
SEL ₁	TEST ₁	Description
L	L	1A to 1B
H	L	1A to 2B
X	H	1A to 1B and 1A to 2B

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = DON't Care

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Control Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2	—	—	V
V_{IL}	Control Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	—	—	0.8	V
I_{IH}	Control Input HIGH Current	$V_{CC} = \text{Max.}$ $V_i = V_{CC}$	—	—	± 1	μA
I_{IL}	Control Input LOW Current		$V_i = \text{GND}$	—	—	
I_{OZH}	Current During	$V_{CC} = \text{Max.}, V_o = 0$ to 5V	—	—	± 1	μA
I_{OZL}	Bus Switch Disconnect		—	—	± 1	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$	—	-0.7	-1.2	V
I_{OFF}	Switch Power Off Leakage	$V_{CC} = 0\text{V}, V_{IN}$ or $V_o \leq 5.5\text{V}$	—	—	± 1	μA
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND}$ or V_{CC}	—	0.1	3	μA

BUS SWITCH IMPEDANCE OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions	Min.	Typ. ⁽¹⁾	Max.	Unit
R_{ON}	Switch On Resistance ⁽²⁾	$V_{CC} = \text{Min.}, V_{IN} = 0\text{V}, I_{ON} = 12\text{mA}$	—	5	7	Ω
		$V_{CC} = \text{Min.}, V_{IN} = 2.4\text{V}, I_{ON} = 8\text{mA}$	—	10	15	
I_{OS}	Short Circuit Current, A to B ⁽³⁾	$A(B) = 0\text{V}, B(A) = V_{CC}$	100	—	—	mA

NOTES:

1. Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
2. The voltage drop between the indicated ports divided by the current through the switch.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ^(4,5)	$V_{CC} = \text{Max.}$ One Select Pin Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	30	40	$\mu A /$ MHz/ Select
I_{CCD}	Dynamic Power Supply Current ^(4,5)	$V_{CC} = \text{Max.}$ One Test Pin Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	120	160	$\mu A /$ MHz/ Test
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ One Select Pin Toggling $f_i = 10\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	0.3	0.4	mA
			$V_{IN} = V_{CC}$ $V_{IN} = 3.4V$	—	0.6	1.2	
		$V_{CC} = \text{Max.}$ Two Select Pins Toggling $f_i = 10\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	0.6	0.8	
			$V_{IN} = V_{CC}$ $V_{IN} = 3.4V$	—	1.1	2.3	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type. $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND . Switch inputs do not contribute to ΔI_{CC} .
- This parameter represents the current required to switch the internal capacitance of the control inputs at the specified frequency.
Switch inputs generate no significant power supply currents as they transition. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- $C_{PD} = I_{CCD}/V_{CC}$
 C_{PD} = Power Dissipation Capacitance
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_i N)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_i = Control Input Frequency
 N = Number of Control Inputs Toggling at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

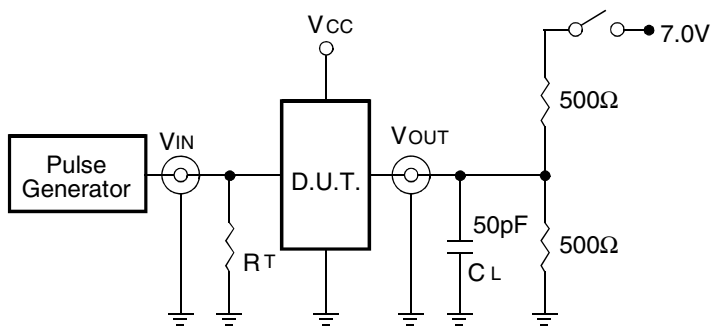
Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Description ⁽¹⁾	$V_{CC} = 5\text{V} \pm 10\%$			$V_{CC} = 4\text{V}$		Unit
		Min.	Typ.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Data Propagation Delay A to B, B to A ⁽²⁾	—	—	0.25	—	0.25	ns
t_{BX}	Switch Multiplex Delay SEL to A	1.5	—	6.5	—	7	ns
t_{PZH} t_{PZL}	Switch CONNECT Delay SEL, TEST to B	1.5	—	6.5	—	7	ns
t_{PHZ} t_{PLZ}	Switch DISCONNECT Delay SEL, TEST to B	1.5	—	7	—	7	ns
$ Q_{CI} $	Charge Injection During Switch DISCONNECT TEST to A or B ⁽³⁾	—	1.5	—	—	—	pC
$ Q_{DCI} $	Differential Charge Injection During Multiplexer Switching SEL to A or B ⁽³⁾	—	0.5	—	—	—	pC

NOTES:

1. See test circuits and waveforms.
2. The bus switch contributes no Propagation Delay other than the RC Delay of the load interacting with the RC of the switch.
3. $|Q_{CI}|$ is the charge injection for a single switch DISCONNECT and applies to either single switches or multiplexers. $|Q_{DCI}|$ is the charge injection for a multiplexer as the multiplexed port switches from one path to another. Charge injection is reduced because the injection from the DISCONNECT of the first path is compensated by the CONNECT of the second path.

TEST CIRCUITS AND WAVEFORMS



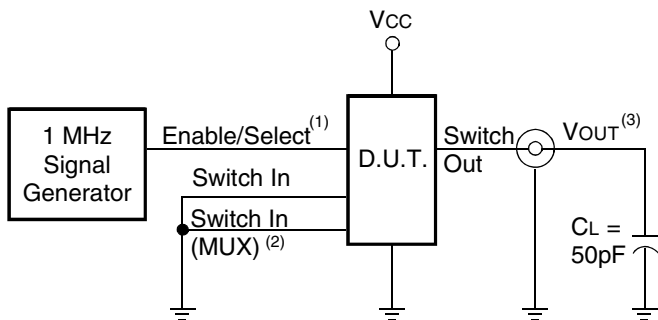
Test Circuits for All Outputs

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

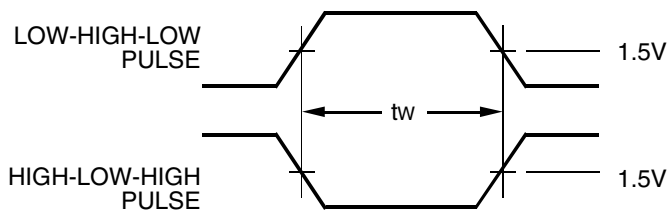
CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



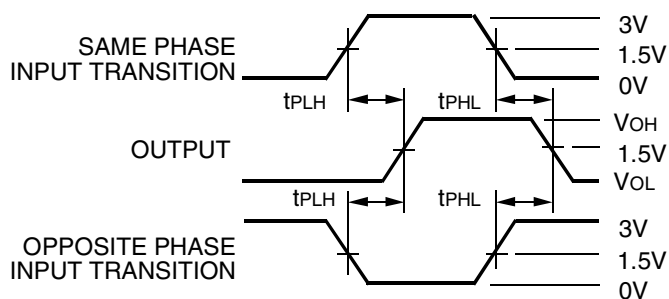
Charge Injection

NOTES:

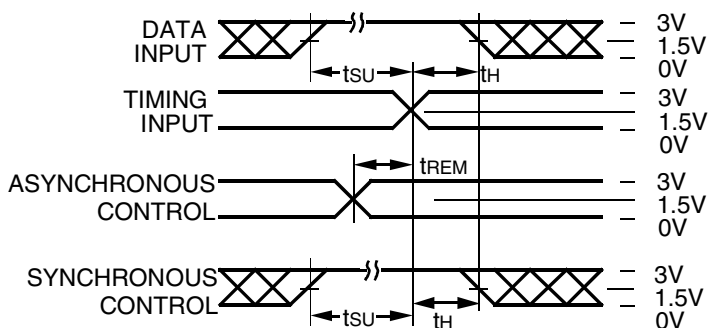
- Select is used with multiplexers for measuring IQdcil during multiplexer select. During all other tests Enable is used.
- Used with multiplexers to measure IQdcil only.
- Charge Injection = $\Delta V_{out} C_L$, with Enable toggling for IQdcil or Select toggling for IQdcil. ΔV_{out} is the change in V_{out} and is measured with a 10MΩ probe.



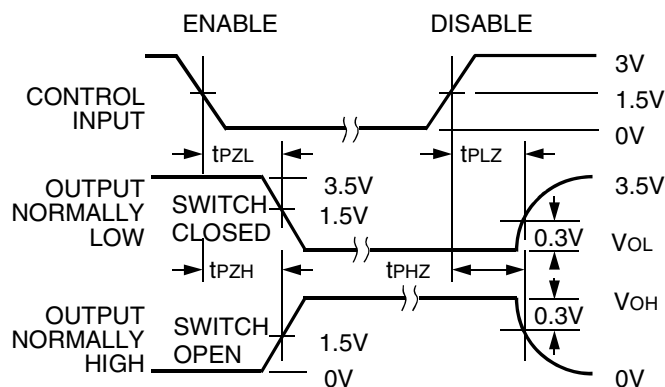
Pulse Width



Propagation Delay



Set-up, Hold, and Release Times

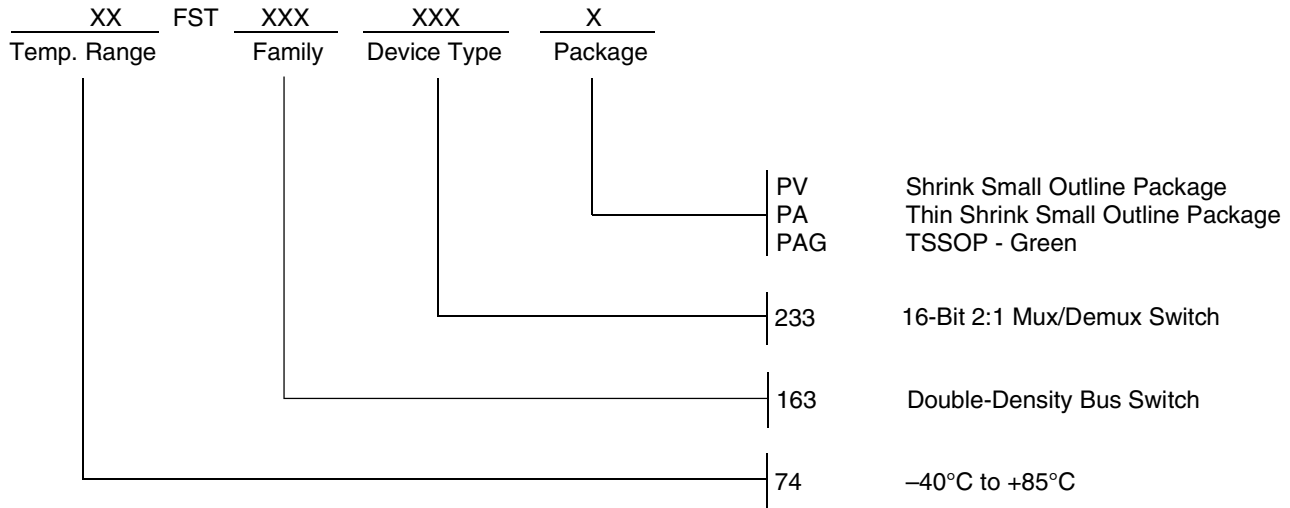


Enable and Disable Times

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$.

ORDERING INFORMATION



CORPORATE HEADQUARTERS
6024 Silver Creek Valley Road
San Jose, CA 95138

for SALES:
800-345-7015 or 408-284-8200
fax: 408-284-2775
www.idt.com

for Tech Support:
logichelp@idt.com