

Model CCHD-575 is the industry's lowest jitter clock oscillator in a 5x7.5 mm package. It features a typical phase jitter of 82 fSec RMS at 100 MHz. Close-in phase noise is -90 dBc/Hz @ 10 Hz while its floor is at -168 dBc/Hz. This oscillator may be small in size but it packs a punch inside. Its output driver is capable of driving ± 24 mA. This translates to a rise/fall time of ~600ps at 100 MHz with a 15pF load.

Applications include
DACs
ADCs
Low Phase Signal Sources
Test and Measurement

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CCHD-575

Ultra-Low Phase Noise Oscillator



CCHD-575 Model
5x7.5 mm SMD, 3.3V, CMOS

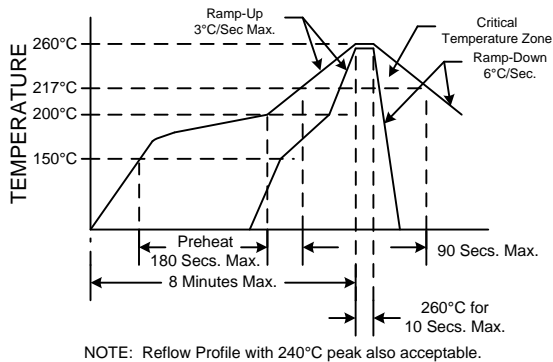
Frequency Range:	50 MHz to 130 MHz
Temperature Range:	0°C to +70°C
	-20°C to +70°C (Option M)
	-40°C to +85°C (Option X)
Storage:	-55°C to 90°C
Input Voltage:	3.3V ±0.3V
Input Current:	15mA Typ., 25mA Max
Output:	CMOS
	45/55% Max @ 50% Vdd
Symmetry:	2nsec Max @ 20% to 80% Vdd
Rise/Fall Time:	“0” = 10% Vdd Max
Logic:	“1” = 90% Vdd Min.
	Load: 15pF
	Output Current: ±24mA Max
Phase Jitter: (12kHz~80MHz)	82 fSec RMS Typ. @ 100 MHz
Phase Noise Typical:	See plots
Phase Noise Floor:	-168dBc/Hz Typ., -165dBc/Hz Max
Sub-harmonics:	None
Aging:	<3ppm 1st/yr, <1ppm thereafter

CCHD-575 Options:

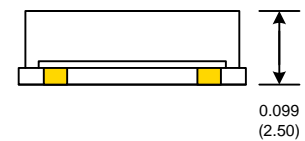
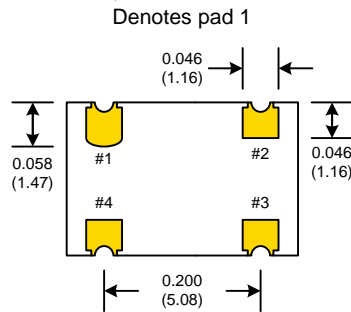
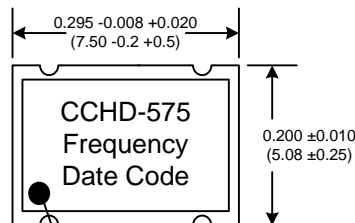
Temperature Range:	0°C to +70°C (±20ppm, ±25ppm, ±50ppm)
	-20°C to +70°C (±25ppm, ±50ppm)
	-40°C to +85°C (±25ppm, ±50ppm)

Part Number Example:
CCHD-575X-25-100.000 = 3.3V, 45/55, -40°C to +85°C (±25ppm), 100 MHz

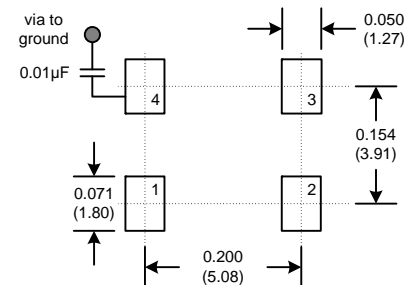
RECOMMENDED REFLOW SOLDERING PROFILE



Pad	Connection
1	NC
2	GND
3	Output
4	Vdd



SUGGESTED PAD LAYOUT



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