Isolated CAN Transceiver with Integrated High Voltage, Bus-Side, Linear Regulator

Preliminary Technical Data

ADM3052

FEATURES

- Isolated CAN transceiver
- Integrated V_+ linear regulator
- Bus side powered by V_+ and V_-
- 11 V to 25 V operation on V_+
- 5 V or 3.3 V operation on V_{DD1}
- Complies with ISO 11898 Standard
- High speed data rates up to 1 Mbps
- Short Circuit Protection on bus pins
- Integrated bus mis-wire protection
- Unpowered nodes do not disturb the bus
- Connect 110 or more nodes on the bus
- Thermal shutdown protection
- High common-mode transient immunity: >25 kV/µs
- Safety and regulatory approvals (pending)
  - UL recognition: 5000 V_{RMS} for 1 minute per UL 1577
  - VDE Certificates of Conformity
    - DIN VVDE V 0884-10 (VDE V 0884-10):2006-12
    - VIORM = 848V peak
- Industrial operating temperature range (−40°C to +85°C)
- Available in wide-body, 16-lead SOIC package

APPLICATIONS

- CAN data buses
- Industrial field networks
- DeviceNet applications

FUNCTIONAL BLOCK DIAGRAM

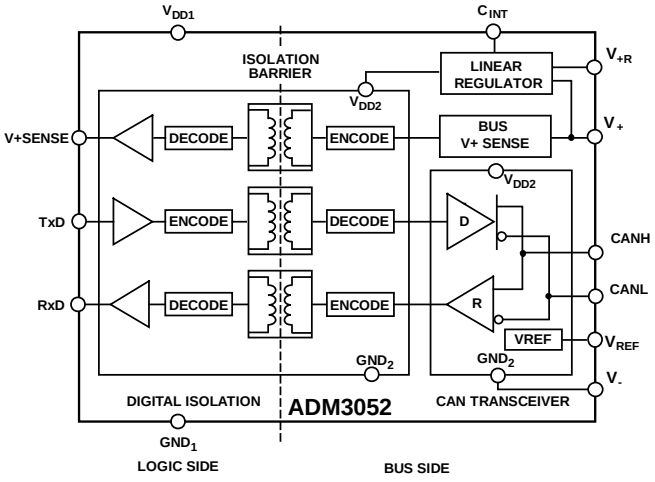

Figure 1.

GENERAL DESCRIPTION

The ADM3052 is an isolated controller area network (CAN) physical layer transceiver with a V_+ integrated linear regulator. The ADM3052 complies with the ISO 11898 standard.

The device employs Analog Devices, Inc., *i*Coupler® technology to combine a 3-channel isolator, a CAN transceiver and an LDO regulator into a single package. The power is isolated between a single 3.3V or 5V supply on V_{DD1}, the logic side, and a single 24V supply provided on V_+, the bus side.

The ADM3052 creates an isolated interface between the CAN protocol controller and the physical layer bus. It is capable of running at data-rates up to 1Mbps.

The device has integrated mis-wire protection on the bus pins, V+, V−, CANH and CANL.

The device has current-limiting and thermal shutdown features to protect against output short circuits and situations where the bus might be shorted to ground or power terminals. The part is fully specified over the industrial temperature range and is available in a 16-lead, wide-body SOIC package.

Rev. PrG

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SPECIFICATIONS

All voltages are relative to their respective ground; 3.0 V ≤ V_{DD1} ≤ 5.5 V. T_A = −40°C to +85°C, V_+ = 11 V to 25 V, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
SUPPLY CURRENT						
Power Supply Current Logic Side						
TxD/RxD Data Rate 1 Mbps	I_{DD1}		2.5		mA	
Power Supply Current Bus Side						
Recessive State	I_+		10		mA	R_L = 60 Ω, see Figure 10
Dominant State	I_+		64		mA	R_L = 60 Ω, see Figure 10
TxD/RxD Data Rate 1 Mbps	I_+		48		mA	R_L = 60 Ω, see Figure 10
EXTERNAL RESISTOR						
Resistance	R_P	297	300	303	Ω	
Power Rating			0.75		W	
DRIVER						
Logic Inputs						
Input Voltage High	V_{IH}	0.7 V_{DD1}			V	TxD
Input Voltage Low	V_{IL}			0.25 V_{DD1}	V	TxD
CMOS Logic Input Currents	I_{IH}, I_{IL}			500	µA	TxD
Differential Outputs						
Recessive Bus Voltage	V_{CANL}, V_{CANH}	2.0		3.0	V	V_{TxD} = 4 V, R_L = ∞, see Figure 7
CANH Output Voltage,	V_{CANH}	2.75		4.5	V	V_{TxD} = 1 V, see Figure 7
CANL Output Voltage	V_{CANL}	0.5		2.0	V	V_{TxD} = 1 V, see Figure 7
Differential Output Voltage	V_{OD}	1.5		3.0	V	V_{TxD} = 1 V, R_L = 45 Ω, see Figure 7
	V_{OD}	−500		+50	mV	V_{TxD} = 4 V, R_L = ∞, see Figure 7
Short-Circuit Current, CANH	I_{SCCANH}			−200	mA	V_{CANH} = −5 V
Short-Circuit Current, CANH	I_{SCCANH}		−100		mA	V_{CANH} = −36 V
Short-Circuit Current, CANL	I_{SCCANL}			200	mA	V_{CANL} = 36 V
RECEIVER						
Differential Inputs						
Differential Input Voltage Recessive	V_{IDR}	−1.0		+0.5	V	−7 V < V_{CANL}, V_{CANH} <12 V, see Figure 8, C_L = 15 pF
Differential Input Voltage Dominant	V_{IDD}	0.9		5.0	V	−7 V < V_{CANL}, V_{CANH} <12 V, see Figure 8, C_L = 15 pF
Input Voltage Hysteresis	V_{HYS}		150		mV	See Figure 4.
CANH, CANL Input Resistance	R_{IN}	5		25	kΩ	
Differential Input Resistance	R_{DIFF}	20		100	kΩ	
Logic Outputs						
Output Low Voltage	V_{OL}		0.2	0.4	V	I_{OUT} = 1.5 mA
Output High Voltage	V_{OH}	V_{DD1} − 0.3	V_{DD1} − 0.2		V	I_{OUT} = −1.5 mA
Short-Circuit Current	I_{OS}	7		85	mA	V_{OUT} = GND_1 or V_{DD1}
VOLTAGE REFERENCE						
Reference Output Voltage	V_{REF}	2.025		3.025	V	|I_{REF} = 50 µA|
BUS VOLTAGE SENSE						
V_+Sense Output Voltage Low	V_{OL}		0.2	0.4	V	$I_{O+SENSE}$ = 1.5 mA
V_+Sense Output Voltage High	V_{OH}	V_{DD1}- 0.3	V_{DD1}- 0.2		V	$I_{O+SENSE}$ = −1.5 mA
Bus Voltage Sense Threshold Voltage	V_{+TH}	7.5		10	V	
COMMON-MODE TRANSIENT IMMUNITY[1]		25			kV/µs	V_{CM} = 1 kV, transient magnitude = 800 V

[1] CM is the maximum common-mode voltage slew rate that can be sustained while maintaining specification-compliant operation. V_{CM} is the common-mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common-mode is slewed. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

TIMING SPECIFICATIONS

All voltages are relative to their respective ground; 3.0 V ≤ V_{DD1} ≤ 5.5 V. T_A = −40°C to +85°C, V_+ = 11 V to 25 V, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DRIVER						
Maximum Data Rate		1			Mbps	
Propagation Delay from TxD On to Bus Active	t_{onTxD}			90	ns	See Figure 2 and Figure 9, R_L = 60 Ω, C_L = 100 pF
Propagation Delay from TxD Off to Bus Inactive	t_{offTxD}			120	ns	See Figure 2 and Figure 9, R_L = 60 Ω, C_L = 100 pF
RECEIVER						
Propagation Delay from TxD On to Receiver Active	t_{onRxD}			200	ns	See Figure 2 and Figure 9, R_L = 60 Ω, C_L = 100 pF
Propagation Delay from TxD Off to Receiver Inactive	t_{offRxD}			250	ns	See Figure 2 and Figure 9, R_L = 60 Ω, C_L = 100 pF
Bus Dominant to RxD Low	t_{dRxDL}			1	µs	See Figure 2 and Figure 9, R_L = 60 Ω, C_L = 100 pF
POWER UP						
Enable Time, V_+ High to V_+Sense Low	t_{SE}			300	µs	See Figure 5
Disable Time, V_+ Low to V_+Sense High	t_{SD}			10	ms	See Figure 5

SWITCHING CHARACTERISTICS

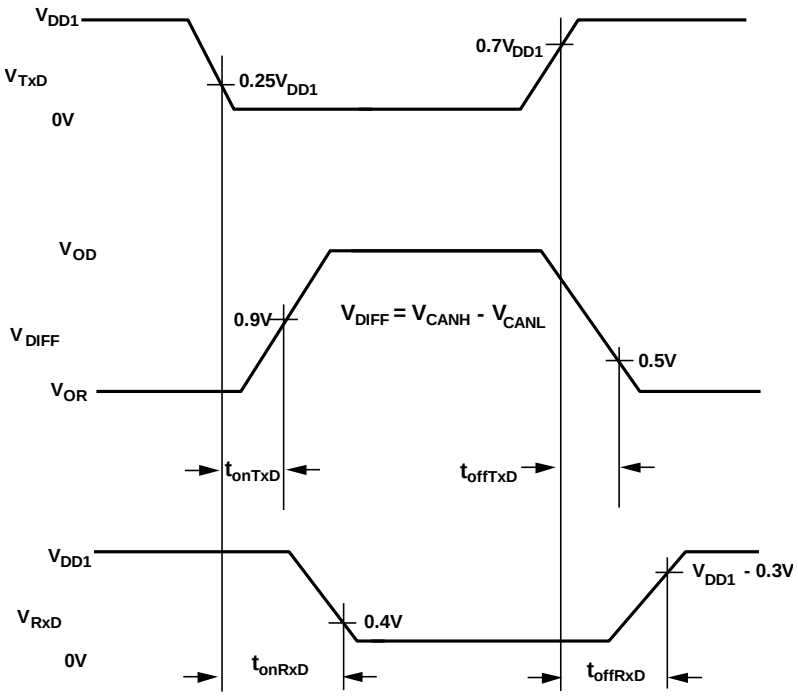


Figure 2. Driver and Receiver Propagation Delay

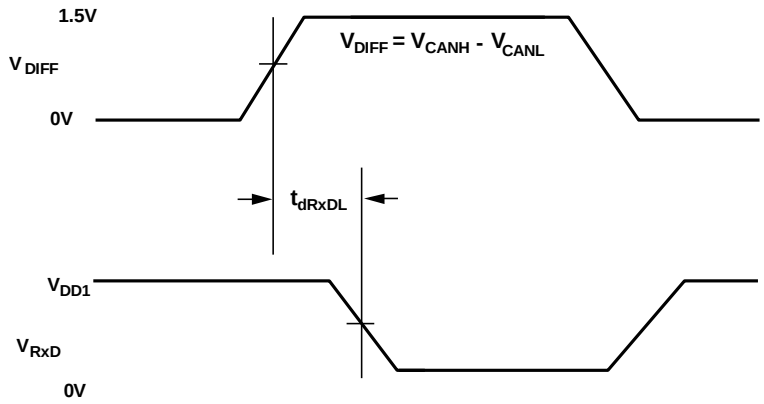


Figure 3. Bus Dominant to RxDL

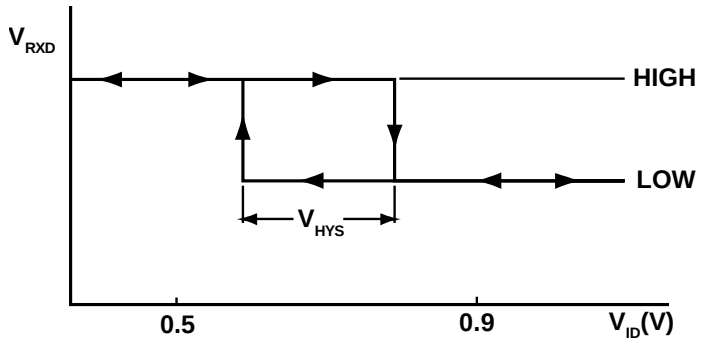


Figure 4. Receiver Input Hysteresis

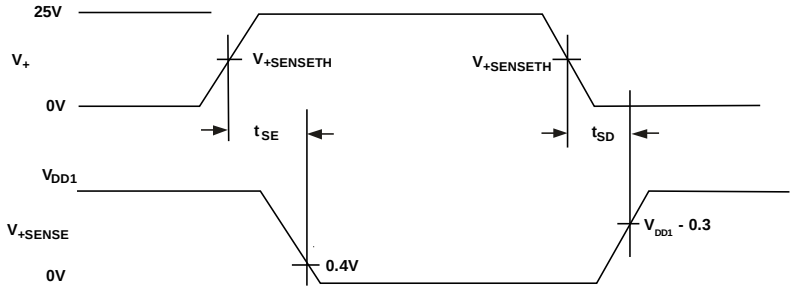


Figure 5. V_{+SENSE} Enable/Disable Time

REGULATORY INFORMATION

Table 3. Pending ADM3052 Approvals

Organization	Approval Type	Notes
UL	Recognized under the component recognition program of underwriters laboratories, Inc.	In accordance with UL 1577, each ADM3052 is proof tested by applying an insulation test voltage ≥6000 V rms for 1 second (current leakage detection limit = 5 μA)
VDE	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12	In accordance with DIN V VDE V 0884-10, each ADM3052 is proof tested by applying an insulation test voltage ≥1590 V peak for 1 second (partial discharge detection limit = 5 pC)

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 4.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		5000	V rms	1-minute duration
Minimum External Air Gap (External Clearance)	L(I01)	7.7	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	7.6	mm	Measured from input terminals to output terminals, shortest distance along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303-1
Isolation Group		IIIa		Material group (DIN VDE 0110)

VDE 0884 INSULATION CHARACTERISTICS (PENDING)

This isolator is suitable for basic electrical isolation only within the safety limit data. Maintenance of the safety data must be ensured by means of protective circuits.

Table 5.

Description	Conditions	Symbol	Characteristic	Unit
CLASSIFICATIONS				
Installation Classification per DIN VDE 0110 for Rated				
Mains Voltage				
≤150 V rms			I to IV	
≤300 V rms			I to III	
≤400 V rms			I to II	
Climatic Classification			40/85/21	
Pollution Degree	DIN VDE 0110		2	
VOLTAGE				
Maximum Working Insulation Voltage		V_{IORM}	848	V peak
Input-to-Output Test Voltage		V_{PR}		
Method b1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production tested, t_m = 1 sec, partial discharge < 5 pC		1590	V peak
Method a			1357	V peak
After Environmental Tests, Subgroup 1	$V_{IORM} \times 1.6 = V_{PR}$, t_m = 60 sec, partial discharge <5 pC			
Method a			1018	V peak
After Input and/or Safety Test, Subgroup 2/3):	$V_{IORM} \times 1.2 = V_{PR}$, t_m = 60 sec, partial discharge <5 pC			
Highest Allowable Overvoltage		V_{TR}	6000	V peak
SAFETY-LIMITING VALUES				
Case Temperature		T_S	150	°C
Input Current		$I_{S, INPUT}$	265	mA
Output Current		$I_{S, OUTPUT}$	335	mA
Insulation Resistance at T_S		R_S	$>10^9$	Ω

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. All voltages are relative to their respective ground.

Table 6.

Parameter	Rating
V_{DD1}	−0.5 V to +6 V
V_+	−36 V to +36 V
V_{+R}	−36 V to +36 V
Digital Input Voltage	
TxD	−0.5 V to V_{DD1} + 0.5 V
Digital Output Voltage	
RxD	−0.5 V to V_{DD1} + 0.5 V
V_{+SENSE}	−0.5 V to V_{DD1} + 0.5 V
CANH, CANL	−36 V to +36 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +150°C
ESD (Human Body Model) on CANH, CANL, V+ and V− pins	TBD
Lead Temperature	
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
θ_{JA} Thermal Impedance	53°C/W
T_J Junction Temperature	130°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

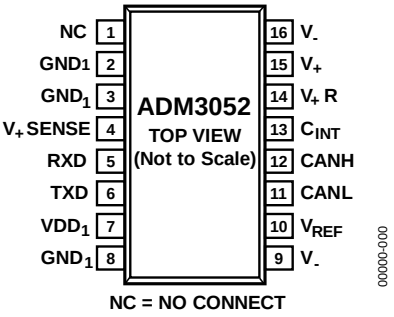


Figure 6. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NC	No Connect.
2	GND_1	Ground, Logic Side.
3	GND_1	Ground, Logic Side.
4	V_{+SENSE}	Bus Voltage Sense. A High Level on V_{+SENSE} indicates that there is Power connected on the bus on V_+ and V_-. A Low Level on V_{+SENSE} indicates that Power is not connected on the bus on V_+ and V_-.
5	RXD	Receiver Output Data.
6	TXD	Driver Input Data.
7	V_{DD1}	Power Supply Logic side. Decoupling capacitor to GND_1 required; capacitor value should be between 0.01 µF and 0.1 µF.
8	GND_1	Ground, Logic Side.
9	V_-	Ground, Bus Side.
10	V_{REF}	Reference voltage output.
11	CANL	Low-Level CAN Voltage Input/Output.
12	CANH	High-Level CAN Voltage Input/Output.
13	C_{INT}	A capacitor of 1 µF, 10 V is required on this pin.
14	V_{+R}	Connect a 300 Ω, 750 mW resistor between V_+R and V_+.
15	V_+	Bus Power Connection. Connect a 300 Ω, 750 mW resistor between V_+R and V_+.
16	V_-	Ground, Bus Side.

TEST CIRCUITS

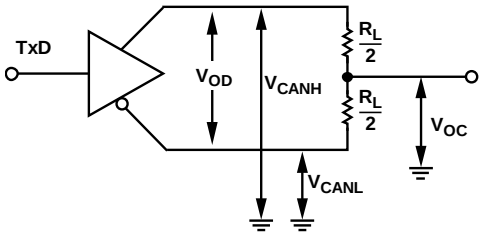


Figure 7. Driver Voltage Measurement

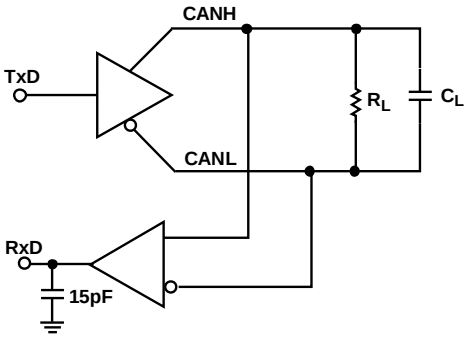


Figure 9. Switching Characteristics Measurements

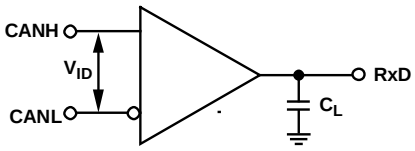


Figure 8. Receiver Voltage Measurements

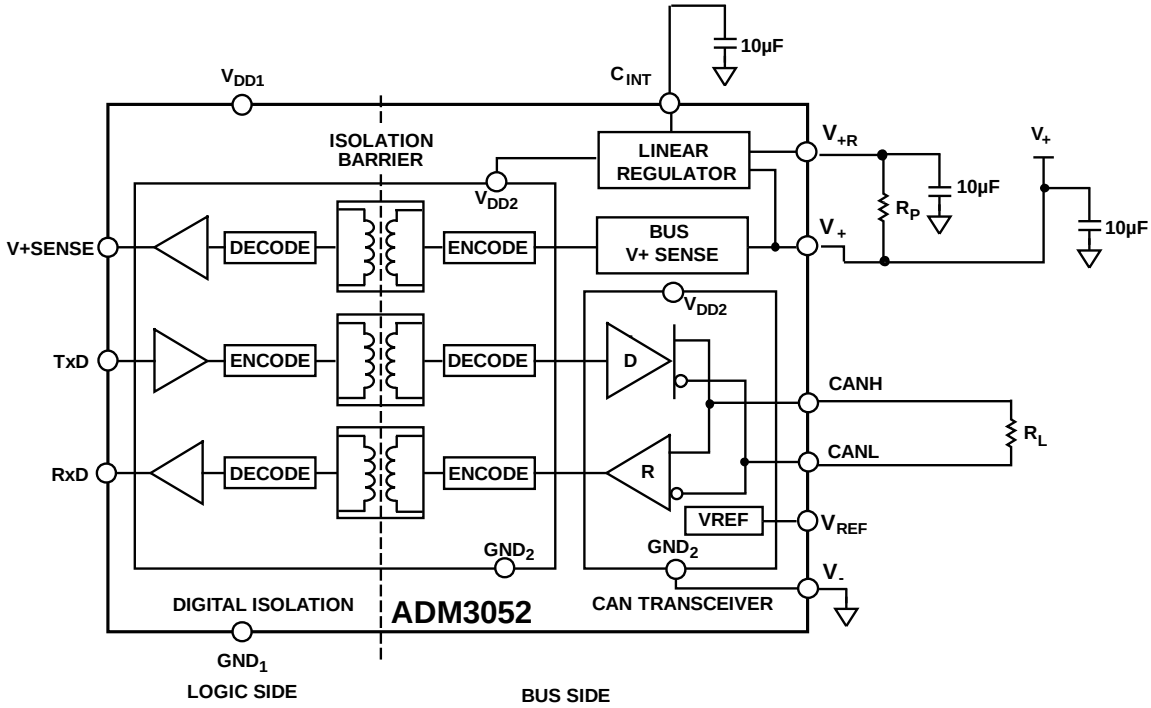


Figure 10. Supply Current Measurement Test Circuit

CIRCUIT DESCRIPTION

ELECTRICAL ISOLATION

In the ADM3052, electrical isolation is implemented on the logic side of the interface. Therefore, the part has two main sections: a digital isolation section and a transceiver section (see Figure 11). The driver input signal, which is applied to the TxD pin and referenced to the logic ground (GND_1), is coupled across an isolation barrier to appear at the transceiver section referenced to the isolated ground (V_-). Similarly, the receiver input and V+SENSE, which is referenced to the isolated ground in the transceiver section, is coupled across the isolation barrier to appear at the RxD pin and V+SENSE referenced to the logic ground respectively.

*i*Coupler *Technology*

The digital signals transmit across the isolation barrier using *i*Coupler technology. This technique uses chip scale transformer windings to couple the digital signals magnetically from one side of the barrier to the other. Digital inputs are encoded into waveforms that are capable of exciting the primary transformer winding. At the secondary winding, the induced waveforms are decoded into the binary value that was originally transmitted.

Positive and negative logic transitions at the input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than ~1 µs, a periodic set of refresh pulses, indicative of the correct input state, are sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than about 5 µs, then the input side is assumed to be unpowered or nonfunctional, in which case the output is forced to a default state (see Table 9).

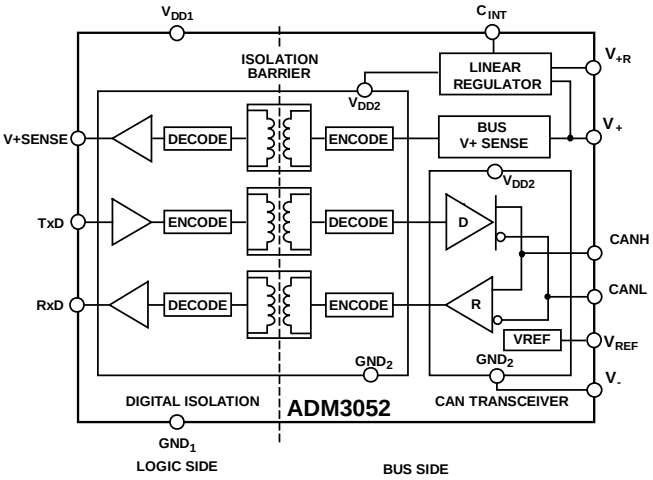


Figure 11. Digital Isolation and Transceiver Sections

TRUTH TABLES

The truth tables in this section use the abbreviations shown in Table 8.

Table 8. Truth Table Abbreviations

Letter	Description
H	High level
L	Low level
I	Indeterminate
X	Don't Care
Z	High impedance (off)
NC	Disconnected

Table 9. Transmitting

Supply Status		Input	Outputs			
V_{DD1}	V_+	TxD	Bus State	CANH	CANL	V+Sense
On	On	L	Dominant	H	L	L
On	On	H	Recessive	Z	Z	L
On	On	Floating	Recessive	Z	Z	L
Off	On	X	Recessive	Z	Z	I
On	Off	L	I	I	I	H

Table 10. Receiving

Supply Status		Inputs		Outputs	
V_{DD1}	V_+	V_{ID} = CANH – CANL	Bus State	RxD	V+Sense
On	On	≥ 0.9V	Dominant	L	L
On	On	≤ 0.5V	Recessive	H	L
On	On	0.5V < V_{ID} < 0.9V	I	I	L
On	On	Inputs open	Recessive	H	L
Off	On	X	X	I	I
On	Off	X	X	H	H

THERMAL SHUTDOWN

The ADM3052 contains thermal shutdown circuitry that protects the part from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature under this condition and disables the driver outputs. This circuitry is designed to disable the driver outputs when a junction temperature of 150°C is reached. As the device cools, the drivers re-enable at a temperature of 140°C.

LINEAR REGULATOR

The linear regulator takes the V+ bus power (ranging between 11V and 25V) and regulates this voltage to 5V, to provide power to the internal bus-side circuitry (iCoupler isolation, V+sense and transceiver circuits). The linear regulator uses two regulation loops to share the power dissipation between the internal die and an external resistor. This reduces the internal heat dissipation in the package. The 300Ω external resistor should be capable of dissipating 750mW of power and have a tolerance of 1%.

MAGNETIC FIELD IMMUNITY

The limitation on the magnetic field immunity of the *i*Coupler is set by the condition in which an induced voltage in the receiving coil of the transformer is large enough to either falsely set or reset the decoder. The following analysis defines the conditions under which this may occur. The 3 V operating condition of the ADM3052 is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1 V. The decoder has a sensing threshold of about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated.

The voltage induced across the receiving coil is given by

$$V = \left(\frac{-d\beta}{dt}\right)\sum \pi r_n^2 \; ; \; n = 1, 2, \ldots, N$$

where:
β is the magnetic flux density (gauss).
N is the number of turns in the receiving coil.
r_n is the radius of the nth turn in the receiving coil (cm).

Given the geometry of the receiving coil and an imposed requirement that the induced voltage is, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field can be determined using Figure 12.

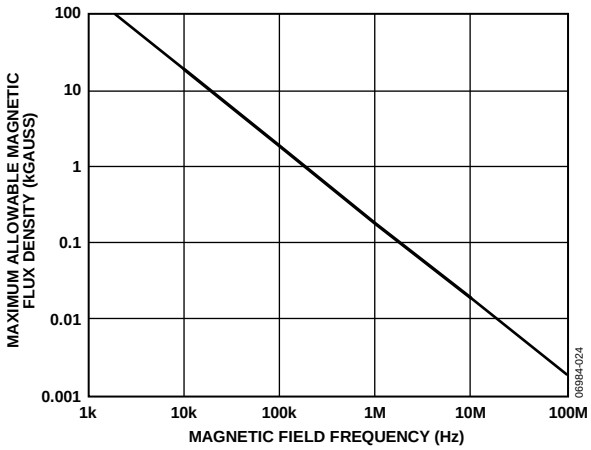


Figure 12. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse and is the worst-case polarity, it reduces the received pulse from >1.0 V to 0.75 V, still well above the 0.5 V sensing threshold of the decoder.

Figure 13 shows the magnetic flux density values in terms of more familiar quantities, such as maximum allowable current flow at given distances away from the ADM3052 transformers.

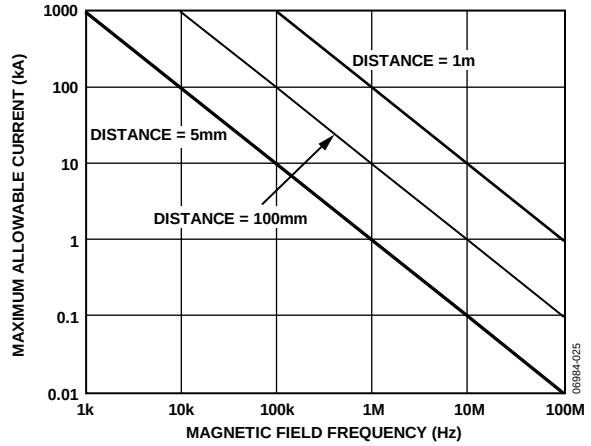


Figure 13. Maximum Allowable Current for Various Current-to-ADM3052 Spacings

With combinations of strong magnetic field and high frequency, any loops formed by PCB traces can induce error voltages large enough to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

APPLICATIONS INFORMATION

TYPICAL APPLICATIONS

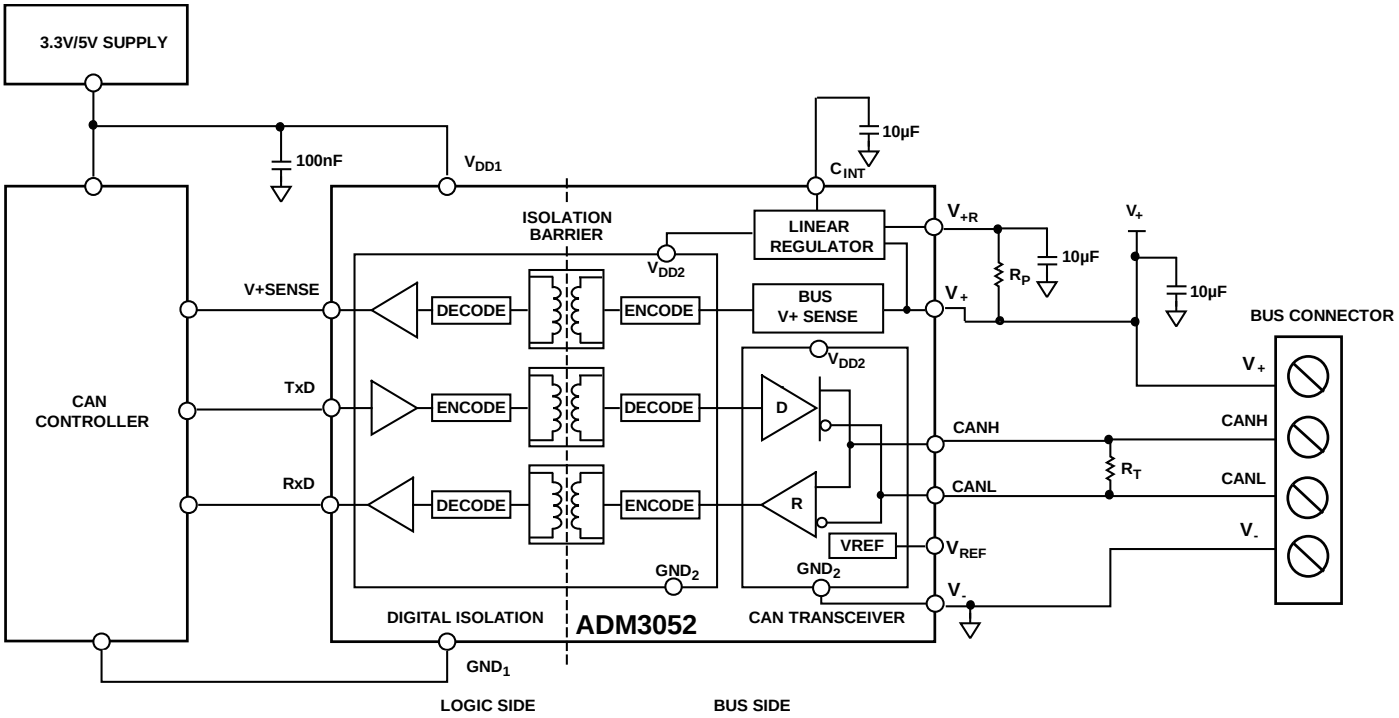
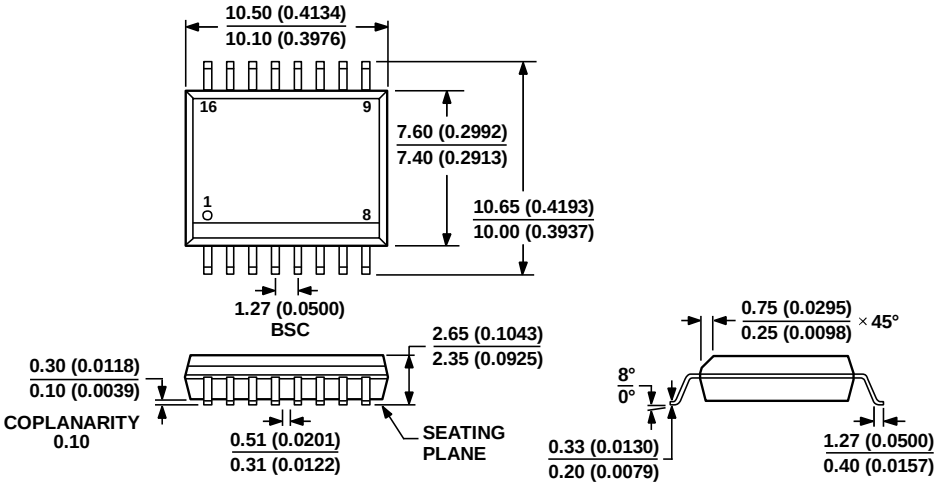


Figure 14. Typical Isolated CAN Node using the ADM3052

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

032707-B

Figure 15. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADM3052BRWZ	−40°C to +85°C	16-Lead SOIC_W	RW-16
ADM3052BRWZ-REEL7	−40°C to +85°C	16-Lead SOIC_W	RW-16

[1] Z = RoHS Compliant Part.

NOTES

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