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SEMICONDUCTOR ™

MM74HC165
Parallel-in/Serial-out 8-Bit Shift Register

General Description

The MM74HC165 high speed PARALLEL-IN/SERIAL-OUT SHIFT REGISTER utilizes advanced silicon-gate CMOS technology. It has the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

This 8-bit serial shift register shifts data from Q_A to Q_H when clocked. Parallel inputs to each stage are enabled by a low level at the SHIFT/LOAD input. Also included is a gated CLOCK input and a complementary output from the eighth bit.

Clocking is accomplished through a 2-input NOR gate permitting one input to be used as a CLOCK INHIBIT function. Holding either of the CLOCK inputs high inhibits clocking, and holding either CLOCK input low with the SHIFT/LOAD input high enables the other CLOCK input. Data transfer occurs on the positive going edge of the clock. Parallel loading is inhibited as long as the SHIFT/LOAD input is HIGH. When taken LOW, data at the parallel inputs is loaded directly into the register independent of the state of the clock.

The 74HC logic family is functionally as well as pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns (clock to Q)
- Wide operating supply voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent supply current: 80 μA maximum (74HC Series)
- Fanout of 10 LS-TTL loads

Ordering Code:

Order Number	Package Number	Package Description
MM74HC165M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC165SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC165MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC165	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP

Top View
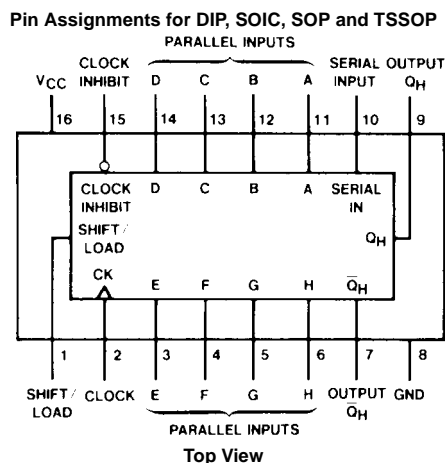
Function Table

Inputs					Internal Outputs		Output Q_H
Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A. . .H	Q_A	Q_B	
L	X	X	X	a. . .h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{AN}	Q_{GN}
H	L	↑	L	X	L	Q_{AN}	Q_{GN}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = HIGH Level (steady state), L = LOW Level (steady state)
X = Irrelevant (any input, including transitions)
↑ = Transition from LOW-to-HIGH level
Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{AN}, Q_{GN} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

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Logic Diagrams
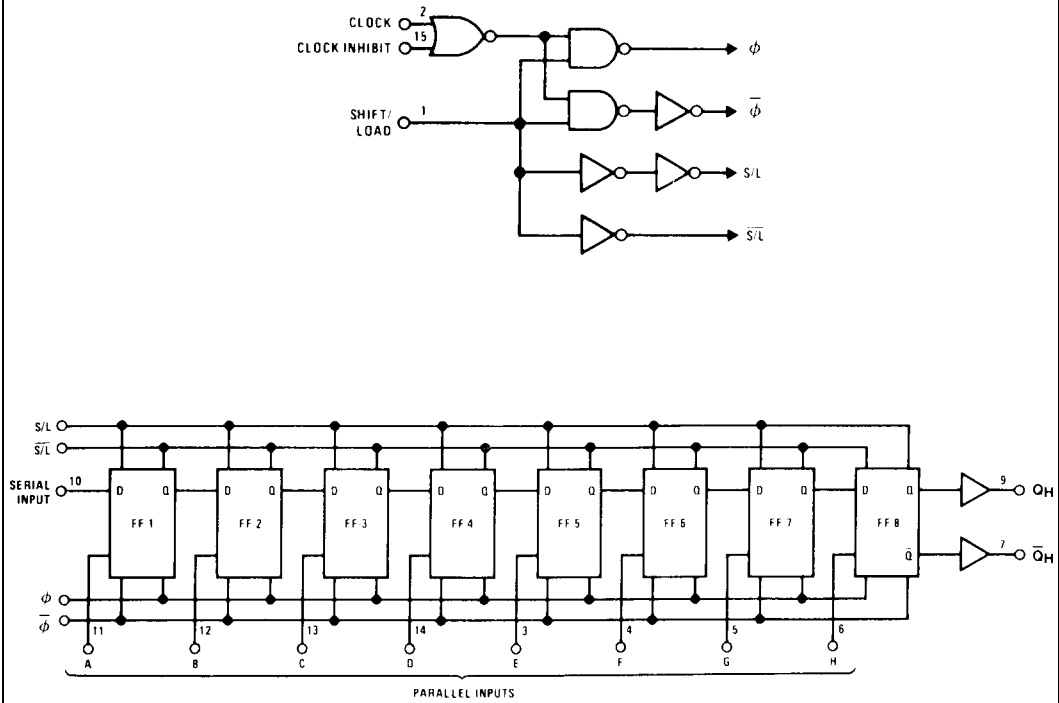
Absolute Maximum Ratings(Note 1)

(Note 2)

Supply Voltage (V$_{CC}$)	−0.5 to +7.0V
DC Input Voltage (V$_{IN}$)	−1.5 to V$_{CC}$ +1.5V
DC Output Voltage (V$_{OUT}$)	−0.5 to V$_{CC}$ +0.5V
Clamp Diode Current (I$_{IK}$, I$_{OK}$)	±20 mA
DC Output Current, per pin (I$_{OUT}$)	±25 mA
DC V$_{CC}$ or GND Current, per pin (I$_{CC}$)	±50 mA
Storage Temperature Range (T$_{STG}$)	−65°C to +150°C
Power Dissipation (P$_D$)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T$_L$)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V$_{CC}$)	2	6	V
DC Input or Output Voltage			
(V$_{IN}$, V$_{OUT}$)	0	V$_{CC}$	V
Operating Temperature Range (T$_A$)	−40	+85	°C
Input Rise or Fall Times			
(t$_r$, t$_f$) V$_{CC}$ = 2.0V		1000	ns
V$_{CC}$ = 4.5V		500	ns
V$_{CC}$ = 6.0V		400	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: − 12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V$_{CC}$	T$_A$ = 25°C	T$_A$ = −40 to 85°C	T$_A$ = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V$_{IH}$	Minimum HIGH Level		2.0V		1.5	1.5	1.5	V
	Input Voltage		4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V$_{IL}$	Maximum LOW Level		2.0V		0.5	0.5	0.5	V
	Input Voltage		4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V$_{OH}$	Minimum HIGH Level	V$_{IN}$ = V$_{IH}$ or V$_{IL}$					
	Output Voltage	|I$_{OUT}$| ≤ 20 µA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V$_{IN}$ = V$_{IH}$ or V$_{IL}$					
		|I$_{OUT}$| ≤ 4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I$_{OUT}$| ≤ 5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V$_{OL}$	Maximum LOW Level	V$_{IN}$ = V$_{IH}$ or V$_{IL}$					
	Output Voltage	|I$_{OUT}$| ≤ 20 µA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V$_{IN}$ = V$_{IH}$ or V$_{IL}$					
		|I$_{OUT}$| ≤ 4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I$_{OUT}$| ≤ 5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I$_{IN}$	Maximum Input Current	V$_{IN}$ = V$_{CC}$ or GND V$_{CC}$ = 2–6V	6.0V		±0.1	±1.0	±1.0	µA
I$_{CC}$	Maximum Quiescent Supply Current	V$_{IN}$ = V$_{CC}$ or GND I$_{OUT}$ = 0 µA V$_{CC}$ = 2–6V	6.0V		8.0	80	160	µA

Note 4: For a power supply of 5V ±10% the worst case output voltages (V$_{OH}$, and V$_{OL}$) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V$_{IH}$ and V$_{IL}$ occur at V$_{CC}$ = 5.5V and 4.5V respectively. (The V$_{IH}$ value at 5.5V is 3.85V.) The worst case leakage current (I$_{IN}$, I$_{CC}$, and I$_{OZ}$) occur for CMOS at the higher voltage and so the 6.0V values should be used.

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AC Electrical Characteristics

$V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay H to Q_H or $\overline{Q}_H$		15	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Serial Shift/Parallel Load to Q_H		13	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Output		15	25	ns
t_S	Minimum Setup Time Serial Input to Clock, Parallel or Data to Shift/Load		10	20	ns
t_S	Minimum Setup Time Shift/Load to Clock		11	20	ns
t_S	Minimum Setup Time Clock Inhibit to Clock		10	20	ns
t_H	Minimum Hold Time Serial Input to Clock or Parallel Data to Shift/Load			0	ns
t_W	Minimum Pulse Width Clock			16	ns

AC Electrical Characteristics

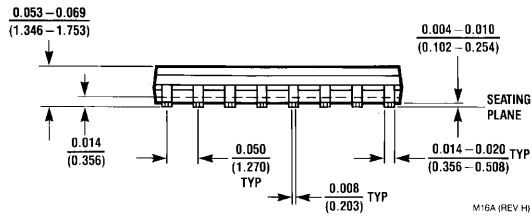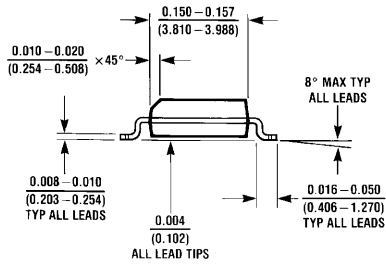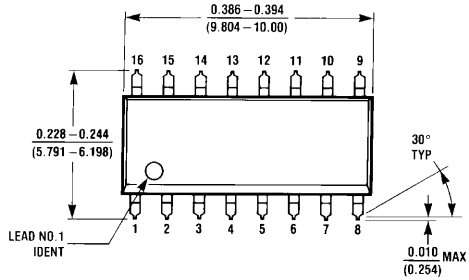$C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$ Typ	$T_A = 25°C$ Guaranteed Limits	$T_A = -40$ to $85°C$	$T_A = -55$ to $125°C$	Units
f_{MAX}	Maximum Operating Frequency		2.0V	10	5	4	4	MHz
			4.5V	45	27	21	18	MHz
			6.0V	50	32	25	21	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay H to Q_H or $\overline{Q}_H$		2.0V	70	150	189	225	ns
			4.5V	21	30	38	45	ns
			6.0V	18	26	33	39	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Serial Shift/Parallel Load to Q_H		2.0V	70	175	220	260	ns
			4.5V	21	35	44	52	ns
			6.0V	18	30	37	44	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Output		2.0V	70	150	189	225	ns
			4.5V	21	30	38	45	ns
			6.0V	18	26	33	39	ns
t_S	Minimum Setup Time Serial Input to Clock, or Parallel Data to Shift/Load		2.0V	35	100	125	150	ns
			4.5V	11	20	25	30	ns
			6.0V	9	17	21	25	ns
t_S	Minimum Setup Time Shift/Load to Clock		2.0V	38	100	125	150	ns
			4.5V	12	20	25	30	ns
			6.0V	9	17	21	25	ns
t_S	Minimum Setup Time Clock Inhibit to Clock		2.0V	35	100	125	150	ns
			4.5V	11	20	25	30	ns
			6.0V	9	17	21	25	ns
t_H	Minimum Hold Time Serial Input to Clock or Parallel Data to Shift/Load		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Pulse Width, Clock		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	18	20	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	9	15	19	22	ns
			6.0V	8	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns

AC Electrical Characteristics (Continued)

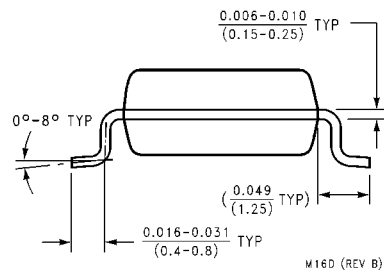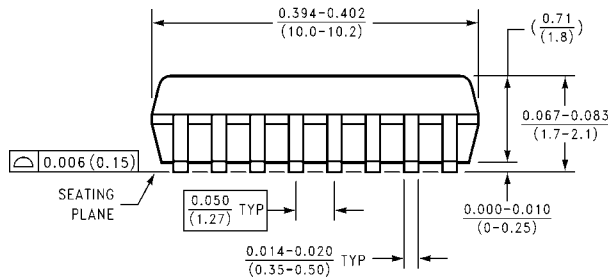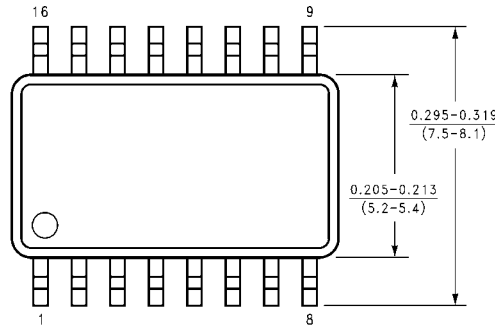| Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	$T_A = -40$ to $85°C$	$T_A = -55$ to $125°C$		Units
				Typ	Guaranteed Limits			
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		100				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

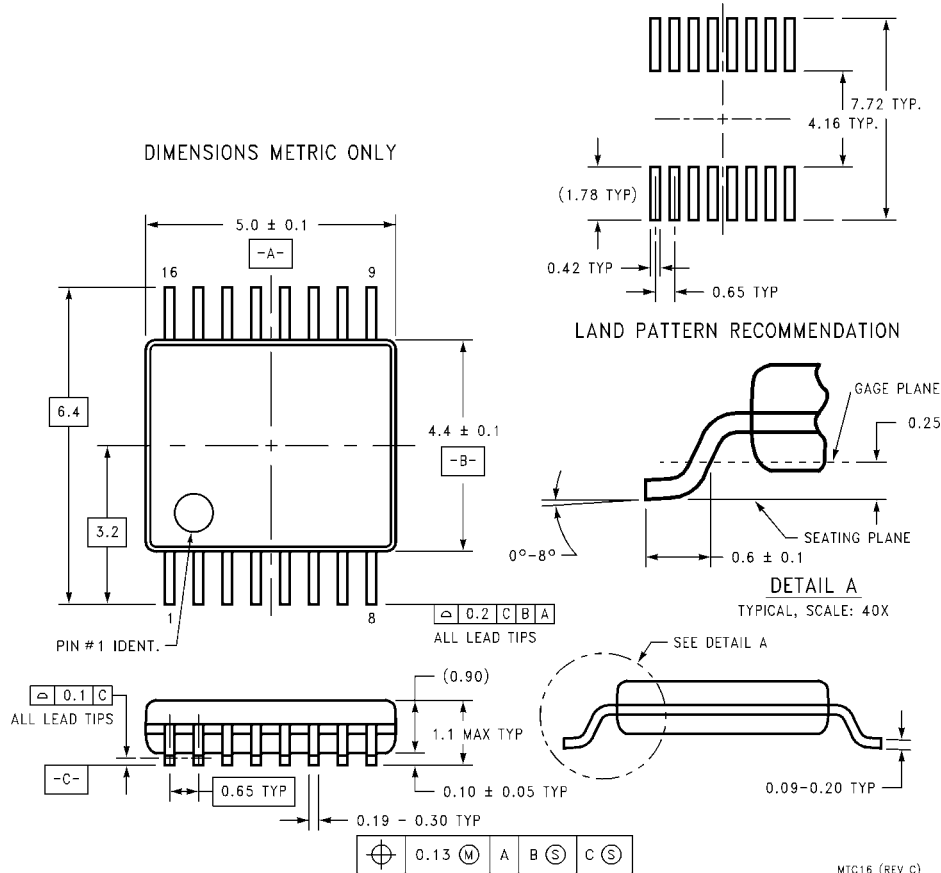**Physical Dimensions** inches (millimeters) unless otherwise noted

0.386 − 0.394
(9.804 − 10.00)

0.228 − 0.244
(5.791 − 6.198)

30°
TYP

LEAD NO.1
IDENT

0.010 MAX
(0.254)

0.150 − 0.157
(3.810 − 3.988)

0.010 − 0.020
(0.254 − 0.508) × 45°

8° MAX TYP
ALL LEADS

0.008 − 0.010
(0.203 − 0.254)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.053 − 0.069
(1.346 − 1.753)

0.004 − 0.010
(0.102 − 0.254)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008
(0.203) TYP

0.014 − 0.020 TYP
(0.356 − 0.508)

M16A (REV H)

16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A

0.295−0.319
(7.5−8.1)

0.205−0.213
(5.2−5.4)

0.394−0.402
(10.0−10.2)

(0.71)
(1.8)

0.067−0.083
(1.7−2.1)

0.006−0.010 TYP
(0.15−0.25)

0.006 (0.15)

SEATING
PLANE

0.050 TYP
(1.27)

0.000−0.010
(0−0.25)

0.014−0.020 TYP
(0.35−0.50)

0°−8° TYP

(0.049 TYP)
(1.25)

0.016−0.031 TYP
(0.4−0.8)

M16D (REV B)

16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

DIMENSIONS METRIC ONLY

7.72 TYP.
4.16 TYP.

(1.78 TYP)

0.42 TYP
0.65 TYP

LAND PATTERN RECOMMENDATION

5.0 ± 0.1
−A−

16   9

6.4

4.4 ± 0.1
−B−

3.2

GAGE PLANE
0.25

SEATING PLANE
0°−8°
0.6 ± 0.1

DETAIL A
TYPICAL, SCALE: 40X

1   8
⌖ 0.2 C B A
ALL LEAD TIPS

PIN #1 IDENT.

SEE DETAIL A

⌖ 0.1 C
ALL LEAD TIPS

(0.90)

1.1 MAX TYP

−C−
0.65 TYP
0.10 ± 0.05 TYP

0.19 − 0.30 TYP

0.09−0.20 TYP

⌖ 0.13 Ⓜ A B Ⓢ C Ⓢ

MTC16 (REV C)

16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)
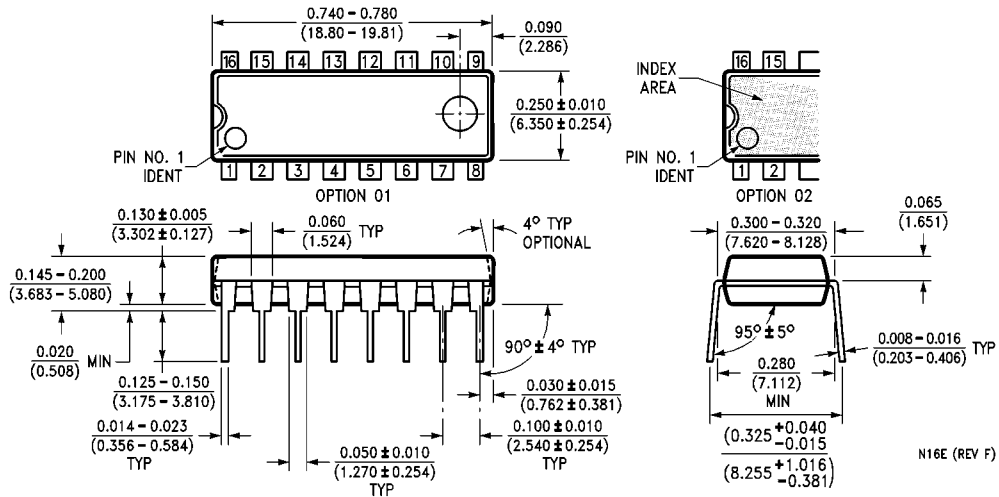
16-Lead Plastic Dual-In-Line Package (PDIP), MS-001, 0.300" Wide
Package N16E

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