ARM Cortex™-M0

32-BIT MICROCONTROLLER

NuMicro™ Family
NUC130 Product Brief

For additional information or questions, please contact: Nuvoton Technology Corporation.

Contents

Figures

Tables

1 GENERAL DESCRIPTION

The NuMicro™ NUC100 Series is 32-bit microcontrollers with embedded ARM® Cortex™-M0 core for industrial control and applications which need rich communication interfaces. The Cortex™-M0 is the newest ARM® embedded processor with 32-bit performance and at a cost equivalent to traditional 8-bit microcontroller. NuMicro™ NUC100 Series includes NUC100, NUC120, NUC130 and NUC140 product line.

The NuMicro™ NUC130 Automotive Line with CAN function embeds Cortex™-M0 core running up to 50 MHz with 32K/64K/128K-byte embedded flash, 4K/8K/16K-byte embedded SRAM, and 4K-byte loader ROM for the ISP. It also equips with plenty of peripheral devices, such as Timers, Watchdog Timer, RTC, PDMA, UART, SPI, I^2C, I^2S, PWM Timer, GPIO, LIN, CAN, PS/2, 12-bit ADC, Analog Comparator, Low Voltage Reset Controller and Brown-out Detector.

Product Line	UART	SPI	I^2C	USB	LIN	CAN	PS/2	I^2S
NUC100	•	•	•				•	•
NUC120	•	•	•	•			•	•
NUC130	•	•	•		•	•	•	•
NUC140	•	•	•	•	•	•	•	•

Table 1-1 Connectivity Supported Table

2 FEATURES

The equipped features are dependent on the product line and their sub products.

2.1 NuMicro™ NUC130 Features – Automotive Line

- Core
  - ARM® Cortex™-M0 core runs up to 50 MHz
  - One 24-bit system timer
  - Supports low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Build-in LDO for wide operating voltage ranges from 2.5 V to 5.5 V
- Flash Memory
  - 32K/64K/128K bytes Flash for program code
  - 4KB flash for ISP loader
  - Support In-system program (ISP) application code update
  - 512 byte page erase for flash
  - Configurable data flash address and size for 128KB system, fixed 4KB data flash for the 32KB and 64KB system
  - Support 2 wire ICP update through SWD/ICE interface
  - Support fast parallel programming mode by external programmer
- SRAM Memory
  - 4K/8K/16K bytes embedded SRAM
  - Support PDMA mode
- PDMA (Peripheral DMA)
  - Support 9 channels PDMA for automatic data transfer between SRAM and peripherals
- Clock Control
  - Flexible selection for different applications
  - Built-in 22.1184 MHz high speed OSC for system operation
    - Trimmed to ± 1 % at +25 ℃ and V_{DD} = 5 V
    - Trimmed to ± 3 % at -40 ℃ ~ +85 ℃ and V_{DD} = 2.5 V ~ 5.5 V
  - Built-in 10 KHz low speed OSC for Watchdog Timer and Wake-up operation
  - Support one PLL, up to 50 MHz, for high performance system operation
  - External 4~24 MHz high speed crystal input for precise timing operation
  - External 32.768 kHz low speed crystal input for RTC function and low power system operation
- GPIO
  - Four I/O modes:
    - Quasi bi-direction
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable
  - I/O pin can be configured as interrupt source with edge/level setting
  - High driver and high sink IO mode support
- Timer

- Support 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle and continuous counting operation modes
- Support event counting function
- Support input capture function

- Watchdog Timer
  - Multiple clock sources
  - 8 selectable time out period from 1.6ms ~ 26.0sec (depends on clock source)
  - WDT can wake-up from power down or idle mode
  - Interrupt or reset selectable on watchdog time-out
- RTC
  - Support software compensation by setting frequency compensate register (FCR)
  - Support RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Support Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Support periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Support wake-up function
- PWM/Capture
  - Built-in up to four 16-bit PWM generators provide eight PWM outputs or four complementary paired PWM outputs
  - Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit prescaler and one Dead-Zone generator for complementary paired PWM
  - Up to eight 16-bit digital Capture timers (shared with PWM timers) provide eight rising/falling capture inputs
  - Support Capture interrupt
- UART
  - Up to three UART controllers
  - UART ports with flow control (TXD, RXD, CTS and RTS)
  - UART0 with 64-byte FIFO is for high speed
  - UART1/2(optional) with 16-byte FIFO for standard device
  - Support IrDA (SIR) and LIN function
  - Support RS-485 9-bit mode and direction control.
  - Programmable baud-rate generator up to 1/16 system clock
  - Support PDMA mode
- SPI
  - Up to four sets of SPI controller
  - Master up to 32 MHz, and Slave up to 10 MHz (chip working @ 5V)
  - Support SPI master/slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 1 to 32 bits
  - MSB or LSB first data transfer
  - Rx and Tx on both rising or falling edge of serial clock independently
  - 2 slave/device select lines when it is as the master, and 1 slave/device select line when it is as the slave
  - Support byte suspend mode in 32-bit transmission
  - Support PDMA mode
  - Support three wire, no slave select signal, bi-direction interface

- I^2C
  - Up to two sets of I^2C device
  - Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allow versatile rate control
  - Support multiple address recognition (four slave address with mask option)
- I^2S
  - Interface with external audio CODEC
  - Operate as either master or slave mode
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Mono and stereo audio data supported
  - I^2S and MSB justified data format supported
  - Two 8 word FIFO data buffers are provided, one for transmit and one for receive
  - Generates interrupt requests when buffer levels cross a programmable boundary
  - Support two DMA requests, one for transmit and one for receive
- PS/2 Device Controller
  - Host communication inhibit and request to send detection
  - Reception frame error detection
  - Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
  - Double buffer for data reception
  - S/W override bus
- CAN 2.0
  - Supports CAN protocol version 2.0 part A and B
  - Bit rates up to 1M bit/s
  - 32 Message Objects
  - Each Message Object has its won identifier mask
  - Programmable FIFO mode (concatenation of Message Object)
  - Maskable interrupt
  - Disabled Automatic Re-transmission mode for Time Triggered CAN applications
  - Support power down wake-up function
- EBI (External bus interface) support (100-pin and 64-pin Package Only)
  - Accessible space: 64KB in 8-bit mode or 128KB in 16-bit mode
  - Support 8-/16-bit data width
  - Support byte write in 16-bit data width mode
- ADC
  - 12-bit SAR ADC with 700K SPS
  - Up to 8-ch single-end input or 4-ch differential input
  - Single scan/single cycle scan/continuous scan
  - Each channel with individual result register
  - Scan on enabled channels
  - Threshold voltage detection
  - Conversion start by software programming or external input

- Support PDMA mode

- Analog Comparator
  - Up to two analog comparator
  - External input or internal bandgap voltage selectable at negative node
  - Interrupt when compare result change
  - Power down wake-up
- One built-in temperature sensor with 1℃ resolution
- Brown-Out detector
  - With 4 levels: 4.5 V/3.8 V/2.7 V/2.2 V
  - Support Brown-Out Interrupt and Reset option
- Low Voltage Reset
  - Threshold voltage levels: 2.0 V
- Operating Temperature: -40℃~85℃
- Packages:
  - All Green package (RoHS)
  - LQFP 100-pin / 64-pin / 48-pin

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 NuMicro™ NUC130 Products Selection Guide

3.1.1 NuMicro™ NUC130 Automotive Line Selection Guide

Part number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity						I^2S	Comp.	PWM	ADC	RTC	EBI	ISP ICP	Package
							UART	SPI	I^2C	USB	LIN	CAN								
NUC130LC1CN	32 KB	4 KB	4 KB	4 KB	up to 35	4x32-bit	3	1	2	-	2	1	1	1	4	8x12-bit	v	-	v	LQFP48
NUC130LD2CN	64 KB	8 KB	4 KB	4 KB	up to 35	4x32-bit	3	1	2	-	2	1	1	1	4	8x12-bit	v	-	v	LQFP48
NUC130LE3CN	128 KB	16 KB	Definable	4 KB	up to 35	4x32-bit	3	1	2	-	2	1	1	1	4	8x12-bit	v	-	v	LQFP48
NUC130RC1CN	32 KB	4 KB	4 KB	4 KB	up to 49	4x32-bit	3	2	2	-	2	1	1	2	6	8x12-bit	v	v	v	LQFP64
NUC130RD2CN	64 KB	8 KB	4 KB	4 KB	up to 49	4x32-bit	3	2	2	-	2	1	1	2	6	8x12-bit	v	v	v	LQFP64
NUC130RD3CN	128 KB	16 KB	Definable	4 KB	up to 49	4x32-bit	3	2	2	-	2	1	1	2	6	8x12-bit	v	v	v	LQFP64
NUC130VE3CN	128 KB	16 KB	Definable	4 KB	up to 80	4x32-bit	3	4	2	-	2	1	1	2	8	8x12-bit	v	v	v	LQFP100

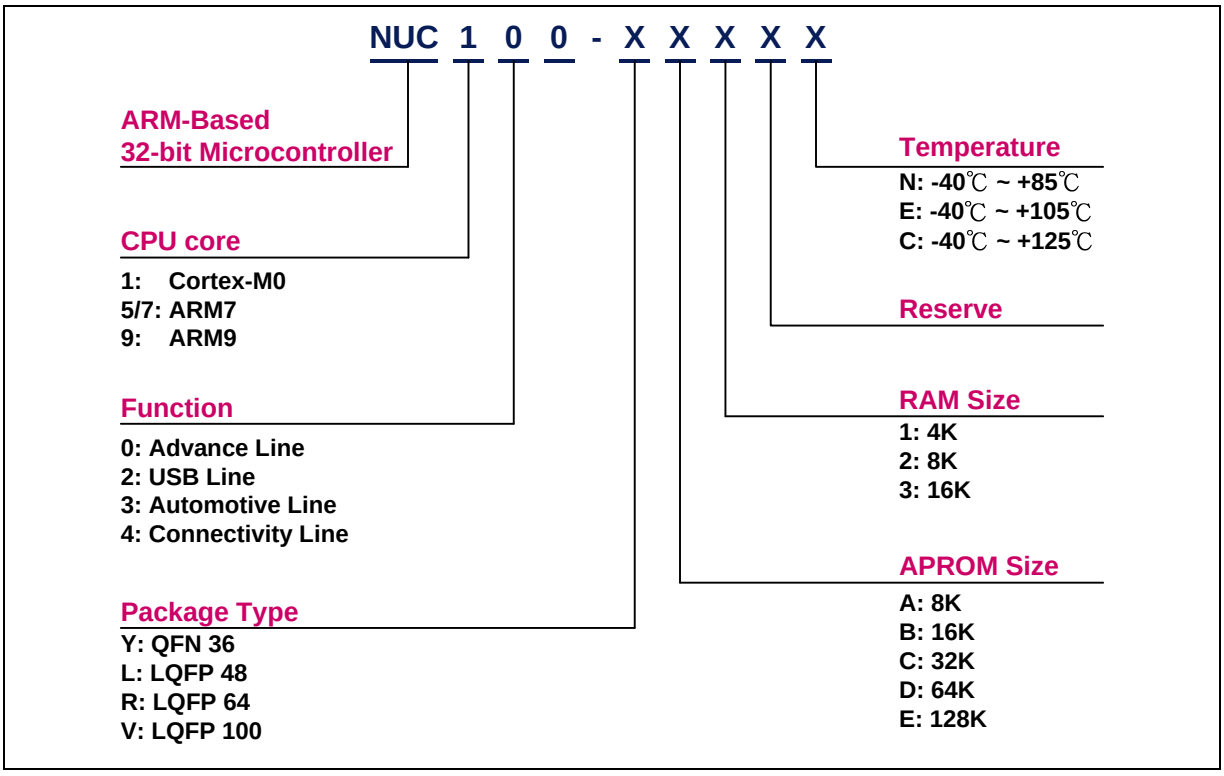


Figure 3-1 NuMicro™ NUC100 Series selection code

3.2 Pin Configuration

3.2.1 NuMicro™ NUC130 Pin Diagram

3.2.1.1 NuMicro™ NUC130 LQFP 100 pin

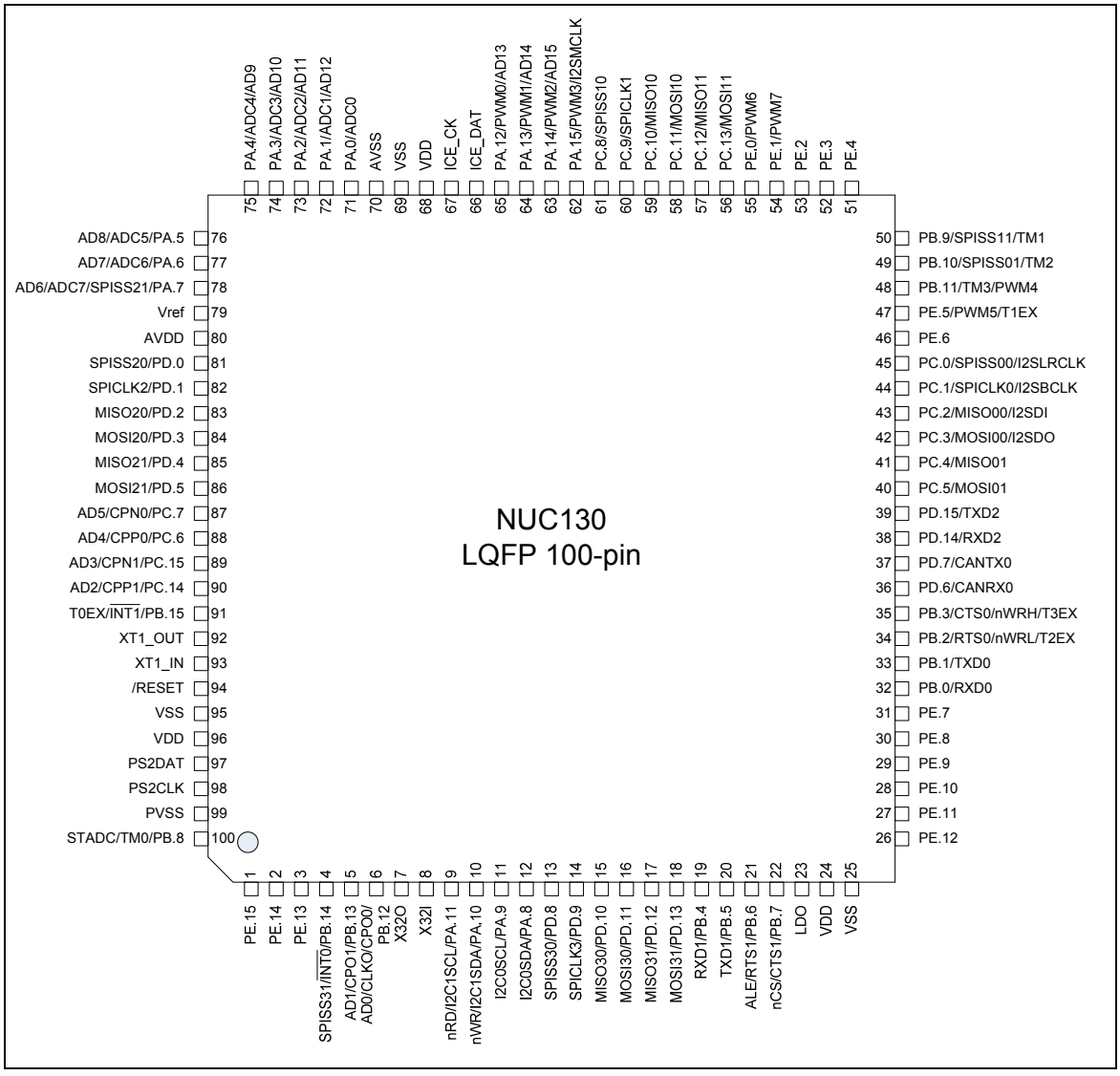


Figure 3-2 NuMicro™ NUC130 LQFP 100-pin Pin Diagram

3.2.1.2 NuMicro™ NUC130 LQFP 64 pin

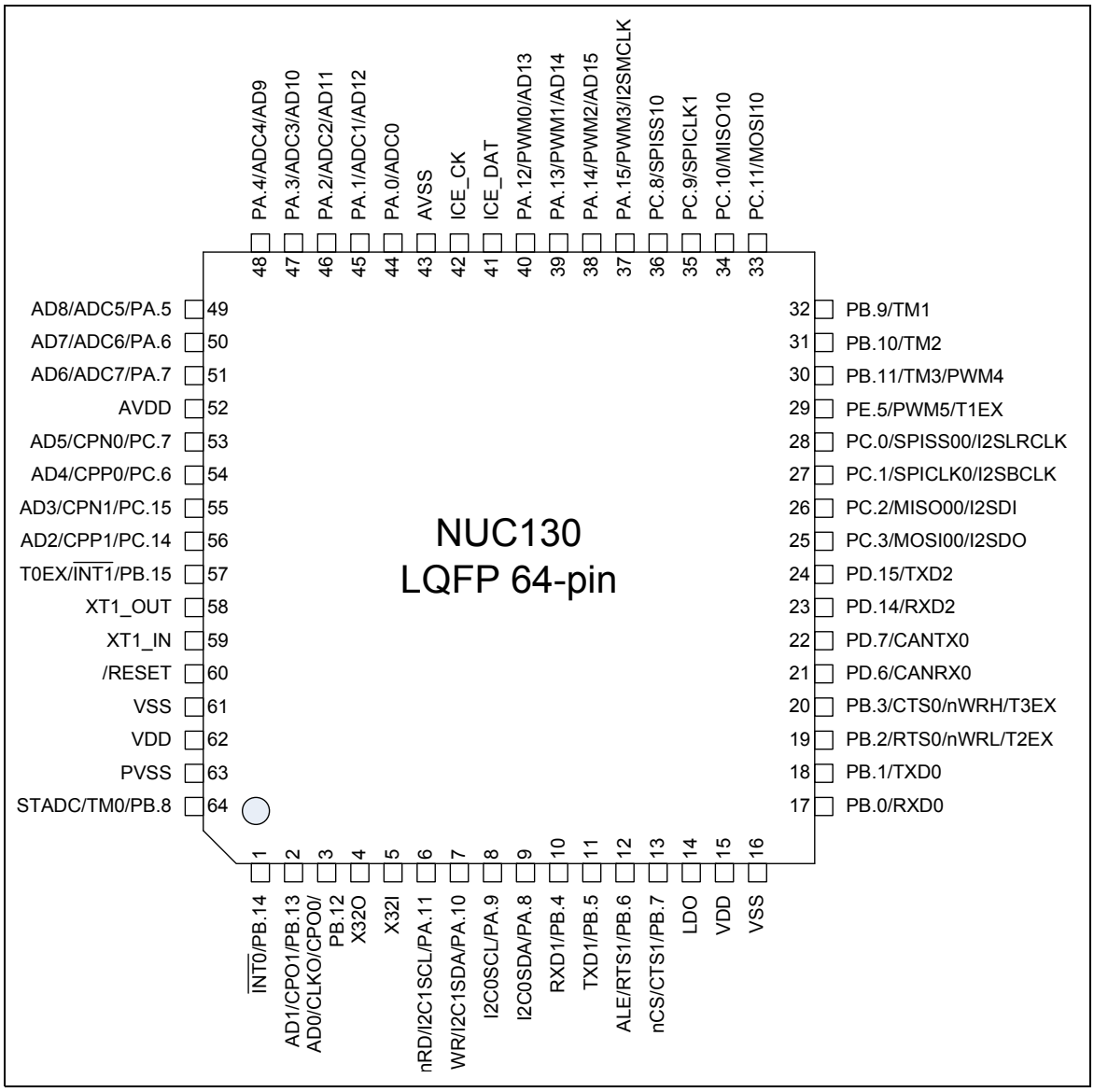


Figure 3-3 NuMicro™ NUC130 LQFP 64-pin Pin Diagram

3.2.1.3 NuMicro™ NUC130 LQFP 48 pin

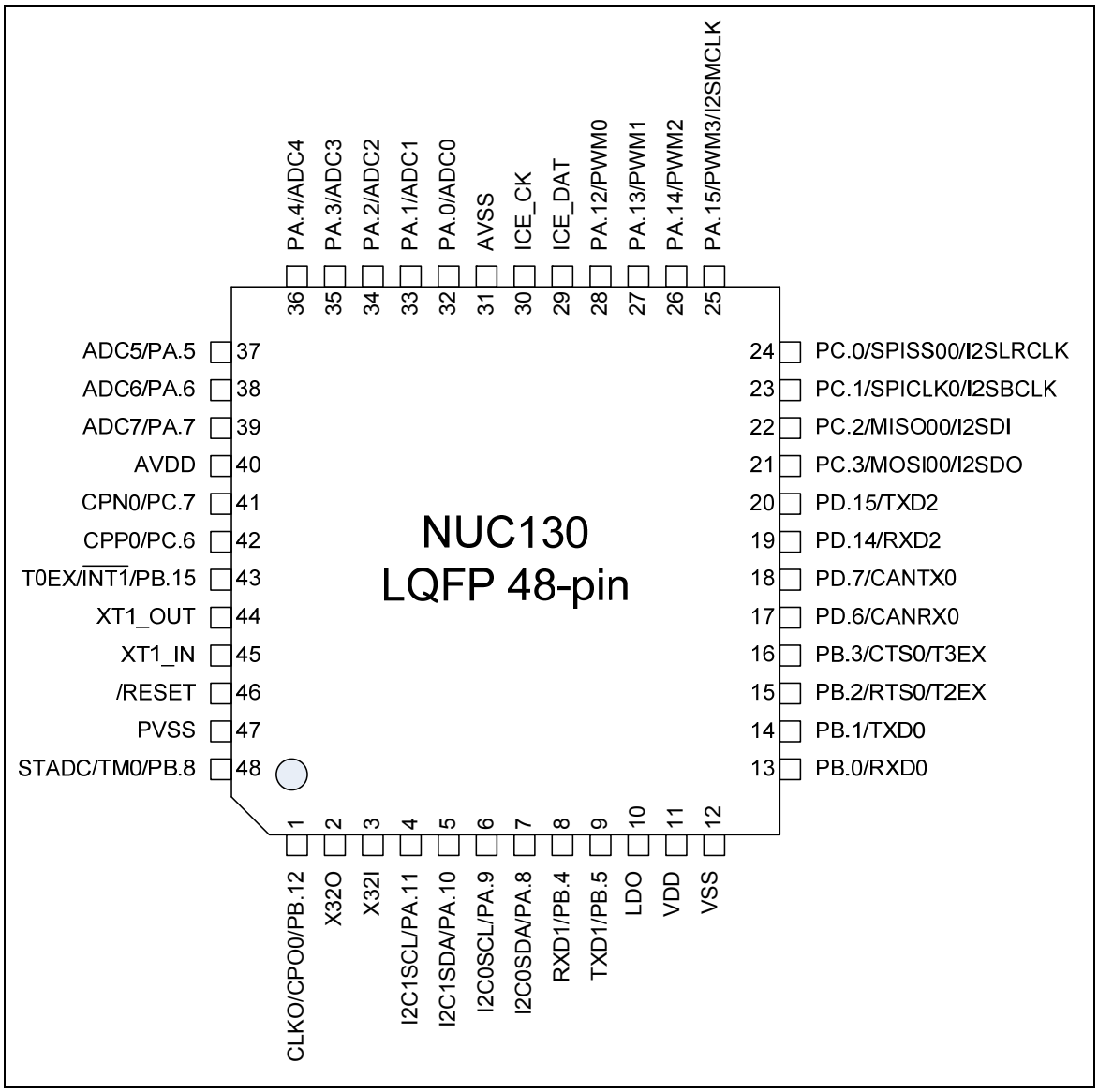


Figure 3-4 NuMicro™ NUC130 LQFP 48-pin Pin Diagram

3.3 Pin Description

3.3.1 NuMicro™ NUC130 Pin Description

3.3.1.1 NuMicro™ NUC130 Pin Description

Pin No.			Pin Name	Pin Type		Description
LQFP 100	LQFP 64	LQFP 48				
1			PE.15	**I/O**		General purpose input/output digital pin
2			PE.14	**I/O**		General purpose input/output digital pin
3			PE.13	**I/O**		General purpose input/output digital pin
4	1		PB.14	**I/O**		General purpose input/output digital pin
			/INT0	**I**		/INT0: External interrupt1 input pin
			SPISS31	**I/O**		SPISS31: SPI3 2nd slave select pin
5	2		PB.13	**I/O**		General purpose input/output digital pin
			CPO1	**O**		Comparator1 output pin
			AD1	**I/O**		EBI Address/Data bus bit1
6	3	1	PB.12	**I/O**		General purpose input/output digital pin
			CPO0	**O**		Comparator0 output pin
			CLKO	**O**		Frequency Divider output pin
			AD0	**I/O**		EBI Address/Data bus bit0
7	4	2	X32O	**O**		External 32.768 kHz low speed crystal output pin
8	5	3	X32I	**I**		External 32.768 kHz low speed crystal input pin
9	6	4	PA.11	**I/O**		General purpose input/output digital pin
			I2C1SCL	**I/O**		I2C1SCL: I2C1 clock pin
			nRD	**O**		EBI read enable output pin
10	7	5	PA.10	**I/O**		General purpose input/output digital pin
			I2C1SDA	**I/O**		I2C1SDA: I2C1 data input/output pin
			nWR	**O**		EBI write enable output pin
11	8	6	PA.9	**I/O**		General purpose input/output digital pin
			I2C0SCL	**I/O**		I2C0SCL: I2C0 clock pin
12	9	7	PA.8	**I/O**		General purpose input/output digital pin
			I2C0SDA	**I/O**		I2C0SDA: I2C0 data input/output pin
13			PD.8	**I/O**		General purpose input/output digital pin

Pin No.			Pin Name	Pin Type		Description
LQFP 100	LQFP 64	LQFP 48				
			SPISS30	I/O		SPISS30: SPI3 slave select pin
14			PD.9	I/O		General purpose input/output digital pin
			SPICLK3	I/O		SPICLK3: SPI3 serial clock pin
15			PD.10	I/O		General purpose input/output digital pin
			MISO30	I/O		MISO30: SPI3 MISO (Master In, Slave Out) pin
16			PD.11	I/O		General purpose input/output digital pin
			MOSI30	I/O		MOSI30: SPI3 MOSI (Master Out, Slave In) pin
17			PD.12	I/O		General purpose input/output digital pin
			MISO31	I/O		MISO31: SPI3 2nd MISO (Master In, Slave Out) pin
18			PD.13	I/O		General purpose input/output digital pin
			MOSI31	I/O		MOSI31: SPI3 2nd MOSI (Master Out, Slave In) pin
19	10	8	PB.4	I/O		General purpose input/output digital pin
			RXD1	I		RXD1: Data receiver input pin for UART1
20	11	9	PB.5	I/O		General purpose input/output digital pin
			TXD1	O		TXD1: Data transmitter output pin for UART1
21	12		PB.6	I/O		General purpose input/output digital pin
			RTS1	O		RTS1: Request to Send output pin for UART1
			ALE	O		EBI address latch enable output pin
22	13		PB.7	I/O		General purpose input/output digital pin
			CTS1	I		CTS1: Clear to Send input pin for UART1
			nCS	O		EBI chip select enable output pin
23	14	10	LDO	P		LDO output pin
24	15	11	VDD	P		Power supply for I/O ports and LDO source for internal PLL and digital function
25	16	12	VSS	P		Ground
26			PE.12	I/O		General purpose input/output digital pin
27			PE.11	I/O		General purpose input/output digital pin
28			PE.10	I/O		General purpose input/output digital pin
29			PE.9	I/O		General purpose input/output digital pin
30			PE.8	I/O		General purpose input/output digital pin

Pin No.			Pin Name	Pin Type		Description
LQFP 100	LQFP 64	LQFP 48				
31			PE.7	I/O		General purpose input/output digital pin
32	17	13	PB.0	I/O		General purpose input/output digital pin
			RXD0	I		RXD0: Data receiver input pin for UART0
33	18	14	PB.1	I/O		General purpose input/output digital pin
			TXD0	O		TXD0: Data transmitter output pin for UART0
34	19	15	PB.2	I/O		General purpose input/output digital pin
			RTS0	O		RTS0: Request to Send output pin for UART0
			nWRL	O		EBI low byte write enable output pin
			T2EX	I		Timer2 external capture input pin
35	20	16	PB.3	I/O		General purpose input/output digital pin
			CTS0	I		CTS0: Clear to Send input pin for UART0
			nWRH	O		EBI high byte write enable output pin
			T3EX	I		Timer3 external capture input pin
36	21	17	PD.6	I/O		General purpose input/output digital pin
			CANRX0	I		CAN Bus0 RX Input
37	22	18	PD.7	I/O		General purpose input/output digital pin
			CANTX0	O		CAN Bus0 TX Output
38	23	19	PD.14	I/O		General purpose input/output digital pin
			RXD2	I		RXD2: Data receiver input pin for UART2
39	24	20	PD.15	I/O		General purpose input/output digital pin
			TXD2	O		TXD2: Data transmitter output pin for UART2
40			PC.5	I/O		General purpose input/output digital pin
			MOSI01	I/O		MOSI01: SPI0 2nd MOSI (Master Out, Slave In) pin
41			PC.4	I/O		General purpose input/output digital pin
			MISO01	I/O		MISO01: SPI0 2nd MISO (Master In, Slave Out) pin
42	25	21	PC.3	I/O		General purpose input/output digital pin
			MOSI00	I/O		MOSI00: SPI0 MOSI (Master Out, Slave In) pin
			I2SDO	O		I2SDO: I2S data output
43	26	22	PC.2	I/O		General purpose input/output digital pin

Pin No.			Pin Name	Pin Type		Description
LQFP 100	LQFP 64	LQFP 48				
			MISO00	I/O		MISO00: SPI0 MISO (Master In, Slave Out) pin
			I2SDI	I		I2SDI: I^2S data input
44	27	23	PC.1	I/O		General purpose input/output digital pin
			SPICLK0	I/O		SPICLK0: SPI0 serial clock pin
			I2SBCLK	I/O		I2SBCLK: I^2S bit clock pin
45	28	24	PC.0	I/O		General purpose input/output digital pin
			SPISS00	I/O		SPISS00: SPI0 slave select pin
			I2SLRCLK	I/O		I2SLRCLK: I^2S left right channel clock
46			PE.6	I/O		General purpose input/output digital pin
47	29		PE.5	I/O		General purpose input/output digital pin
			PWM5	I/O		PWM5: PWM output/Capture input
			T1EX	I		Timer1 external capture input
48	30		PB.11	I/O		General purpose input/output digital pin
			TM3	I/O		TM3: Timer3 event counter input / toggle output
			PWM4	I/O		PWM4: PWM output/Capture input
49	31		PB.10	I/O		General purpose input/output digital pin
			TM2	I/O		TM2: Timer2 event counter input / toggle output
			SPISS01	I/O		SPISS01: SPI0 2nd slave select pin
50	32		PB.9	I/O		General purpose input/output digital pin
			TM1	I/O		TM1: Timer1 event counter input / toggle output
			SPISS11	I/O		SPISS11: SPI1 2nd slave select pin
51			PE.4	I/O		General purpose input/output digital pin
52			PE.3	I/O		General purpose input/output digital pin
53			PE.2	I/O		General purpose input/output digital pin
54			PE.1	I/O		General purpose input/output digital pin
			PWM7	I/O		PWM7: PWM output/Capture input
55			PE.0	I/O		General purpose input/output digital pin
			PWM6	I/O		PWM6: PWM output/Capture input
56			PC.13	I/O		General purpose input/output digital pin

Pin No.			Pin Name	Pin Type		Description
LQFP 100	LQFP 64	LQFP 48				
			MOSI11	I/O		MOSI11: SPI1 2nd MOSI (Master Out, Slave In) pin
57			PC.12	I/O		General purpose input/output digital pin
			MISO11	I/O		MISO11: SPI1 2nd MISO (Master In, Slave Out) pin
58	33		PC.11	I/O		General purpose input/output digital pin
			MOSI10	I/O		MOSI10: SPI1 MOSI (Master Out, Slave In) pin
59	34		PC.10	I/O		General purpose input/output digital pin
			MISO10	I/O		MISO10: SPI1 MISO (Master In, Slave Out) pin
60	35		PC.9	I/O		General purpose input/output digital pin
			SPICLK1	I/O		SPICLK1: SPI1 serial clock pin
61	36		PC.8	I/O		General purpose input/output digital pin
			SPISS10	I/O		SPISS10: SPI1 slave select pin
			MCLK	O		EBI clock output
62	37	25	PA.15	I/O		General purpose input/output digital pin
			PWM3	I/O		PWM3: PWM output/Capture input
			I2SMCLK	O		I2SMCLK: I2S master clock output pin
63	38	26	PA.14	I/O		General purpose input/output digital pin
			PWM2	I/O		PWM2: PWM output/Capture input
			AD15	I/O		EBI Address/Data bus bit15
64	39	27	PA.13	I/O		General purpose input/output digital pin
			PWM1	I/O		PWM1: PWM output/Capture input
			AD14	I/O		EBI Address/Data bus bit14
65	40	28	PA.12	I/O		General purpose input/output digital pin
			PWM0	I/O		PWM0: PWM output/Capture input
			AD13	I/O		EBI Address/Data bus bit13
66	41	29	ICE_DAT	I/O		Serial Wired Debugger Data pin
67	42	30	ICE_CK	I		Serial Wired Debugger Clock pin
68			VDD	P		Power supply for I/O ports and LDO source for internal PLL and digital circuit
69			VSS	P		Ground
70	43	31	AVSS	AP		Ground Pin for analog circuit

Pin No.			Pin Name	Pin Type		Description
LQFP 100	LQFP 64	LQFP 48				
71	44	32	PA.0	I/O		General purpose input/output digital pin
			ADC0	AI		ADC0: ADC analog input
72	45	33	PA.1	I/O		General purpose input/output digital pin
			ADC1	AI		ADC1: ADC analog input
			AD12	I/O		EBI Address/Data bus bit12
73	46	34	PA.2	I/O		General purpose input/output digital pin
			ADC2	AI		ADC2: ADC analog input
			AD11	I/O		EBI Address/Data bus bit11
74	47	35	PA.3	I/O		General purpose input/output digital pin
			ADC3	AI		ADC3: ADC analog input
			AD10	I/O		EBI Address/Data bus bit10
75	48	36	PA.4	I/O		General purpose input/output digital pin
			ADC4	AI		ADC4: ADC analog input
			AD9	I/O		EBI Address/Data bus bit9
76	49	37	PA.5	I/O		General purpose input/output digital pin
			ADC5	AI		ADC5: ADC analog input
			AD8	I/O		EBI Address/Data bus bit8
77	50	38	PA.6	I/O		General purpose input/output digital pin
			ADC6	AI		ADC6: ADC analog input
			AD7	I/O		EBI Address/Data bus bit7
78	51	39	PA.7	I/O		General purpose input/output digital pin
			ADC7	AI		ADC7: ADC analog input
			SPISS21	I/O		SPISS21: SPI2 2nd slave select pin
			AD6	I/O		EBI Address/Data bus bit6
79			VREF	AP		Voltage reference input for ADC
80	52	40	AVDD	AP		Power supply for internal analog circuit
81			PD.0	I/O		General purpose input/output digital pin
			SPISS20	I/O		SPISS20: SPI2 slave select pin
82			PD.1	I/O		General purpose input/output digital pin
			SPICLK2	I/O		SPICLK2: SPI2 serial clock pin

Pin No.			Pin Name	Pin Type		Description
LQFP 100	LQFP 64	LQFP 48				
83			PD.2	I/O		General purpose input/output digital pin
			MISO20	I/O		MISO20: SPI2 MISO (Master In, Slave Out) pin
84			PD.3	I/O		General purpose input/output digital pin
			MOSI20	I/O		MOSI20: SPI2 MOSI (Master Out, Slave In) pin
85			PD.4	I/O		General purpose input/output digital pin
			MISO21	I/O		MISO21: SPI2 2nd MISO (Master In, Slave Out) pin
86			PD.5	I/O		General purpose input/output digital pin
			MOSI21	I/O		MOSI21: SPI2 2nd MOSI (Master Out, Slave In) pin
87	53	41	PC.7	I/O		General purpose input/output digital pin
			CPN0	AI		CPN0: Comparator0 Negative input pin
			AD5	I/O		EBI Address/Data bus bit5
88	54	42	PC.6	I/O		General purpose input/output digital pin
			CPP0	AI		CPP0: Comparator0 Positive input pin
			AD4	I/O		EBI Address/Data bus bit4
89	55		PC.15	I/O		General purpose input/output digital pin
			CPN1	AI		CPN1: Comparator1 Negative input pin
			AD3	I/O		EBI Address/Data bus bit3
90	56		PC.14	I/O		General purpose input/output digital pin
			CPP1	AI		CPP1: Comparator1 Positive input pin
			AD2	I/O		EBI Address/Data bus bit2
91	57	43	PB.15	I/O		General purpose input/output digital pin
			/INT1	I		/INT1: External interrupt0 input pin
			T0EX	I		Timer0 external capture input
92	58	44	XT1_OUT	O		External 4~24 MHz high speed crystal output pin
93	59	45	XT1_IN	I		External 4~24 MHz high speed crystal input pin
94	60	46	/RESET	I		External reset input: Low active, set this pin low reset chip to initial state. With internal pull-up.
95	61		VSS	P		Ground
96	62		VDD	P		Power supply for I/O ports and LDO source for internal PLL and digital circuit
97			PS2DAT	I/O		PS/2 Data pin

Pin No.			Pin Name	Pin Type		Description
LQFP 100	LQFP 64	LQFP 48				
98			PS2CLK	**I/O**		PS/2 clock pin
99	63	47	PVSS	**P**		PLL Ground
100	64	48	PB.8	**I/O**		General purpose input/output digital pin
			STADC	**I**		STADC: ADC external trigger input.
			TM0	**I/O**		TM0: Timer0 event counter input / toggle output

Note: Pin Type I=Digital Input, O=Digital Output; AI=Analog Input; P=Power Pin; AP=Analog Power

4 BLOCK DIAGRAM

4.1 NuMicro™NUC130 Block Diagram

4.1.1 NuMicro™ NUC130 Block Diagram

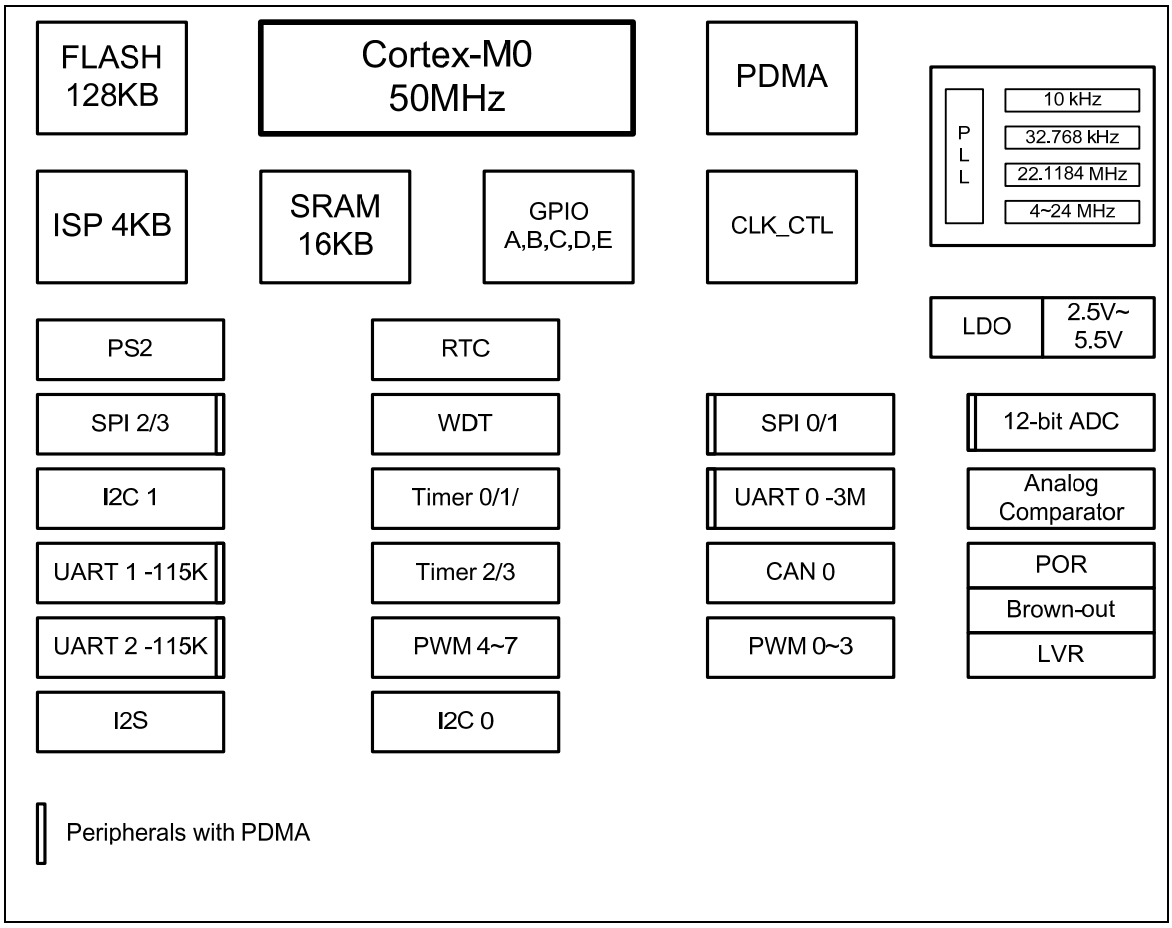


Figure 4-1 NuMicro™ NUC130 Block Diagram

5 ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN.	MAX	UNIT
DC Power Supply	VDD–VSS	-0.3	+7.0	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into VDD		-	120	mA
Maximum Current out of VSS			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

5.2 DC Electrical Characteristics

5.2.1 NuMicro™ NUC130/NUC140 DC Electrical Characteristics

(VDD-VSS=3.3 V, TA = 25°C, FOSC = 50 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V_{DD}	2.5		5.5	V	V_{DD} =2.5 V ~ 5.5 V up to 50 MHz
Power Ground	V_{SS} AV_{SS}	-0.3			V	
LDO Output Voltage	V_{LDO}	-10%	2.5	+10%	V	V_{DD} > 2.7 V
Analog Operating Voltage	AV_{DD}	0		V_{DD}	V	
Analog Reference Voltage	Vref	0		AV_{DD}	V	
Operating Current Normal Run Mode @ 50 MHz	I_{DD1}		51		mA	V_{DD} = 5.5 V@50 MHz, enable all IP and PLL, XTAL=12 MHz
	I_{DD2}		25		mA	V_{DD} = 5.5 V@50 MHz, disable all IP and enable PLL, XTAL=12 MHz
	I_{DD3}		48		mA	V_{DD} = 3 V@50 MHz, enable all IP and PLL, XTAL=12 MHz
	I_{DD4}		23		mA	V_{DD} = 3 V@50 MHz, disable all IP and enable PLL, XTAL=12 MHz
Operating Current Normal Run Mode @ 12 MHz	I_{DD5}		19		mA	V_{DD} = 5.5 V@12 MHz, enable all IP and disable PLL, XTAL=12 MHz
	I_{DD6}		7		mA	V_{DD} = 5.5 V@12 MHz, disable all IP and disable PLL, XTAL=12 MHz
	I_{DD7}		17		mA	V_{DD} = 3 V@12 MHz, enable all IP and disable PLL, XTAL=12 MHz

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
	I_{DD8}		6		mA	V_{DD} = 3 V@12 MHz, disable all IP and disable PLL, XTAL=12 MHz
Operating Current Normal Run Mode @ 4 MHz	I_{DD9}		11		mA	V_{DD} = 5 V@4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I_{DD10}		3		mA	V_{DD} = 5 V@4 MHz, disable all IP and disable PLL, XTAL=4 MHz
	I_{DD11}		10		mA	V_{DD} = 3 V@4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I_{DD12}		2.5		mA	V_{DD} = 3 V@4 MHz, disable all IP and disable PLL, XTAL=4 MHz
Operating Current Idle Mode @ 50 MHz	I_{IDLE1}		35		mA	V_{DD}= 5.5 V@50 MHz, enable all IP and PLL, XTAL=12 MHz
	I_{IDLE2}		15		mA	V_{DD}=5.5 V@50 MHz, disable all IP and enable PLL, XTAL=12 MHz
	I_{IDLE3}		33		mA	V_{DD} = 3 V@50 MHz, enable all IP and PLL, XTAL=12 MHz
	I_{IDLE4}		13		mA	V_{DD} = 3 V@50 MHz, disable all IP and enable PLL, XTAL=12 MHz
Operating Current Idle Mode @ 12 MHz	I_{IDLE5}		10		mA	V_{DD} = 5.5 V@12 MHz, enable all IP and disable PLL, XTAL=12 MHz
	I_{IDLE6}		4.5		mA	V_{DD} = 5.5 V@12 MHz, disable all IP and disable PLL, XTAL=12 MHz
	I_{IDLE7}		9		mA	V_{DD} = 3 V@12 MHz, enable all IP and disable PLL, XTAL=12 MHz

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
	I_{IDLE8}		3.5		mA	V_{DD} = 3 V@12 MHz, disable all IP and disable PLL, XTAL=12 MHz
Operating Current Idle Mode @ 4 MHz	I_{IDLE9}		4		mA	V_{DD} = 5 V@4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I_{IDLE10}		2.5		mA	V_{DD} = 5 V@4 MHz, disable all IP and disable PLL, XTAL=4 MHz
	I_{IDLE11}		3.5		mA	V_{DD} = 3 V@4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I_{IDLE12}		1.5		mA	V_{DD} = 3 V@4 MHz, disable all IP and disable PLL, XTAL=4 MHz
Standby Current Power down Mode	I_{PWD1}		12		µA	V_{DD} = 5.5 V, RTC OFF, No load @ Disable BOV function
	I_{PWD2}		9		µA	V_{DD} = 3.3 V, RTC OFF, No load @ Disable BOV function
	I_{PWD3}				µA	V_{DD} = 5.5 V, RTC run , No load @ Disable BOV function
	I_{PWD4}				µA	V_{DD} = 3.3 V, RTC run , No load @ Disable BOV function
Input Current PA, PB, PC, PD, PE (Quasi-bidirectional mode)	I_{IN1}		-50	-60	µA	V_{DD} = 5.5 V, V_{IN} = 0 V or V_{IN}=V_{DD}
Input Current at /RESET[1]	I_{IN2}	-55	-45	-30	µA	V_{DD} = 3.3 V, V_{IN} = 0.45 V
Input Leakage Current PA, PB, PC, PD, PE	I_{LK}	-2	-	+2	µA	V_{DD} = 5.5 V, 0<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current PA~PE (Quasi-bidirectional mode)	I_{TL} [3]	-650	-	-200	µA	V_{DD} = 5.5 V, V_{IN}<2.0 V
Input Low Voltage PA, PB, PC, PD, PE (TTL input)	V_{IL1}	-0.3	-	0.8	V	V_{DD} = 4.5 V
		-0.3	-	0.6		V_{DD} = 2.5 V
Input High Voltage PA, PB, PC, PD, PE (TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5 V
		1.5	-	V_{DD} +0.2		V_{DD} =3.0 V
Input Low Voltage PA, PB, PC, PD, PE (Schmitt input)	V_{IL2}	-0.5	-	0.4 V_{DD}	V	

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Input High Voltage PA, PB, PC, PD, PE (Schmitt input)	V_{IH2}	0.6 V_{DD}	-	V_{DD}+0.5	V	
Hysteresis voltage of PA~PE (Schmitt input)	V_{HY}		0.2 V_{DD}		V	
Input Low Voltage XT1[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5 V
		0	-	0.4		V_{DD} = 3.0 V
Input High Voltage XT1[*2]	V_{IH3}	3.5	-	V_{DD} +0.2	V	V_{DD} = 5.5 V
		2.4	-	V_{DD} +0.2		V_{DD} = 3.0 V
Input Low Voltage X32I[*2]	V_{IL4}	0	-	0.4	v	
Input High Voltage X32I[*2]	V_{IH4}	1.7		2.5	V	
Negative going threshold (Schmitt input), /RESET	V_{ILS}	-0.5	-	0.3 V_{DD}	V	
Positive going threshold (Schmitt input), /RESET	V_{IHS}	0.7 V_{DD}	-	V_{DD}+0.5	V	
Source Current PA, PB, PC, PD, PE (Quasi-bidirectional Mode)	I_{SR11}	-300	-370	-450	μA	V_{DD} = 4.5 V, V_S = 2.4 V
	I_{SR12}	-50	-70	-90	μA	V_{DD} = 2.7 V, V_S = 2.2 V
	I_{SR12}	-40	-60	-80	μA	V_{DD} = 2.5 V, V_S = 2.0 V
Source Current PA, PB, PC, PD, PE (Push-pull Mode)	I_{SR21}	-20	-24	-28	mA	V_{DD} = 4.5 V, V_S = 2.4 V
	I_{SR22}	-4	-6	-8	mA	V_{DD} = 2.7 V, V_S = 2.2 V
	I_{SR22}	-3	-5	-7	mA	V_{DD} = 2.5 V, V_S = 2.0 V
Sink Current PA, PB, PC, PD, PE (Quasi-bidirectional and Push-pull Mode)	I_{SK1}	10	16	20	mA	V_{DD} = 4.5 V, V_S = 0.45 V
	I_{SK1}	7	10	13	mA	V_{DD} = 2.7 V, V_S = 0.45 V
	I_{SK1}	6	9	12	mA	V_{DD} = 2.5 V, V_S = 0.45 V
Brown-Out voltage with BOV_VL [1:0] =00b	$V_{BO2.2}$	2.1	2.2	2.3	V	
Brown-Out voltage with BOV_VL [1:0] =01b	$V_{BO2.7}$	2.6	2.7	2.8	V	
Brown-Out voltage with BOV_VL [1:0] =10b	$V_{BO3.8}$	3.6	3.8	4.0	V	
Brown-Out voltage with BOV_VL [1:0] =11b	$V_{BO4.5}$	4.3	4.5	4.7	V	
Hysteresis range of BOD voltage	V_{BH}	30	-	150	mV	V_{DD} = 2.5 V~5.5 V

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Bandgap voltage	V_{BG}	1.20	1.26	1.32	V	V_{DD} = 2.5 V~5.5 V

Note:

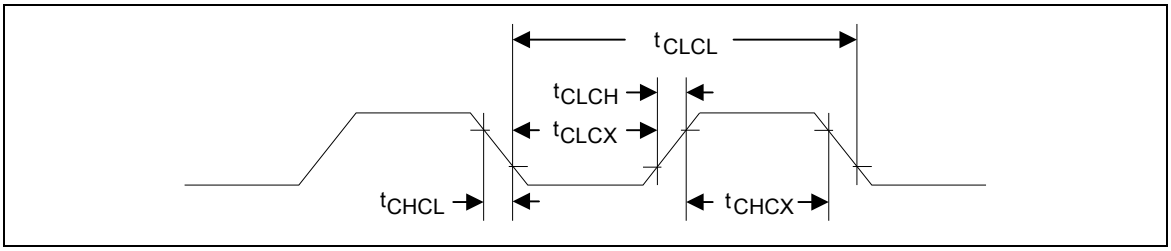
1. /RESET pin is a Schmitt trigger input.

2. Crystal Input is a CMOS input.

3. Pins of PA, PB, PC, PD and PE can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5 V, 5he transition current reaches its maximum value when V_{IN} approximates to 2 V.

5.3 AC Electrical Characteristics

5.3.1 External 4~24 MHz High Speed Oscillator



Note: Duty cycle is 50%.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CHCX}	Clock High Time		20	-	-	nS
t_{CLCX}	Clock Low Time		20	-	-	nS
t_{CLCH}	Clock Rise Time		-	-	10	nS
t_{CHCL}	Clock Fall Time		-	-	10	nS

5.3.2 External 4~24 MHz High Speed Crystal

PARAMETER	CONDITION	MIN.	TYP..	MAX.	UNIT
Input clock frequency	External crystal	4	12	24	MHz
Temperature	-	-40	-	85	℃
VDD	-	2.5	5	5.5	V

5.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4 MHz ~ 24 MHz	without	without	without

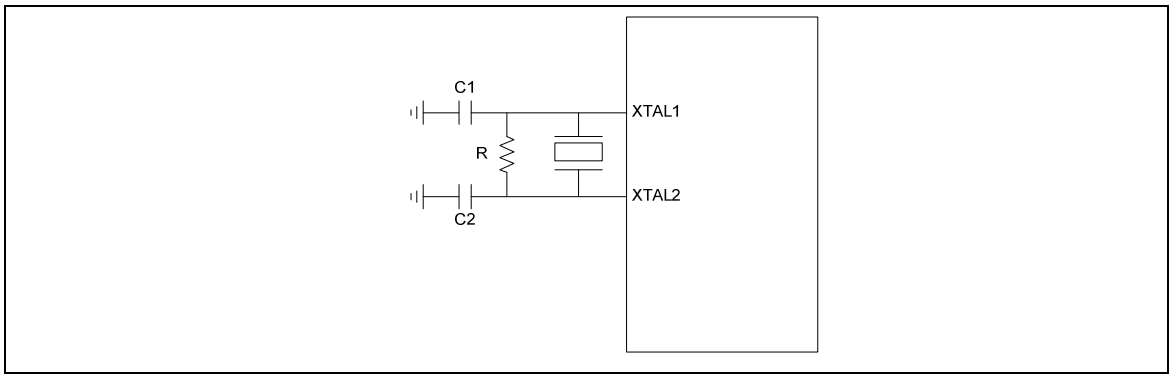


Figure 5-1 Typical Crystal Application Circuit

5.3.3 External 32.768 kHz Low Speed Crystal

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	-	32.768	-	kHz
Temperature	-	-40	-	85	℃
VDD	-	2.5	-	5.5	V

5.3.4 Internal 22.1184 MHz High Speed Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage[1]	-	2.5	-	5.5	V
Center Frequency	-	-	22.1184	-	MHz
Calibrated Internal Oscillator Frequency	+25 C; V_{DD} =5 V	-1	-	+1	%
	-40 C~+85 C; VDD=2.5 V~5.5 V	-3	-	+3	%
Operation Current	V_{DD} =5 V	-	500	-	uA

5.3.5 Internal 10 kHz Low Speed Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage[1]	-	2.5	-	5.5	V
Center Frequency	-	-	10	-	kHz
Calibrated Internal Oscillator Frequency	+25 C; V_{DD} =5 V	-30	-	+30	%
	-40 C~+85 C; V_{DD}=2.5 V~5.5 V	-50	-	+50	%

Note: Internal operation voltage comes from LDO.

5.4 Analog Characteristics

5.4.1 Specification of 12-bit SARADC

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
-	Resolution	-	-	12	Bit
DNL	Differential nonlinearity error	-	±3	-	LSB
INL	Integral nonlinearity error	-	±4	-	LSB
EO	Offset error	-	±1	10	LSB
EG	Gain error (Transfer gain)	-	1	1.005	-
-	Monotonic	Guaranteed			
FADC	ADC clock frequency	-	-	16	MHz
TCAL	Calibration time	-	127	-	Clock
TS	Sample time	-	7	-	Clock
TADC	Conversion time	-	13	-	Clock
FS	Sample rate	-	-	600	K SPS
VLDO	Supply voltage	-	2.5	-	V
VADD		3	-	5.5	V
IDD	Supply current (Avg.)	-	0.5	-	mA
IDDA		-	1.5	-	mA
VREF	Reference voltage	-	VDDA	-	V
IREFP	Reference current (Avg.)	-	1	-	mA
VIN	Reference voltage	0	-	VREF	V
CIN	Capacitance	-	5	-	pF

5.4.2 Specification of LDO and Power management

PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
Input Voltage	2.7	5	5.5	V	V_{DD} input voltage
Output Voltage	-10%	2.5	+10%	V	V_{DD} > 2.7 V
Temperature	-40	25	85	℃	
Quiescent Current (PD=0)	-	100	-	uA	
Quiescent Current (PD=1)	-	5	-	uA	
Iload (PD=0)	-	-	100	mA	
Iload (PD=1)	-	-	100	uA	
Cbp	-	10	-	uF	Resr=1ohm

Note:

1. It is recommended that a 10uF or higher capacitor and a 100nF bypass capacitor are connected between VDD and the closest VSS pin of the device.

2. For ensuring power stability, a 10uF or higher capacitor must be connected between LDO pin and the closest VSS pin of the device.

5.4.3 Specification of Low Voltage Reset

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	1.7	-	5.5	V
Quiescent current	VDD5V=5.5 V	-	-	5	uA
Temperature	-	-40	25	85	℃
Threshold voltage	Temperature=25°	1.7	2.0	2.3	V
	Temperature=-40°	-	2.4	-	V
	Temperature=85°	-	1.6	-	V
Hysteresis	-	0	0	0	V

5.4.4 Specification of Brown-Out Detector

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	2.5	-	5.5	V
Quiescent current	AVDD=5.5 V	-	-	125	μA
Temperature	-	-40	25	85	℃
Brown-out voltage	BOV_VL[1:0]=11	4.3	4.5	4.7	V
	BOV_VL [1:0]=10	3.6	3.8	4.0	V
	BOV_VL [1:0]=01	2.6	2.7	2.8	V
	BOV_VL [1:0]=00	2.1	2.2	2.3	V
Hysteresis	-	30	-	150	mV

5.4.5 Specification of Power-On Reset (5 V)

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Temperature	-	-40	25	85	℃
Reset voltage	V+	-	2	-	V
Quiescent current	Vin>reset voltage	-	1	-	nA

5.4.6 Specification of Temperature Sensor

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltage[1]		2.5	-	5.5	V
Temperature		-40	-	125	℃
Current consumption		6.4	-	10.5	uA
Gain			-1.76		mV/℃
Offset	Temp=0 ℃		720		mV

Note: Internal operation voltage comes from LDO.

5.4.7 Specification of Comparator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Temperature	-	-40	25	85	℃
VDD	-	2.4	3	5.5	V
VDD current	20 uA@VDD=3 V	-	20	40	uA
Input offset voltage	-	-	5	15	mV
Output swing	-	0.1	-	VDD-0.1	V
Input common mode range	-	0.1	-	VDD-1.2	V
DC gain	-	-	70	-	dB
Propagation delay	@VCM=1.2 V and VDIFF=0.1 V	-	200	-	ns
Comparison voltage	20 mV@VCM=1 V 50 mV@VCM=0.1 V 50 mV@VCM=VDD-1.2 @10 mV for non-hysteresis	10	20	-	mV
Hysteresis	One bit control W/O and W. hysteresis @VCM=0.4 V ~ VDD-1.2 V	-	±10	-	mV
Wake-up time	@CINP=1.3 V CINN=1.2 V	-	-	2	us

5.4.8 Specification of USB PHY

5.4.8.1 USB DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input high (driven)		2.0			V
V_{IL}	Input low				0.8	V
V_{DI}	Differential input sensitivity	|PADP-PADM|	0.2			V
V_{CM}	Differential common-mode range	Includes V_{DI} range	0.8		2.5	V
V_{SE}	Single-ended receiver threshold		0.8		2.0	V
	Receiver hysteresis			200		mV
V_{OL}	Output low (driven)		0		0.3	V
V_{OH}	Output high (driven)		2.8		3.6	V
V_{CRS}	Output signal cross voltage		1.3		2.0	V
R_{PU}	Pull-up resistor		1.425		1.575	kΩ
R_{PD}	Pull-down resistor		14.25		15.75	kΩ
V_{TRM}	Termination Voltage for upstream port pull up (RPU)		3.0		3.6	V
Z_{DRV}	Driver output resistance	Steady state drive*		10		Ω
C_{IN}	Transceiver capacitance	Pin to GND			20	pF

*Driver output resistance doesn't include series resistor resistance.

5.4.8.2 USB Full-Speed Driver Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{FR}	Rise Time	C_L=50p	4		20	ns
T_{FF}	Fall Time	C_L=50p	4		20	ns
T_{FRFF}	Rise and fall time matching	$T_{FRFF}=T_{FR}/T_{FF}$	90		111.11	%

5.4.8.3 USB Power Dissipation

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{VDDREG} (Full Speed)	VDDD and VDDREG Supply Current (Steady State)	Standby		50		uA
		Input mode				uA
		Output mode				uA

5.5 SPI Dynamic Characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
SPI master mode (VDD = 4.5V ~ 5.5V, 30pF loading Capacitor)					
t_{DS}	Data setup time	4	2	-	ns
t_{DH}	Data hold time	0	-	-	ns
t_V	Data output valid time	-	7	11	ns
SPI master mode (VDD = 3.0V ~ 3.6V, 30pF loading Capacitor)					
t_{DS}	Data setup time	5	3	-	ns
t_{DH}	Data hold time	0	-	-	ns
t_V	Data output valid time	-	13	18	ns
SPI slave mode (VDD = 4.5V ~ 5.5V, 30pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2*PCLK+4	-	-	ns
t_V	Data output valid time	-	2*PCLK+11	2*PCLK+19	ns
SPI slave mode (VDD = 3.0V ~ 3.6V, 30pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2*PCLK+6	-	-	ns
t_V	Data output valid time	-	2*PCLK+19	2*PCLK+25	ns

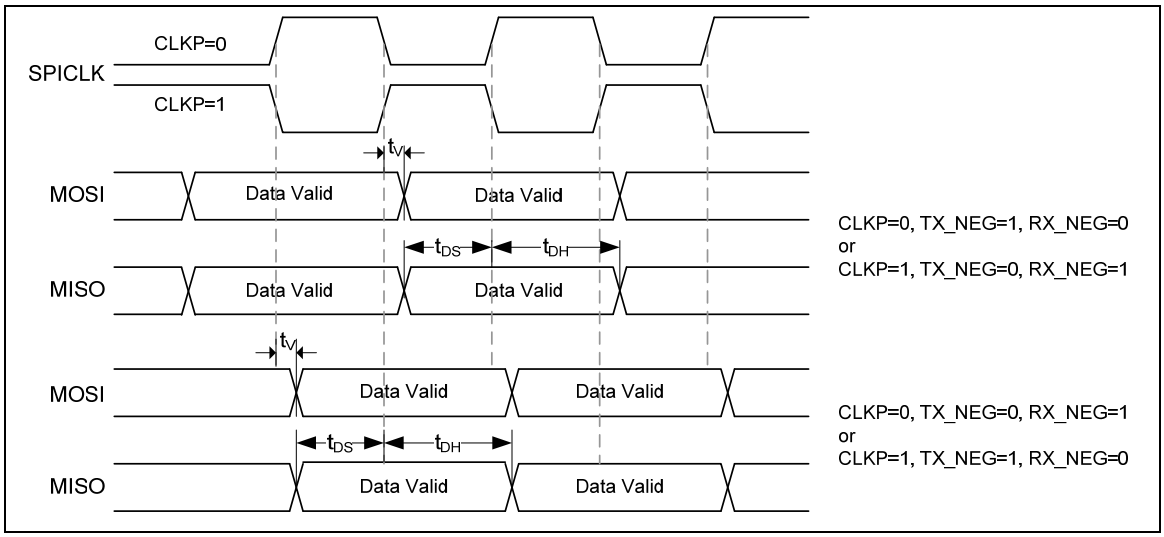


Figure 5-2 SPI Master dynamic characteristics tiMINg

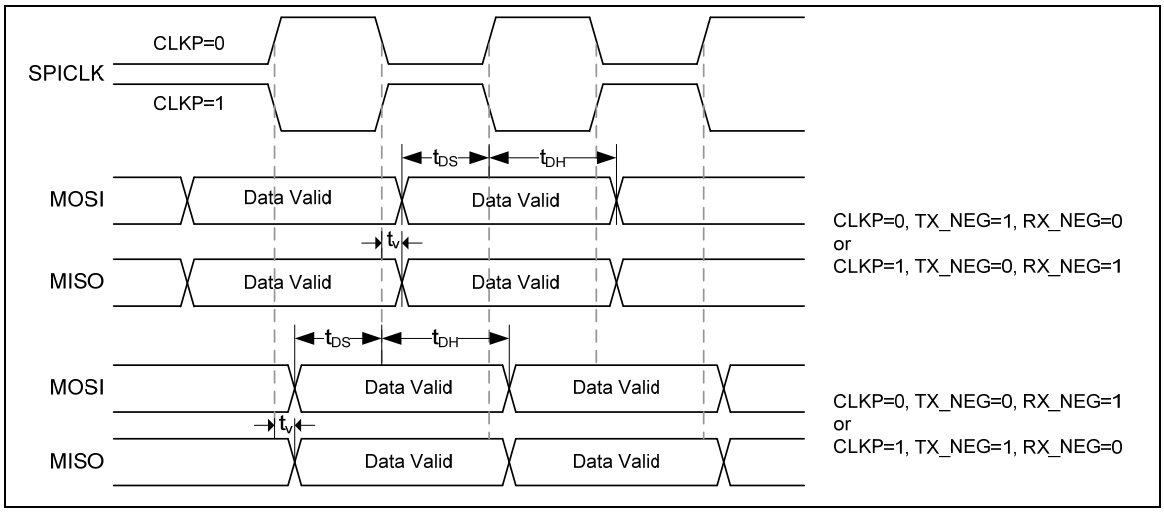
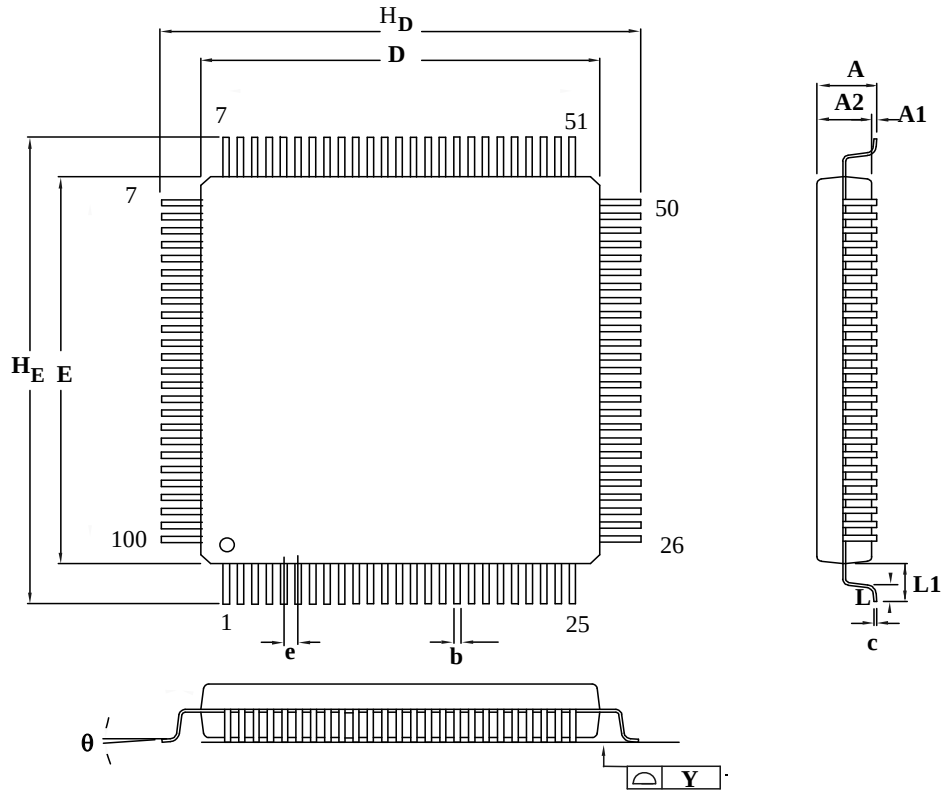


Figure 5-3 SPI Slave dynamic characteristics timing

6 PACKAGE DIMENSIONS

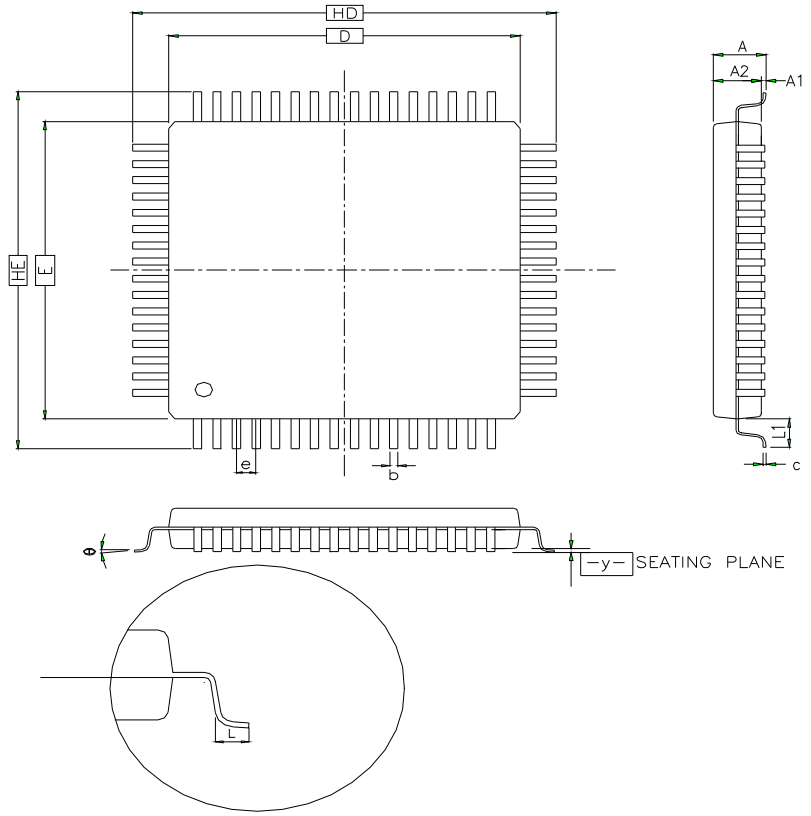
6.1 100L LQFP (14x14x1.4 mm footprint 2.0mm)



Controlling Dimension : Millimeters

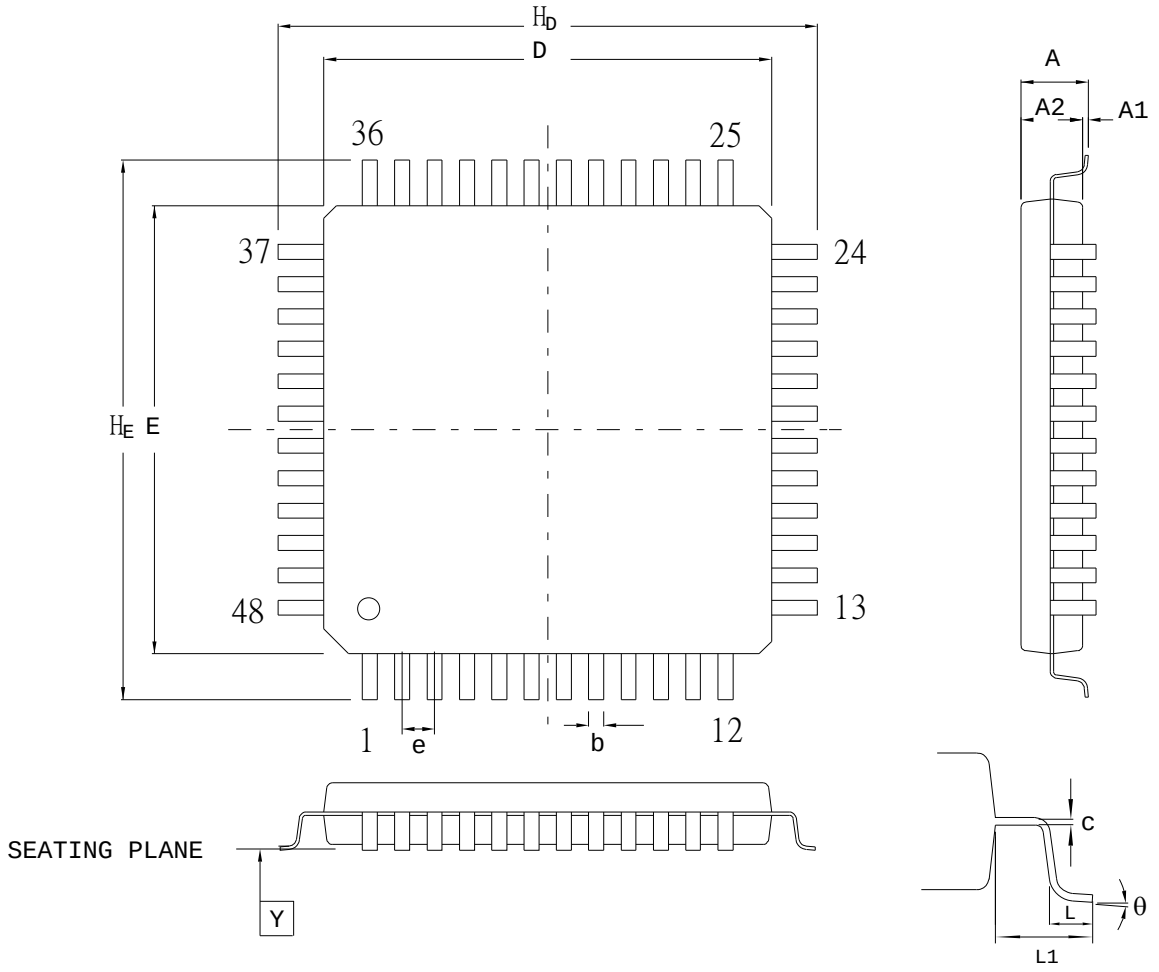
Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A1	0.002	—	—	0.05	—	—
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.556	13.90	14.00	14.10
E	0.547	0.551	0.556	13.90	14.00	14.10
e	—	0.020	—	—	0.50	—
H_D	0.622	0.630	0.638	15.80	16.00	16.20
H_E	0.622	0.630	0.638	15.80	16.00	16.20
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	—	0.039	—	—	1.00	—
y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

6.2 64L LQFP (10x10x1.4mm footprint 2.0 mm)



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A_1	0.002	—	0.006	0.05	—	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.008	0.011	0.17	0.20	0.27
c	0.004	—	0.008	0.09	—	0.20
D	—	0.393	—	—	10.00	—
E	—	0.393	—	—	10.00	—
e	—	0.020	—	—	0.50	—
H_D	—	0.472	—	—	12.00	—
H_E	—	0.472	—	—	12.00	—
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
y	—	0.004	—	—	0.10	—
θ	0°	3.5°	7°	0°	3.5°	7°

6.3 48L LQFP (7x7x1.4mm footprint 2.0mm)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7 °	0°	—	7 °

7 REVISION HISTORY

VERSION	DATE	PAGE/ CHAP.	DESCRIPTION
V1.00	March 1, 2010	-	Preliminary version initial issued
V1.01	April 9, 2010	Ch4	Modify the block diagram
V1.02	May 31, 2010	7.2	Add operation current of DC characteristics
V1.03	Aug. 23, 2010	7.2	Modify operation current of DC characteristics
V2.00	Nov. 11, 2010	-	Update low density and selection table
V3.00	May 6, 2011	All	Revise from NUC130XXXAN or NUC130XXXBN to NUC130XXXCN Revise NUC130 selection guide Revise DC Electrical Characteristics
V3.01	June 22, 2011	5.4.6 3.3.1.1 5.5 5.4.4	modify temperature sensor spec Revise Pin description position for multi-function T2EX, T3EX, nRD, nWR update title of SPI Dynamic Characteristics update BOD spec

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.