

FEATURES

- Replaces 8 Potentiometers
- Operates From Single +5 V Supply
- 1 MHz 2-Quadrant Multiplying Bandwidth
- No Signal Inversion
- Eight Individual Channels
- 3-Wire Serial Input
- 500 kHz Update Data Loading Rate
- +3 Volt Output Swing
- Midscale Preset
- Low 95 mW Power Dissipation

APPLICATIONS

- Trimmer Replacement
- Dynamic Level Adjustment
- Special Waveform Generation and Modulation
- Programmable Gain Amplifiers

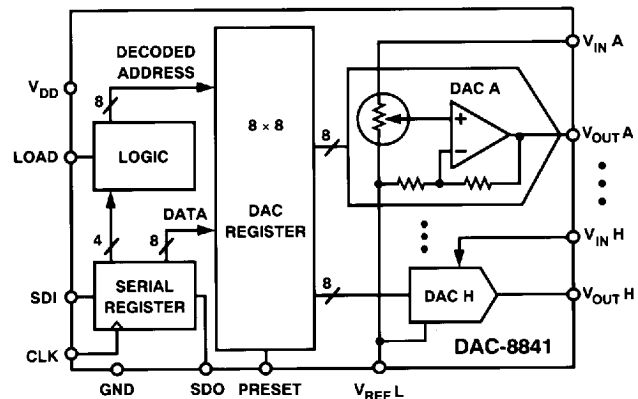
GENERAL DESCRIPTION

The DAC-8841 provides eight general purpose digitally controlled voltage adjustment devices. The TrimDAC™ capability replaces the mechanical trimmer function in new designs. It is ideal for ac or dc gain control of up to 1 MHz bandwidth signals.

Internally the DAC-8841 contains eight voltage output CMOS digital-to-analog converters, each with separate reference inputs. Each DAC has its own DAC register which holds its output state. These DAC registers are updated from an internal serial-to-parallel shift register which is loaded from a standard 3-wire serial input digital interface. Twelve data bits make up the data word clocked into the serial input register. This data word is decoded where the first 4 bits determine the address of the DAC register to be loaded with the last 8 bits of data. A serial data output pin at the opposite end of the serial register allows simple daisy-chaining in multiple DAC applications without additional external decoding logic.

TrimDAC is a trademark of Analog Devices, Inc.

FUNCTIONAL BLOCK DIAGRAM



The DAC-8841 consumes only 95 mW from a +5 V power supply. For dual polarity applications see the DAC-8840 which provides full 4-quadrant-multiplying ± 3 V signal capability while operating from ± 5 V power supplies.

The DAC-8841 is available in 24-pin plastic DIP, cerdip, and SOIC-24 packages. For MIL-STD/883 applications, contact ADI sales for the DAC-8841BW/883 data sheet which specifies operation over -55°C to $+125^{\circ}\text{C}$.

REV. A

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DAC-8841 — SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

$V_{DD} = +5\text{ V}$, All $V_{INX} = +1.5\text{ V}$, $V_{REFL} = 0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ apply for DAC-8841F, unless otherwise noted.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---------------------------------|---------------------|--|---------|-----------|-----------|--------------------------------|
| STATIC ACCURACY | | | | | | |
| Resolution | N | All Specifications Apply for DACs A, B, C, D, E, F, G, H | 8 | | | Bits |
| Integral Nonlinearity | INL | Note 1 | | $\pm 1/2$ | ± 1.5 | LSB |
| Differential Nonlinearity | DNL | All Devices Monotonic, Note 1 | | | ± 1 | LSB |
| Half-Scale Output Voltage | V_{HS} | $\overline{PR} = 0\text{ V}$, Sets D = 80_H | 1.475 | 1.500 | 1.525 | V |
| Zero-Scale Output Voltage | V_{ZS} | Digital Code = 00_H | | 20 | 100 | mV |
| Output Voltage Drift | TCV_{HS} | $\overline{PR} = 0\text{ V}$, Sets D = 80_H | | 10 | | $\mu\text{V}/^\circ\text{C}$ |
| SIGNAL INPUTS | | | | | | |
| Input Voltage Range | IVR | Applies to All Inputs V_{INX} or V_{REFL} | 0 | | 1.5 | V |
| Input Resistance | R_{IN} | D = 55_H ; Code Dependent | 4 | 10 | | k Ω |
| Input Capacitance | C_{IN} | Code Dependent | | 19 | 30 | pF |
| REF Low Resistance | R_{REFL} | D = AB_H ; Code Dependent | 0.3 | 0.75 | | k Ω |
| REF Low Capacitance | C_{REFL} | Code Dependent | | 190 | 250 | pF |
| DAC OUTPUTS | | | | | | |
| Voltage Range | OVR | Applies to All Outputs V_{OUTX} $R_L = 10\text{ k}\Omega$ | 0 | | 3 | V |
| Output Current | I_{OUT} | $\Delta V_{OUT} < 25\text{ mV}$, $V_{INX} = 1.375\text{ V}$, $\overline{PR} = 0\text{ V}$ | ± 5 | 7 | | mA |
| Capacitive Load | C_L | No Oscillation | | | 200 | pF |
| DYNAMIC PERFORMANCE | | | | | | |
| Multiplying Gain Bandwidth | GBW | Applies to All DACs $V_{INX} = 100\text{ mV p-p} + 1.0\text{ V dc}$ Measured 10% to 90% | 1 | 2.5 | | MHz |
| Slew Rate | +SR -SR | $\Delta V_{OUTX} = +3\text{ V}$ $\Delta V_{OUTX} = -3\text{ V}$ | 1.3 | 4.0 | | V/ μs |
| Total Harmonic Distortion | THD | $V_{INX} = 1\text{ V p-p} + 1.0\text{ V dc}$, D = FF_H , $f = 1\text{ kHz}$, $f_{LP} = 80\text{ kHz}$ | | | 0.01 | % |
| Spot Noise Voltage | e_N | $f = 1\text{ kHz}$ | | 0.17 | | $\mu\text{V}/\sqrt{\text{Hz}}$ |
| Output Settling Time | t_S | $\pm 1\text{ LSB Error Band}$, 8_{10} to 255_{10} | | 3.5 | 6 | μs |
| Channel to Channel Crosstalk | C_T | Measured Between Adjacent Channels, $f = 100\text{ kHz}$ | 60 | 70 | | dB |
| Digital Feedthrough | Q | $V_{REFL} = +1.5\text{ V}$, D = 0 to FF_H | | 6 | | nVs |
| POWER SUPPLIES | | | | | | |
| Positive Supply Current | I_{DD} | $\overline{PR} = 0\text{ V}$ | | 19 | 26 | mA |
| Power Dissipation | P_{DISS} | | | 95 | 130 | mW |
| DC Power Supply Rejection Ratio | PSRR | $\overline{PR} = 0\text{ V}$ | | | 0.01 | %/% |
| Power Supply Range | PSR | V_{DD} | 4.75 | 5.00 | 5.25 | V |
| DIGITAL INPUTS | | | | | | |
| Logic High | V_{IH} | | 2.4 | | | V |
| Logic Low | V_{IL} | | | | 0.8 | V |
| Input Current | I_L | | | | ± 10 | μA |
| Input Capacitance | C_{IL} | | | | 8 | pF |
| Input Coding | | | | Binary | | |
| DIGITAL OUTPUT | | | | | | |
| Logic High | V_{OH} | $I_{OH} = -0.4\text{ mA}$ | 3.5 | | | V |
| Logic Low | V_{OL} | $I_{OL} = 1.6\text{ mA}$ | | | 0.4 | V |
| TIMING SPECIFICATIONS | | | | | | |
| Input Clock Pulse Width | t_{CH} , t_{CL} | | 80 | | | ns |
| Data Setup Time | t_{DS} | | 40 | | | ns |
| Data Hold Time | t_{DH} | | 20 | | | ns |
| CLK to SDO Propagation Delay | t_{PD} | | | | 120 | ns |
| DAC Register Load Pulse Width | t_{LD} | | 70 | | | ns |
| Preset Pulse Width | t_{PR} | | 50 | | | ns |
| Clock Edge to Load Time | t_{CKLD} | | 30 | | | ns |
| Load Edge to Next Clock Edge | t_{LDCK} | | 60 | | | ns |

NOTE
¹INL and DNL tests do not include operation at codes 0 thru 7 due to zero-scale output voltage. For bias voltages above 100 mV on V_{REFL} , INL and DNL are maintained over all codes.

Specifications subject to change without notice.

WAFER TEST LIMITS: $V_{DD} = +5\text{ V}$, All $V_{INX} = +1.5\text{ V}$, $V_{REFL} = 0\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

| Parameter | Symbol | Conditions | DAC-8841GBC Limits | Units |
|---------------------------------|------------|--|--------------------|----------------------|
| Integral Nonlinearity | INL | Note 1 | ± 1.5 | LSB max |
| Differential Nonlinearity | DNL | All Devices Monotonic, Note 1 | ± 1 | LSB max |
| Half-Scale Output Voltage | V_{HS} | $\overline{PR} = 0\text{ V}$, Sets $D = 80_H$ | 1.475/1.525 | V min/max |
| Input Resistance (V_{INX}) | R_{IN} | $D = 55_H$; Code Dependent | 4 | k Ω min |
| REF Low Resistance | R_{REFL} | $D = AB_H$; Code Dependent | 0.3 | k Ω min |
| DAC Output Voltage Range | OVR | $R_L = 10\text{ k}\Omega$ | 3 | V min |
| DAC Output Current | I_{OUT} | $\Delta V_{OUT} < 25\text{ mV}$ | ± 5 | mA min |
| Slew Rate | | Measured 10% to 90% | | |
| Positive | SR+ | $\Delta V_{OUTX} = +3\text{ V}$ | 1.3 | V/ μs min |
| Negative | SR- | $\Delta V_{OUTX} = -3\text{ V}$ | 1.3 | V/ μs min |
| Positive Supply Current | I_{DD} | $\overline{PR} = 0\text{ V}$ | 26 | mA max |
| DC Power Supply Rejection Ratio | PSRR | $\overline{PR} = 0\text{ V}$, $\Delta V_{DD} = \pm 5\%$ | 0.01 | %/% max |
| Logic Input High | V_{IH} | | 2.4 | V min |
| Logic Input Low | V_{IL} | | 0.8 | V max |
| Logic Input Current | I_L | | ± 10 | μA max |
| Logic Output High | V_{OH} | $I_{OH} = -0.4\text{ mA}$ | 3.5 | V min |
| Logic Output Low | V_{OL} | $I_{OL} = 1.6\text{ mA}$ | 0.4 | V max |

NOTE

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

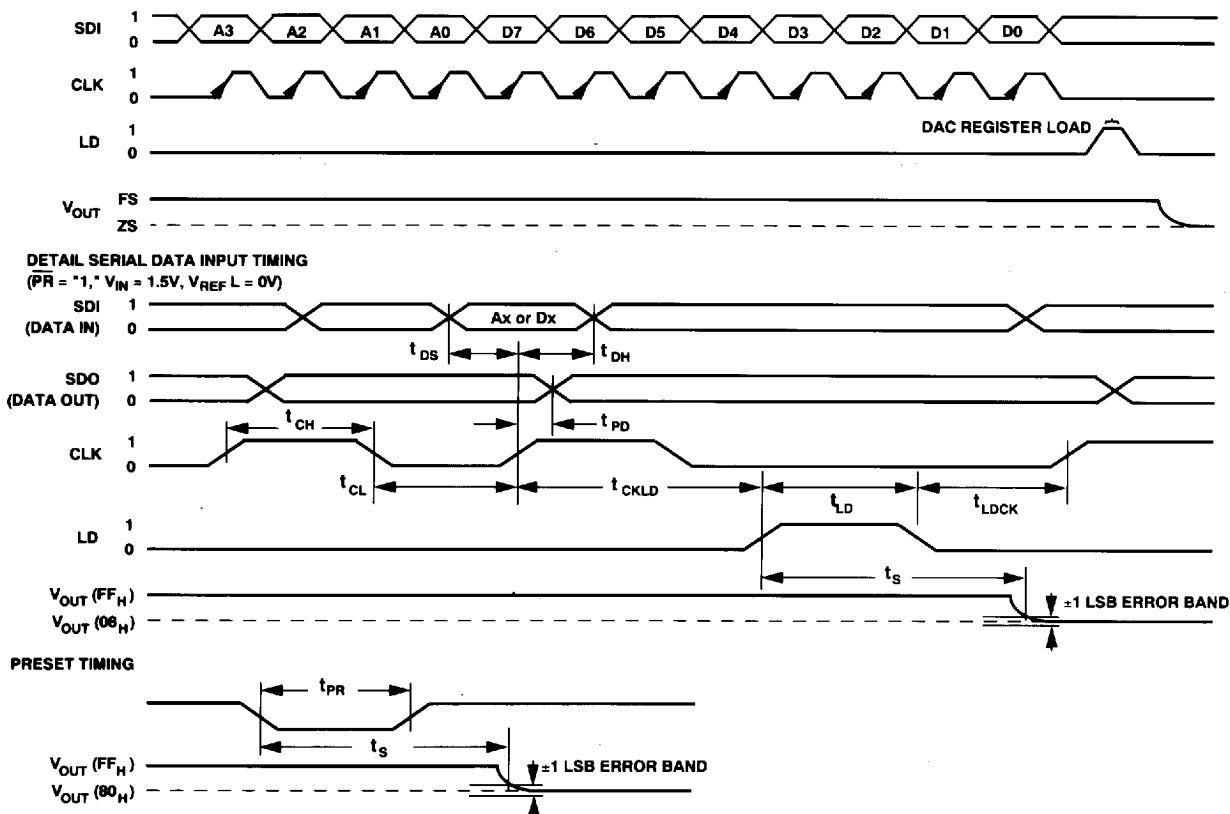


Figure 1. Timing Diagram

DAC-8841

ABSOLUTE MAXIMUM RATINGS

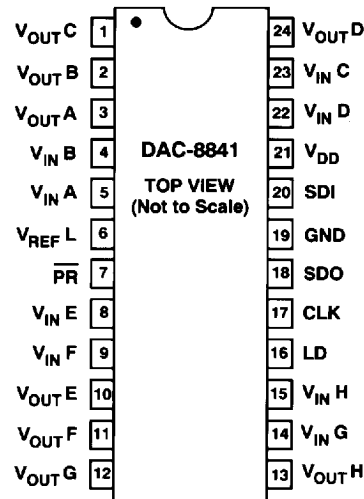
($T_A = +25^\circ\text{C}$, unless otherwise noted)

| | | |
|--|-------|---|
| V_{DD} to GND | | -0.3 V, +7 V |
| V_{INX} to GND | | V_{DD} |
| V_{REFL} to GND | | V_{DD} |
| V_{OUTX} to GND | | V_{DD} |
| Short Circuit I_{OUTX} to GND | | Continuous |
| Digital Input & Output Voltage to GND | | V_{DD} |
| Operating Temperature Range | | |
| Extended Industrial: DAC-8841F | | -40°C to $+85^\circ\text{C}$ |
| Maximum Junction Temperature ($T_J \text{ max}$) | | $+150^\circ\text{C}$ |
| Storage Temperature | | -65°C to $+150^\circ\text{C}$ |
| Lead Temperature (Soldering, 10 sec) | | $+300^\circ\text{C}$ |
| Package Power Dissipation | | ($T_J \text{ Max} - T_A$)/ θ_{JA} |
| Thermal Resistance θ_{JA} | | |
| Cerdip | | 64°C/W |
| P-DIP | | 57°C/W |
| SOIC-24 | | 70°C/W |

DAC-8841 PIN DESCRIPTION

| Pin | Mnemonic | Description |
|-----|------------|--|
| 1 | V_{OUTC} | DAC C Output |
| 2 | V_{OUTB} | DAC B Output |
| 3 | V_{OUTA} | DAC A Output |
| 4 | V_{INB} | DAC B Reference Input |
| 5 | V_{INA} | DAC A Reference Input |
| 6 | V_{REFL} | DAC Input Reference Low |
| 7 | PR | Preset Input, Active Low, All DAC Registers = 80_H |
| 8 | V_{INE} | DAC E Reference Input |
| 9 | V_{INF} | DAC F Reference Input |
| 10 | V_{OUTE} | DAC E Output |
| 11 | V_{OUTF} | DAC F Output |
| 12 | V_{OUTG} | DAC G Output |
| 13 | V_{OUTH} | DAC H Output |
| 14 | V_{ING} | DAC G Reference Input |
| 15 | V_{INH} | DAC H Reference Input |
| 16 | LD | Load DAC Register Strobe, Active High Input that Transfers the Data Bits from the Serial Input Register into the Decoded DAC Register. See Table I |
| 17 | CLK | Serial Clock Input, Positive Edge Triggered |
| 18 | SDO | Serial Data Output, Active Totem Pole Output |
| 19 | GND | Ground |
| 20 | SDI | Serial Data Input |
| 21 | V_{DD} | Positive 5 V Power Supply |
| 22 | V_{IND} | DAC D Reference Input |
| 23 | V_{INC} | DAC C Reference Input |
| 24 | V_{OUTD} | DAC D Output |

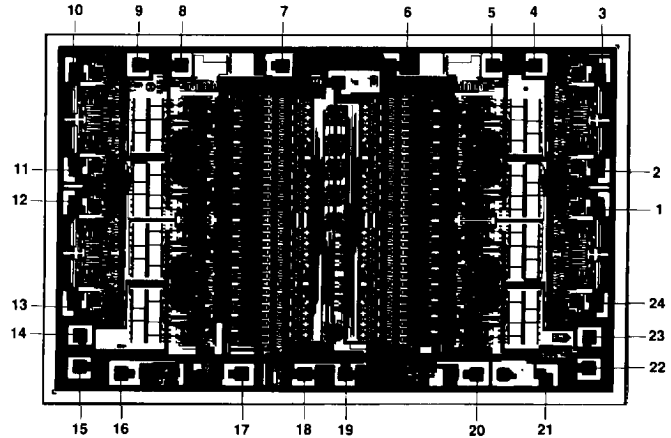
PIN CONFIGURATIONS



DICE CHARACTERISTICS

DIE SIZE 0.117×0.185 inch, 21,645 sq. mils
(2.9718×4.699 mm, 13,964 sq. mm)

The die backside is electrically common to V_{DD} .



| | |
|----------------|----------------|
| 1. V_{OUTC} | 13. V_{OUTH} |
| 2. V_{OUTB} | 14. V_{ING} |
| 3. V_{OUTA} | 15. V_{INH} |
| 4. V_{INB} | 16. LD |
| 5. V_{INA} | 17. CLK |
| 6. V_{REFL} | 18. SDO |
| 7. PR | 19. GND |
| 8. V_{INE} | 20. SDI |
| 9. V_{INF} | 21. V_{DD} |
| 10. V_{OUTE} | 22. V_{IND} |
| 11. V_{OUTF} | 23. V_{INC} |
| 12. V_{OUTG} | 24. V_{OUTD} |

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



ORDERING GUIDE

| Model | Temperature Range | Package Option |
|------------|-------------------|----------------|
| DAC8841FP | -40°C to +85°C | Plastic DIP |
| DAC8841FW | -40°C to +85°C | Cerdip |
| DAC8841FS | -40°C to +85°C | SOIC |
| DAC8841GBC | -25°C | Dice |

For devices processed in total compliance to MIL-STD 883, contact your local sales office for the DAC8841BW/883 data sheet.

Table I. Serial Input Decode Table

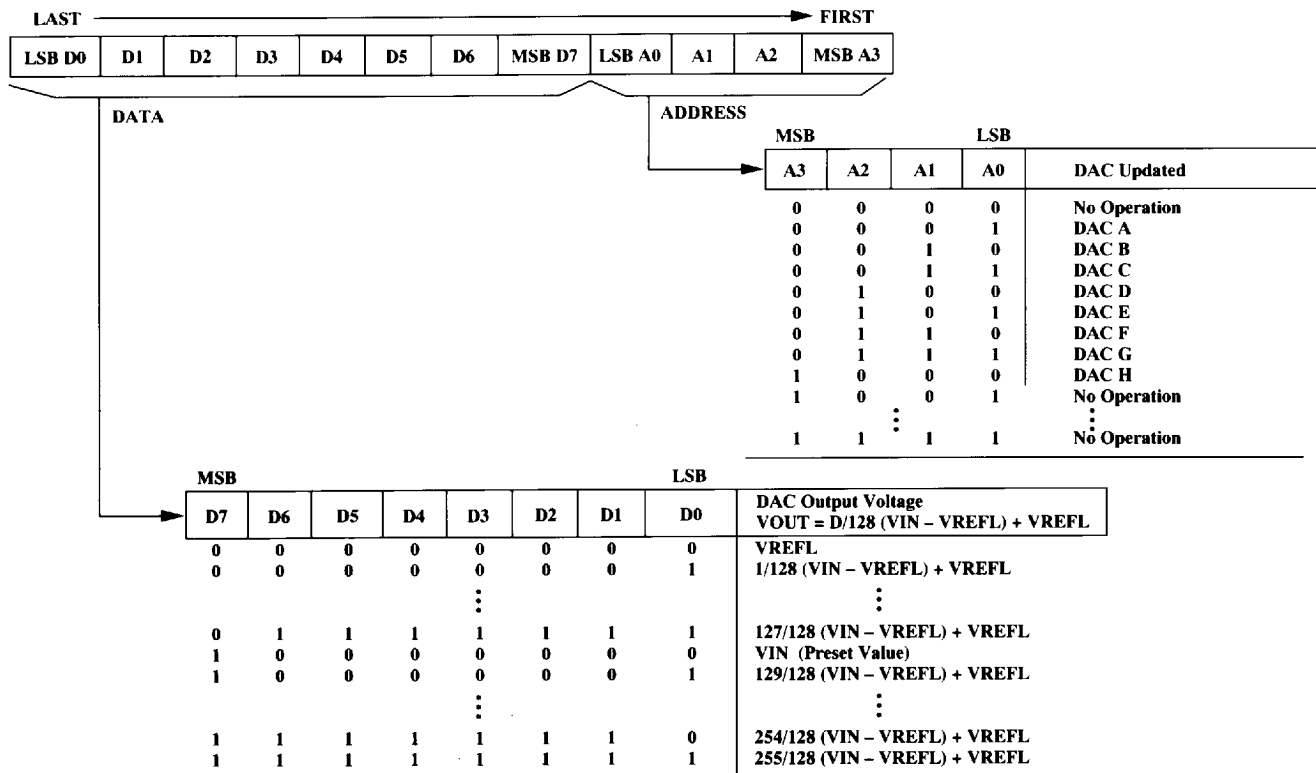


Table II. Logic Control Input Truth Table

| SDI | CLK | LD | \overline{PR} | Input Shift Register Operation |
|-----|-----|----|-----------------|---|
| X | L | L | H | No Operation |
| X | | L | H | Shift One Bit In from SDI (Pin 20), Shift One Bit* Out from SDO (Pin 18) |
| X | X | L | L | All DAC Registers = 80_H |
| X | L | H | H | Load Serial Register Data into DAC(X) Register |

*Data shifted into the SDI pin appears twelve clocks later at the SDO pin.

DAC-8841—Typical Performance Characteristics

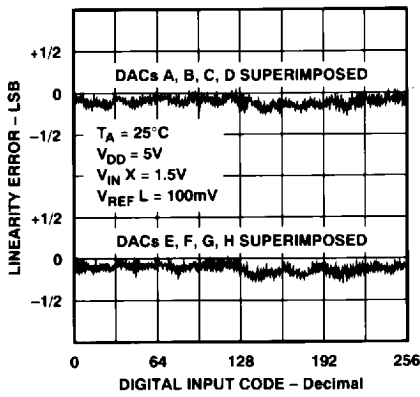


Figure 2. Linearity Error vs. Digital Input Code

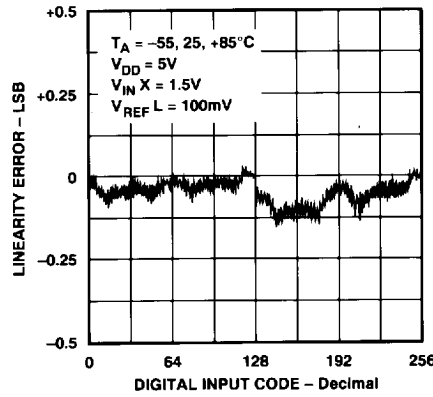


Figure 3. Linearity Error vs. Digital Input Code vs. Temperature

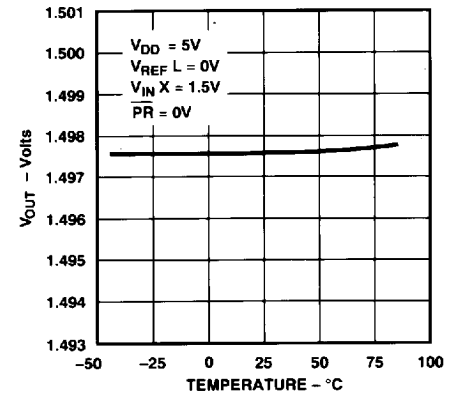


Figure 4. Half Scale vs. Temperature

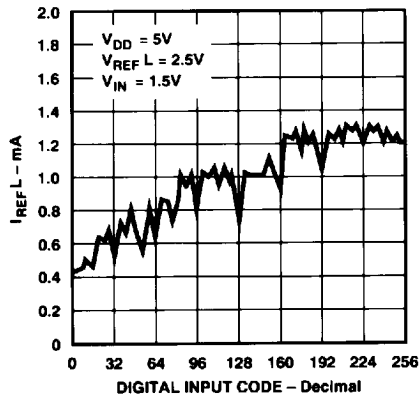


Figure 5. $I_{REF L}$ Input Current vs. Digital Code

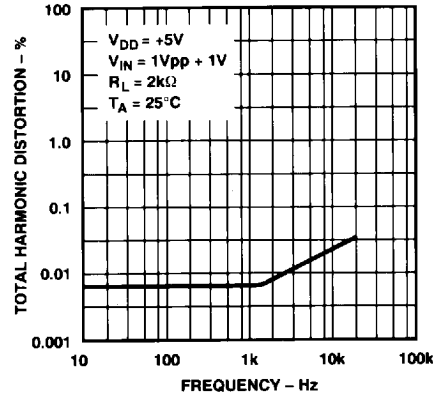


Figure 6. Total Harmonic Distortion vs. Frequency

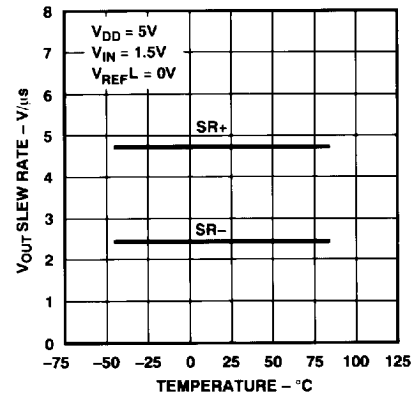


Figure 7. V_{OUT} Slew Rate vs. Temperature

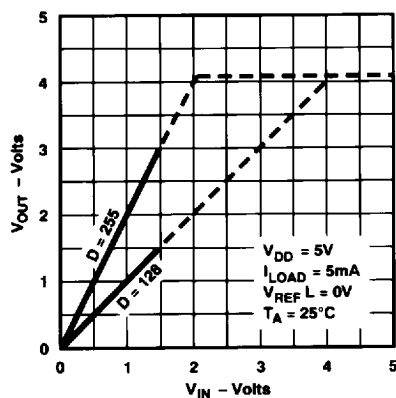


Figure 8. Full-Scale Output to Positive Saturation

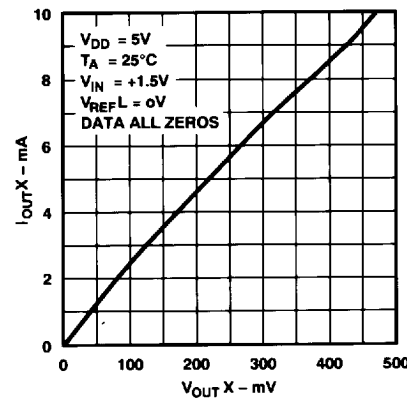


Figure 9. Zero-Scale Output Detail

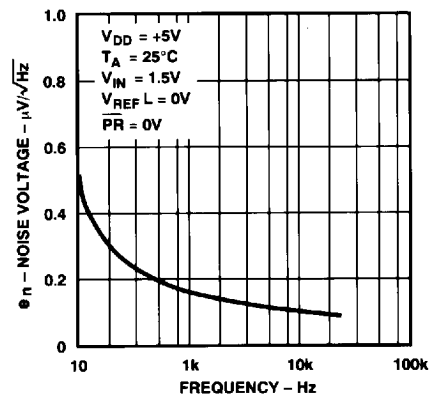


Figure 10. Voltage Noise Density vs. Frequency

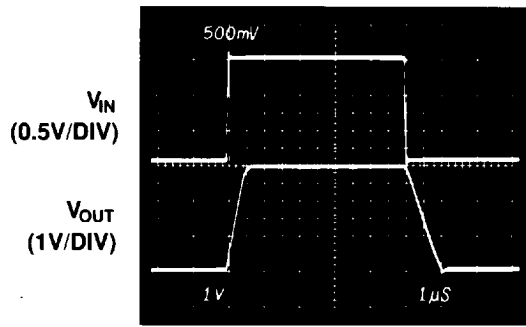
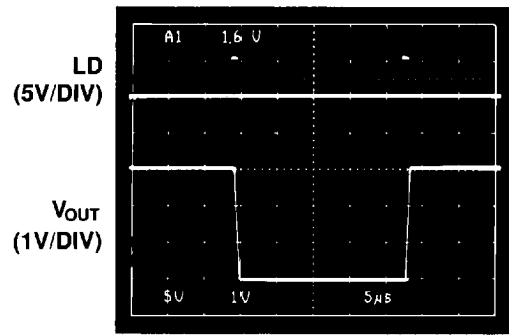
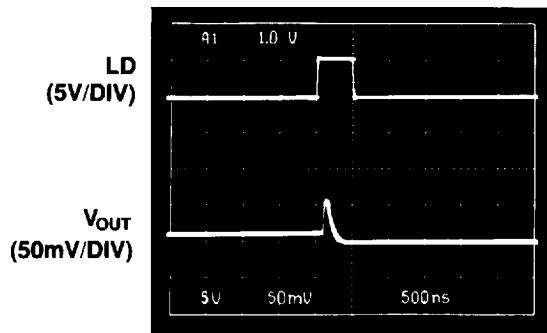


Figure 11. Pulse Response



DIGITAL CODE = 255 → 8 → 255

Figure 12. Settling Time



DIGITAL CODE = 128 → 127

Figure 13. Worst Case 1 LSB Digital Step Change

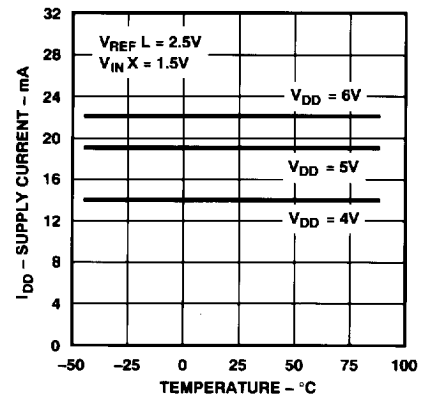


Figure 14. Supply Current vs. Temperature

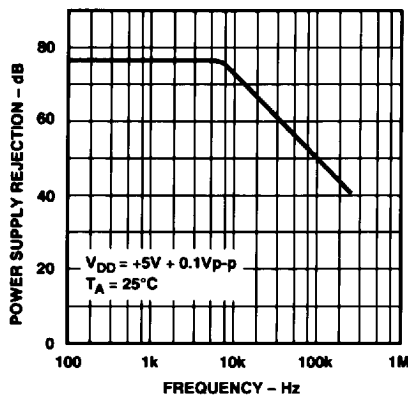


Figure 15. PSRR vs. Frequency

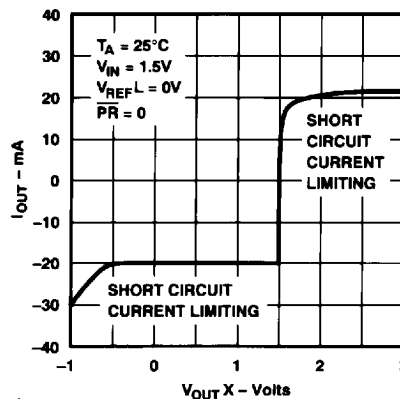


Figure 16. DAC Output Current vs. V_{OUTX}

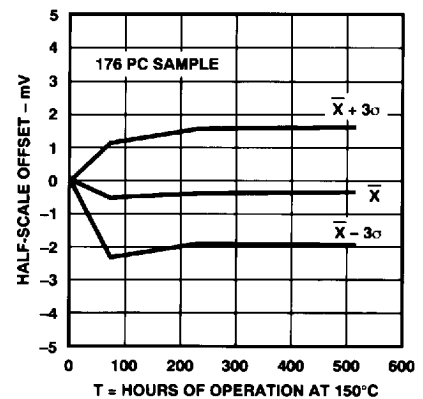


Figure 17. Output Drift Delta Accelerated by Burn-In

DAC-8841

CIRCUIT OPERATION

The DAC-8841 is a general purpose multiple-channel ac or dc signal level adjustment device designed to replace potentiometers used in the three-terminal connection mode. Eight independent channels of programmable signal level control are available in this 24-pin package device. The outputs are completely buffered providing up to 5 mA of drive current to drive external loads. The DAC and amplifier combination shown in Figure 18 produces two-quadrant multiplication of the signal inputs applied to V_{IN} times the digital input control word. In addition the DAC-8841 provides a 1 MHz gain-bandwidth product in the two-quadrant multiplying channel. Operating from a 5 V power supply, analog inputs to +1.5 V which generate outputs to +3 V are easily accommodated.

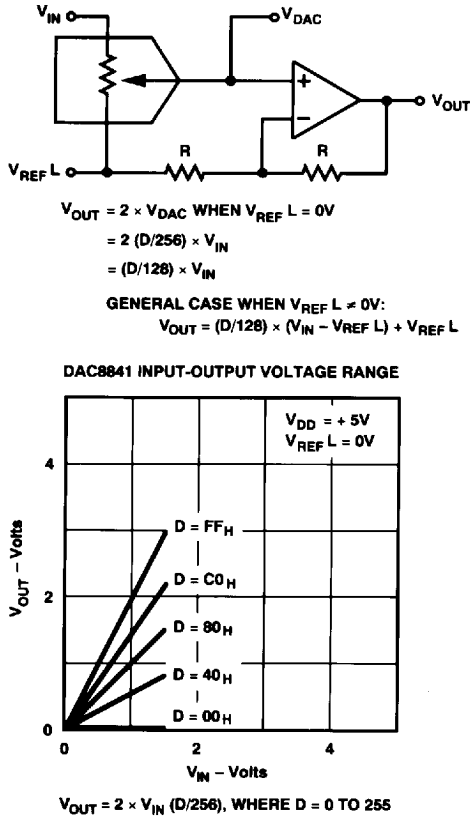


Figure 18. DAC Plus Amplifier Combine to Produce Two-Quadrant Multiplication

In order to be easy to use with a controlling microprocessor, a simple layout-efficient three-wire serial data interface was chosen. This interface can be easily adapted to almost all microcomputer and microprocessor systems. A clock (CLK), serial data input (SDI) and a load (LD) strobe pin make up the three-wire interface. The 12-bit input data word used to change the value of the internal DAC registers contains a 4-bit address and 8-bits of data. Using this combination, any DAC register can be changed without disturbing the other devices. A serial data output (SDO) pin simplifies cascading multiple DAC-8841s without adding address decoder chips to the system.

During system power up a logic low on the preset \overline{PR} pin forces all DAC registers to 80_H which in turn forces all the buffer amplifier outputs to equal half-scale. The transfer equation (1) shows that in the preset condition (80_H) that V_{OUT} will equal V_{IN} . The asynchronous \overline{PR} input pin can be activated at any time to force the DAC registers to the half-scale code 80_H . This is generally the most convenient place to start for general purpose adjustment applications.

ADJUSTING AC OR DC SIGNAL LEVELS

The two-quadrant multiplication operation of the DAC-8841 is shown in Figure 18. For dc operation the equation describing the relationship between V_{IN} , digital inputs and V_{OUT} is:

$$V_{OUT}(D) = (D/128) \times (V_{IN} - V_{REF L}) + V_{REF L} \quad (1)$$

where D is a decimal number between 0 and 255.

The actual output voltages generated with a fixed 1.5 V dc input on V_{IN} and $V_{REF L} = 0 V$ are summarized in this table.

| Decimal Input (D) | $V_{OUT}(D)$ | Comments ($V_{IN} = 1.5 V$, $V_{REF L} = 0 V$) |
|-------------------|--------------|--|
| 0 | 0.000 V* | Zero Scale |
| 1 | 0.012* | |
| 2 | 0.024* | |
| 127 | 1.488 | |
| 128 | 1.500 | Half Scale = V_{IN} |
| 129 | 1.512 | |
| 254 | 2.976 | |
| 255 | 2.988 | Full Scale (FS) $\approx 2 \times V_{IN}$ |

*See "Operation Near Ground."

Notice that the output polarity is the same as the input polarity when the DAC register is loaded with 255 (in binary = all ones). Also note that the output does not exactly equal two times the input voltage. This is a result of the R-2R ladder DAC chosen. When the DAC register is loaded with 0, the output is $V_{REF L}$. The actual voltage measured when setting up a DAC in this example will vary within the ± 1 LSB linearity error specification of the DAC-8841. The actual voltage error would be $\pm 0.012 V$.

Operation Near ground - The input stage of the internal buffer amplifier functions down to ground, but the output stage cannot pull lower than the internal ground voltage. When a DAC output tries to output a voltage at or below the internal ground potential, it saturates and appears like a 50 Ω resistor to ground. The typical saturation voltage appearing at the output is 20 mV, see Figure 9. The 100 mV worst case zero-scale voltage specification reflects this saturation effect, including the worst case anticipated variation of the internal ground resistances, quiescent currents and buffer sinking current. Linearity is measured between code 8_{10} and code 255_{10} to avoid this saturation effect. In summary, the transfer function of each DAC will be a straight line from code 8 to code 255 when $V_{REF L} = 0 V$. For input codes 0 to 7, some DAC outputs will be saturated in the zero-scale output voltage region; therefore, changing digital code 0 to 1 may not change the output voltage when $V_{REF L} = 0 V$.

SIGNAL INPUTS (V_{IN}A, B, C, D, E, F, G, H)

The eight independent V_{IN} inputs have a code dependent input resistance whose worst case minimum value is specified in the electrical characteristics table. Use a suitable amplifier capable of driving this input resistance in parallel with the specified input capacitance. These reference inputs are designed to receive not only dc, but ac input voltages. This results from the incorporation of a true bilateral analog switch in the DAC design, see Figure 19. The DAC switch operation has been designed to operate in the break-before-make format to minimize transient loading of the inputs. The reference input voltage range can operate from ground (GND) to 1.5 V. That is, the operating input voltage range, when V_{REFL} = 0 V, is:

$$0 V < V_{INX} < 1.5 V \tag{2}$$

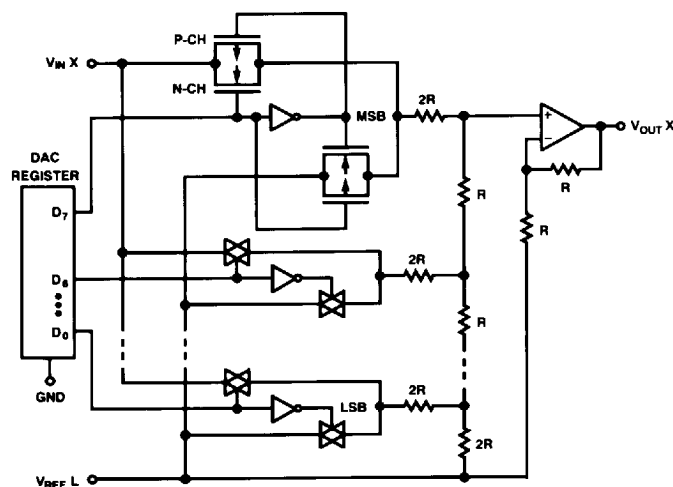


Figure 19. DAC-8841 TrimDAC Equivalent Circuit (One Channel)

The reference inputs can withstand input voltages up to V_{DD}; however due to the internal amplifier's gain of two configuration, the output voltage of the circuit reaches its maximum specified value of 3 V when the input voltage equals 1.5 V and V_{REFL} = 0 V; see Figure 18.

The reference low input V_{REFL} is the bottom end of the DAC (see Figure 18). This input is normally tied to ground; however it can be biased above ground. When V_{REFL} is biased above ground, its value and that of V_{INX} should be chosen in agreement with Equation 3.

$$V_{OUT} \leq V_{DD} - 2 V \tag{3}$$

Also for the general case the headroom restriction to V_{DD} for V_{INX} and V_{REFL} is given by Equation 4.

$$V_{INX}, V_{REFL} \leq V_{DD} - 2 V \tag{4}$$

According to the above equations, the DAC-8841 can only be operated under certain combinations of V_{INX} and V_{REFL}. The shaded area in Figure 20 defines the theoretical allowable ranges of operation. Note that V_{REFL} can be biased higher than V_{INX}. Linearity will vary with the reference voltages and supply conditions. If a symmetrical output ac signal is desired, then the symmetrical ac input on V_{INX} should be offset to V_{REFL}. The output signal will then be with respect to V_{REFL}.

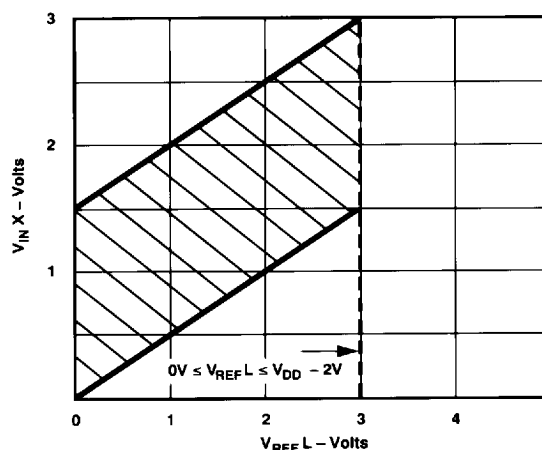


Figure 20. DAC-8841 Input Voltage Operating Boundaries

For example, biasing V_{REFL} equal to one volt would accept a 1 V p-p ac input signal on V_{IN}. This input signal could then be attenuated or given a gain-of-two depending on the DAC data setting.

DAC OUTPUTS (V_{OUT}A, B, C, D, E, F, G, H)

The eight D/A converter outputs are fully buffered by the DAC-8841s internal amplifier. This amplifier is designed to drive up to 1 kΩ loads in parallel with 200 pF. However in order to minimize internal device power consumption, it is recommended whenever possible to use larger values of load resistance. The amplifier output stage can handle shorts to GND; however, care should be taken to avoid continuous short circuit operation. See Figure 16 "DAC output current versus V_{OUTX}" graph.

The amplifier output is guaranteed to operate to within 2 V of V_{DD} under all load conditions and temperature. Figure 8 shows typical operation to positive output saturation with a 5 mA load.

The low output impedance of the buffers minimizes crosstalk between analog input channels. At 100 kHz 70 dB of channel-to-channel isolation exists. It is recommended to use good circuit layout practice such as guard traces between analog channels and power supply bypass capacitors. A 0.01 μF ceramic in parallel with a 1-10 μF tantalum capacitor provides a good power supply bypass for most frequencies encountered.

DIGITAL INTERFACING

The four digital input pins (CLK, SDI, LD, \overline{PR}) of the DAC-8841 were designed for TTL and 5 V CMOS logic compatibility. The SDO output pin offers good fanout in CMOS logic applications and can easily drive several DAC-8841s.

The Logic Control Input Truth Table II describes how to shift data into the internal 12-bit serial input register. Note that the CLK is a positive edge-sensitive input. If mechanical switches are used for breadboard, product evaluation they should be debounced by a flipflop or other suitable means.

The required address plus data input format is defined in the Serial Input Decode Table I. Note there are 8 address states that result in no operation (NOP) or activity in the DAC-8841 when the active high load strobe LD is activated. This NOP can be used in cascaded applications where only one DAC out of several packages needs updating. It takes 12 clocks on the CLK

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pin to fully load the serial input shift register. Data on the SDI input pin is subject to the timing diagram (Figure 1) data setup and data hold time requirements. After the twelfth clock pulse, the processor needs to activate the LD strobe to have the DAC-8841 decode the serial register contents and update the target DAC register with the 8-bit data word. This needs to be done before the thirteenth positive clock edge. The timing requirements are in the electrical characteristic table and in the Figure 1 timing diagram. After twelve clock edges data initially loaded into the shift register at SDI appears at the shift register output SDO.

There is some digital feedthrough from the digital input pins. Operating the clock only when the DAC registers require updating minimizes the effect of the digital feedthrough on the analog signal channels.

Figure 21 shows a three-wire interface for a single DAC-8841 that easily cascades for multiple packages.

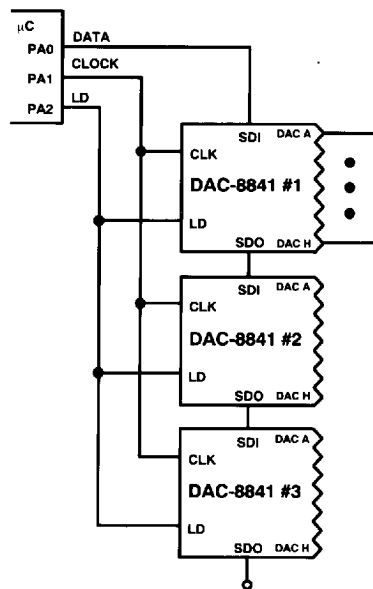


Figure 21. Three-Wire Interface

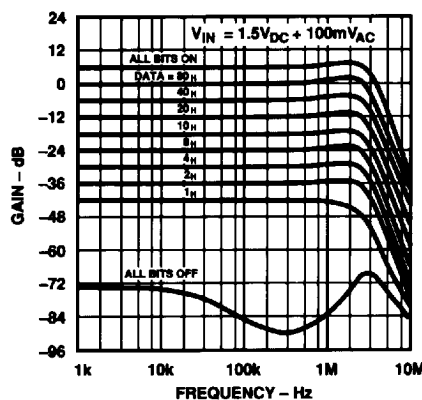


Figure 22. Gain (V_{OUT}/V_{IN}) and Feedthrough vs. Frequency

