



# N-Channel 30-V (D-S) MOSFET

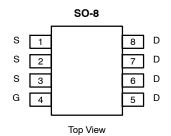
PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$r_{DS(on)}\left(\Omega\right)$	I <sub>D</sub> (A)			
30	0.012 @ V <sub>GS</sub> = 10 V	12.5			
	0.018 @ V <sub>GS</sub> = 4.5 V	10.2			

#### **FEATURES**

- TrenchFET® Power MOSFET
- Lead (Pb)-Free Version is RoHS Compliant

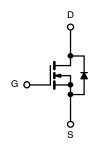


Pb-free Available



Ordering Information: Si4894DY-T1

Si4894DY-T1-E3 (Lead (Pb)-Free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^{\circ}$ C UNLESS OTHERWISE NOTED)							
Parameter		Symbol	10 secs	Steady State	Unit		
Drain-Source Voltage		$V_{DS}$	30		٧		
Gate-Source Voltage		$V_{GS}$	±20				
O-ation David Oranget (T. 45000)	T <sub>A</sub> = 25°C	I <sub>D</sub>	12.5	8.5			
Continuous Drain Current (T <sub>J</sub> = 150°C) <sup>a</sup>	T <sub>A</sub> = 70°C		10	6.8	Α		
Pulsed Drain Current		I <sub>DM</sub>	20				
Continuous Source Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	2.7	1.3	Α		
Maximum Davier Dissipations	T <sub>A</sub> = 25°C		3.0	1.4	W		
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 70°C	P <sub>D</sub>	1.9	0.9	٧٧		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to 150		°C		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
	t ≤ 10 sec	R <sub>thJA</sub>	35	42	°C/W	
Maximum Junction-to-Ambient <sup>a</sup>	Steady State		73	90		
Maximum Junction-to-Foot (Drain)	Steady State	R <sub>thJF</sub>	16	20		

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

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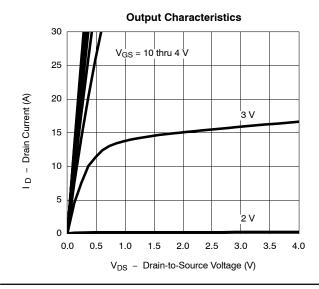


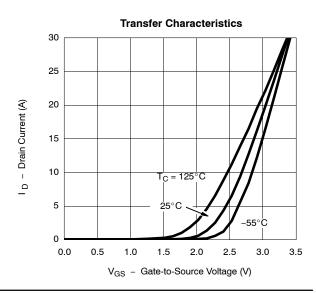
SPECIFICATIONS (T <sub>J</sub> = 25°C UNLESS OTHERWISE NOTED)									
Parameter	Symbol	mbol Test Condition		Тур	Max	Unit			
Static				•					
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	0.8		1.8	V			
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS}$ = 0 V, $V_{GS}$ = $\pm 20$ V			±100	nA			
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55 ^{\circ}\text{C}$			1 5	μΑ			
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30			Α			
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	$V_{GS} = 10 \text{ V, } I_D = 12.5 \text{ A}$		0.010	0.012	Ω			
		$V_{GS} = 4.5 \text{ V}, I_D = 10.2 \text{ A}$		0.015	0.018				
Forward Transconductance <sup>a</sup>	9fs	$V_{DS} = 15 \text{ V}, I_{D} = 12.5 \text{ A}$		30		S			
Diode Forward Voltagea	V <sub>SD</sub>	$I_S = 2.7 \text{ A}, V_{GS} = 0 \text{ V}$		0.7	1.1	V			
Dynamic <sup>b</sup>									
		$V_{DS} = 15 \text{ V}, \ V_{GS} = 5 \text{ V}, \ I_D = 12.5 \text{ A}$		11.5	17				
Total Gate Charge	Qg			20	30	nC			
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS}$ = 15 V, $V_{GS}$ = 10 V, $I_{D}$ = 12.5 A		3.0					
Gate-Drain Charge	Q <sub>gd</sub>			4.5					
Gate Resistance	R <sub>g</sub>		0.5		2.4	Ω			
Turn-On Delay Time	t <sub>d(on)</sub>			10	20				
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 15 $\Omega$		5	10	1			
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 1 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 6 \Omega$		30	60	ns			
Fall Time	tf			10	20	1			
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 2.7 A, di/dt = 100 A/μs		30	60	1			

#### Notes

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





Pulse test; pulse width  $\leq 300 \ \mu s$ , duty cycle  $\leq 2\%$ .

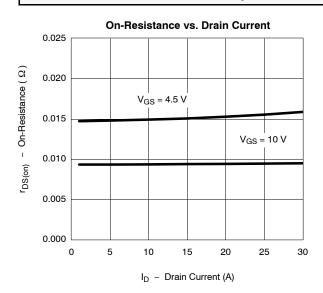
Guaranteed by design, not subject to production testing.

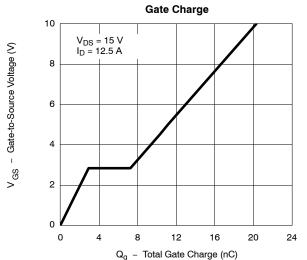


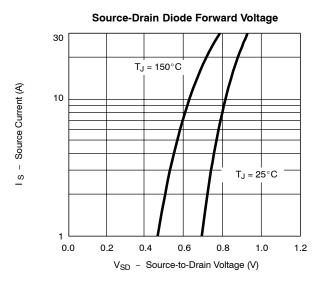


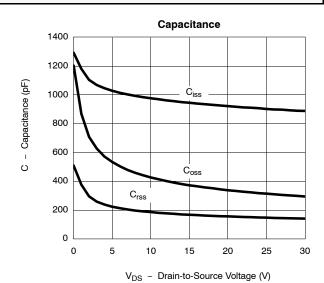


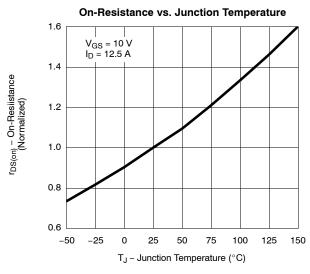
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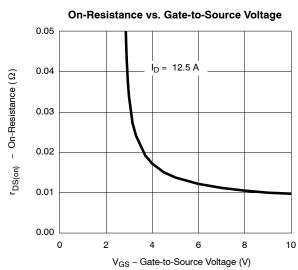








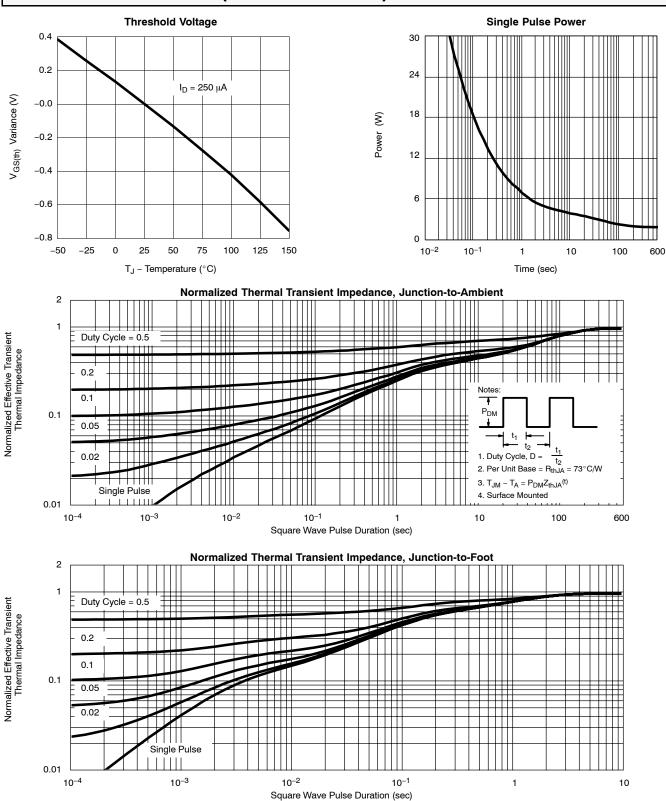




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#### TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="http://www.vishay.com/ppg?71162">http://www.vishay.com/ppg?71162</a>.





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