Dual Mode DisplayPort™ to HDMI™ Level Shifter with Integrated I²C ID for HDMI™ Detection

Features

- Converts low-swing AC coupled differential input to HDMI™ rev 1.3 compliant open-drain current steering Rx terminated differential output
- Compliant to VESA Interop Guidelines
- HDMI level shifting operation up to 2.5Gbps per lane (250MHz pixel clock)
- Integrated 50-ohm termination resistors for AC-coupled differential inputs.
- Enable/Disable feature to turn off TMDS outputs to enter low power state.
- I²C buffer for ATC DDC Cap test support
- I²C ID, located at address 80h/81h, used for HDMI detection
- Transparent operation: no re-timing or configuration required
- 3.3 Power supply required
- Integrated ESD protection to 8KV Contact on all I/O pins per IEC61000-4-2, level 4
- Level shifter for HPD signal from HDMI/DVI connector
- Integrated pull-down on HPD_sink input guarantees "input low" when no display is plugged in
- Packaging (Pb-free & Green available)
  - 42 TQFN, 9mm × 3.5mm (ZHE)
  - 48 TQFN, 7mm x 7mm (ZDE)

Description

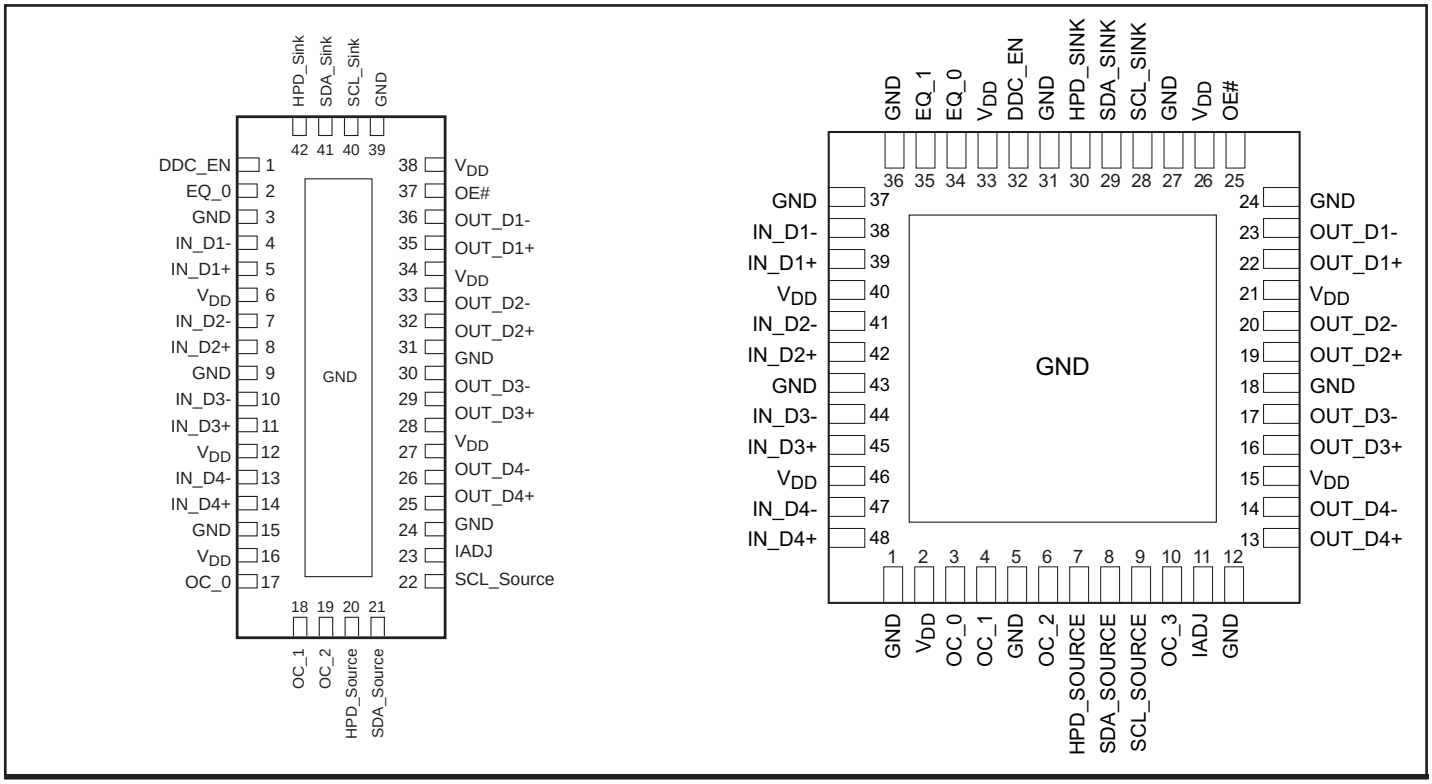
Pericom Semiconductor's PI3VDP101LS provides the ability to use a Dual-mode DP transmitter in HDMI™/DVI mode. This flexibility provides the user a choice of how to connect to their favorite display. All signal paths accept AC coupled video signals. The PI3VDP101LS converts this AC coupled signal into an HDMI rev 1.3 compliant signal with proper signal swing. This conversion is automatic and transparent to the user.

The PI3VDP101LS supports up to 2.5Gbps, which provides 12-bits of color depth per channel, as indicated in HDMI rev 1.3.

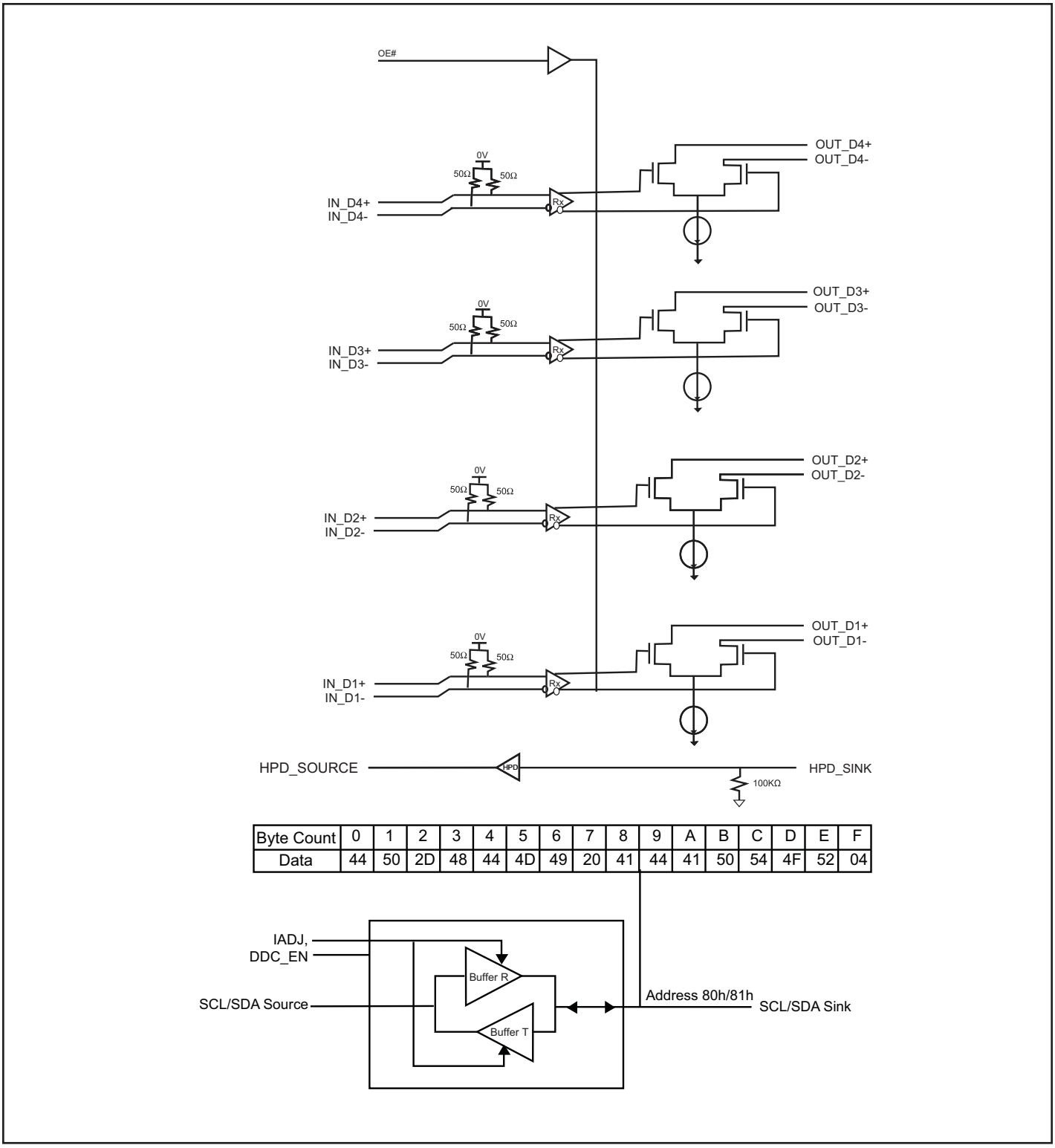
Each complete HDMI/DVI channel also has slower speed, side band signals, that are required to be switched. Pericom's solution provides a complete solution by integrating the side band buffer together with the high speed level shifter in a single solution. Using Equalization at the input of each of the high speed channels, Pericom can successfully eliminate deterministic jitter caused by long cables from the source to the sink. The elimination of the deterministic jitter allows the user to use much longer cables.

The maximum DVI/HDMI Bandwidth of 2.5 Gbps provides 36-bit Deep Color™ support, which is offered by HDMI revision 1.3. The PI3VDP101LS also provides enhanced robust ESD/EOS protection of 8KV, which is required by many consumer video networks today.

Pin Configurations



Block Diagram



Byte Count	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Data	44	50	2D	48	44	4D	49	20	41	44	41	50	54	4F	52	04

I2C ROM Block Read/Write format:

Pericom's PI3VDP101LS supports the mandatory DDC buffer ID access sequence per the VESA approved DisplayPort™ Interoperability guidelines.

										Status	
I2C Transaction	**Transmitting**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**R/W#**	**Master**	**Slave**
Start	Master									Mandatory	–
7-bit Address + command	Master	1	0	0	0	0	0	0	1	Mandatory	–
Read data	Slave	Data Byte 0								–	Mandatory
Acknowledge (1 bit)	Master									Mandatory	–
Read data	Slave	Data Byte N (N = 1 to 14)								–	Mandatory
Read data	Slave	Data byte 15								–	Mandatory
Not acknowledge (1 bit)	Master									Mandatory	–
Stop	Master									Mandatory	–

Maximum Ratings (Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.....–65°C to +150°C
Supply Voltage to Ground Potential.....–0.5V to +5V
DC Input Voltage.....–0.5V to V_{DD}
DC Output Current.....120mA
Power Dissipation.....1.0W

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 2: Signal Descriptions

Pin Name	Type	Description
OE#	5.5V tolerant low-voltage single-ended input	Enable for level shifter path OE# = 1: IN_D Termination >100KΩ, OUT_D Outputs High-Z OE# = 0: IN_D Termination 50Ω, OUT_D Outputs Active
IN_D4+	Differential input	Low-swing diff input from GMCH PCIE outputs. IN_D4+ makes a differential pair with IN_D4–.
IN_D4–	Differential input	Low-swing diff input from GMCH PCIE outputs. IN_D4– makes a differential pair with IN_D4+.
IN_D3+	Differential input	Low-swing diff input from GMCH PCIE outputs. IN_D3+ makes a differential pair with IN_D3–.
IN_D3–	Differential input	Low-swing diff input from GMCH PCIE outputs. IN_D3– makes a differential pair with IN_D3+.
IN_D2+	Differential input	Low-swing diff input from GMCH PCIE outputs. IN_D2+ makes a differential pair with IN_D2–.
IN_D2–	Differential input	Low-swing diff input from GMCH PCIE outputs. IN_D2– makes a differential pair with IN_D2+.
IN_D1+	Differential input	Low-swing diff input from GMCH PCIE outputs. IN_D1+ makes a differential pair with IN_D1–.
IN_D1–	Differential input	Low-swing diff input from GMCH PCIE outputs. IN_D1– makes a differential pair with IN_D1+.
OUT_D4+	TMDS Differential output	HDMI 1.3 compliant TMDS output. OUT_D4+ makes a differential output signal with OUT_D4–.
OUT_D4–	TMDS Differential output	HDMI 1.3 compliant TMDS output. OUT_D4– makes a differential output signal with OUT_D4+.
OUT_D3+	TMDS Differential output	HDMI 1.3 compliant TMDS output. OUT_D3+ makes a differential output signal with OUT_D3–.
OUT_D3–	TMDS Differential output	HDMI 1.3 compliant TMDS output. OUT_D3– makes a differential output signal with OUT_D3+.
OUT_D2+	TMDS Differential output	HDMI 1.3 compliant TMDS output. OUT_D2+ makes a differential output signal with OUT_D2–.

(Continued)

Pin Name	Type	Description
OUT_D2–	TMDS Differential output	HDMI 1.3 compliant TMDS output. OUT_D2– makes a differential output signal with OUT_D2+.
OUT_D1+	TMDS Differential output	HDMI 1.3 compliant TMDS output. OUT_D1+ makes a differential output signal with OUT_D1–.
OUT_D1–	TMDS Differential output	HDMI 1.3 compliant TMDS output. OUT_D1– makes a differential output signal with OUT_D1+.
HPD_SINK	5V tolerance single-ended input	Low Frequency, 0V to 5V (nominal) input signal. This signal comes from the HDMI connector. Voltage High indicates "plugged" state; voltage low indicated "unplugged". HPD_SINK is pulled down by an integrated 100K ohm pull-down resistor.
HPD_SOURCE	3.3V single-ended output	HPD_SOURCE: 0V to 3.3V (nominal) output signal. This is level-shifted version of the HPD_SINK signal.
SCL_SOURCE	Single-ended open-drain buffered DDC I/O	DDC Data I/O. Pulled up by external 3.3V termination.
SDA_SOURCE	Single-ended open-drain buffered DDC I/O	DDC Data I/O. Pulled up by external 3.3V termination.
SCL_SINK	Single-ended 5V open-drain buffered DDC I/O	5V DDC Clock I/O. Pulled up by external termination to 5V.
SDA_SINK	Single-ended 5V open-drain buffered DDC I/O	5V DDC Data I/O. Pulled up by external termination to 5V.
V_{DD}	3.3V DC Supply	3.3V ± 10%
OC_0 OC_1 OC_2 OC_3 EQ_0 EQ_1	Output and Input jitter elimination control	Control pins are to enable Jitter elimination features. For normal operation these pins are tied GND or to V_{DD}. Please see the truth tables for more information.
IADJ	3.3V control signal	I^2C I/O adjustment for different external pull-up values. If HIGH, then external pull-ups should be in the range of 1KΩ to 2KΩ. If IADJ is LOW, then the external pull-ups should be between 3.6Kohm and 5.1Kohm.
DDC_EN	3.3V control signal	

Truth Table 1

OC_3(2)	OC_2(1)	OC_1(1)	OC_0(1)	Vswing (mV)	Pre/De-emphasis
0	0	0	0	500	0
0	0	0	1	600	0
0	0	1	0	750	0
0	0	1	1	1000	0
0	1	0	0	500	0
0	1	0	1	500	1.5dB
0	1	1	0	500	3.5dB
0	1	1	1	500	6dB
1	0	0	0	400	0
1	0	0	1	400	3.5dB
1	0	1	0	400	6dB
1	0	1	1	400	9dB
1	1	0	0	1000	0
1	1	0	1	1000	-3.5dB
1	1	1	0	1000	-6dB
1	1	1	1	1000	-9dB

Truth Table 2

EQ_1(2)	EQ_0(1)	Equalization @ 1.25GHz (dB)
0	0	3
0	1	6
1	0	9
1	1	12

Notes:

1) These signals have internal 100kΩ pull-ups.

2) For 42-TQFN package, these signals are internally connected to GND directly.
For 48-TQFN package, these signals have internal 100kΩ pull-ups, with external connection.

Functional Truth Table

IADJ	External Pull-Up Range for resistor. Voltage should be 3.3V +/-10%
H	1kΩ to 2kΩ (HDMI spec)
L	3.6Kohm to 5.1Kohm (4.7kΩ typically)

DDC_EN	Source Port/Sink Port
L	Hi-Z (I2C buffer disable)
H	I2C buffer enable

Electrical Characteristics

Power Supplies and Temperature Range

Symbol	Parameter	Min	Nom	Max	Units	Comments
V_{DD}	3.3V Power Supply	3.0	3.3	3.6	V	
I_{CC}	Max Current			100	mA	Total current from V_{DD} 3.3V supply when de-emphasis/pre-emphasis is set to 0dB.
I_{CCQ}	Standby Current			2	mA	OE# = HIGH
T_{CASE}	Case temperature range for operation with spec.	-40		85	Celsius	

OE# Description

OE#	Device State	Comments
Asserted (low voltage)	Differential input buffers and output buffers enabled. Input impedance = 50Ω	Normal functioning state for IN_D to OUT_D level shifting function.
Unasserted (high voltage)	Low-power state. Differential input buffers and termination are disabled. Differential inputs are in a high-impedance state. OUT_D level-shifting outputs are disabled. OUT_D level-shifting outputs are in high-impedence state. Internal bias currents are turned off.	Intended for lowest power condition when: • No display is plugged in or • The level shifted data path is disabled HPD_SINK input and HPD_SOURCE output are not affected by OE# SCL_SOURCE, SCL_SINK, SDA_SOURCE and SDA_SINK signals and functions are not affected by OE#

Differential Input Characteristics for IN_D and RX_IN signals

Symbol	Parameter	Min	Nom	Max	Units	Comments
Tbit	Unit Interval	360			ps	Tbit is determined by the display mode. Nominal bit rate ranges from 250Mbps to 2.5Gbps per lane. Nominal Tbit at 2.5 Gbps=400ps. 360ps=400ps-10%
$V_{RX-DIFFp-p}$	Differential Input Peak to Peak Voltage	0.175		1.200	V	VRX-DIFFp-p=2'|VRX-D+ x VRX-D-| Applies to IN_D and RX_IN signals
T_{RX-EYE}	Minimum Eye Width at IN_D input pair	0.8			Tbit	The level shifter may add a maximum of 0.02UI jitter
$V_{CM-AC-pp}$	AC Peak Common Mode Input Voltage			100	mV	VCM-AC-pp = |VRX-D+ + VRX-D-|/2 - VRX-CM-DC. VRX-CM-DC = DC(avg) of|VRX-D+ + VRX-D-|/2 VCM-AC-pp includes all frequencies above 30 kHz.
Z_{RX-DC}		40	50	60	Ω	Required IN_D+ as well as IN_D- DC impedance (50Ω ± 20% tolerance).
$V_{RX-Bias}$		0		2.0	V	Intended to limit power-up stress on chipset's PCIE output buffers.
$Z_{RX-HIGH-Z}$		100			kΩ	Differential inputs must be in a high impedance state when OE# is HIGH.

TMDS Outputs

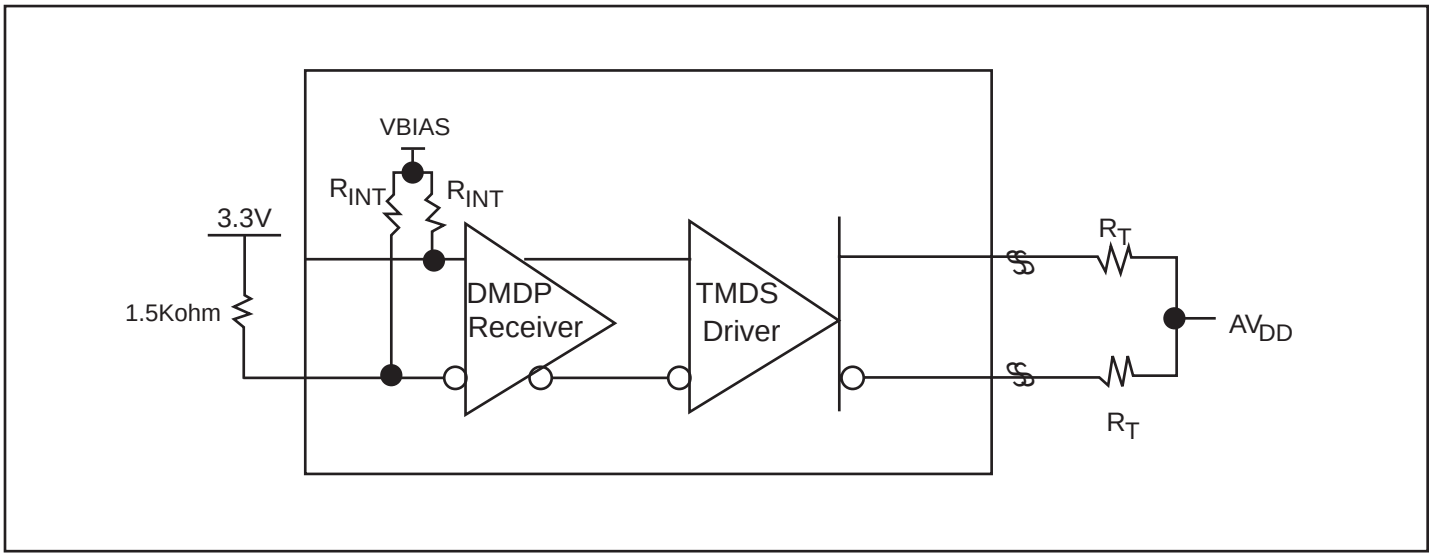
The level shifter's TMDS outputs are required to meet HDMI 1.3 specifications.
The HDMI 1.3 Specification is assumed to be the correct reference in instances where this document conflicts with the HDMI 1.3 specification.

Differential Output Characteristics for TMDS_OUT signals

Symbol	Parameter	Min	Nom	Max	Units	Comments
V_H	Single-ended high level output voltage	AVDD-10mV	AVDD	AVDD+10mV	V	AVDD is the DC termination voltage in the HDMI or DVI Sink. AVDD is nominally 3.3V
V_L	Single-ended low level output voltage	AVDD-600mV	AVDD-500mV	AVDD-400mV	V	The open-drain output pulls down from AVDD.
V_{SWING}	Single-ended output swing voltage	450mV	500mV	600mV	V	Swing down from TMDS termination voltage (3.3V ± 10%)
I_{OFF}	Single-ended current in High-Z state			10	µA	Measured with TMDS outputs pulled up to AVDD Max (3.6V)through 50Ω resistors.
T_R	Rise time	125ps		0.4Tbit	ps	Max Rise/Fall time @2.7Gbps = 148ps 125ps = 148-15%
T_F	Fall time	125ps		0.4Tbit	ps	Max Rise/Fall time @2.7Gbps = 148ps 125ps = 148-15%
$T_{SKEW-INTRA}$	Intra-pair differential skew			30	ps	This differential skew budget is in addition to the skew presented between D+ and D- paired input pins. HDMI revision 1.3 source allowable intra-pair skew is 0.15 Tbit.
$T_{SKEW-INTER}$	Inter-pair lane-to-lane output skew			100	ps	This lane-to-lane skew budget is in addition to skew between differential input pairs
T_{JIT}	Jitter added to TMDS signals			25	ps	Jitter budget for TMDS signals as they pass through the level shifter. 25ps = 0.056 Tbit at 2.25 Gbps

TMDS output oscillation elimination

The inputs do not incorporate a squelch circuit. Therefore, we recommend the input to be externally biased to prevent output oscillation. Pericom recommends to add a 1.5KΩ pull-up to the CLK- input.



TMDS Input Fail-Safe Recommendation

HPD Input Characteristics

Symbol	Parameter	Min	Nom	Max	Units	Comments
V_{IH-HPD}	Input High Level	2.0	5.0	5.5	V	Low-speed input changes state on cable plug/unplug
V_{IL-HPD}	HPD_sink Input Low Level	0		0.8	V	
I_{IN-HPD}	HPD_sink Input Leakage Current			70	µA	Measured with HPD_sink at V_{IH-HPD} max and V_{IL-HPD} min
$V_{OH-HPDB}$	HPD_sink Output High-Level	2.5		V_{DD}	V	V_{DD} = 3.3V ± 10%
$V_{OL-HPDB}$	HPD_sink Output Low-Level	0		0.02	V	
T_{HPD}	HPD_sink to HPD_source propagation delay			200	ns	Time from HPD_sink changing state to HPD_source changing state. Includes HPD_source rise/fall time
$T_{RF-HPDB}$	HPD_source rise/fall time	1		20	ns	Time required to transition from $V_{OH-HPDB}$ to $V_{OL-HPDB}$ or from $V_{OL-HPDB}$ to $V_{OH-HPDB}$

OE# Input

Symbol	Parameter	Min	Nom	Max	Units	Comments
V_{IH}	Input High Level	2.0		V_{DD}	V	TMDS enable input changes state on cable plug/unplug
V_{IL}	Input Low Level	0		0.8	V	
I_{IN}	Input Leakage Current			10	µA	Measured with input at V_{IH-EN} max and V_{IL-EN} min

Termination Resistors

Symbol	Parameter	Min	Nom	Max	Units	Comments
R_{HPD}	HPD_sink input pull-down resistor.	80K	100K	120K	Ω	Guarantees HPD_sink is LOW when no display is plugged in.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
DDC Pins (SCL_Source, SDA_Source, SCL_Sink, SDA_Sink)					
$V_{I(DDC)}$	Input voltage	GND		5.5	V

Symbol	Parameter	Min.	Typ.	Max.	Units
I²C Pins (SCL_Sink, SDA_Sink)					
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage	-0.5		0.8	V

Symbol	Parameter	Min.	Typ.	Max.	Units
I²C Pins (SCL_Source, SDA_Source)					
V_{IH}	High-level input voltage	1.4		3.3	V
V_{IL}	Low-level input voltage	-0.5		0.6	V
V_{ICL}	Low-level input voltage contention (1)	-0.5		0.4	V

Notes:
1. V_{IL} specification is for the first low level seen by the SCL_Source/SDA_Source lines. V_{ICL} is for the second and subsequent low levels seen by the SCL_Source/SDA_Source lines.

Electrical Characteristics (over recommended operating conditions unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Units
I²C Pins (SCL_Source, SDA_Source)						
$\|I_{ikg}\|$	Input leakage current	V_I = 5.5 V	-50		50	µA
		$V_I = V_{DD}$	-10		10	
$\|I_{OH}\|$	High-level output current	V_O = 3.6 V	-10		10	µA
$\|I_{IL}\|$	Low-level input current	V_{IL} = GND	-40		40	µA
V_{OL}	Low-level output voltage	I_{OL} = 0.8 mA IADJ = H	0.4		0.85	V
C_{IO}	Input/output capacitance	V_I = 5.0 V or 0 V, Freq = 100kHz			25	pF
		V_I = 3.0 V or 0 V, Freq = 100kHz			10	
$V_{OH(TTL)}$[1]	TTL High-level output voltage	I_{OH} = -8 mA	2.4			V
$V_{OL(TTL)}$[1]	TTL Low-level output voltage	I_{OL} = 8 mA			0.4	V
I²C Pins (SCL_Sink, SDA_Sink Port)						
$\|I_{ikg}\|$	Input leakage current	V_I = 5.5 V	-50		50	µA
		$V_I = V_{DD}$	-10		10	
$\|I_{OH}\|$	High-level output current	V_O = 3.6 V	-10		10	µA
$\|I_{IL}\|$	Low-level input current	V_{IL} = GND	-10		10	µA
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, IADJ = H			0.2	V
C_I	Input capacitance	V_I = 5.0 V or 0 V, Freq = 100kHz			25	pF
		V_I = 3.0 V or 0 V, Freq = 100kHz			10	

Note:
1. Voh/Vol of external driver at the Source and Sink ports.

Switching Characteristics

I²C PINS (Source and Sink)						
Symbol	**Parameter**	**Test Conditions**	**Min.**	**Typ.(1)**	**Max.**	**Units**
t_{PLH}	Propagation delay time, low-to-high-level output SCL_Source/SDA_Source to SCL_Sink/SDA_Sink	IADJ = V_{DD} C_{LOAD} = 300 pF			500	ns
t_{PHL}	Propagation delay time, high-to-low-level output SCL_Source/SDA_Source to SCL_Sink/SDA_Sink	Tbuffer : Rpu = 2K, Vpu = 3.3V			136	
t_{PLH}	Propagation delay time, low-to-high-level output SCL_Sink/SDA_Sink to SCL_Source/SDA_Source	Rbuffer : Rpu = 1.2K, Vpu = 3.3V or Rpu = 1.8K, Vpu = 5V IADJ = GND C_{LOAD} = 100 pF			450	
t_{PHL}	Propagation delay time, high-to-low-level output SCL_Sink/SDA_Sink to SCL_Source/SDA_Source				136	
t_r	SCL_Source/SDA_Source Output signal rise time	See Fig. A			999	
t_f	SCL_Source/SDA_Source Output signal fall time				90	
t_r	SCL_Sink/SDA_Sink Output signal rise time				999	
t_f	SCL_Sink/SDA_Sink Output signal fall time				90	
t_{set}	Enable to start condition	See figure 9		6	10	
t_{hold}	Enable after stop condition			6	10	

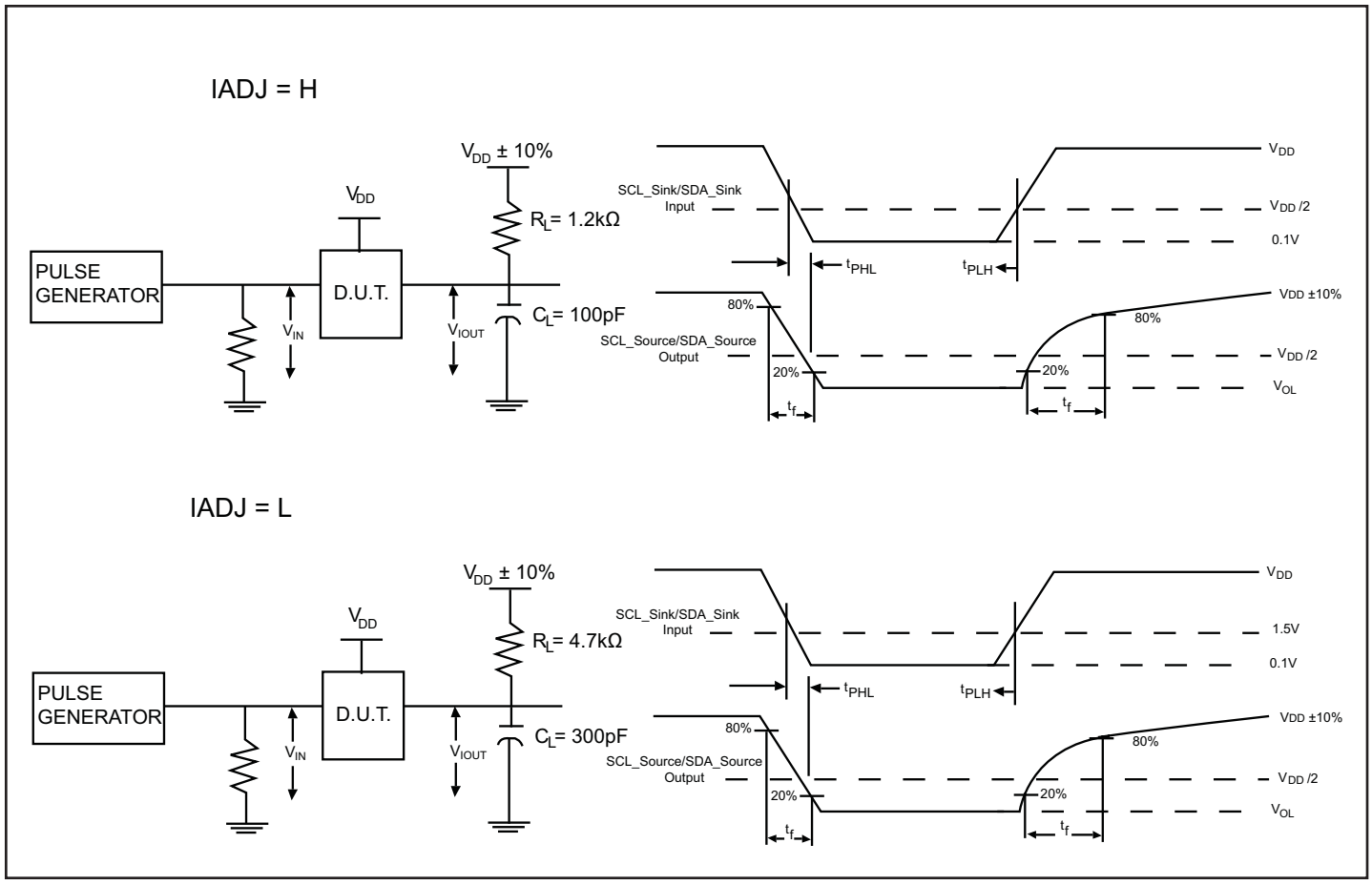


Figure A. I²C Timing Test Circuit and Definition

Recommended Power Supply Decoupling Circuit

Figure 1 is the recommended power supply decoupling circuit configuration. It is recommended to put 0.1µF decoupling capacitors on each V_{DD} pins of our part, there are four 0.1µF decoupling capacitors are put in Figure 1 with an assumption of only four V_{DD} pins on our part, if there is more or less V_{DD} pins on our Pericom parts, the number of 0.1µF decoupling capacitors should be adjusted according to the actual number of V_{DD} pins. On top of 0.1µF decoupling capacitors on each V_{DD} pins, it is recommended to put a 10µF decoupling capacitor near our part's V_{DD}, it is for stabilizing the power supply for our part. Ferrite bead is also recommended for isolating the power supply for our part and other power supplies in other parts of the circuit. But, it is optional and depends on the power supply conditions of other circuits.

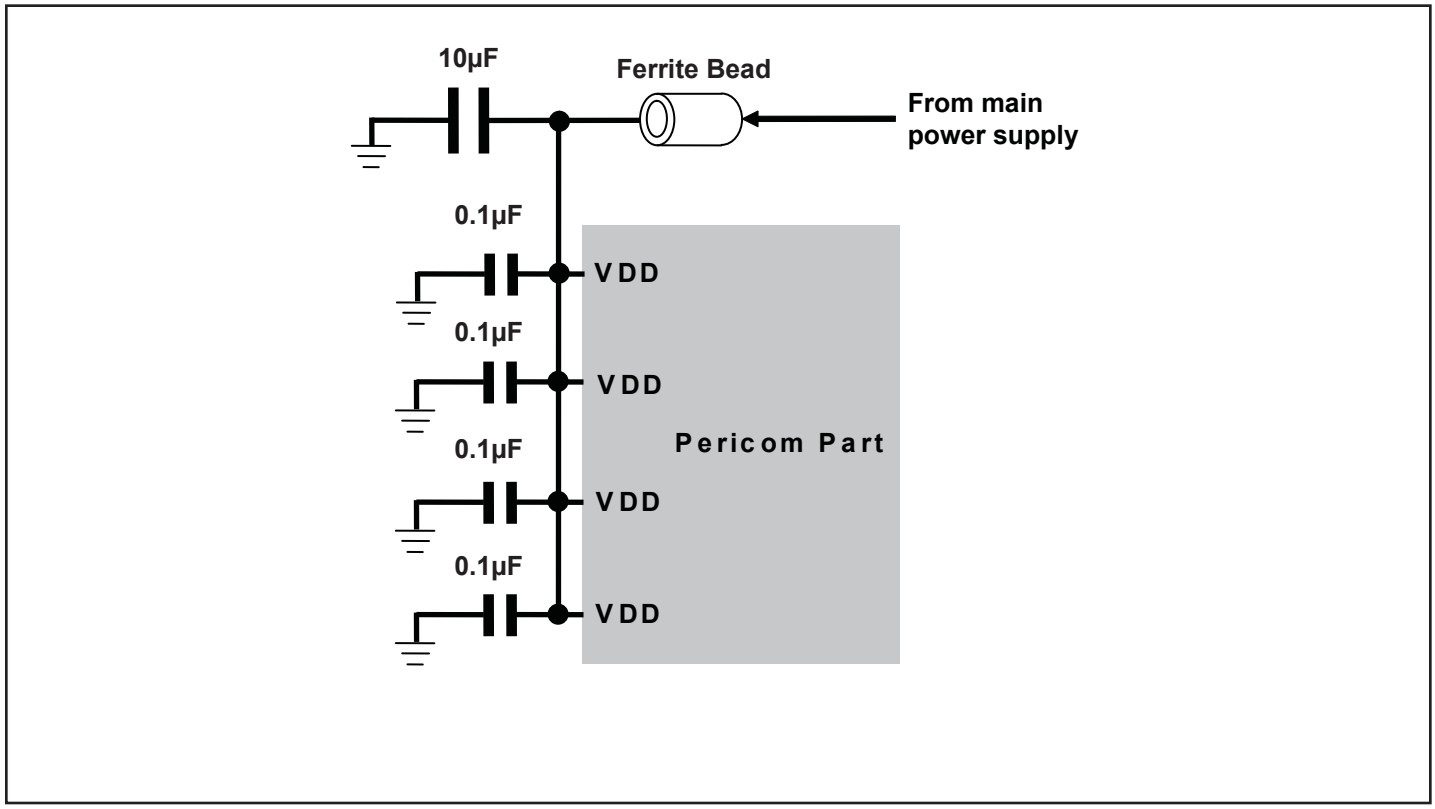


Figure 1 Recommended Power Supply Decoupling Circuit Diagram

Requirements on the Decoupling Capacitors

There is no special requirement on the material of the capacitors. Ceramic capacitors are generally being used with typically materials of X5R or X7R.

Layout and Decoupling Capacitor Placement Consideration

i. Each 0.1µF decoupling capacitor should be placed as close as possible to each V_{DD} pin.
ii. V_{DD} and GND planes should be used to provide a low impedance path for power and ground.
iii. Via holes should be placed to connect to V_{DD} and GND planes directly.
iv. Trace should be as wide as possible
v. Trace should be as short as possible.
vi. The placement of decoupling capacitor and the way of routing trace should consider the power flowing criteria.
vii. 10µF capacitor should also be placed closed to our part and should be placed in the middle location of 0.1µF capacitors.
viii. Avoid the large current circuit placed close to our part; especially when it is shared the same V_{DD} and GND planes. Since large current flowing on our V_{DD} or GND planes will generate a potential variation on the V_{DD} or GND of our part.

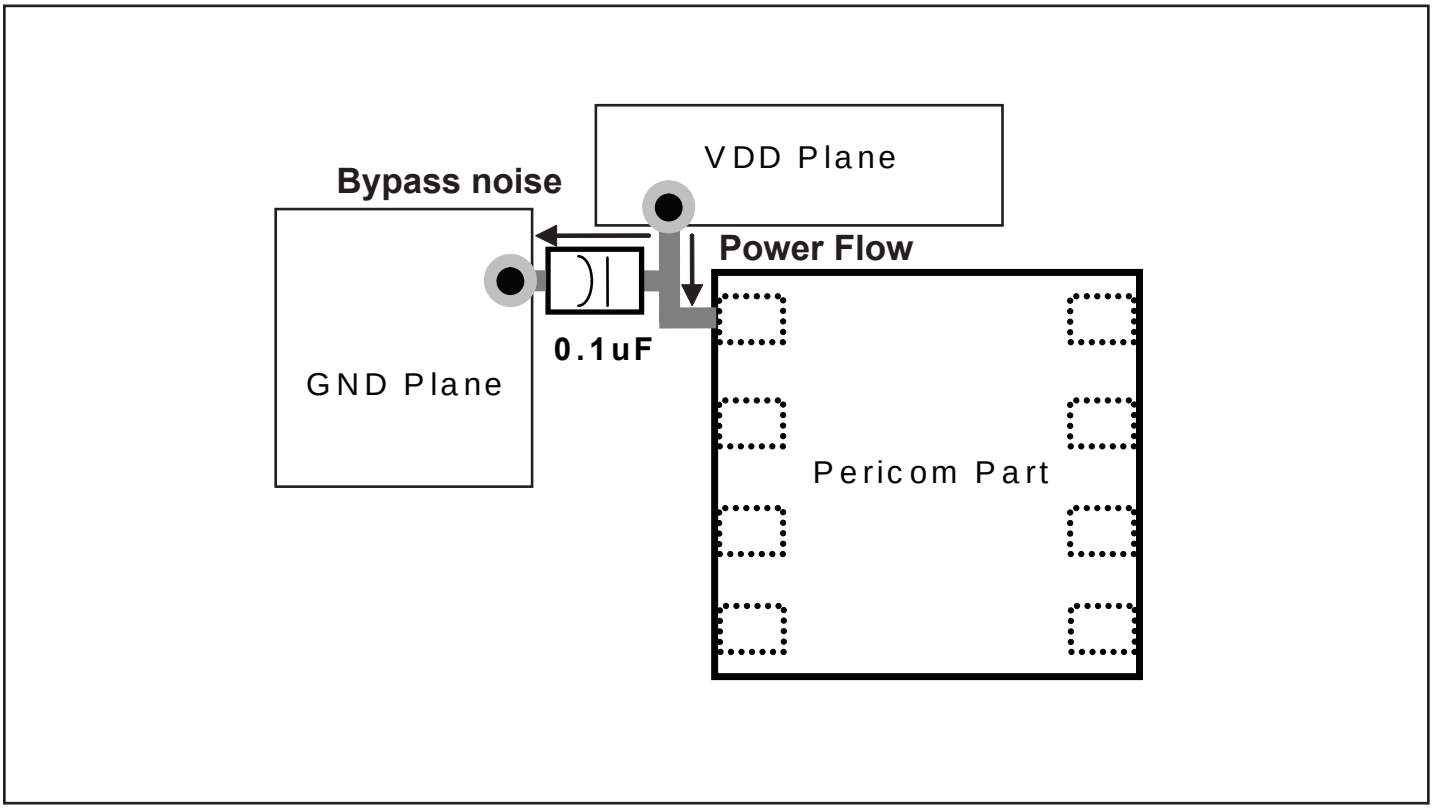
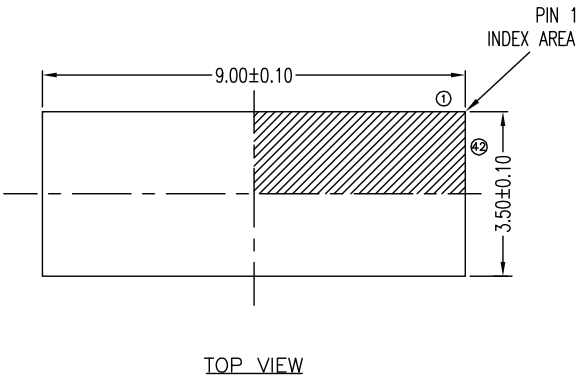
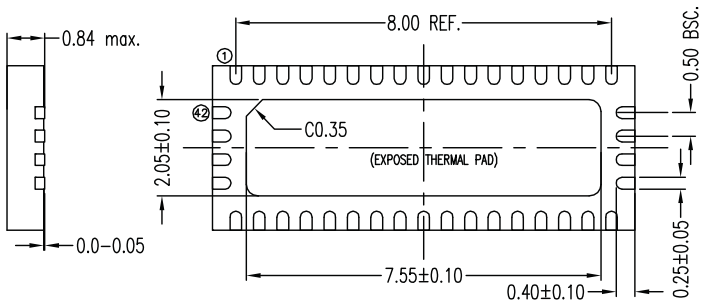


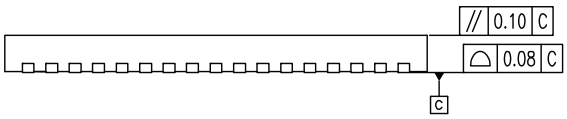
Figure 2 Layout and Decoupling Capacitor Placement Diagram

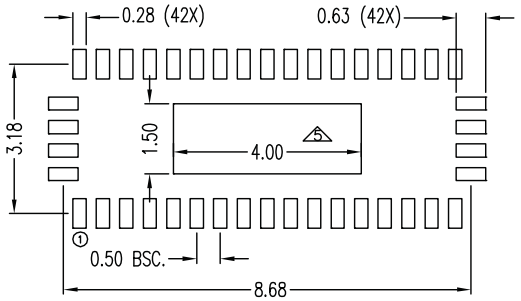


TOP VIEW



BOTTOM VIEW





RECOMMENDED LAND PATTERN (TOP VIEW)

Notes:
1. All dimensions are in millimeters, angles in degrees.
2. Coplanarity applies to the exposed thermal pad as well as the terminals.
3. Refer JEDEC MO-220
4. Recommended Land Pattern is for reference only.
5. Thermal Pad Soldering Area

PERICOM Semiconductor Corporation

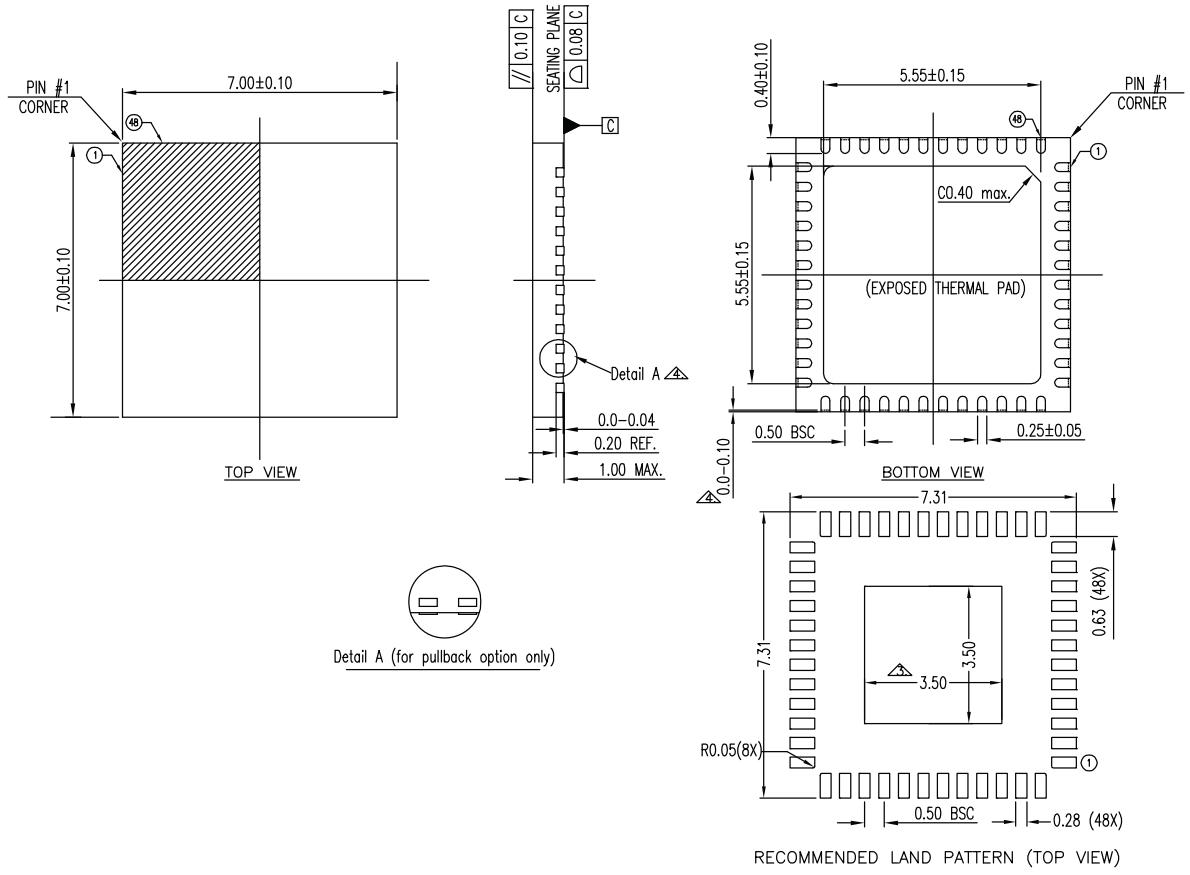
DATE: 02/17/09

DESCRIPTION: 42-contact Thin Fine Pitch Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZH (ZH42)

DOCUMENT CONTROL #: PD-2035 **REVISION: C**

09-0116



Notes:
1. All dimensions are in millimeters, angles are in degrees.
2. Refer JEDEC MO-220/VKKD
3. Thermal Pad Soldering Area
4. Depending on the method of lead termination at the edge of the package, pull back maybe present.
5. Recommended Land Pattern is for reference only.

PERICOM Semiconductor Corporation — DATE: 02/12/09

DESCRIPTION: 48-Contact, Thin Fine Pitch Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZD (ZD48)

DOCUMENT CONTROL #: PD-2045 REVISION: D

09-0117

Note:
- For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information

Ordering Code	Package Code	Package Description
PI3VDP101LSZHE	ZHE	42-contact Pb-free & Green, TQFN
PI3VDP101LSZDE	ZDE	48-contact Pb-free & Green, TQFN

Notes:
- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- Adding an X Suffix = Tape/Reel