To our customers,

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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

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The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M66242P/FP

4-CH 12-BIT PWM GENERATOR

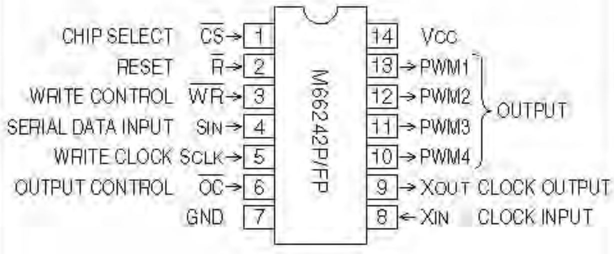
DESCRIPTION

M66242 Integrated Circuit has four 12-bit PWM (pulse width modulation) circuits which are built by using the CMOS (complementary metal oxide semiconductor) process.
This IC controls PWM waveform by adjusting the "H" width according to serial data sent from MCU (micro controller unit) or other device. Each channel can be independently controlled.
High-resolution digital-analog converter can be formed easily by connecting a low-pass filter circuit to the output pins of this circuit.

FEATURES

- Built-in four 12-bit high-resolution pulse width modulation circuits
- Easy digital-analog conversion – Quick output waveform smoothing
  Control by 1.22mV possible per step (V_{CC} =5V)
- Serial data input
- "H" level width setting type
- 4 independently controlled channels
- All 4 channels reset by reset input ($\overline{R}$) High-impedance status after reset
- All 4 channels controlled by output control input ($\overline{OC}$)
- Settings take effect after ongoing cycle is completed
- Input: TTL level
- Output: CMOS 3-state output
  Output current I_O = ±4mA
- V_{CC} =5V ± 10%

PIN CONFIGURATION (TOP VIEW)

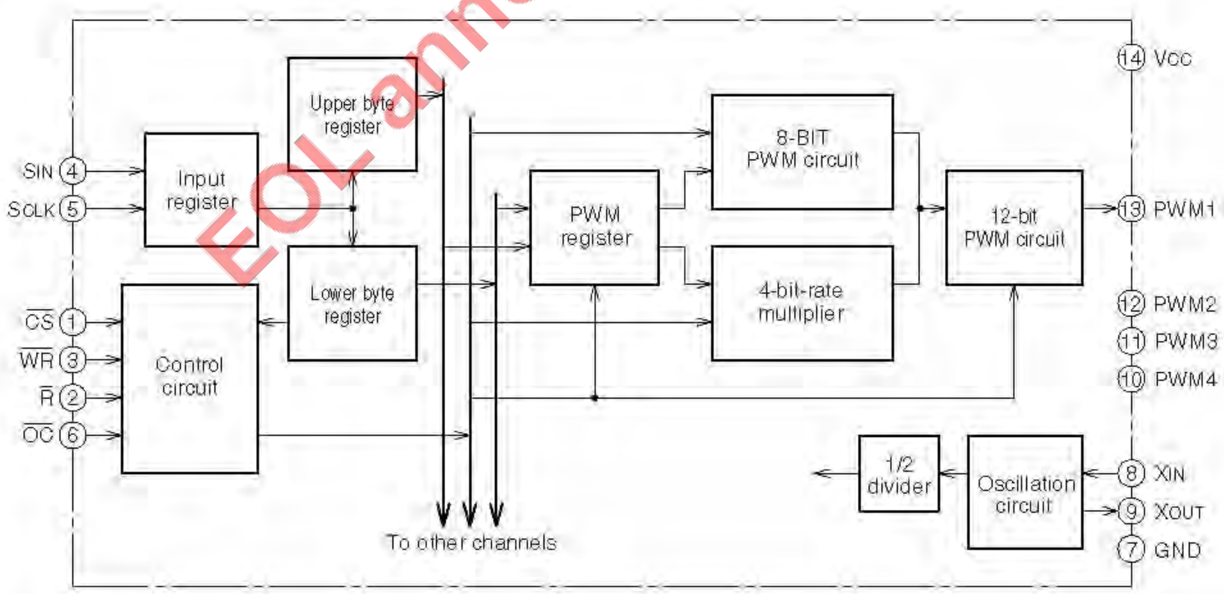


Outline 14P4
14P2N-A

APPLICATION

- Analog signal control in televisions and audio systems
- Control of lamps, heaters and motors
- For software servo in home appliances and industrial machinery

BLOCK DIAGRAM (EACH CHANNEL)



FUNCTION

The PWM output waveform of each channel is controlled by taking in PWM data from MCU or other device via serial data input SIN.
Twelve-bit PWM data is input being divided between upper 8 bits (upper byte) and lower 4 bits.
The lower 4-bit data is combined with command data such as channel designation and input as 8-bit data (lower byte).
The lower byte should be written first, and then the upper byte. Even if only the upper byte is to be changed, rewrite from the lower byte.
The PWM waveform changes according to the new setting from the next cycle.
One cycle of PWM waveform (4096 divisions; 12-bit resolution) are divided into 16 (2^4) subsections t. Each subsection consists of 256 (2^8; 8-bit resolution) minimum bits τ (=2/fXIN**).
One subsection t consists of a 8-bit PWM waveform (basic waveform). The "H" width of this waveform is determined according to the upper 8 bits of PWM data. One cycle has 16 subsections t, each of which has this basic waveform. Among them, those which are designated by the 4-bit-rate multiplier are conditioned to have a "H" width that is longer by τ. The lower 4 bits of PWM data are used to specify those subsections (t_m). The waveform of other subsections remains unchanged.
A PWM waveform (12-bit resolution) is a combination of two types of waveforms which are different in "H" width, as described above.
When output control input $\overline{OC}$ is "H", the output of every channel turns high-impedance from the next cycle.
When reset input $\overline{R}$ is "L", the output of every channel turns high-impedance as soon as the ongoing cycle is completed, and PWM data of all channels is reset. If $\overline{R}$ input is changed from "L" to "H", the next cycle starts, however, the output of the channels remains high-impedance.
To enable output, rewrite input data for each channel.

**)fXIN: Clock XIN repeat frequency

PIN DESCRIPTIONS

Pin	Name	Input/Output	Functions
$\overline{R}$	Reset input	Input	"L": All 4 channels put in high impedance state.
$\overline{CS}$	Chip select input	Input	"L": Communication with MCU becomes possible. $\overline{WR}$, SIN and SCLK put in enable state.
$\overline{WR}$	Write control input	Input	"L": Serial data written "L"-to-"H" edge: Written data stored in upper or lower byte.
SIN	Serial data input	Input	Inputs 8-bit serial data from MCU synchronously with clock pulses.
SCLK	Write clock input	Input	Inputs sync clock pulses for 8-bit serial data writing.
$\overline{OC}$	Output control input	Input	"H": All 4 channels put in high-impedance state.
PWM1~PWM4	PWM outputs 1 thru 4	Output	Outputs PWM waveform. (CMOS 3-state output)
XIN	Clock input	Input	Inputs/outputs signals generated by clock signal generation circuit. Oscillation frequency is determined by connecting ceramic or quartz resonator between XIN and XOUT. The frequency of internal clock (PWM timing clock) signals is the 1/2 divider of the frequency input from clock input XIN. When external clock signals are used, connect clock generator to XIN pin and leave XOUT open.
XOUT	Clock output	Output	

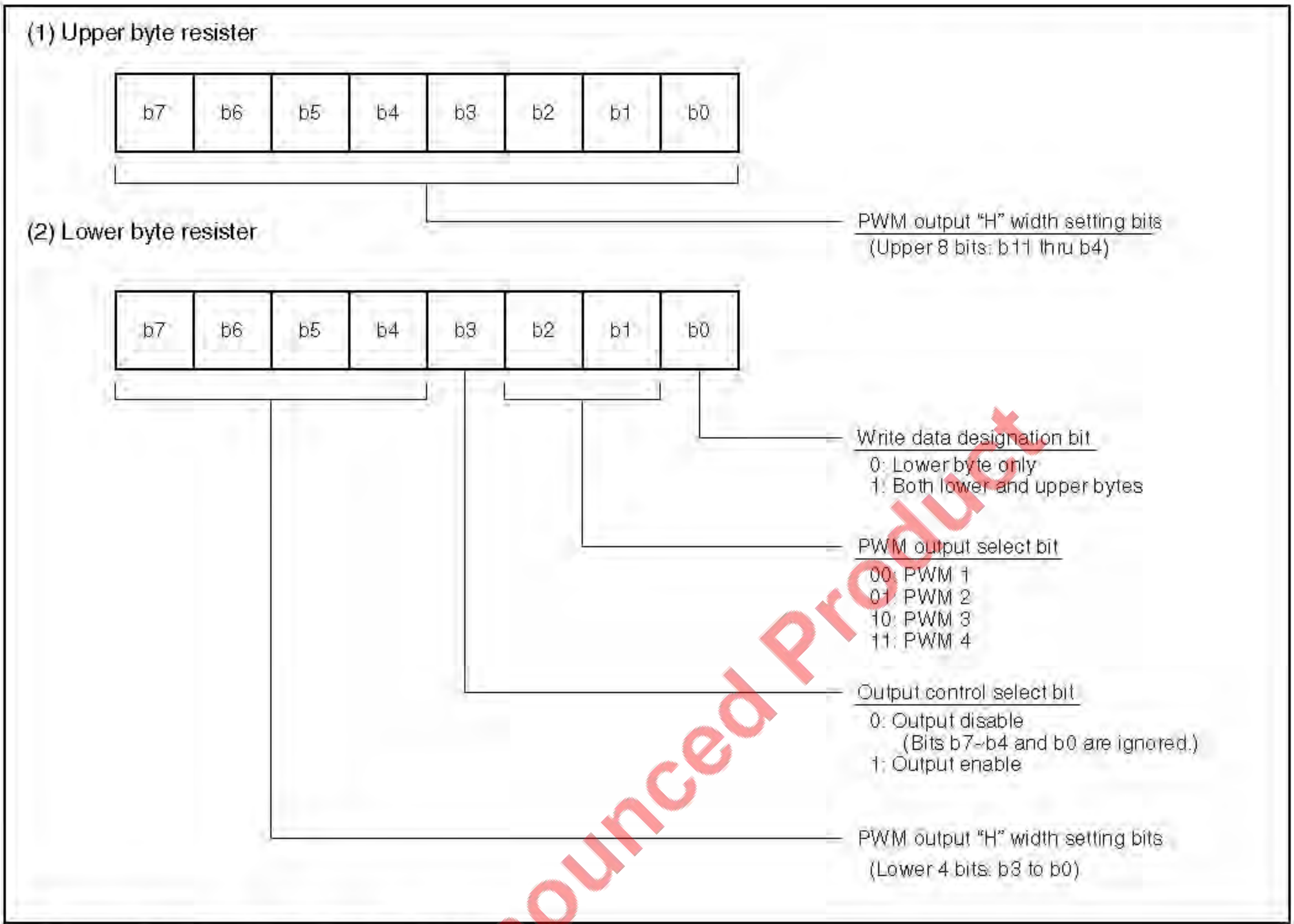


Fig. 1 Upper and Lower Byte Resister Makeup

Table 1 Mode Selection

Mode		Input serial data: Lower byte data	Input serial data: Upper byte data
PWM data setting (output enable)	Lower 4-bit data setting	b7 b6 b5 b4 1 b2 b1 0	——
	12-bit data setting	b7 b6 b5 b4 1 b2 b1 1	b7 b6 b5 b4 b3 b2 b1 b1
Output disable		X X X X 0 b2 b1 X	——

Table 2 Patterns of Lower 4 Bits and Subsections Whose "H" Width Is Increased

PWM register b3-b0	Subsections t_m whose H width is increased by τ (m =0 thru 15)	Number of Subsections
0000	Nothing	0
0001	m=8	1
0010	m=4, 12	2
0100	m=2, 6, 10, 14	4
1000	m=1, 3, 5, 7, 9, 11, 13, 15	8
1111	m=1~15 (m≠0)	15

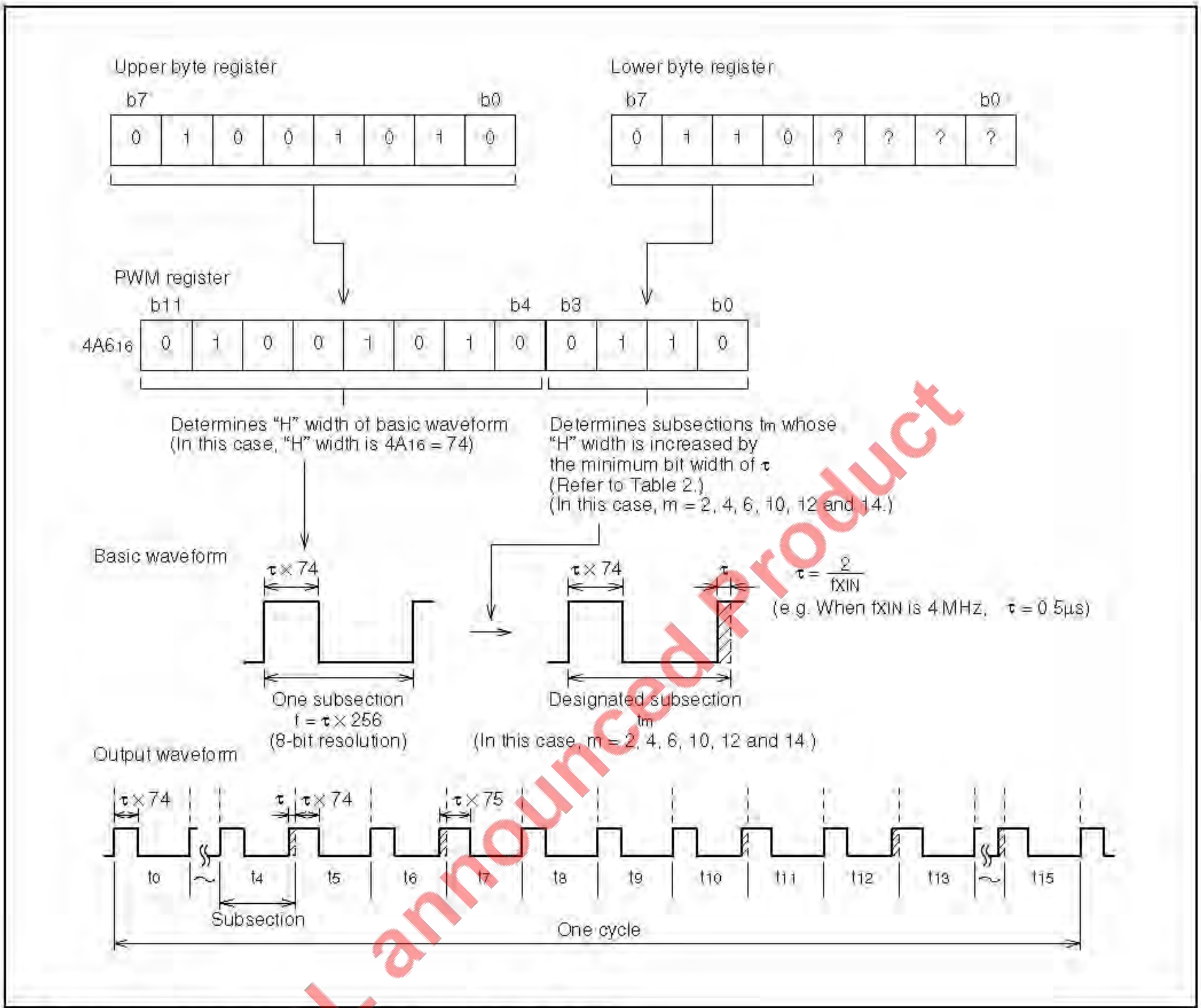


Fig. 2 PWM Waveform Output Example (Input data: 4A6 16)

OPERATION

Serial Data Input

When chip select $\overline{CS}$ is "L" and write control input $\overline{WR}$ is "L", data input to S_{IN} at the edge where write clock input S_{CLK} status shifts from "L" to "H" is written. (See Fig. 3.)
At the edge where $\overline{WR}$ rises from "L" to "H", the latest 8-bit data writing is completed, and input data is stored in lower (or upper) byte register. When writing on the lower byte or writing on both upper and lower bytes is completed, data on the lower byte register or, in the latter case, data on both lower and upper byte registers is written on the PWM register of the channel designated by lower bytes b2 and b1. All setting process ends with this writing, and PWM waveform changes according to the setting from the next cycle.

PWM Waveform Output

(1) 12-bit PWM output

One PWM waveform cycle is divided into 16(2^4) subsections t, and each subsection is further divided into 256 (2^8) minimum resolution bits τ (= $2/f_{XIN}$)
The "H" width of subsection t basic waveform is determined by the upper 8 bits of PWM data.
(In Fig. 2 above, "H" width is $4A_{16}$ = 74 × τ)
Among these 16 subsections t, subsections t_m designated by the lower 4 bits of PWM data have "H" width that is longer by τ.
[In Fig. 2 above, the "H" width of designated 6 subsections (m =2, 4, 6, 10, 12 and 14) is $4B_{16}$ = 75 × τ.]

The "H" width of undesignated subsections remains unchanged.

As explained above, one cycle of waveform is a combination of two waveforms different in the "H" width.

(In Fig. 2 above, one cycle consists of 10 subsections whose H width is $74 \times \tau$ and 6 subsections whose "H" width is $75 \times \tau$.)

Note: It is impossible to set one whole cycle to "H" level.

(2) 8-bit PWM output

As can be seen from the 12-bit PWM waveform output process as described above, 8-bit resolution PWM waveform can be output by fixing the lower 4 bits of PWM data to 0000_2.

All subsections from t_{10} to t_{15} have the "H" width as determined by the upper 8 bits of PWM data.

Note: It is impossible to set one whole cycle to "H" level.

Output Control

(1) Serial data input

By using data on lower byte register b3 (output control selection bit), output of each channel can be controlled independently. The state of the selected PWM output changes after the completion of the ongoing cycle.

When b3 is set 0, lower byte register b0 (write data designation bit) is reset. Do not write on upper byte in this case.

(2) Output control input

The status of all 4 channel outputs during a cycle is determined depending on the status of output control input $\overline{OC}$ at the start of the cycle. (See Fig. 6.)

Even when output is in a high-impedance state, data on each PWM register is retained, and data can be rewritten.

(3) Reset

When reset input $\overline{R}$ turns "L", all operation is reset as soon as the ongoing cycle is completed: The outputs of all 4 channels turns high-impedance. The PWM register of each channel is reset.

When $\overline{R}$ is shifted from "L" to "H", a next cycle starts, and data writing becomes possible. However, outputs stay in the high-impedance state. (See Fig. 6.)

To resume output, write input data for each channel.

Initial State

After power-on, outputs and PWM register data are unstable.

(1) Reset

Reset input $\overline{R}$ is kept on "L" level for more than one cycle (2.048ms when f_{XIN} is 4 MHz) or more, this integrated circuit is put in a reset state.

If stabilization needs more time, e. g. when a quartz resonator is used, keep $\overline{R}$ on "L" level for an adequate period of time.

(2) Serial data input

When starting using this integrated circuit without resetting, input false lower byte data (b0 =0) to stabilize lower byte register b0 data, and then input normal data.

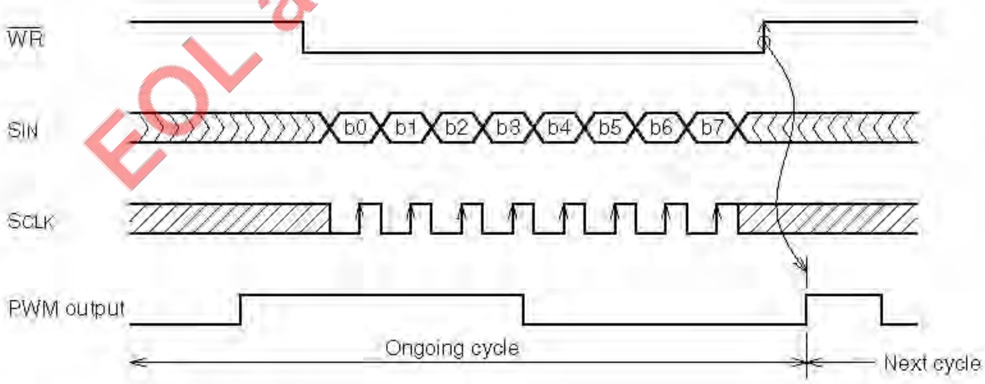


Fig. 3 Serial Data Write Timing

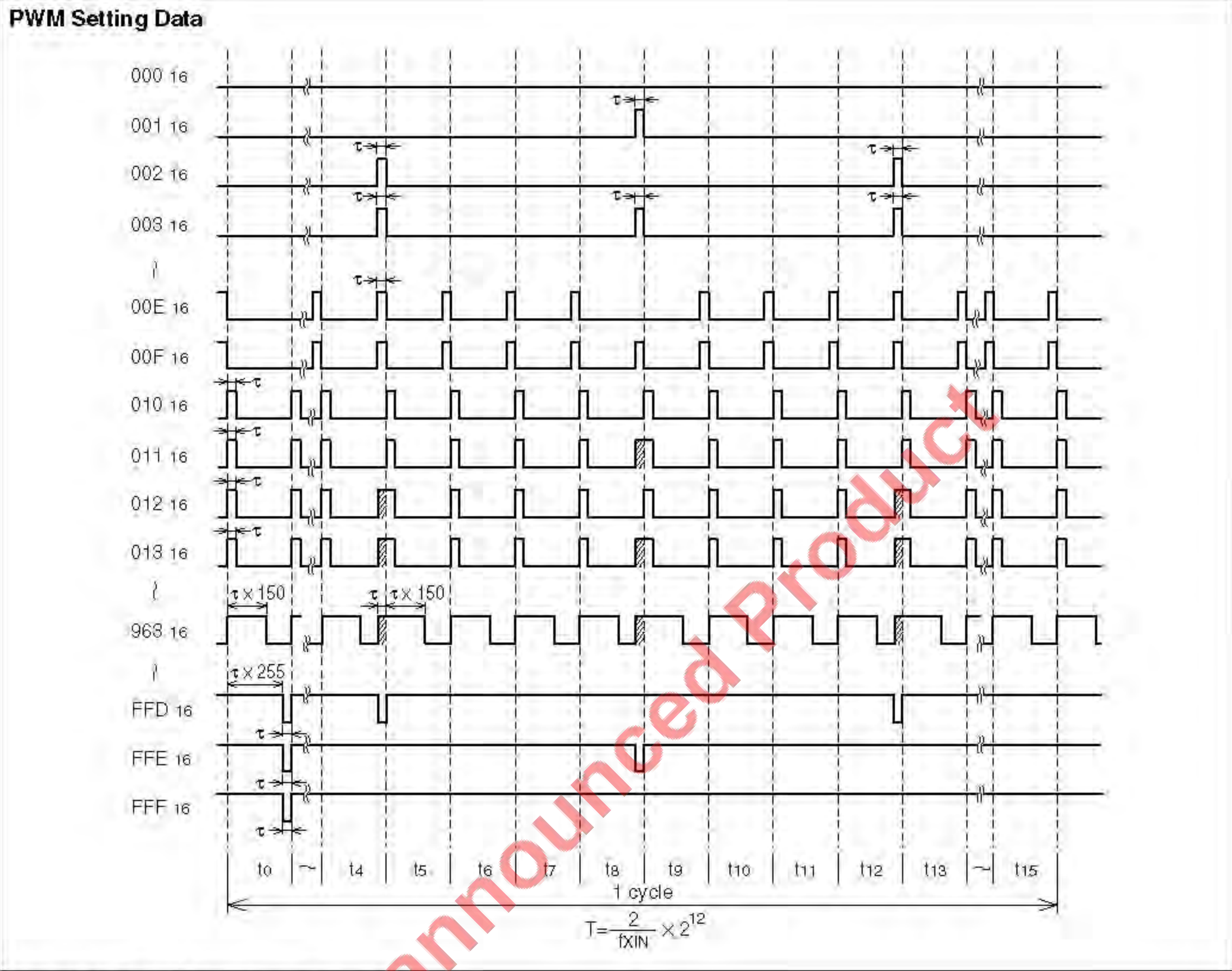


Fig. 4 12-bit PWM Waveform Output Example

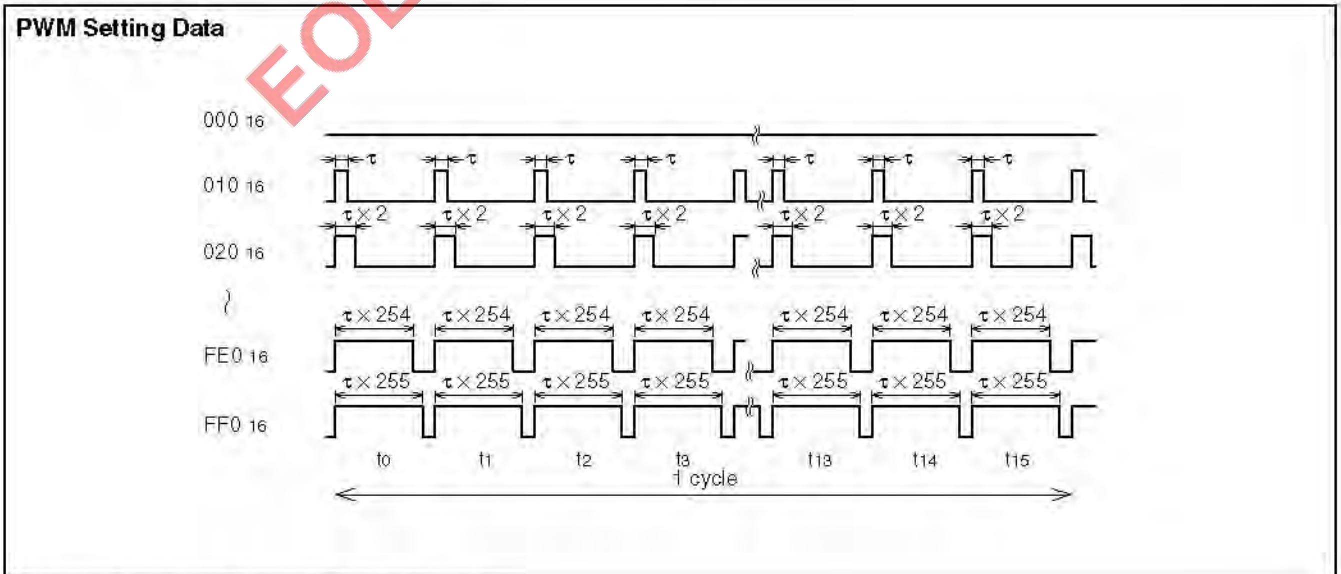


Fig. 5 8-bit PWM Waveform Output Example

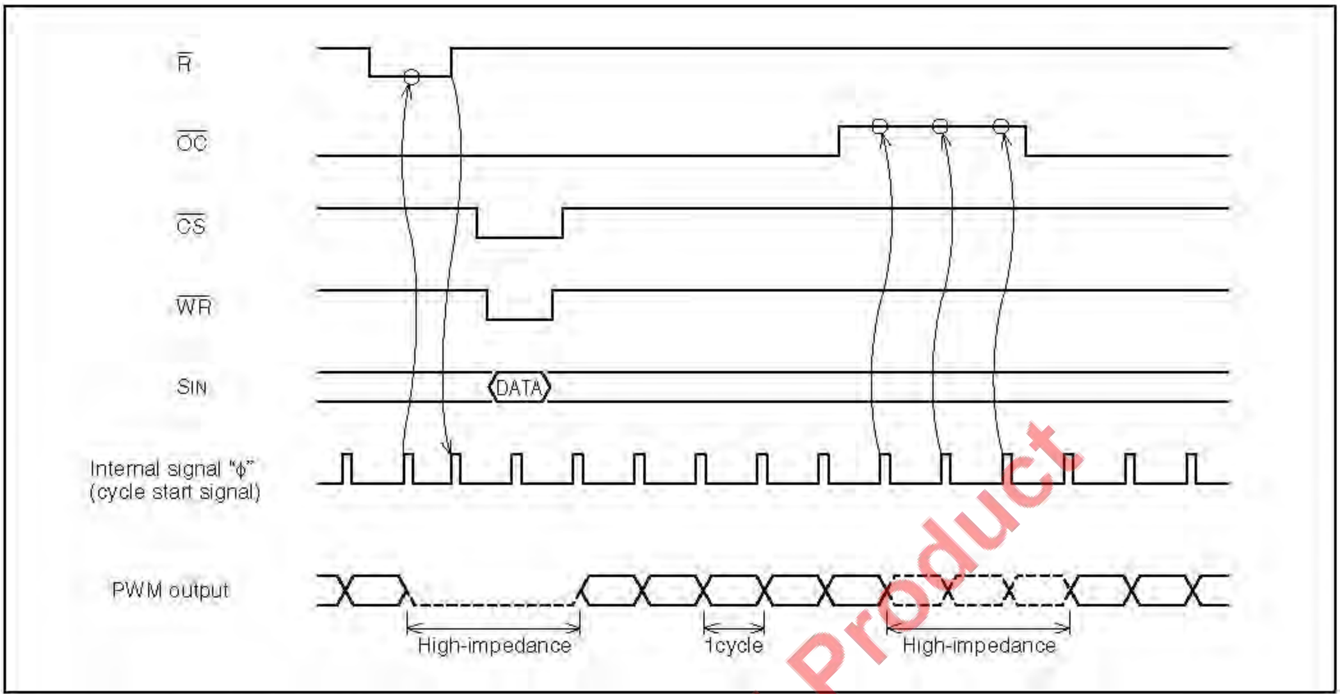


Fig. 6 Output Control Timing Chart

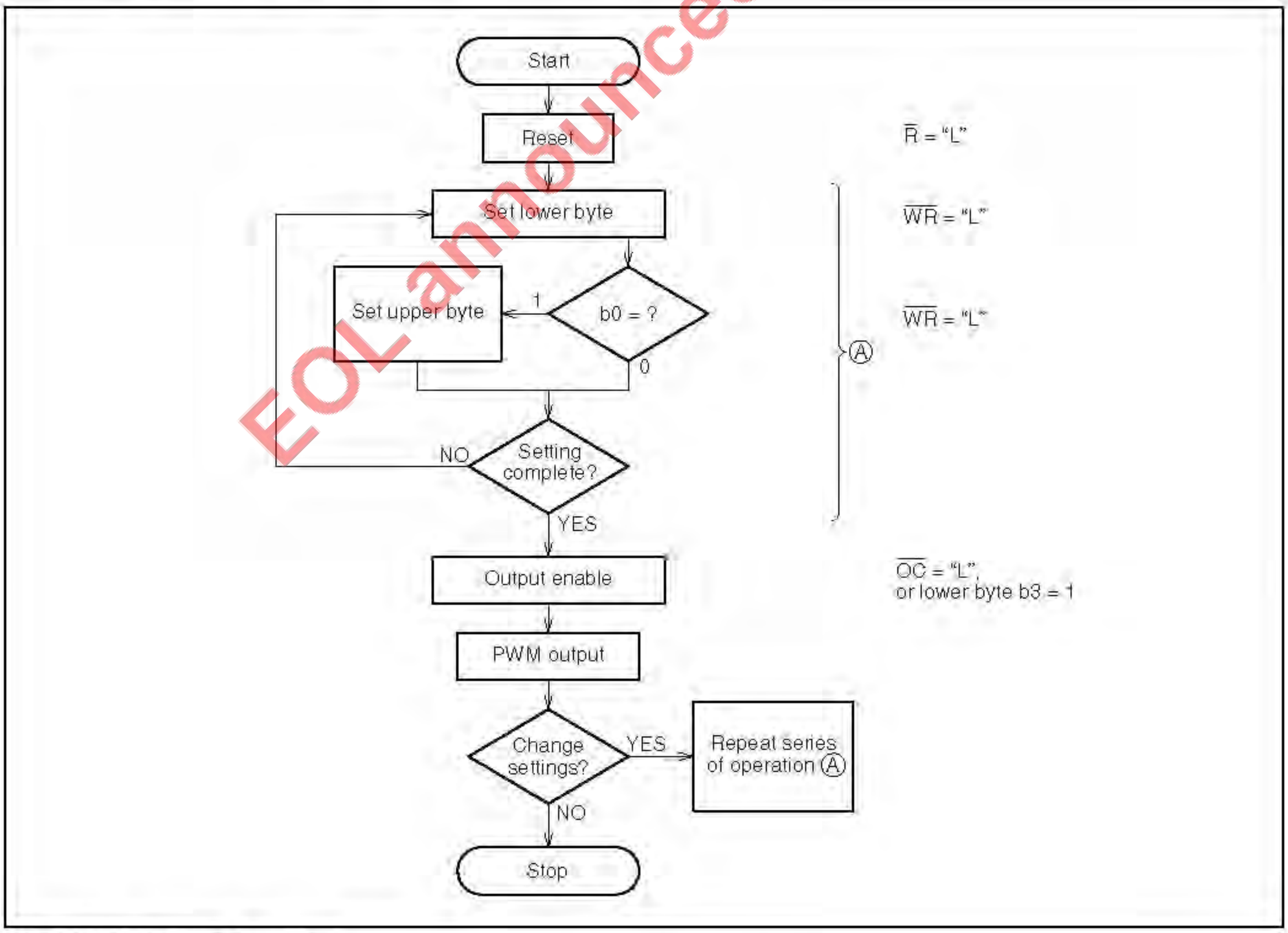


Fig. 7 PWM Setting Flow Chart

ABSOLUTE MAXIMUM RATINGS (Ta = –20°C ~ 75°C unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		–0.5 ~ +7.0	V
V_I	Input voltage		–0.5 ~ V_{CC} + 0.5	V
V_O	Output voltage	When output is "H" or under high-impedance condition	–0.5 ~ V_{CC} + 0.5	V
I_{IK}	Input protection diode current	V_I<0V	–10	mA
		V_I>V_{CC}	10	
I_{OK}	Output parasite diode current	V_O<0V	–10	mA
		V_O>V_{CC}	10	
I_O	Output current		±15	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±40	mA
P_d	Power dissipation		150	mW
T_{stg}	Storage temperature		–65 ~ 150	°C

RECOMMENDED OPERATIONAL CONDITIONS

Symbol	Parameter		Limits			Unit
			Min	Typ.	Max.	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	"H" Input voltage	XIN	0.8V_{CC}		V_{CC}	V
		Other input	2.0		V_{CC}	V
V_{IL}	"L" Input voltage	XIN	0		0.2V_{CC}	V
		Other input	0		0.8	V
I_{OH}	"H" Output current	PWM1~4 V_{OH}≥V_{CC}–0.8	0		–4	mA
I_{OL}	"L" Output current	PWM1~4 V_{OL}≤0.5	0		4	mA
T_{opr}	Ambient temperature		–20		75	°C

ELECTRICAL CHARACTERISTICS (Ta = –20°C ~ 75°C, V_{CC} = 5V±10% unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" Output voltage	PWM1~4	I_{OH}=–4mA	V_{CC}–0.8	4.7		V
V_{OL}	"L" Output voltage	PWM1~4	I_{OL}=4mA		0.2	0.5	V
I_{IH}	"H" Input current		V_I=V_{CC}			1.0	µA
I_{IL}	"L" Input current		V_I=GND			–1.0	µA
I_{OZH}	"H" output current under off condition		V_O=V_{CC}			5.0	µA
I_{OZL}	"L" output current under off condition		V_O=GND			–5.0	µA
I_{CC}	Power dissipation		V_I=V_{CC}, GND, I_O=0µA			40	µA
ΔI_{CC}	Maximum quiescent power dissipation		V_I=2.4, 0.4V (Note 1)		0.4	2.9	mA

Note 1: Only one input (excluding XIN) should be set to this voltage. Other inputs should be connected to VCC or GND.

SWITCHING CHARACTERISTICS (Ta = –20°C ~ 75°C, Vcc = 5V±10% unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.*	Max.	
fmax		XIN	CL=50pF (Note 2)	16	25		MHz
tPLH	Output "L"–"H", "H"–"L"	XIN			25	100	ns
tPHL		PWM1~4			25	100	ns

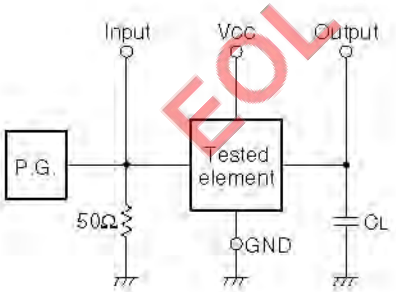
*: Standard values are measured under conditions of Vcc = 5V and Ta = 25°C.

TIMING CHARACTERISTICS (Ta = –20°C ~ 75°C, Vcc = 5V±10% unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.*	Max.	
tC(X)	XIN cycle time		62.5	40		ns
tW(XH)	XIN "H" pulse width		32.5	20		ns
tW(XL)	XIN "L" pulse width		30	10		ns
tW(S)	SCLK pulse width		30	5		ns
tWRH	$\overline{\text{WR}}$ "H" hold time		6tc (X)			ns
tsu(CS)	CS "L" setup time after $\overline{\text{WR}}$↓		30	10		ns
tsu(WR)	$\overline{\text{WR}}$ "L" setup time after SCLK↑		30	5		ns
tsu(S)	SIN setup time after SCLK↑		50	5		ns
th(CS)	CS "L" hold time after $\overline{\text{WR}}$↓		30	10		ns
th(WR)	$\overline{\text{WR}}$ "L" hold time after SCLK↑		10	5		ns
th(S)	SIN hold time after SCLK↑		10	5		ns
th(SCLK)	SCLK hold time after $\overline{\text{WR}}$↑		30	5		ns
tr	Input rise time				25	ns
tf	Input fall time				25	ns

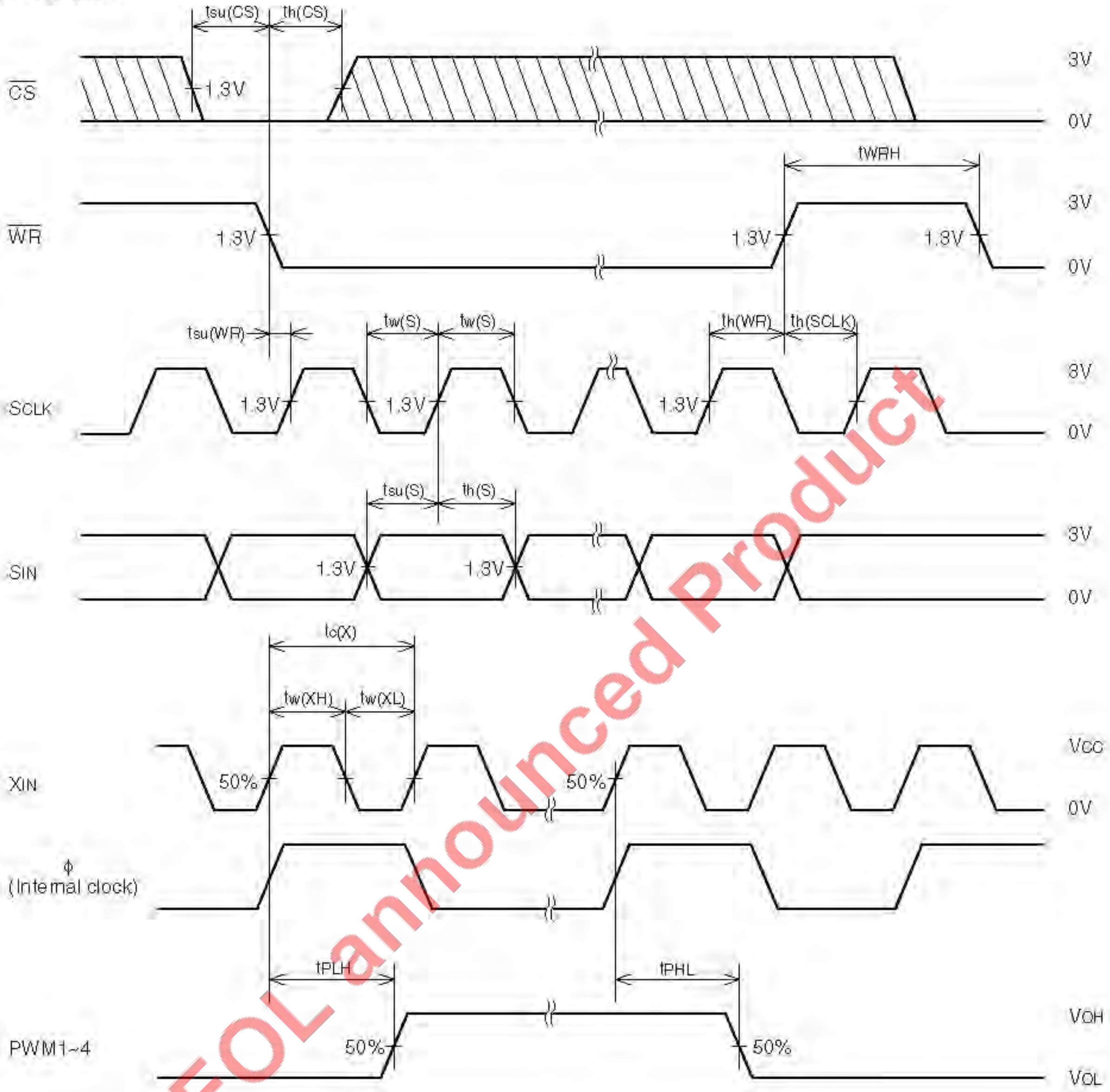
*: Standard values are measured under conditions of Vcc = 5V and Ta = 25°C.

NOTE 2: TEST CIRCUIT



(1) Pulse generator (PG) characteristics: tr=tf=6ns
(2) Capacitance CL includes connection floating capacitance and probe input capacitance.

TIMING CHARTS



Note 3:
(1) Shaded portions indicate that switching is possible during those periods.
(2) PWM outputs 1 to 4 change synchronously with internal clock signals ϕ. The frequency of these signals is the 1/2 divider of the frequency input from XIN.

APPLICATION EXAMPLE (Combination with electronic control M5283P for amplifier system)