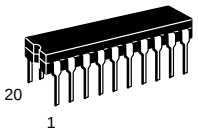
MC145442
MC145443

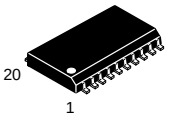
Single-Chip 300-Baud Modem

The MC145442 and MC145443 silicon–gate CMOS single–chip low–speed modems contain a complete frequency shift keying (FSK) modulator, demodulator, and filter. These devices are with CCITT V.21 (MC145442) and Bell 103 (MC145443) specifications. Both devices provide full–duplex or half–duplex 300–baud data communication over a pair of telephone lines. They also include a carrier detect circuit for the demodulator section and a duplexer circuit for direct operation on a telephone line through a simple transformer.

- MC145442 Compatible with CCITT V.21
- MC145443 Compatible with Bell 103
- Low–Band and High–Band Band–Pass Filters On–Chip
- Simplex, Half–Duplex, and Full–Duplex Operation
- Originate and Answer Mode
- Analog Loopback Configuration for Self Test
- Hybrid Network Function On–Chip
- Carrier Detect Circuit On–Chip
- Adjustable Transmit Level and $\overline{CD}$ Delay Timing
- On–Chip Crystal Oscillator (3.579 MHz)
- Single + 5 V Power Supply Operation
- Internal Mid–Supply Generator
- Power–Down Mode
- Pin Compatible with MM74HC943
- Capable of Driving – 9 dBm into a 600 Ω Load



P SUFFIX
PLASTIC DIP
CASE 738

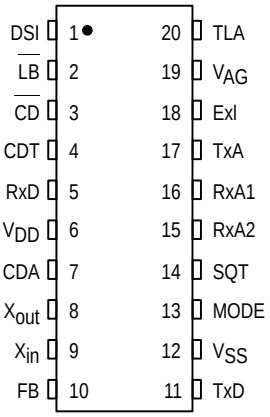


DW SUFFIX
SOG PACKAGE
CASE 751D

ORDERING INFORMATION

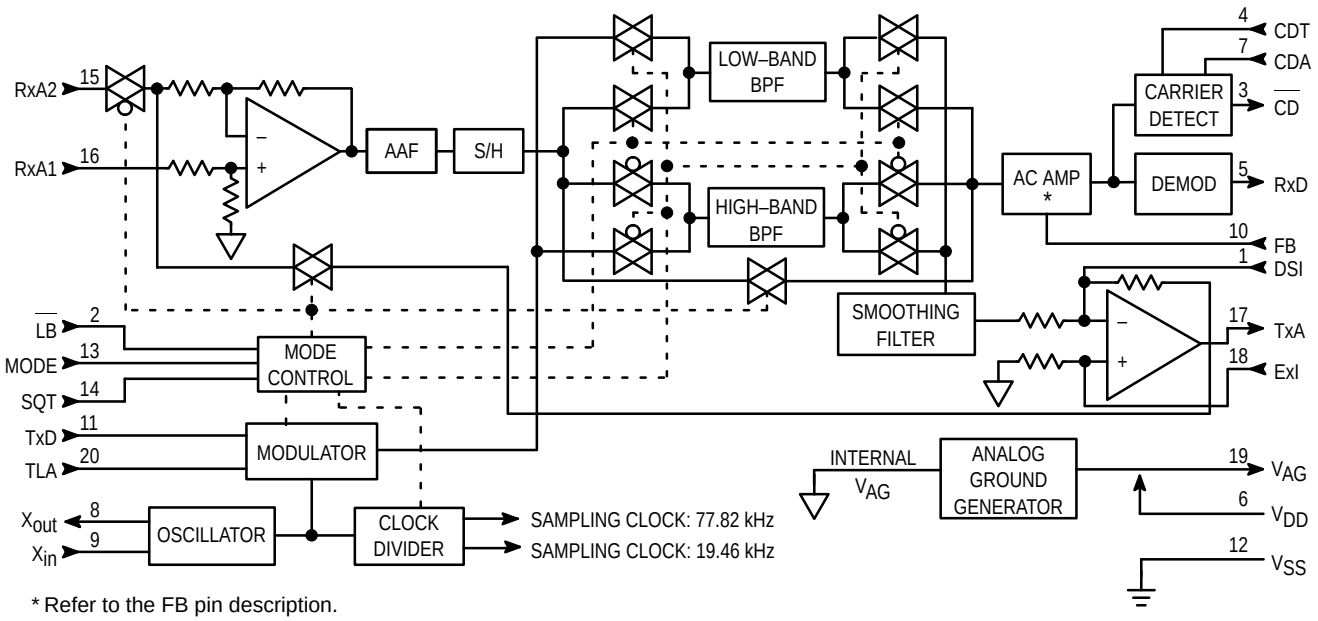
MC145442P	Plastic DIP
MC145443P	Plastic DIP
MC145442DW	SOG Package
MC145443DW	SOG Package

PIN ASSIGNMENT



REV 1
8/95

BLOCK DIAGRAM



* Refer to the FB pin description.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	– 0.5 to + 7.0	V
DC Input Voltage	V_{in}	– 0.5 to V_{DD} + 0.5	V
DC Output Voltage	V_{out}	– 0.5 to V_{DD} + 0.5	V
Clamp Diode Current, per Pin	I_{IK}, I_{OK}	± 20	mA
DC Output Current, per Pin	I_{out}	± 28	mA
Power Dissipation	P_D	500	mW
Operating Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	4.5	5.5	V
DC Input or Output Voltage	V_{in}, V_{out}	0	V_{DD}	V
Input Rise or Fall Time	t_r, t_f	—	500	ns
Crystal Frequency*	$f_{crystal}$	3.2	5.0	MHz

* Changing the crystal frequency from 3.579 MHz will change the output frequencies. The change in output frequency will be proportional to the change in crystal frequency.

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 V ± 10%, T_A = – 40 to + 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
High–Level Input Voltage	$\overline{LB}$ X_{in}, TxD, Mode, SQT	V_{IH}	V_{DD} – 0.8 3.15	— —	— —	V
Low–Level Input Voltage	$\overline{LB}$ X_{in}, TxD, Mode, SQT	V_{IL}	— —	— —	0.8 1.1	V
High–Level Output Voltage I_{OH} = 20 µA I_{OH} = 2 mA I_{OH} = 20 µA	 $\overline{CD}$, RxD CD, RxD X_{out}	V_{OH}	 V_{DD} – 0.1 3.7 —	 — — V_{DD} – 0.05	 — — —	V
Low–Level Output Voltage I_{OL} = 20 µA I_{OL} = 2 mA I_{OL} = 20 µA	 $\overline{CD}$, RxD CD, RxD X_{out}	V_{OL}	 — — —	 — — 0.05	 0.1 0.4 —	V
Input Current	$\overline{LB}$, TxD, Mode, SQT RxA1, RxA2 X_{in}	I_{in}	— — —	— 10 —	± 1.0 ± 12 ± 10	µA
Quiesent Supply Current (X_{in} or $f_{crystal}$ = 3.579 MHz)		I_{DD}	—	7	10	mA
Power–Down Supply Current			—	200	300	µA
Input Capacitance	X_{in} All Other Inputs	C_{in}	— —	10 —	— 10	pF
V_{AG} Output Voltage (I_O = ± 10 µA)		V_{AG}	2.4	2.5	2.6	V
CDA Output Voltage (I_O = ± 10 µA)		V_{CDA}	1.1	1.2	1.3	V
Line Driver Feedback Resistor		R_f	10	20	30	kΩ

AC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5.0 V ± 10%, T_A = – 40 to + 85°C, Crystal Frequency = 3.579 MHz ± 0.1%; See Figure 1)

Characteristic		Min	Typ	Max	Unit
TRANSMITTER					
Power Output on TxA R_L = 1.2 kΩ, R_{TLA} = ∞ R_L = 1.2 kΩ, R_{TLA} = 5.5 kΩ		 – 13 – 10	 – 12 – 9	 – 11 – 8	dBm
Second Harmonic Power R_L = 1.2 kΩ		—	– 56	—	dBm
RECEIVE FILTER AND HYBRID					
Hybrid Input Impedance RxA1, RxA2		40	50	—	kΩ
FB Output Impedance		—	16	—	kΩ
Adjacent Channel Rejection		– 48	—	—	dBm
DEMODULATOR					
Receive Carrier Amplitude		– 48	—	– 12	dBm
Dynamic Range		—	36	—	dB
Bit Jitter (S/N = 30 dB, Input = – 38 dBm, Bit Rate = 300 baud)		—	100	—	µs
Bit Bias		—	5	—	%
Carrier Detect Threshold (CDA = 1.2 V or CDA grounded through a 0.1 µF capacitor)	On to Off Off to On	— —	– 44 – 47	— —	dBm

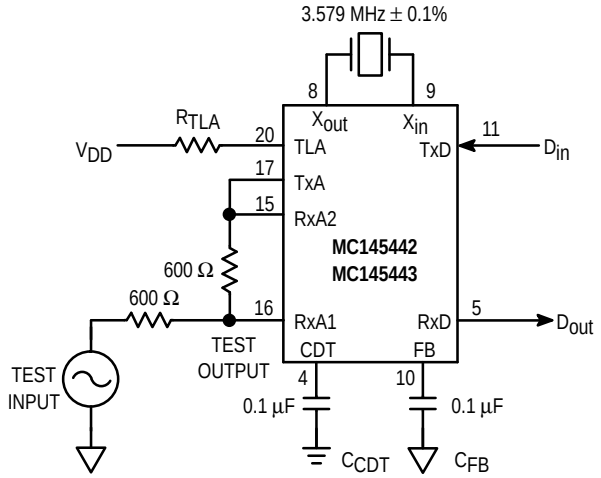


Figure 1. AC Characteristics Evaluation Circuit

PIN DESCRIPTIONS

V_{DD}
Positive Power Supply (Pin 6)

This pin is normally tied to 5.0 V.

V_{SS}
Negative Power Supply (Pin 12)

This pin is normally tied to 0 V.

V_{AG}
Analog Ground (Pin 19)

Analog ground is internally biased to $(V_{DD} – V_{SS})/2$. This pin must be decoupled by a capacitor from V_{AG} to V_{SS} and a capacitor from V_{AG} to V_{DD}. Analog ground is the common bias line used in the switched capacitor filters, limiter, and slicer in the demodulation circuitry.

TLA
Transmit Level Adjust (Pin 20)

This pin is used to adjust the transmit level. Transmit level adjustment range is typically from – 12 dBm to – 9 dBm. (See Applications Information.)

TxD
Transmit Data (Pin 11)

Binary information is input to the transmit data pin. Data entered for transmission is modulated using FSK techniques. A logic high input level represents a mark and a logic low represents a space (see Table 1).

TxA
Transmit Carrier (Pin 17)

This is the output of the line driver amplifier. The transmit carrier is the digitally synthesized sine wave output of the modulator derived from a crystal oscillator reference. When a 3.579 MHz crystal is used the frequency outputs shown in Table 1 apply. (See ***Applications Information***.)

Table 1. Bell 103 and CCITT V.21 Frequency Characteristics

Data	Originate Mode		Answer Mode	
	Transmit	Receive	Transmit	Receive
Bell 103 (MC145443)				
Space	1070 Hz	2025 Hz	2025 Hz	1070 Hz
Mark	1270 Hz	2225 Hz	2225 Hz	1270 Hz
CCITT V.21 (MC145442)				
Space	1180 Hz	1850 Hz	1850 Hz	1180 Hz
Mark	980 Hz	1650 Hz	1850 Hz	980 Hz

NOTE: Actual frequencies may be ± 5 Hz assuming 3.579545 MHz crystal is used.

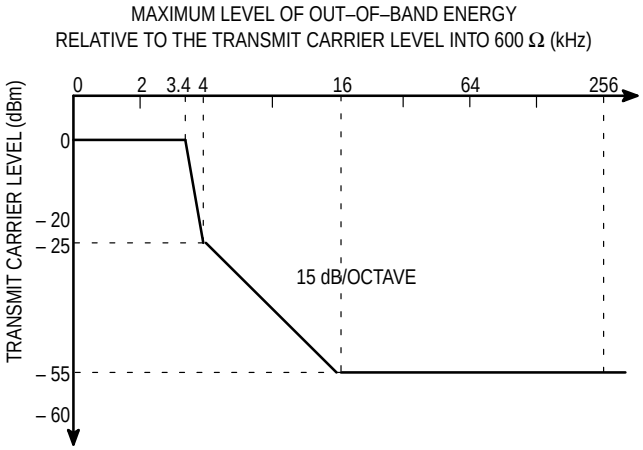


Figure 2. Out–of–Band Energy

ExI
External Input (Pin 18)

The external input is the non–inverting input to the line driver. It is provided to combine an auxiliary audio signal or speech signal to the phone line using the line driver. This pin should be connected to V_{AG} if not used. The average level must be the same as V_{AG} to maintain proper operation. (See ***Applications Information***.)

DSI
Driver Summing Input (Pin 1)

The driver summing input may be used to connect an external signal, such as a DTMF dialer, to the phone line. A series resistor, R_{DSI}, is needed to define the voltage gain A_V (see ***Applications Information*** and Figure 6). When applying a signal to do DSI pin, the modulator should be squelched by bringing SQT (Pin 14) to a logic high level. The voltage gain, A_V, is calculated by the formula $A_V = – R_f/R_{DSI}$ (where $R_f \approx 20$ kΩ). For example, a 20 kΩ resistor for R_{DSI} will provide unity gain ($A_V = – 20$ kΩ/20 kΩ = – 1). This pin **must** be left **open** if not used.

RxD
Receive Data (Pin 6)

The receive data output pin presents the digital binary data resulting from the demodulation of the receive carrier. If no carrier is present, CD high, the receive data output (RxD) is clamped high.

RxA2, RxA1
Receive Carrier (Pins 15, 16)

The receive carrier is the FSK input to the demodulator through the receive band–pass filter. RxA1 is the non–inverting input and RxA2 is the inverting input of the receive hybrid (duplexer) operational amplifier.

$\overline{LB}$
Analog Loopback (Pin 2)

When a high level is applied to this pin (SQT must be low), the analog loopback test is enabled. The analog loopback test connects the TxA pin to the RxA2 pin and the RxA1 to analog ground. In loopback, the demodulator frequencies are switched to the modulation frequencies for the selected mode. (See Tables 1 and 2 and Figures 4c and 4d.)

When LB is connected to analog ground (V_{AG}), the modulator generates an echo cancellation tone of 2100 Hz for MC145442 CCITT V.21 and 2225 Hz for MC145443 Bell 103 systems. For normal operation, this pin should be at a logic low level (V_{SS}).

The power–down mode is enabled when both $\overline{LB}$ and SQT are connected to a logic high level (see Table 2).

Table 2. Functional Table

MODE Pin 13	SQT Pin 14	LB Pin 2	Operating Mode
1	0	0	Originate Mode
0	0	0	Answer Mode
X	0	V_{AG} (V_{DD}/2)	Echo Tone
X	0	1	Analog Loopback
X	1	0	Squelch Mode
X	1	V_{AG} (V_{DD}/2)	Squelch Mode
X	1	1	Power Down

MODE
Mode (Pin 13)

This input selects the pair of transmit and frequencies used during modulation and demodulation. When a logic high level is placed on this input, originate (Bell) or channel 1 (CCITT) is selected. When a low level is placed on this input, answer (Bell) or channel 2 (CCITT) is selected. (See Tables 1 and 2 and Figure 4.)

CDT
Carrier Detect Timing (Pin 4)

A capacitor on this pin to V_{SS} sets the amount of time the carrier must be present before CD goes low (see ***Applications Information*** for the capacitor values).

$\overline{CD}$
Carrier Detect Output (Pin 3)

This output is used to indicate when a carrier has been sensed by the carrier detect circuit. This output goes to a logic low level when a valid signal above the maximum threshold level (defined by CDA, Pin 7) is maintained on the input to the hybrid circuit longer then the response (defined by CDT, Pin 4). This pin is held at the logic low level until the signal falls below the maximum threshold level for longer than the turn off time. (See ***Applications Information*** and Figure 5.)

CDA
Carrier Detect Adjust (Pin 7)

An external voltage may be applied to this pin to adjust the carrier detect threshold. The threshold hysteresis is internally fixed at 3 dB (see ***Applications Information***).

X_{out}, X_{in}
Crystal Oscillator (Pins 8, 9)

A crystal reference oscillator is formed when a 3.579 MHz crystal is connected between these two pins. X_{out} (Pin 8) is the output of the oscillator circuit, and X_{in} (Pin 9) is the input to the oscillator circuit. When using an external clock, apply the clock to the X_{in} (Pin 9) pin and leave X_{out} (Pin 8) open. An internal 10 MΩ resistor and internal capacitors, typically 10 pF on X_{in} and 16 pF on X_{out}, allow the crystal to be connected without any other external components. Printed circuit board layout should keep external stray capacitance to a minimum.

FB
Filter Bias (Pin 10)

This is the negative input to the ac amplifier. In normal operation, this pin is connected to analog ground through a 0.1 µF bypass capacitor in order to cancel the input offset voltage of the limiter. It has a nominal input impedance of 16 kΩ. (see Figure 3).

SQT
Transmit Squelch (Pin 14)

When this input pin is at a logic high level, the modulator is disabled. The line driver remains active if LB is at a logic low level (see Table 2) .

When both LB and SQT are connected to a logic high level, see Table 2, the entire chip is in a power down state and all circuitry except the crystal oscillator is disabled. Total power supply current decreases from 10 mA (Max) to 300 µA (Max).

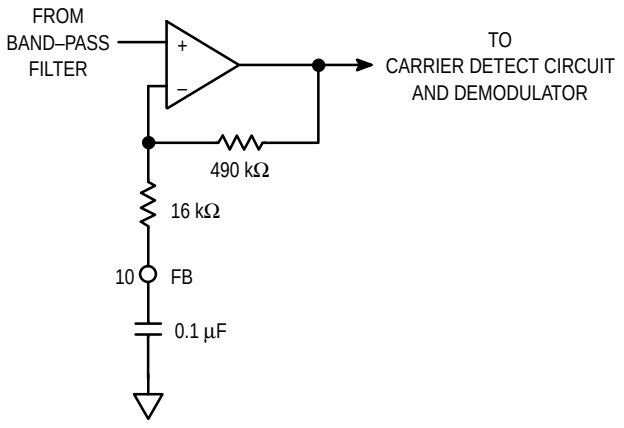


Figure 3. ac Amplifier Circuit

GENERAL DESCRIPTION

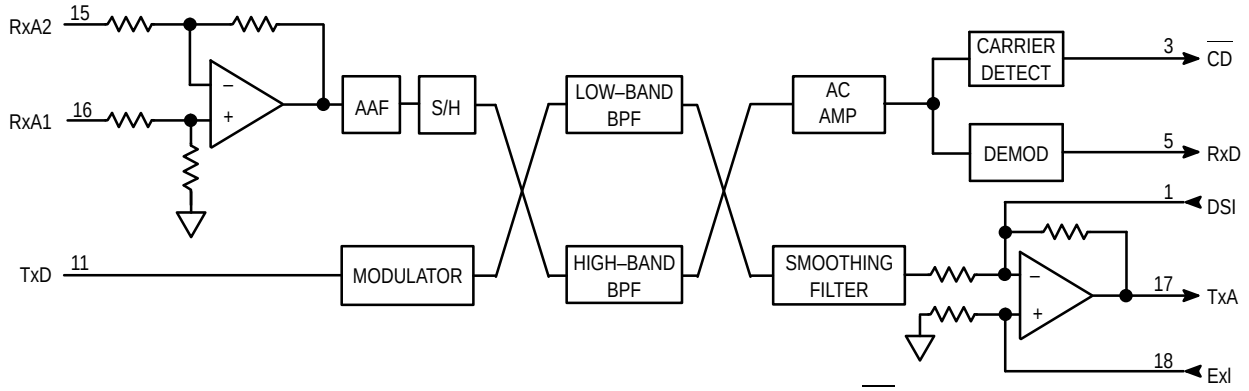
The MC145442 and MC145443 are full–duplex low–speed modems. They provide a 300–baud FSK signal for bidirectional data transmission over the telephone network. They can be operated in one of four basic configurations as determined by the state of MODE (Pin 13) and LB (Pin 2). The normal (non–loopback) and self test (loopback) modes in both answer and originate modes will be discussed.

For an originate or channel 1 mode, a logic high level is placed on MODE (Pin 13) and a logic low level is placed on LB (Pin 2). In this mode, transmit data is input on TxD, where it is converted to a FSK signal and routed through a low–band band–pass filter. The filtered output signal is then buffered by the Tx op–amp line driver, which is capable of driving – 9 dBm onto a 600 Ω line. The receive signal is connected through a hybrid duplexer circuit on Pins 15 and 16, RxA2 and RxA1. The signal then passes through the anti–aliasing filter, the sample–and–hold circuit, is switched into the high–band band–pass filter, and then switched into the ac amplifier circuit. The output of the ac amplifier circuit is routed to the demodulator circuit and demodulated. The resulting digital data is then output through RxD (Pin 5). The carrier detect circuit receives its signal from the output of the ac amplifier circuit and goes low when the incoming signal is detected (see Figure 4a).

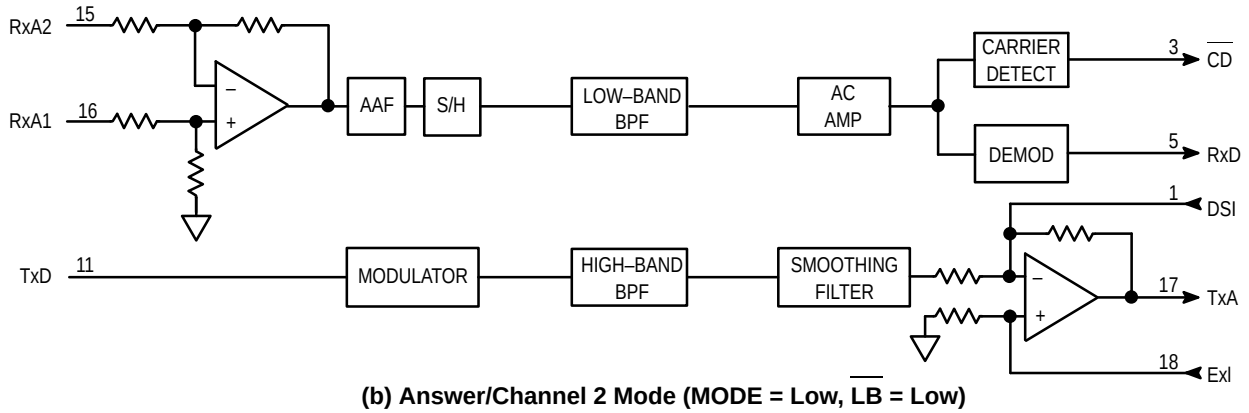
In the answer or channel 2 mode, a logic low level is placed on MODE (Pin 13) and on LB (Pin 2). In this mode, the data follows the same path except the FSK signal is routed to the high–band band–pass filter and the sample–and–hold signal is routed through the low–band band–pass filter. (See Figure 4b.)

In the analog loopback originate or channel 1 mode, a logic high level is placed on MODE (Pin 13) and on LB (Pin 2). This mode is used for a self check of the modulator, demodulator, and low–band pass–band filter circuit. The modulator side is configured exactly like the originate mode above except the line driver output (TxA, Pin 17) is switched to the negative input of the hybrid op–amp. The RxA2 input pin is open in this mode and the non–inverting input of the hybrid circuit is connected to V_{AG}. The sample–and–hold output bypasses the filter so that the demodulator receives the modulated Tx data (see Figure 4c). This test checks all internal device components except the high–band band–pass filter, which can be checked in the answer or channel 2 mode test.

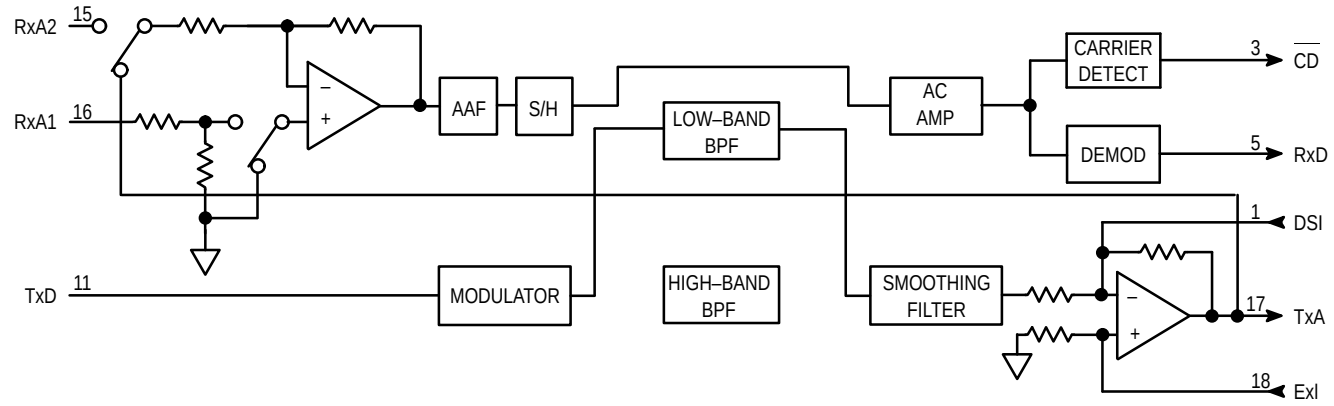
In the analog loopback or channel 2 mode, a logic low level is placed on MODE (Pin 13) and a logic high level on LB (Pin 2). This mode is used for a self check of the modulator, demodulator, and high–band pass–band filter circuit. This configuration is exactly like the originate loopback mode above, except the signal is routed through the high–band pass–band filter (see Figure 4d).



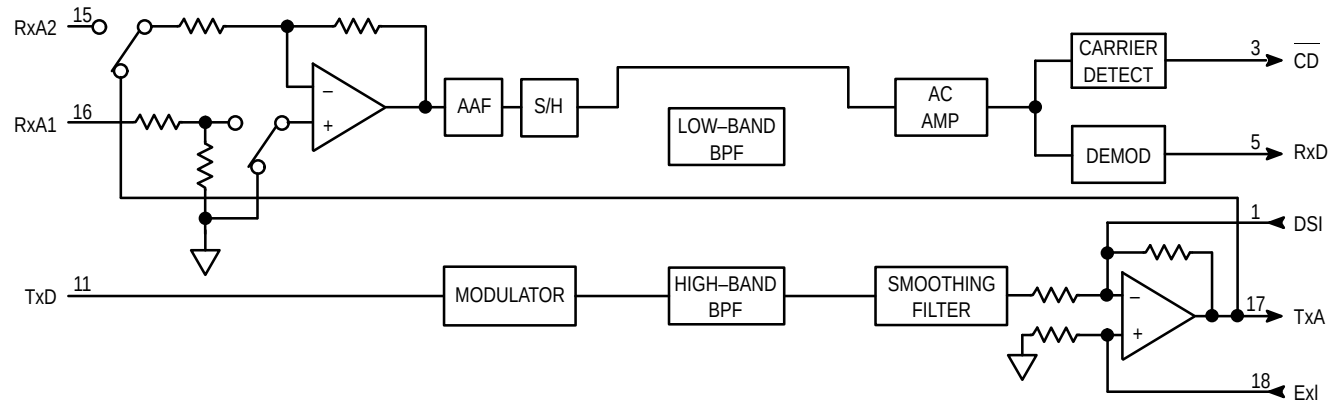
(a) Originate/Channel 1 Mode (MODE = High, $\overline{LB}$ = Low)



(b) Answer/Channel 2 Mode (MODE = Low, $\overline{LB}$ = Low)



(c) Originate/Channel 1 Mode and Analog Loopback State (MODE = High, $\overline{LB}$ = Low)



(d) Answer/Channel 2 Mode and Analog Loopback State (MODE = Low, $\overline{LB}$ = Low)

Figure 4. Basic Operating Modes

APPLICATIONS INFORMATION

CARRIER DETECT TIMING ADJUSTMENT

The value of a capacitor, C_{CDT} at CDT (Pin 4) determines how long a received modem signal must be present above the minimum threshold level before CD (Pin 3) goes low. The C_{CDT} capacitor also determines how long the CD pin stays low after the received modem signal goes below the minimum threshold. The CD pin is used to distinguish a strong modem signal from random noise. The following equations show the relationship between t_{CDL}, the time in seconds required for CD to go low; t_{CDH}, the time in seconds required for CD to go high; and C_{CDT}, the capacitor value in μF.

Valid signal to CD response time: $t_{CDL} \approx 6.4 \times C_{CDT}$

Invalid signal to CD off time: $t_{CDH} \approx 0.54 \times C_{CDT}$

Example: $t_{CDL} \approx 6.4 \times 0.1\ \mu F \approx 0.64$ seconds

$t_{CDH} \approx 0.54 \times 0.1\ \mu F \approx 0.054$ seconds

CARRIER DETECT THRESHOLD ADJUSTMENT

The carrier detect threshold is set by internal resistors to activate CD with a typical – 44 dBm (into 600 Ω) signal and deactivate CD with a typical – 47 dBm signal applied to the input of the hybrid circuit. The carrier detect threshold level can be adjusted by applying an external voltage on CDA (Pin 7). The following equations may be used to find the CDA voltage required for a given threshold voltage. (V_{on} and V_{off} are in Vrms.)

$$V_{CDA} = 244 \times V_{on}$$

$$V_{CDA} = 345 \times V_{off}$$

Example (Internally Set)

V_{on} = 4.9 mV ≈ – 44 dBm: $V_{CDA} = 244 \times 4.9$ mV = 1.2 V

V_{off} = 3.5 mV ≈ – 47 dBm: $V_{CDA} = 345 \times 3.5$ mV = 1.2 V

Example (Externally Set)

V_{on} = 7.7 mV ≈ – 40 dBm: $V_{CDA} = 244 \times 7.7$ mV = 1.9 V

V_{off} = 5.4 mV ≈ – 43 dBm: $V_{CDA} = 345 \times 5.4$ mV = 1.9 V

The CDA pin has an approximate Thevenin equivalent voltage of 1.2 V and an output impedance of 100 kΩ. When using the internal 1.2 V reference a 0.1 μF capacitor should be connected between this pin and V_{SS} (see Figure 5).

TRANSMIT LEVEL ADJUSTMENT

The power output at TxA (Pin 17) is determined by the value of resistor R_{TLA} that is connected between TLA (Pin 20) to V_{DD} (Pin 6). Table 3 shows the R_{TLA} values and the corresponding power output for a 600 Ω load. The voltage at TxA is twice the value of that at ring and tip because TxA feeds the signal through a 600 Ω resistor R_{TX} to a 600 Ω line transformer (see Figure 7). When choosing resistor R_{TLA}, keep in mind that – 9 dBm is the maximum output level allowed from a modem onto the telephone line (in the U.S.). In addition, keep in mind that maximizing the power output from the modem optimizes the signal–to–noise ratio, improving accurate data transmission.

Table 3. Transmit Level Adjust

Output Transmit Level (Typical into 600 Ω)	R_{TLA}
– 12 dBm	∞
– 11 dBm	19.8 kΩ
– 10 dBm	9.2 kΩ
– 9 dBm	5.5 kΩ

THE LINE DRIVER

The line driver is a power amplifier used for driving the telephone line. Both the inverting and noninverting input to the line driver are available for transmitting externally generated tones.

Exl (Pin 18) is the noninverting input to the line driver and gives a fixed gain of 2 (R_i = 50 kΩ). The average signal level must be the same as V_{AG} to maintain proper operation. This pin should be connected to V_{AG} if not used.

The driver summing input (DSI, Pin 1) may be used to connect an external signal, such as a DTMF dialer, to the phone line. When applying a signal to the DSI pin, the modulator should be squelched by bringing SQT (Pin 14) to a logic high level. DSI ***must*** be left ***open*** if not used.

In addition, the DSI pin is the inverting side of the line driver and allows adjustable gain with a series resistor R_{DSI} (see Figure 6). The voltage gain, A_V, is determined by the equation:

$$A_V = - \frac{R_f}{R_{DSI}}$$

where $R_f \approx 20$ kΩ.

Example: A resistor value of 20 kΩ for RDSI will provide unity gain.

$$A_V = - (20\ k\Omega / 20\ k\Omega) = - 1$$

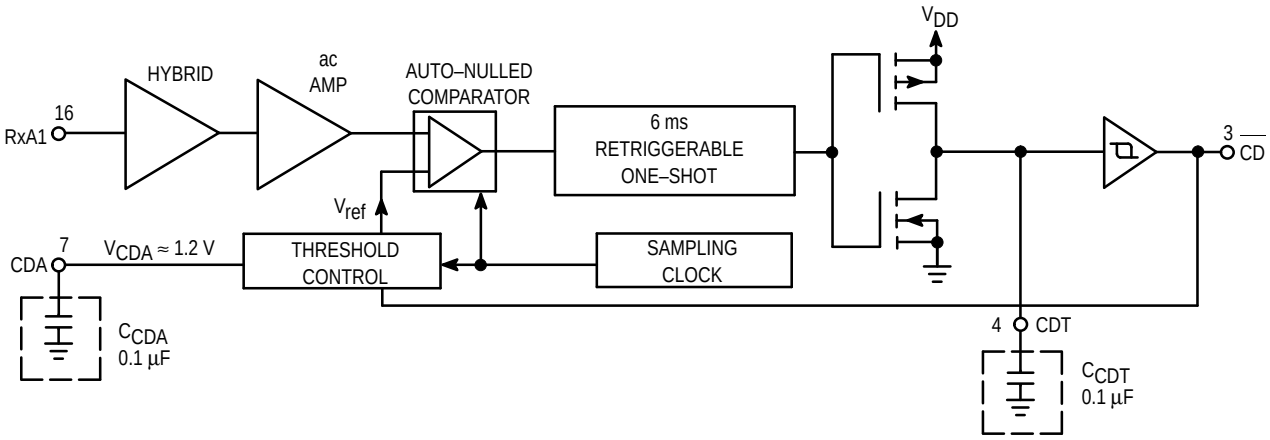


Figure 5. Carrier Detect Circuit

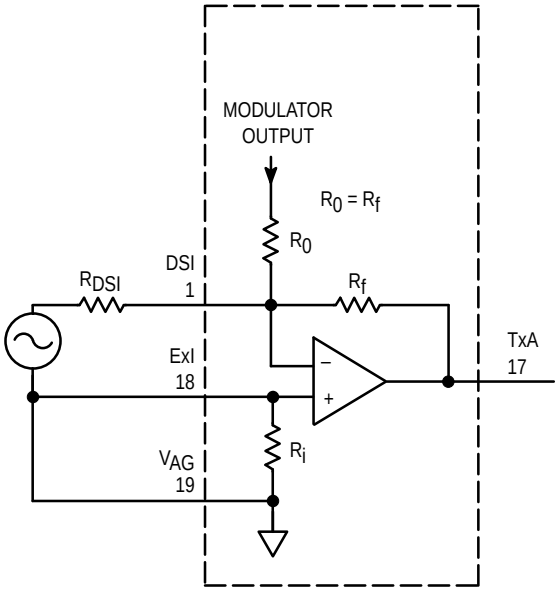
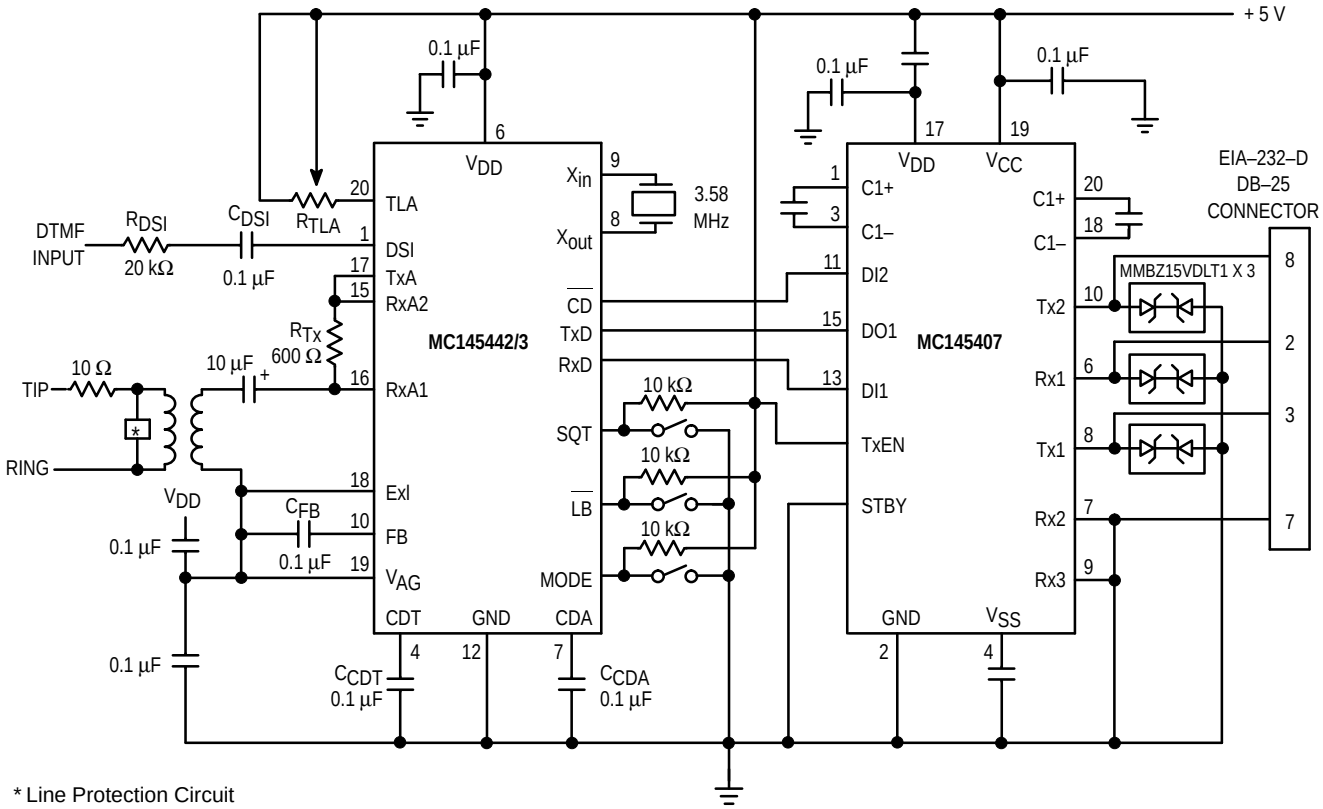


Figure 6. Line Driver Using the DSI Input

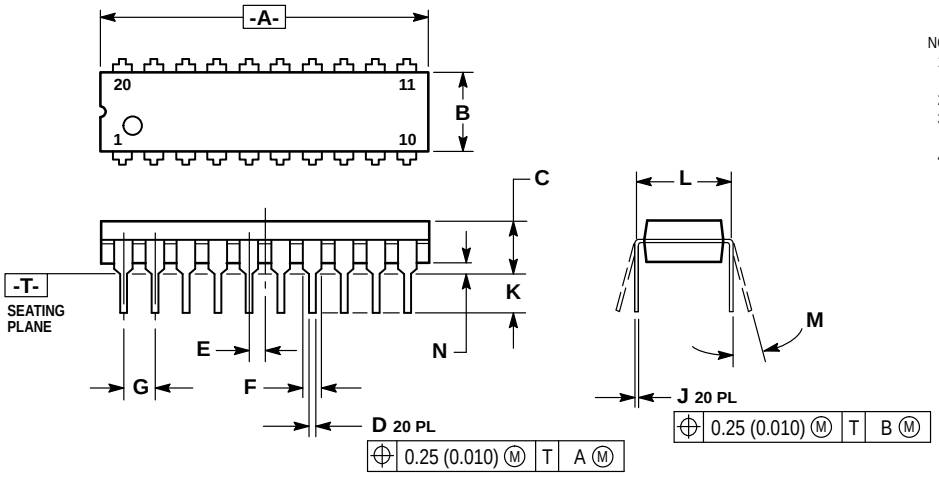


* Line Protection Circuit

Figure 7. Typical MC145442/MC145443 Applications Circuit

PACKAGE DIMENSIONS

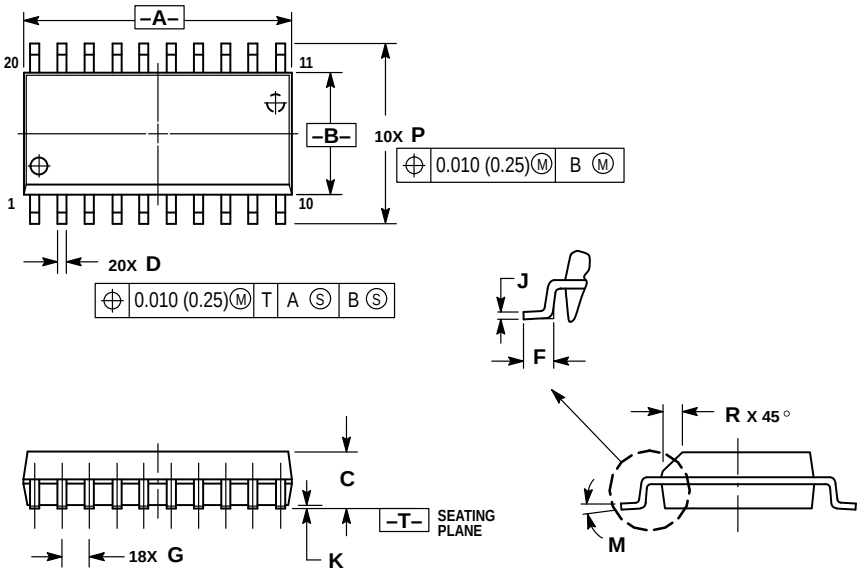
P SUFFIX
PLASTIC DIP
CASE 738–03



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

DW SUFFIX
SOG PACKAGE
CASE 751D–04



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029