8 Gb NAND Flash
H27U8G8T2B

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Document Title

8 Gbit (1024 M x 8 bit) NAND Flash Memory

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial Draft.	Jul. 30. 2008	Preliminary

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FEATURES SUMMARY

HIGH DENSITY NAND FLASH MEMORIES

- Cost effective solutions for mass storage applications

MULTIPLANE ARCHITECTURE

- Array is split into two independent planes. Parallel operations on both planes are available, halving program, read and erase time.

NAND INTERFACE

- x8 bus width.
- Address / Data Multiplexing
- Pin-out compatibility for all densities

SUPPLY VOLTAGE

- 3.3 V device : Vcc = 2.7 V ~3.6 V

MEMORY CELL ARRAY

- (4 K + 128) bytes x 128 pages x 2048 blocks

PAGE SIZE

- (4 K + 128 spare) Bytes

BLOCK SIZE

- (512 K + 16 K spare) Bytes

PAGE READ / PROGRAM

- Random access : 60 us (max.)
- Sequential access : 25 ns (min.)
- Page program time : 800 us (typ.)
- Multi-Plane Program time (2 pages) : 800 us (typ.)

FAST BLOCK ERASE

- Block erase time: 2.5 ms (typ.)
- Multi-Block Erase time (2 blocks) : 2.5 ms (typ.)

ELECTRONIC SIGNATURE

- 1st cycle : Manufacturer Code
- 2nd cycle : Device Code
- 3rd cycle : Internal chip number, Cell Type, Number of Simultaneously Programmed Pages.
- 4th cycle : Page size, Block size, Organization, Spare size
- 5th cycle : Multiplane Information

COPY BACK PROGRAM

- Fast Data Copy without external buffer

CHIP ENABLE DON'T CARE

- Simple interface with microcontroller

STATUS REGISTER

- Normal Status Register (Read/Program/Erase)

HARDWARE DATA PROTECTION

- Device locked during Power transitions.

DATA RETENTION

- 5,000 Program/Erase cycles
  (with 4 bit / 528 byte ECC)
- 10 years Data Retention

PACKAGE

- H27U8G8T2BTR-BX
  : 48-Pin TSOP1 (12 x 20 x 1.2 mm)
  - H27U8G8T2BTR-BX (Lead & Halogen Free)

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1. SUMMARY DESCRIPTION

Hynix NAND H27U8G8T2B Series have 1024 M x 8 bit with spare 32 M x 8 bit capacity. The device is offered in 3.3 V Vcc Power Supply, and with x8 I/O interface. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.

The device contains 2048 blocks, composed by 128 pages. Every cell holds two bits. A program operation allows to write the 4224 byte page in typical 800 us and an erase operation can be performed in typical 2.5 ms on a 512 K byte block.

In addition to this, thanks to multi-plane architecture, it is possible to program 2 pages a time (one per each plane) or to read 2 pages a time (one per each plane) to erase 2 blocks a time (again, one per each plane). As a consequence, multiplane architecture allows program time reduction and erase time reduction.

Data in the page can be read out at 25ns cycle time per byte. The I/O pins serve as the ports for address and data input/ output as well as command input. This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of footprint.

Commands, Data and Addresses are synchronously introduced using $\overline{CE}$, $\overline{WE}$, $\overline{RE}$, ALE and CLE input pin. The on-chip Program/Erase Controller automates all read, program and erase functions including pulse repetition, where required, and internal verification and margining of data. The modify operations can be locked using the $\overline{WP}$ input.

The output pin $\overline{R/B}$ (open drain buffer) signals the status of the device during each operation. In a system with multiple memories the $\overline{R/B}$ pins can be connected all together to provide a global status signal.

The copy back function allows the optimization of defective blocks management: when a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase. Data read out after copy back read (both for single and multiplane cases) is allowed.

Even the write-intensive systems can take advantage of the H27U8G8T2B Series extended reliability of 5 K program/ erase cycles by providing ECC (Error Correcting Code) with real time mapping-out algorithm.

The chip supports $\overline{CE}$ don't care function. This function allows the direct download of the code from the NAND Flash memory device by a microcontroller, since the $\overline{CE}$ transitions do not stop the read operation.

This device includes also extra features like OTP/Unique ID area, Read ID2 extension.

The H27U8G8T2B is available in 48-TSOP1 12 x 20 mm.

1.1 Product List

PART NUMBER	ORGANIZATION	Vcc RANGE	PACKAGE
H27U8G8T2B	x8	2.7V ~ 3.6V	48-TSOP1

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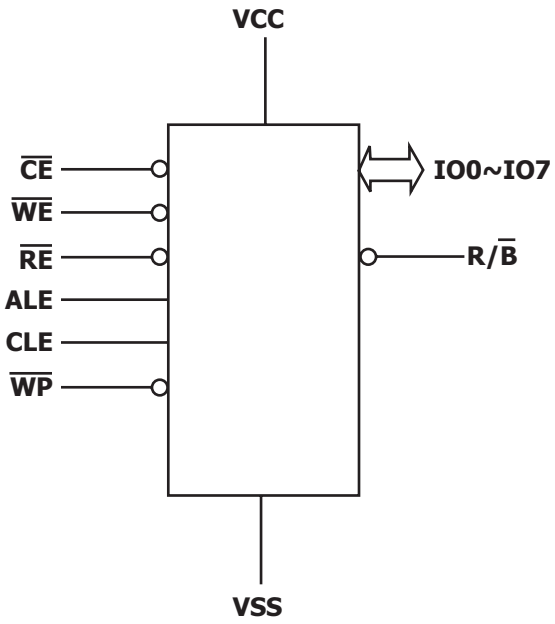

Figure 1 : Logic Diagram

IO7 - IO0	Data Input / Outputs
CLE	Command latch enable
ALE	Address latch enable
$\overline{CE}$	Chip Enable
$\overline{RE}$	Read Enable
$\overline{WE}$	Write Enable
$\overline{WP}$	Write Protect
R/$\overline{B}$	Ready / Busy
Vcc	Power Supply
Vss	Ground
NC	No Connection

Table 1 : Signal Names

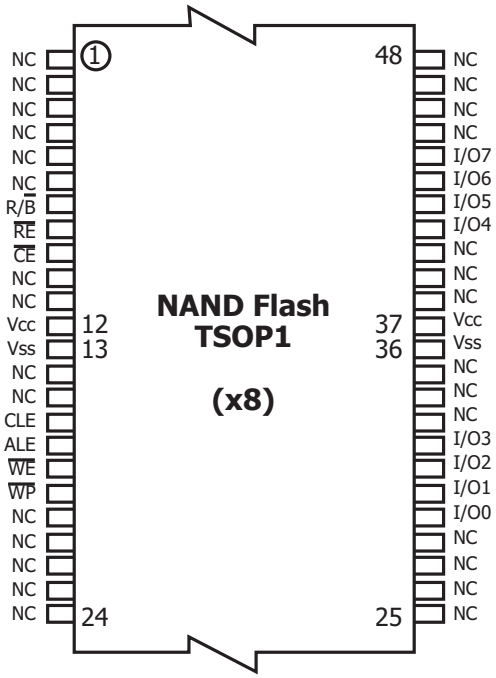

Figure 2 : 48-TSOP1 Contact, x8 Device

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1.2 PIN DESCRIPTION

Pin Name	Description
IO0 ~ IO7	**DATA INPUTS/OUTPUTS** The IO pins allow to input command, address and data and to output data during read / program operations. The inputs are latched on the rising edge of Write Enable ($\overline{WE}$). The I/O buffer float to High-Z when the device is deselected or the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** This input activates the latching of the IO inputs inside the Command Register on the Rising edge of Write Enable ($\overline{WE}$).
ALE	**ADDRESS LATCH ENABLE** This input activates the latching of the IO inputs inside the Address Register on the Rising edge of Write Enable ($\overline{WE}$).
$\overline{CE}$	**CHIP ENABLE** This input controls the selection of the device.
$\overline{WE}$	**WRITE ENABLE** This input acts as clock to latch Command, Address and Data. The IO inputs are latched on the rise edge of $\overline{WE}$.
$\overline{RE}$	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.
$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin, when Low, provides an Hardware protection against undesired modify (program / erase) operations.
R/$\overline{B}$	**READY BUSY** The Ready/Busy output is an Open Drain pin that signals the state of the memory.
Vcc	**SUPPLY VOLTAGE** The Vcc supplies the power for all the operations (Read, Write, Erase).
Vss	**GROUND**
NC	**NO CONNECTION**

Table 2 : Pin Description

NOTE :

1. A 0.1uF capacitor should be connected between the Vcc Supply Voltage pin and the Vss Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

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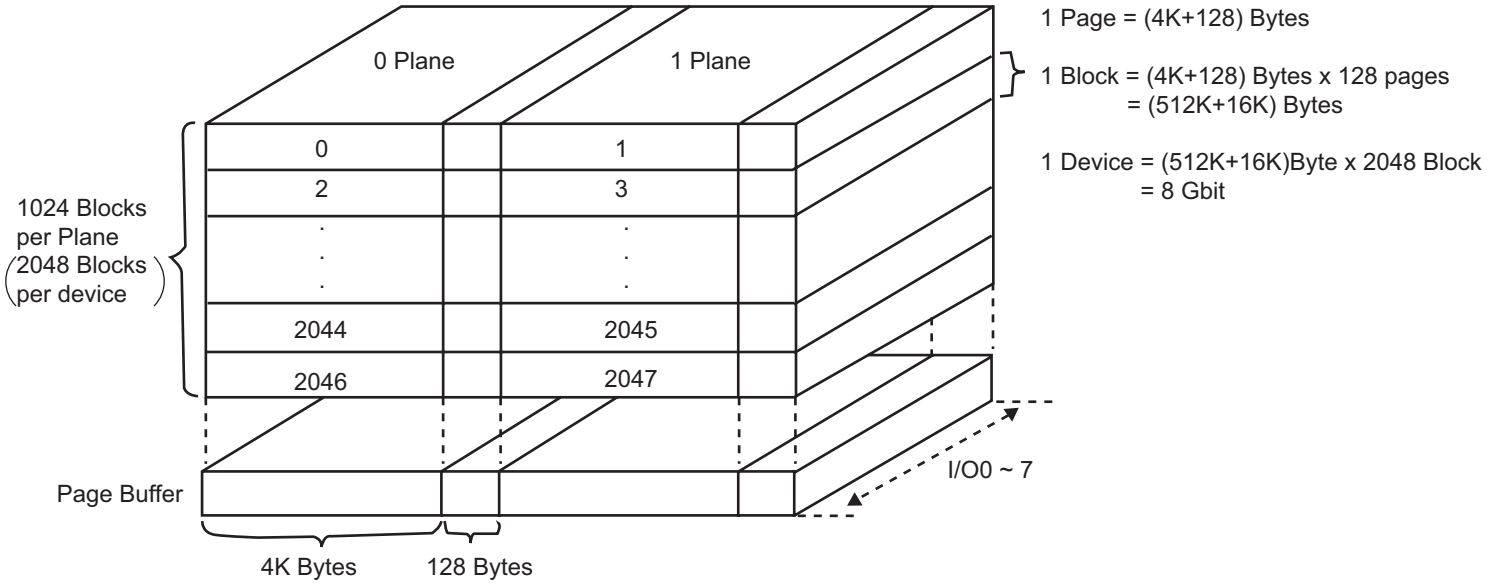

Figure 3 : Array Organization

	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	A11	A12	L(1)	L(1)	L(1)
3rd Cycle	A13	A14	A15	A16	A17	A18	A19	A20
4th Cycle	A21	A22	A23	A24	A25	A26	A27	A28
5th Cycle	A29	A30	L(1)	L(1)	L(1)	L(1)	L(1)	L(1)

Table 3 : Address Cycle Map

NOTE:

1. L must be set to Low.
2. 1st & 2nd cycle are Column Address.
3. 3rd to 5th cycle are Row Address.

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FUNCTION	1st	2nd	3rd	4th	Acceptable Command During Busy
PAGE READ	00h	30h	-	-	
MULTI-PLANE READ	60h	60h	30h	-	
READ FOR COPY-BACK	00h	35h	-	-	
MULTIPLANE READ FOR COPYBACK	60h	60h	35h	-	
READ ID	90h	-	-	-	
RESET	FFh	-	-	-	Yes
PAGE PROGRAM	80h	10h	-	-	
COPY BACK PROGRAM	85h	10h	-	-	
MULTI-PLANE PROGRAM	80h	11h	81h	10h	
MULTI-PLANE COPY BACK PROGRAM	85h	11h	81h	10h	
BLOCK ERASE	60h	D0h	-	-	
MULTI-PLANE BLOCK ERASE	60h	60h	D0h	-	
READ STATUS REGISTER	70h	-	-	-	Yes
RANDOM DATA INPUT	85h	-	-	-	
RANDOM DATA OUTPUT	05h	E0h	-	-	
MULTI-PLANE RANDOM DATA OUTPUT	00h	05h	E0h	-	
PAGE PROGRAM WITH BACKWARD COMPATIBILITY (2 KB)	80h	11h	80h	10h	
COPY BACK PROGRAM WITH BACKWARD COMPATIBILITY (2 KB)	85h	11h	85h	10h	

Table 4 : Command Set

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	MODE	
H	L	L	Rising	H	X	Read Mode	Command Input
L	H	L	Rising	H	X		Address Input (5 cycles)
H	L	L	Rising	H	H	Write Mode	Command Input
L	H	L	Rising	H	H		Address Input (5 cycles)
L	L	L	Rising	H	H	Data Input	
L	L	L	H	Falling	X	Data Output	
X	X	X	H	H	X	During Read (Busy)	
X	X	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X	X	X	X	L	Write Protect	
X	X	H	X	X	0 V / Vcc	Stand By	

NOTE : With the $\overline{CE}$ don't care option $\overline{CE}$ high during latency time does not stop the read operation

Table 5 : Mode Selection

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2. BUS OPERATION

There are six standard bus operations that control the device. These are Command Input, Address Input, Data Input, Data Output, Write Protect, and Standby.

Typically glitches less than 3 ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations.

2.1 Command Input.

Command Input bus operation is used to give a command to the memory device. Command are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See Figure 5 and Table 12 for details of the timings requirements.

2.2 Address Input.

Address Input bus operation allows the insertion of the memory address. To insert the 31 bits needed to access the 8 Gbit device, 5 clock cycles are needed. Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See Figure 6 and Table 12 for details of the timings requirements. In addition, addresses over the addressable space are disregarded even if the user sets them during command insertion.

2.3 Data Input.

Data Input bus operation allows to feed to the device the data to be programmed. The data insertion is serially and timed by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable. See Figure 7 and Table 12 for details of the timings requirements.

2.4 Data Output.

Data Output bus operation allows to read data from the memory array and to check the status register content, the lock status and the ID data. Data can be serially shifted out toggling the Read Enable pin with Chip Enable low, Write Enable High, Address Latch Enable low, and Command Latch Enable low. See Figure 8, 9, 10 and Table 12 for details of the timings requirements.

2.5 Write Protect.

Hardware Write Protection is activated when the Write Protect pin is low. In this condition modify operation does not start and the content of the memory is not altered or it is interrupted without guarantee about memory content not being altered. Write Protect pin is not latched by Write Enable, so as to ensure protection even during power up phases.

2.6 Standby.

In Standby mode the device is deselected, outputs are disabled and Power Consumption is reduced. Stand-by is obtained holding high, at least for 10us, $\overline{CE}$ pin.

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3. DEVICE OPERATION

3.1 Page Read.

Upon initial power up, the device defaults to Read mode. This operation is also initiated by writing 00h and 30h to the command register along with five address cycles. After a 1st page read operation, device remains in read mode, that is to say that a 2nd page read can start just by inputting 5 address cycles and read confirm command; in other words 00h command cycle is not necessary. Also after power up device is in read mode, so 00h command cycle is not necessary to start a read operation. Any operation different from read or random data output causes the device to exit read mode.

Two types of read operations are available: random and serial read in a page. The random read mode is enabled when the page address is changed. The 4,224 bytes of data within the selected page are transferred to the data registers in less than 60us (tR). The system controller may detect the completion of this data transfer (tR) by analyzing the output of R/B pin. Once the data in a page is loaded into the data registers, they may be read out in 25ns cycle time by sequentially pulsing $\overline{RE}$. The repetitive high to low transitions of the $\overline{RE}$ clock make the device output the data starting from the selected column address up to the last column address in the page.

The device may output random data in a page instead of the consecutive sequential data by writing random data output command (05h-E0h as in Figure 13)

The column address of next data, which is going to be output, may be changed to the address which follows random data output command.

Random data output can be operated regardless of how many times it is done in a page.

Check Figure 11, Figure 12 and Figure 13 as a reference.

3.2 Multiplane Page Read

Multi-Plane Page Read is an extension of Page Read for a single plane. Since the device is equipped with two memory planes, a read of two pages (one for each plane) is enabled by activating two sets of 4,224 byte page registers(one for each plane). Multi-Plane Page Read is initiated by repeating command 60h followed by three address cycle twice and then by entering 30h confirm command. In this case only the same page of the same block can be selected from each plane.

After Read Confirm command (30h) the 8,448 bytes of data within the selected two pages are transferred into the data registers in less than 60us(tR). The system controller can detect the completion of data transfer (tR) by monitoring the output of R/B pin.

Once the data are loaded into the data registers, the first plane's data must be read out by issuing command 00h with Five Address Cycles (all 00h), command 05h with two column address and finally E0h and then toggling $\overline{RE}$: if two column address is 00h, then the read-out starts from the beginning of the page, otherwise data-out will start from selected column for random data-out.

The second plane's data must be read out using the command sequence command 00h with Five Address Cycles (all 00h except A20=1), command 05h with two column address and finally E0h and then toggling $\overline{RE}$: if two column address is 00h, then the read-out starts from the beginning of the page, otherwise data-out will start from selected column for random data out.

To execute multiple random data-out within the same two pages selected, the command sequence is command 00h with Five Address Cycles, command 05h with two column address and finally E0h: in 5 address cycles A20=0 allows random read in 1st plane page, while A20=1 allows random read in 2nd plane page (Figure 14).

Restrictions and details for Multi-Plane Page Read are shown in Figure 14. Multi- Plane Read must be used in the block which has been programmed with Multi-Plane Page Program.

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3.3 Page Program

The device is programmed by page. Only a single partial or complete page programming operation within the same page, without an intervening erase operation, is allowed

The addressing must be done in sequential order in a block. A page program cycle consists of a serial data loading period in which up to 4,224 data bytes may be loaded into the data register, followed by a non-volatile memory programming period where the loaded data are programmed into the appropriate cells.

The serial data loading period begins by inputting the Serial Data Input command (80h), followed by five address cycles input and then zero or more serial data input cycles. The words other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page.

The Page Program confirm command (10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are accepted while programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be tested to check for fails in the program operation. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register. Figure 15 and Figure 17 detail the sequence.

3.4 Multiplane Page Program

Device supports multiple plane program: it is possible to program in parallel 2 pages, one per each plane.

A multiple plane program cycle consists of a double serial data loading period in which up to 8,448 bytes of data may be loaded into the data register, followed by a non-volatile memory programming period when the loaded data are programmed into the appropriate cells. The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five address cycles input and then zero or more serial data for the 1st page. Address for this page must be within 1st plane (A<20>=0) and A<19:13> and A<30:21> must be fixed low. Data of 1st page other than those to be programmed do not need to be loaded. The device supports random data input exactly like a normal page program operation. The Dummy Page Program Confirm command (11h) stops 1st page data input and the device goes busy for a short time (tDBSY). Once it has returned ready, 81h command must be issued, followed by page address cycles and zero or more serial data input cycles. Address for this page must be within 2nd plane (A<20>=1) and A<19:13> and A<30:21> must be the valid addresses. The data of 2nd page other than those to be programmed do not need to be loaded. Program Confirm command (10h) makes parallel programming of both pages start. User can check operation status by R/$\overline{B}$ pin or read status register command, as if it were a normal page program; status register command is also available during Dummy Busy time (tDBSY).

In case of fail in 1st or 2nd page program, fail bit of status register will be set: the device supports pass/fail status of each plane (IO0: total; IO1: plane0; IO2: plane1). Figure 16 details the sequence.

3.5 Block Erase

The Block Erase operation is done on a block basis. Block address loading is accomplished giving 3 address cycles initiated by an Erase Setup command (60h). Only addresses A20 to A30 are valid while A13 to A19 are ignored. The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase and erase-verify.

Once the erase process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of an erase by monitoring the RB# output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked.

Figure 18 details the sequence.

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3.6 Multiplane Block Erase

Multiple plane erase allows parallel erase of two blocks, one per each plane.

Block erase setup command (60h) must be repeated two times, each time followed by 1st and 2nd block address cycles respectively (3 cycles each). As for block erase, D0h command makes this operation start.

Multi-plane erase does not need any Dummy Busy Time between 1st and 2nd block address cycles insertion.

Address limitation required for multiple plane program applies also to multiple plane erase, as well as operation progress can be checked like for multiple plane program. Figure 19 details the sequence.

3.7 Copy Back Program

Copy-Back program with Read for Copy-Back is configured to quickly and efficiently rewrite data stored in one page without data reloading when the bit error is not in data stored. Since the time-consuming re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of block is updated and the rest of the block also needs to be copied to the newly assigned free block. Copy-Back operation is a sequential execution of Read for Copy-Back and of copy-back program with the destination page address. A read operation with "35h" command and the address of the source page moves the whole 4,224-byte into the internal data buffer. A bit error is checked by reading sequentially the data output. In the case where there is no bit error, the data do not need to be reloaded. Therefore Copy-Back program operation is initiated by issuing Page-Copy Data-Input command (85h) with destination page address. Actual programming operation begins after Program Confirm command (10h) is issued. Once the program process starts, the Read Status Register command (70h) may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the RB# output, or the Status bit (I/O 6) of the Status Register.

When the Copy-Back Program is complete, the Write Status Bit (I/O 0) may be checked (Figure 20). The command register remains in Read Status command mode until another valid command is written to the command register. During copy-back program, data modification is possible using random data input command (85h) as shown in Figure 21.

Copy-Back Program operation is allowed only within the same memory plane.

3.8 Multiplane Copy Back Program

Two-Plane Copy-Back Program is an extension of Copy-Back Program, for a single plane with 4,224 byte page registers. As for single plane copy-back, a multi plane read operation with "35h" (multi plane read for copy-back) command and the address of the source pages moves the whole 4,224-byte of each page into the internal data buffer of each plane. Since the device is equipped with two memory planes, activating the two sets of 4,224 byte page registers enables a simultaneous programming of two pages. Figure 22 and Figure 23 show the details of the command sequence for the multi-plane copy-back operation in standard operation mode. In order to reduce the buffer size required by host side (8KB buffer size) to perform this operation, new Multiplane Copy-Back Program flows have been introduced as shown from Figure 24 to Figure 25. As depictured the sequences of data out followed by data input for each plane can be performed an indefinite number of times, which depend on the buffer size used by host (e.g. Figure 24 shows the sequence for a host equipped with a 4KB buffer size, whereas the Figure 25 shows the sequence for a host equipped with 2KB buffer size).

3.9 Read Status Register

The device contains a Status Register which may be read to find out whether a read, program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to Table 13 for specific Status Register definitions and to Figure 10 for Status Read sequence. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command (00h) should be given before starting new read cycles.

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3.10 Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Five read cycles sequentially output the manufacturer code (20h), and the device code and 3rd, 4th and 5th cycle ID, respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 26 shows the operation sequence, while following Table 15, Table 16, Table 17, and Table 18 explain the byte meaning. Complete read id code table is Table 14.

3.11 Reset

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when $\overline{WP}$ is high. Refer to Table 13 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The R/$\overline{B}$ pin transitions to low for tRST after the Reset command is written (see Figure 27).

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4. OTHER FEATURES

4.1 Data Protection

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 2.0 V. $\overline{WP}$ pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down. A recovery time is required before internal circuit gets ready for any command sequences as shown in Figure 28. The two-step command sequence for program/erase provides additional software protection.

4.2 Ready/Busy

The device has a Ready/Busy output that provides method of indicating the completion of a page program, erase, copy-back, cache program and random read completion. The R/$\overline{B}$ pin is normally high and goes to low when the device is busy (after a reset, read, program, erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/$\overline{B}$) and current drain during busy (I busy), an appropriate value can be obtained with the following reference chart (Figure 29). Its value can be determined by the following guidance.

4.3 System Interface Using $\overline{CE}$ don't care

To simplify system interface, $\overline{CE}$ may be deasserted during data loading or sequential data reading as shown Figure 30 and 31. So, it is possible to connect NAND Flash to a microprocessor. The only function that was removed from standard NAND Flash to make $\overline{CE}$ don't care operation was disabling of the automatic sequential read function.

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Parameter	Symbol	Min	Typ	Max	Unit
Valid Block Number	N_{VB}	1998		2048	Blocks

Table 6 : Number of Valid Blocks

NOTE:
1. The 1st block is guaranteed to be a valid block at the time of shipment.

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature (Temperature Range Option 1)	0 to 70	°C
	Ambient Operating Temperature (Temperature Range Option 6)	– 40 to 85	°C
T_{BIAS}	Temperature Under Bias	– 50 to 125	°C
T_{STG}	Storage Temperature	– 65 to 150	°C
V_{IO} (2)	Input or Output Voltage	– 0.6 to 4.6	V
V_{CC}	Supply Voltage	– 0.6 to 4.6	V

Table 7 : Absulute maximum ratings

NOTE:
1. Block 0 is guaranteed to be valid at the time of the shipment up to 1K P/E cycles. The number of valid blocks is based on single plane operations and may be little lower on two plane operations.

2. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the HYNIX SURE Program and other relevant quality documents.

3. Minimum Voltage may undershoot to -2 V during transition and for less than 20ns during transitions.

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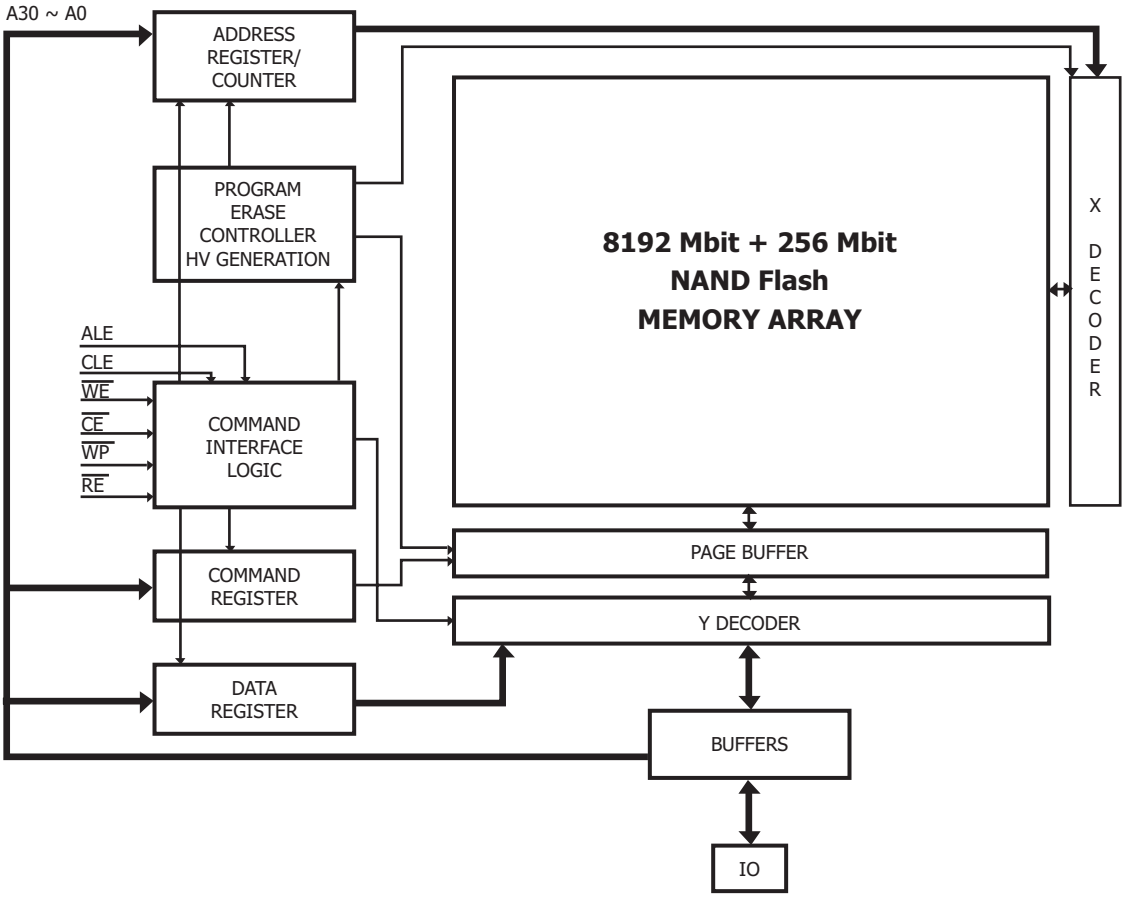

Figure 4 : Block Diagram

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Parameter		Symbol	Test Conditions	3.3 Volt			Unit
				Min	Typ	Max	
Operating Current	Sequential Read	I_{CC1}	t_{RC} = 25 ns, $\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA	-	15	30	mA
	Program	I_{CC2}	-	-	15	30	mA
	Erase	I_{CC3}	-	-	15	30	mA
Stand-by Current (TTL)		I_{CC4}	$\overline{CE}$ = V_{IH}, $\overline{WP}$ = 0 V/V_{CC}	-	-	1	mA
Stand-By Current (CMOS)		I_{CC5}	$\overline{CE}$ = V_{CC} - 0.2, $\overline{WP}$ = 0 V / V_{CC}	-	10	50	uA
Input Leakage Current		I_{LI}	V_{IN} = 0 to 3.6 V	-	-	±10	uA
Output Leakage Current		I_{LO}	V_{OUT} = 0 to 3.6 V	-	-	±10	uA
Input High Voltage		V_{IH}	-	0.8 x V_{CC}	-	V_{CC} + 0.3	V
Input Low Voltage		V_{IL}	-	-0.3	-	0.2 x V_{CC}	V
Output High Voltage Level		V_{OH}	I_{OH} = - 400 uA	2.4	-	-	V
Outpul Low Voltage Level		V_{OL}	I_{OL} = 2.1 mA	-	-	0.4	V
Output Low Current (R/$\overline{B}$)		I_{OL} (R/$\overline{B}$)	V_{OL}= 0.4 V	8	10	-	mA

Table 8 : DC and Opeating Characteristics

Parameter	Value
	3.3 Volt
Input Pulse Levels	0 V to V_{CC}
Input Rise and Fall Times	5 ns
Input and Output Timing Levels	V_{CC} / 2
Output Load (2.5V - 3.6V)	1 TTL GATE and CL = 50 pF

Table 9 : AC Test Conditions

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Item	Symbol	Test Condition	Min	Max	Unit
Input / Output Capacitance	$C_{I/O}$	V_{IL} = 0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	-	10	pF

Table 10 : Pin Capacitance (TA = 25 ℃, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Program Time / Multiplane Program Time	t_{PROG}	-	800	2000	us
Dummy Busy Time for Multiplane Program	t_{DBSY}	-	1	2	us
Number of partial Program Cycles in the same page	Nop	-	-	1	Cycle
Block Erase Time / Multiplane Erase Time	t_{BERS}	-	2.5	10	ms

Table 11 : Program / Erase Characteristics

NOTE :
Typical program time is defined as the time when which more than 50 % of the whole pages are programmed at Vcc = 3.3 V and 25 ℃.

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Parameter	Symbol	3.3 Volt		Unit
		Min	Max	
CLE Setup time	t_{CLS}	12		ns
CLE Hold time	t_{CLH}	5		ns
$\overline{CE}$ Setup time	t_{CS}	20		ns
$\overline{CE}$ Hold time	t_{CH}	5		ns
$\overline{WE}$ Pulse width	t_{WP}	12		ns
ALE Setup time	t_{ALS}	12		ns
ALE Hold time	t_{ALH}	5		ns
Data Setup time	t_{DS}	12		ns
Data Hold time	t_{DH}	5		ns
Write Cycle time	t_{WC}	25		ns
$\overline{WE}$ High Hold time	t_{WH}	10		ns
Address to Data Loading time	t_{ADL}	70		ns
Data Transfer from Cell to Register	t_{R}		60	us
ALE to $\overline{RE}$ Delay	t_{AR}	10		ns
CLE to $\overline{RE}$ Delay	t_{CLR}	10		ns
Ready to RE Low	t_{RR}	20		ns
$\overline{RE}$ Pulse Width	t_{RP}	12		ns
$\overline{WE}$ High to Busy	t_{WB}		100	ns
Read Cycle Time	t_{RC}	25		ns
$\overline{RE}$ Access Time	t_{REA}		20	ns
$\overline{RE}$ High to Output Hi-Z	t_{RHZ}		100	ns
$\overline{CE}$ Access Time	t_{CEA}		30	ns
$\overline{CE}$ High to Output Hi-Z	t_{CHZ}		50	ns
$\overline{RE}$ High to Output Hold	t_{RHOH}	15		ns
$\overline{RE}$ Low to Output Hold	t_{RLOH}	5		ns
$\overline{CE}$ low to $\overline{WE}$ low	t_{CR}	10		ns
$\overline{CE}$ High to Output hold	t_{COH}	15		ns
$\overline{RE}$ High Hold Time	t_{REH}	10		ns
Output Hi-Z to $\overline{RE}$ Low	t_{IR}	0		ns
$\overline{RE}$ High to $\overline{WE}$ Low	t_{RHW}	100		ns
$\overline{WE}$ High to $\overline{RE}$ Low	t_{WHR}	80		ns
Device Resetting Time (Read/Program/Erase)	t_{RST}		2/20/500 [1]	us
Write Protection Time	t_{WW} [2]	100		ns

Table 12 : AC Timing Characteristics

NOTE :
1) If Reset Command (FFh) is written at Ready State, the device goes into Busy for maximum 5 us
2) Program / Erase Enable Operation : $\overline{WP}$ high to $\overline{WE}$ high
   Program / Erase Disable Operation : $\overline{WP}$ low to $\overline{WE}$ high

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IO	Page Program	Block Erase	Read	CODING
0	Pass / Fail	Pass / Fail	NA	Pass: '0' Fail: '1'
1	Plane 0 Pass / Fail	Plane 0 Pass / Fail	NA	Pass: '0' Fail : '1'
2	Plane 1 Pass / Fail	Plane 1 Pass / Fail	NA	Pass: '0' Fail : '1'
3	NA	NA	NA	-
4	NA	NA	NA	-
5	Ready/Busy	Ready/Busy	Ready/Busy	Busy: '0' Ready:'1'
6	Ready/Busy	Ready/Busy	Ready/Busy	Busy: '0' Ready:'1'
7	Write Protect	Write Protect	Write Protect	Protected: '0' Not Protected: '1'

Table 13 : Status Register Coding

DEVICE IDENTIFIER BYTE	DESCRIPTION
1st	Manufacturer Code
2nd	Device Identifier
3rd	Internal Chip Number, Cell Type, etc.
4th	Page Size, Block Size, Spare Size, Organization
5th	Multiplane Information

Table 14 : Device Identifier Coding

Part Number	Voltage	Bus Width	1st cycle (Manufacture Code)	2nd cycle (Device Code)	3rd cycle	4th cycle	5th cycle
H27U8G8T2B	3.3V	x8	ADh	D3h	14h	B6h	34h

Table 15 : Read ID Data Table

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	Description	IO7	IO6	IO5 IO4	IO3 IO2	IO1 IO0
Die / Package	1 2 4 8					0 0 0 1 1 0 1 1
Cell Type	1 bit / cell 2 bit / cell 3 bit / cell 4 bit / cell				0 0 0 1 1 0 1 1	
Number of Simultaneously Programmed Pages	1 2 4 8			0 0 0 1 1 0 1 1		
Interleave Program Between different dice	Not Supported Supported		0 1			
Write Cache	Not Supported Supported	0 1				

Table 16 : 3rd Byte of Device Identifier Description

	Description	IO7	IO6	IO5-4	IO3	IO2	IO1-0
Page Size (Without Spare Area)	1KB 2KB 4KB 8KB						0 0 0 1 1 0 1 1
Spare Area Size (Byte / 512Byte)	8 16					0 1	
Serial Access Time	50 ns 30 ns 25 ns Reserved	0 0 1 1			0 1 0 1		
Block Size (Without Spare Area)	64K 128K 256K 512KB			0 0 0 1 1 0 1 1			
Organization	X8 X16		0 1				

Table 17 : 4th Byte of Device Identifier Description

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	Description	DQ7	DQ6-5-4	DQ3-2	DQ1-0
Planes	1 2 4 8			0 0 0 1 1 0 1 1	
Plane Size (without Spare)	512Mb 1Gb 2Gb 4Gb 8Gb Reserved Reserved Reserved		0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1		
Reserved		0			00

Table 18 : 5th Byte of Device Identifier Description

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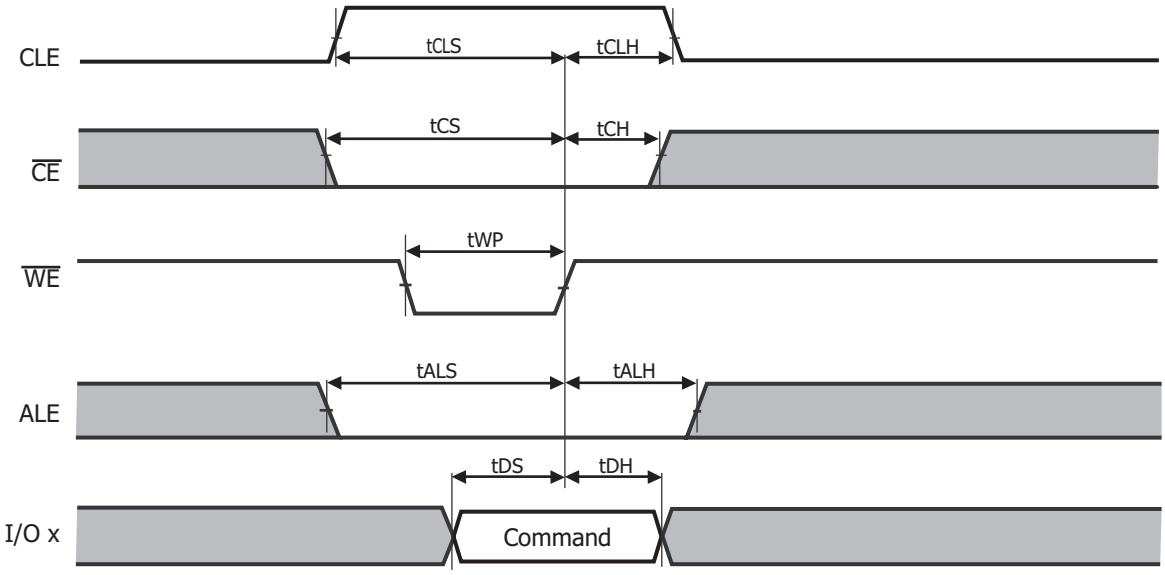

Figure 5 : Command Latch Cycle

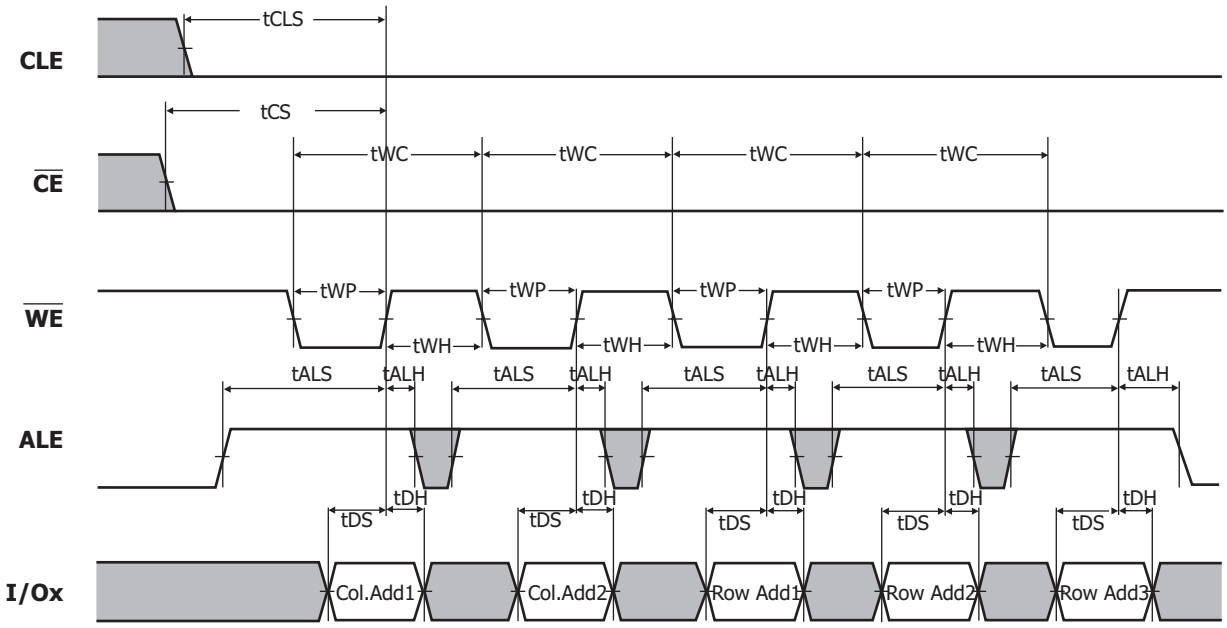

Figure 6 : Address Latch Cycle

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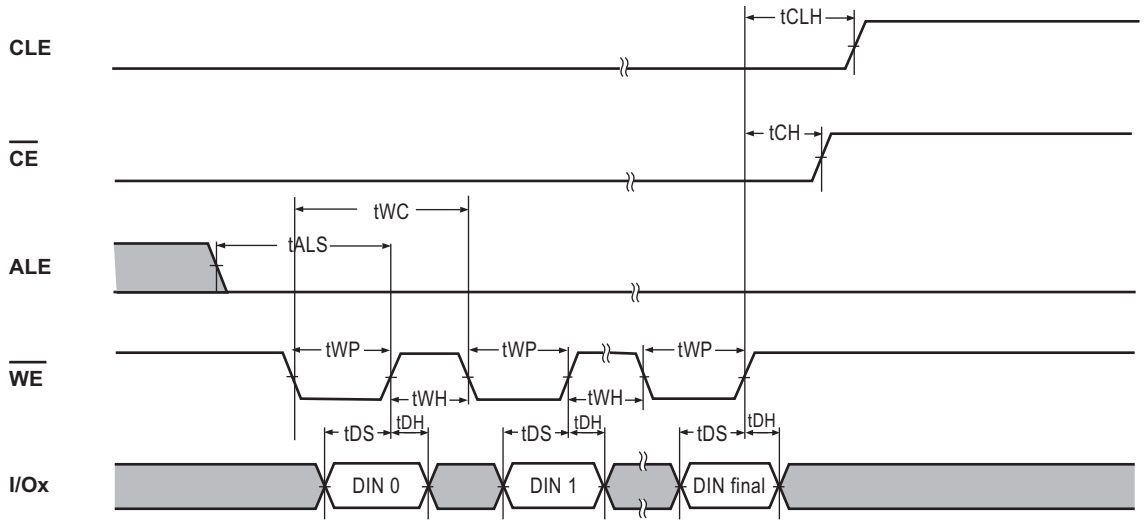
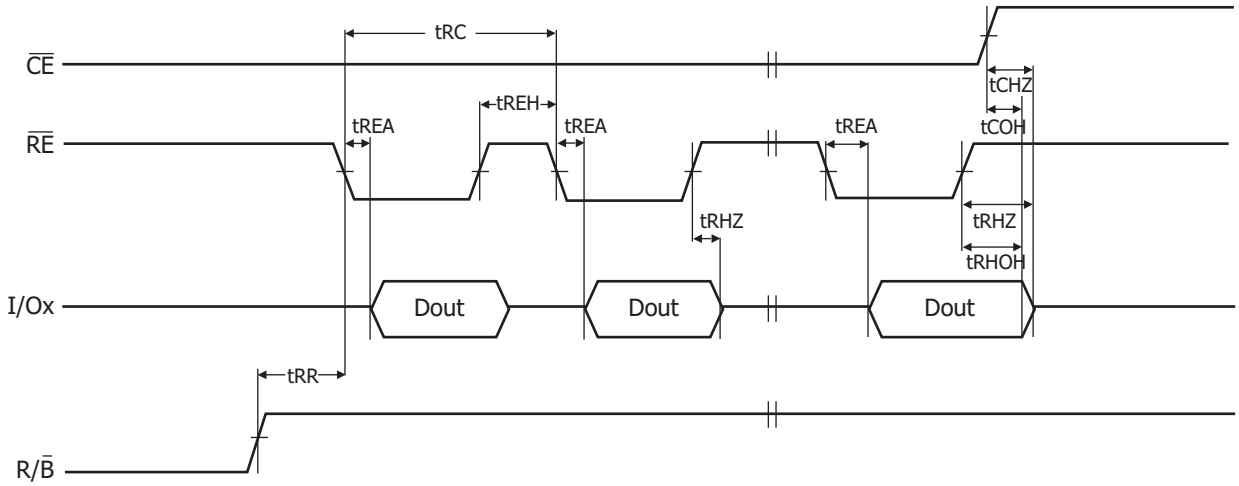


Figure 7 : Input Data Latch Cycle



Notes: Transition is measured at +/-200mV from steady state voltage with load.
This parameter is sampled and not 100% tested. (tCHZ, tRHZ)
tRHOH starts to be valid when frequency is lower than 33MHz.
tRLOH is valid when frequency is higher than 33MHz

Figure 8 : Sequential Out Cycle after Read (CLE = L, $\overline{WE}$ = H, ALE = L)

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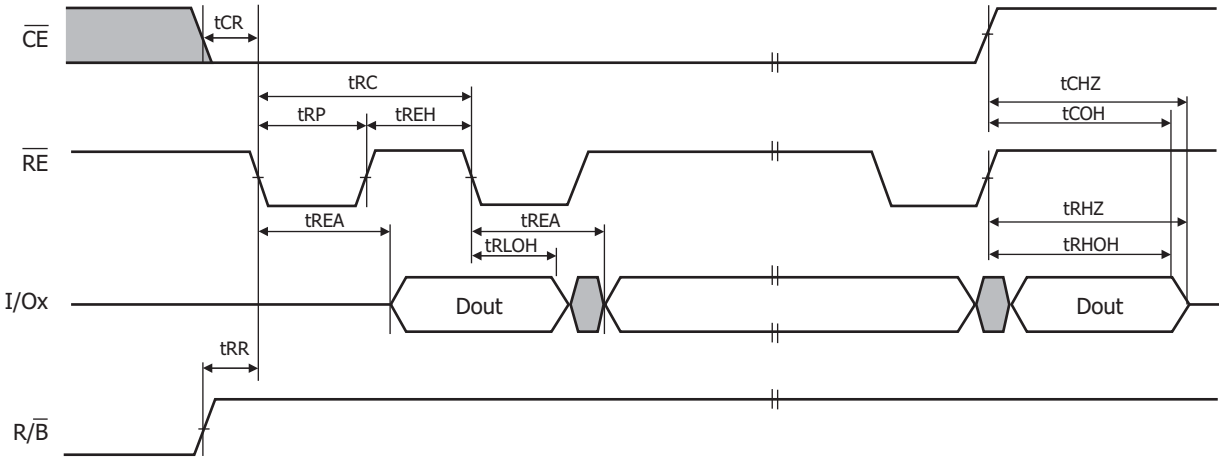

Notes: Transition is measured at +/-200mV from steady state voltage with load.
This parameter is sampled and not 100% tested. (tCHZ, tRHZ)
tRLOH is valid when frequency is higher than 33MHz.
tRHOH starts to be valid when frequency is lower than 33MHz.

Figure 9 : Sequential Out Cycle after Read (EDO type CLE = L, $\overline{WE}$ = H, ALE = L)

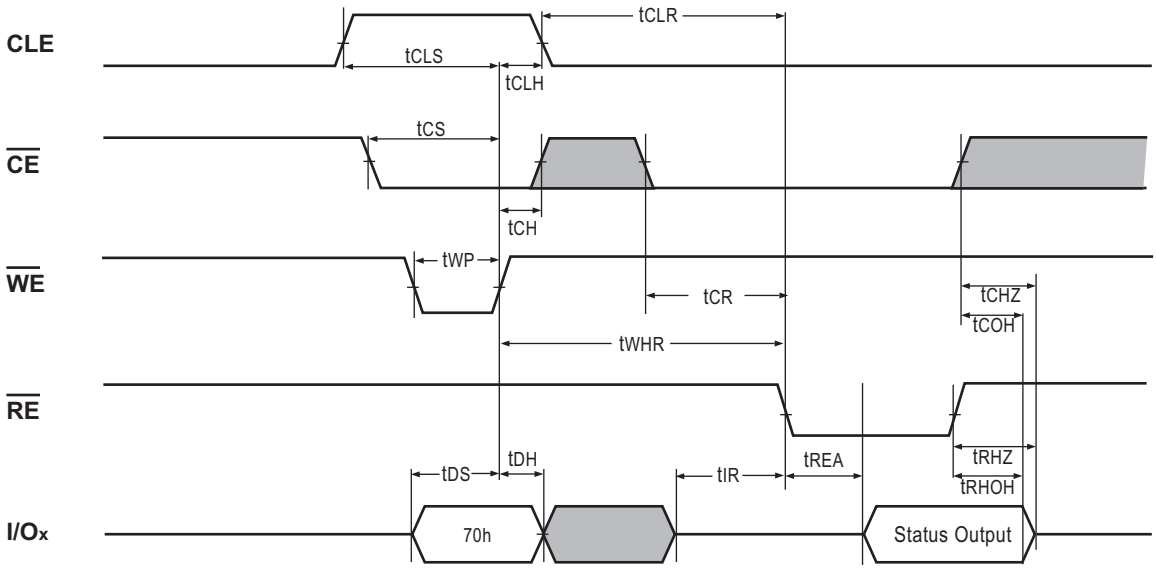

Figure 10 : Read Status Register

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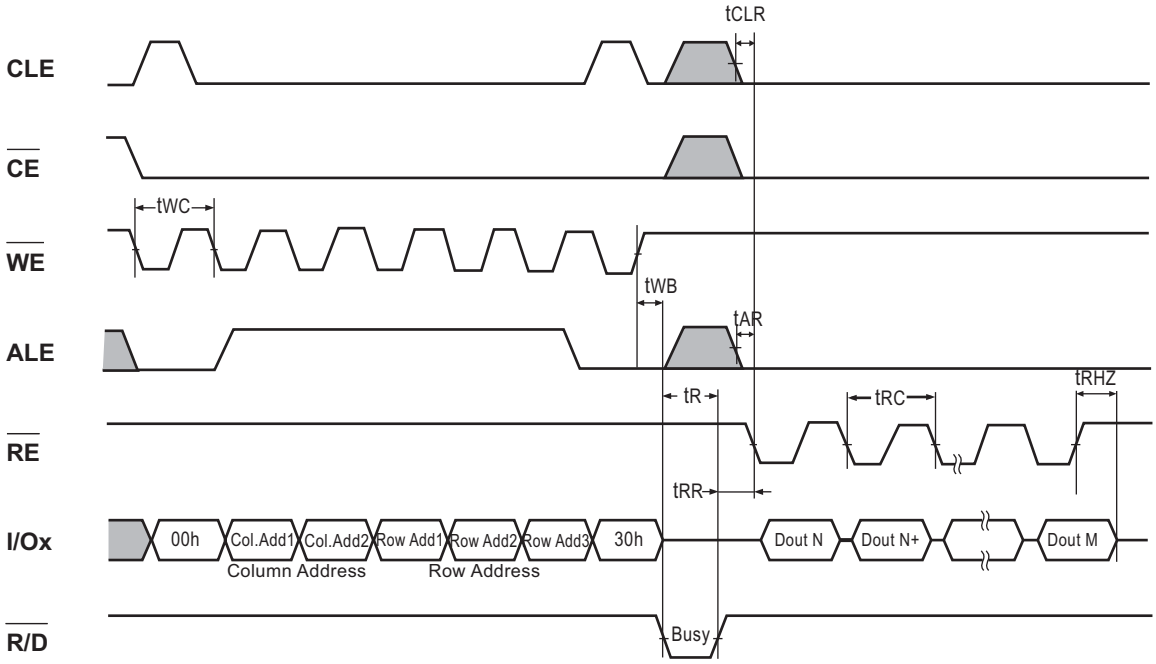

Figure 11 : Page Read Operation

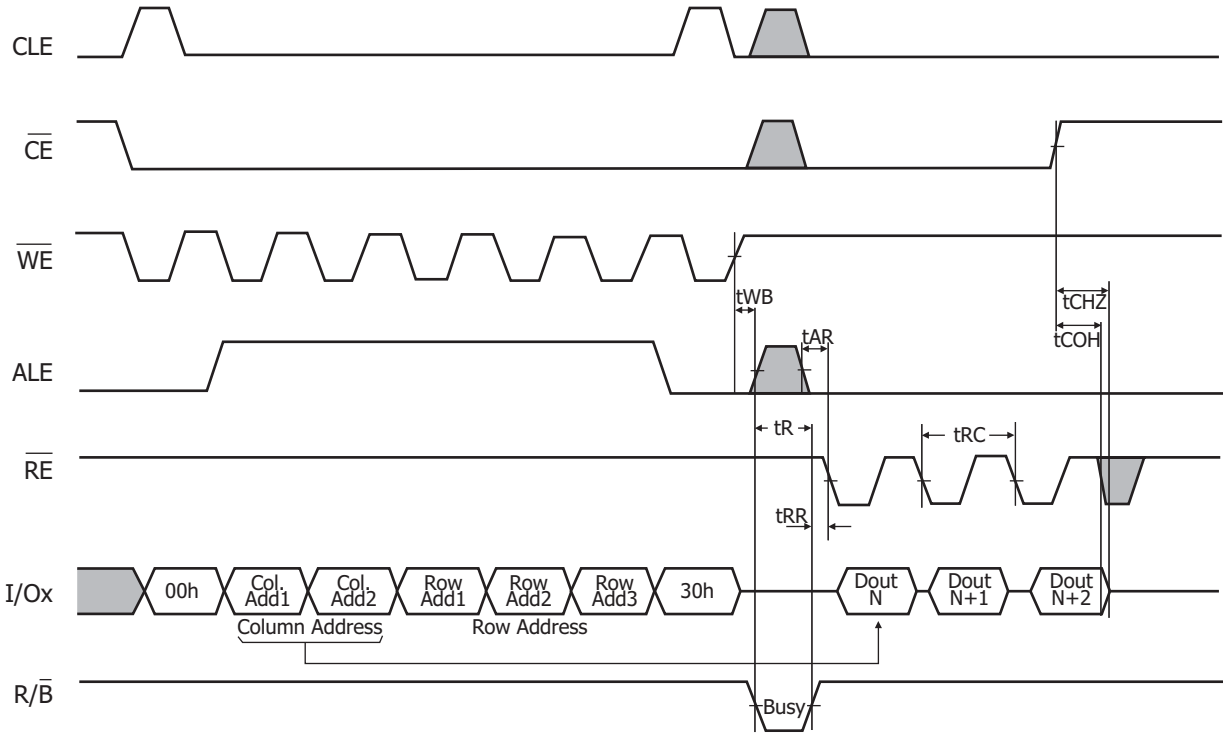

Figure 12 : Page Read Operation (Intercepted by $\overline{CE}$)

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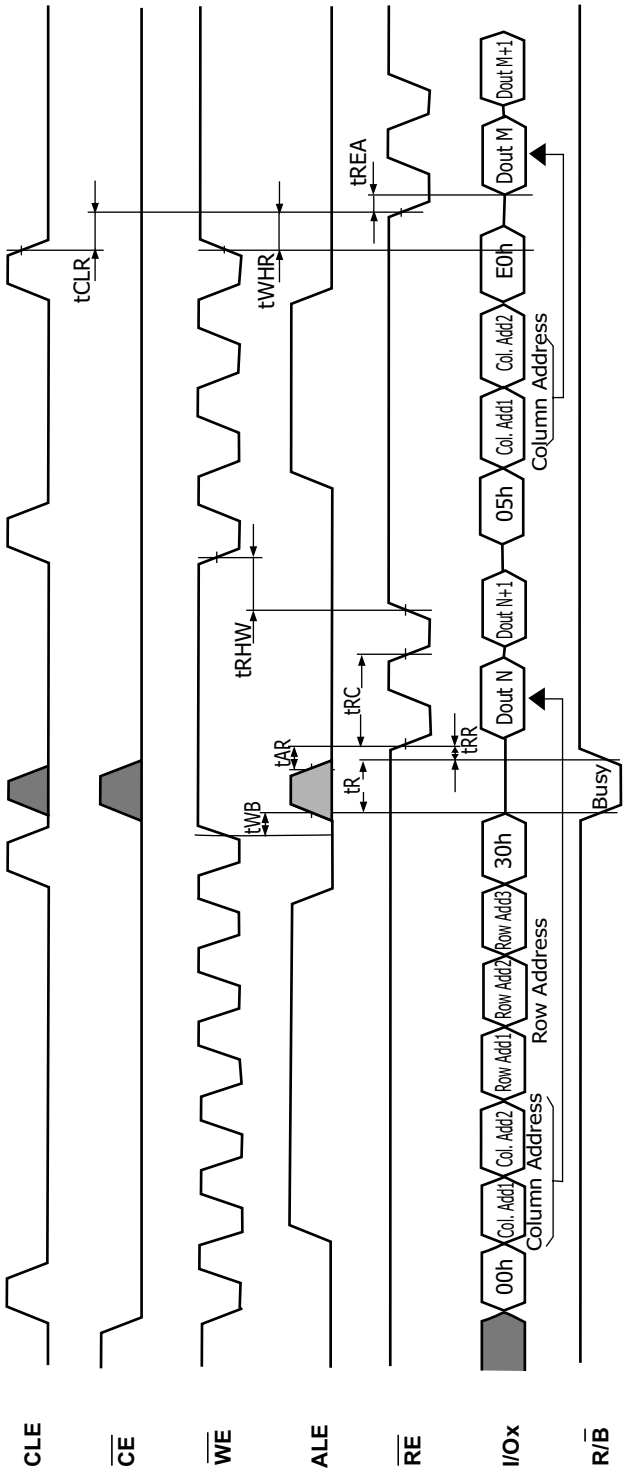

Figure 13 : Random Data Output

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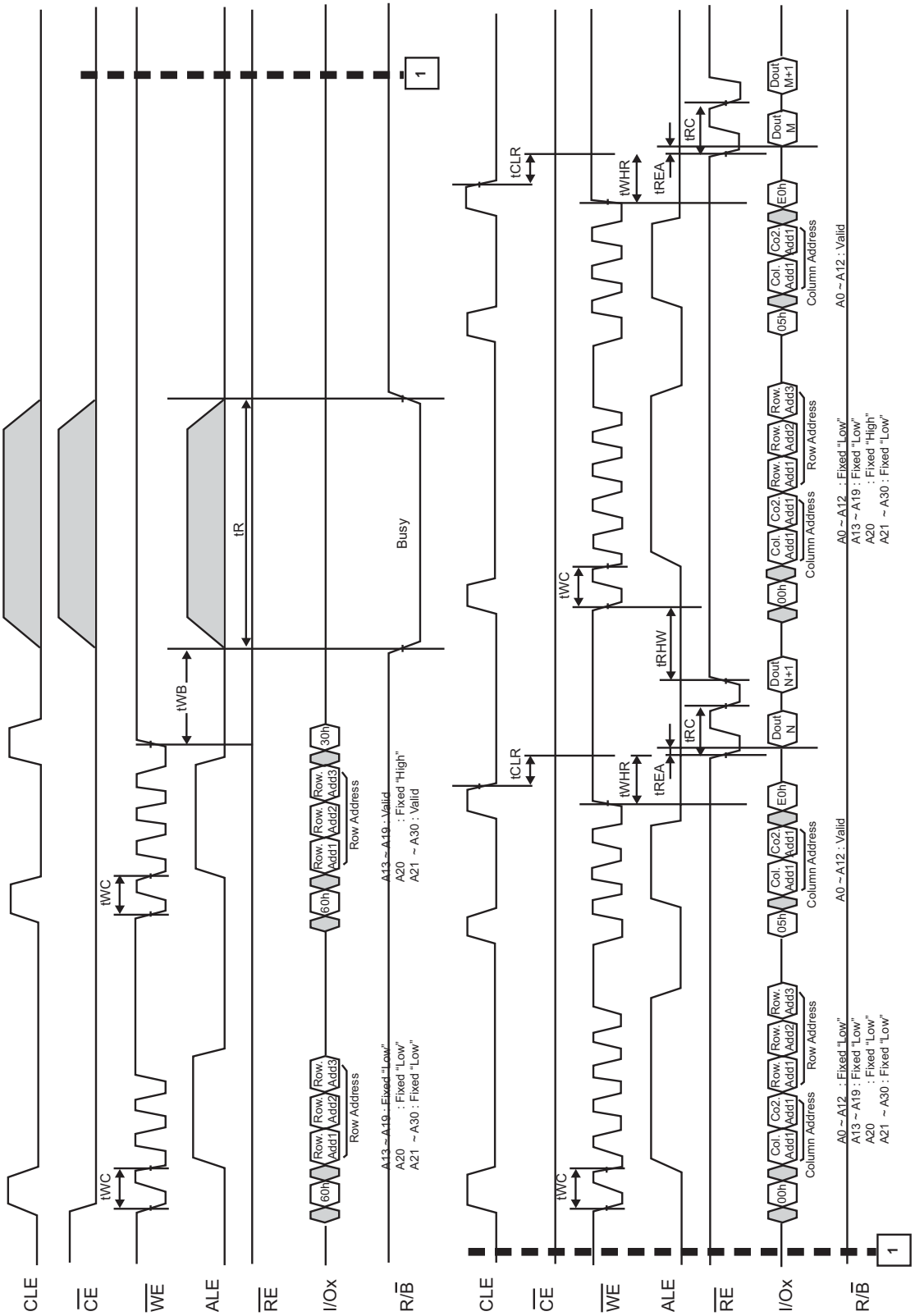

Figure 14 : Multiplane Read Operation with Random Data Output

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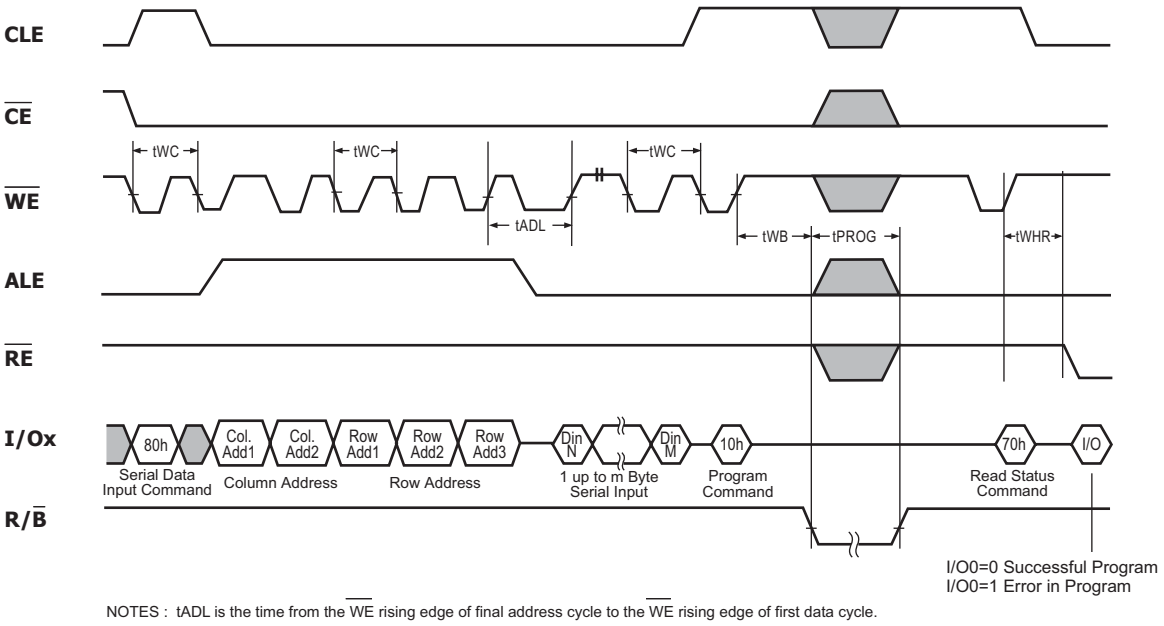

NOTES : tADL is the time from the WE rising edge of final address cycle to the WE rising edge of first data cycle.

Figure 15 : Page Program Operation

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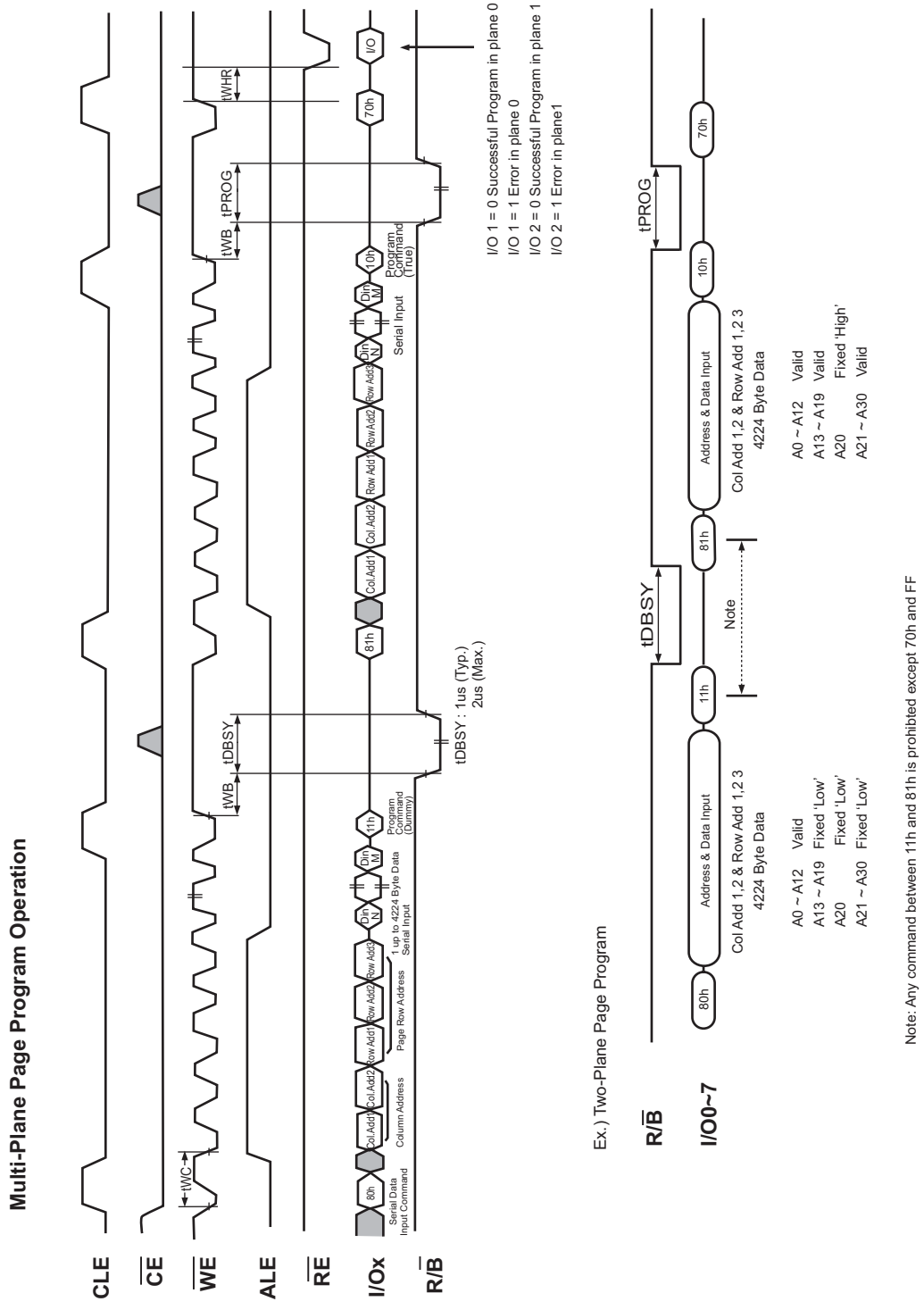

Figure 16 : Multiplane Page Program

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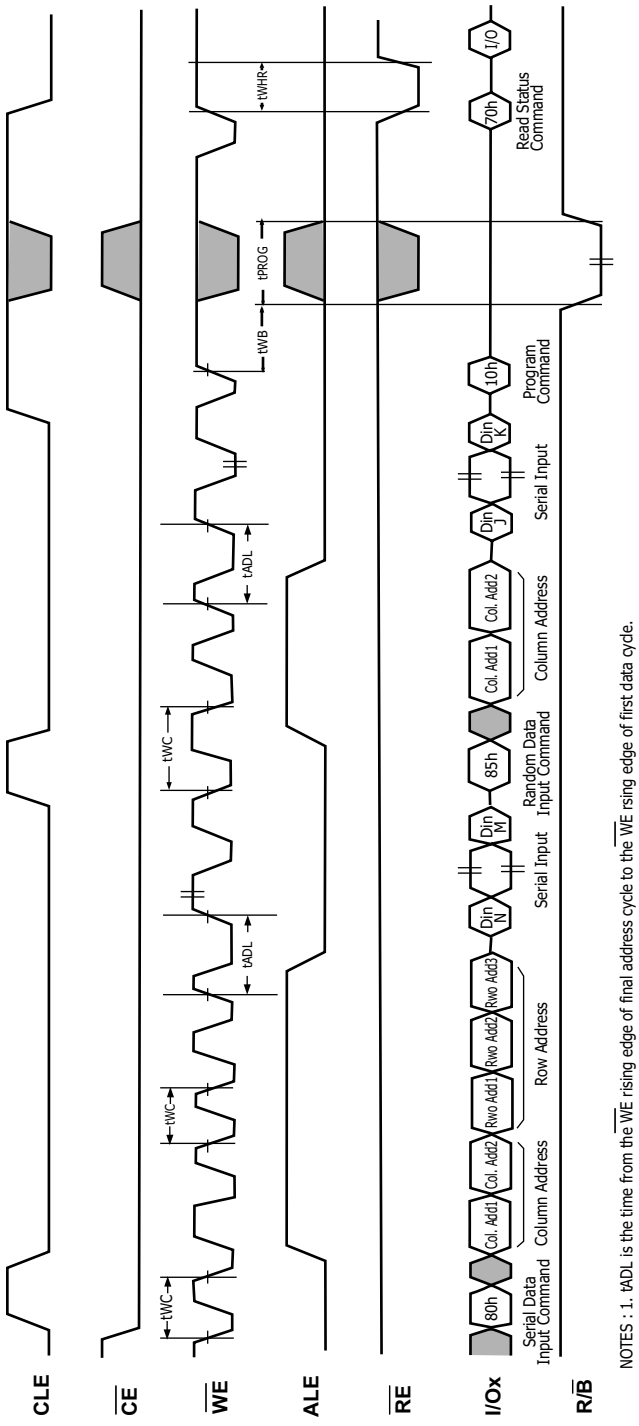

Figure 17 : Random Data Input

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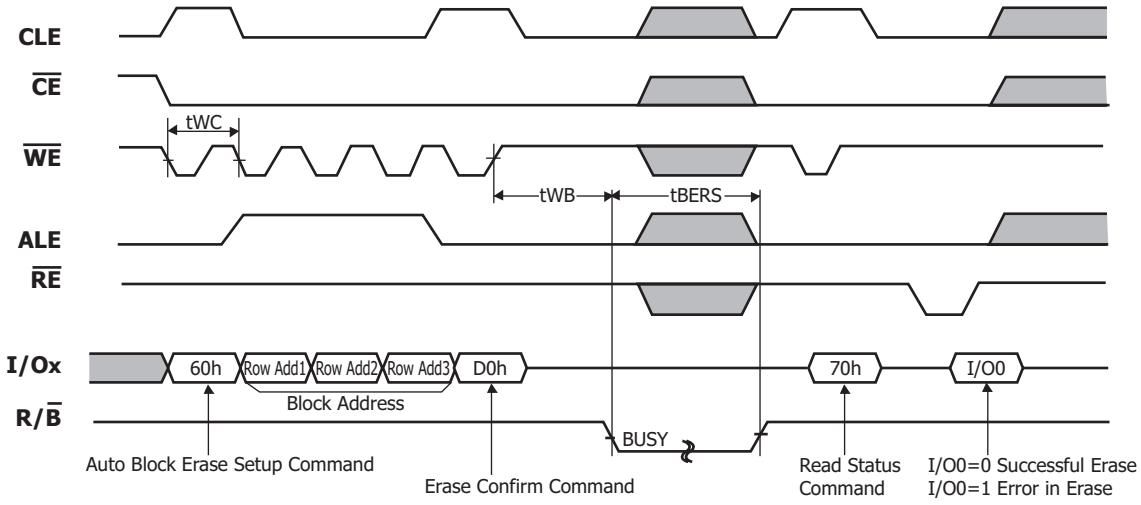

Figure 18 : Block Erase

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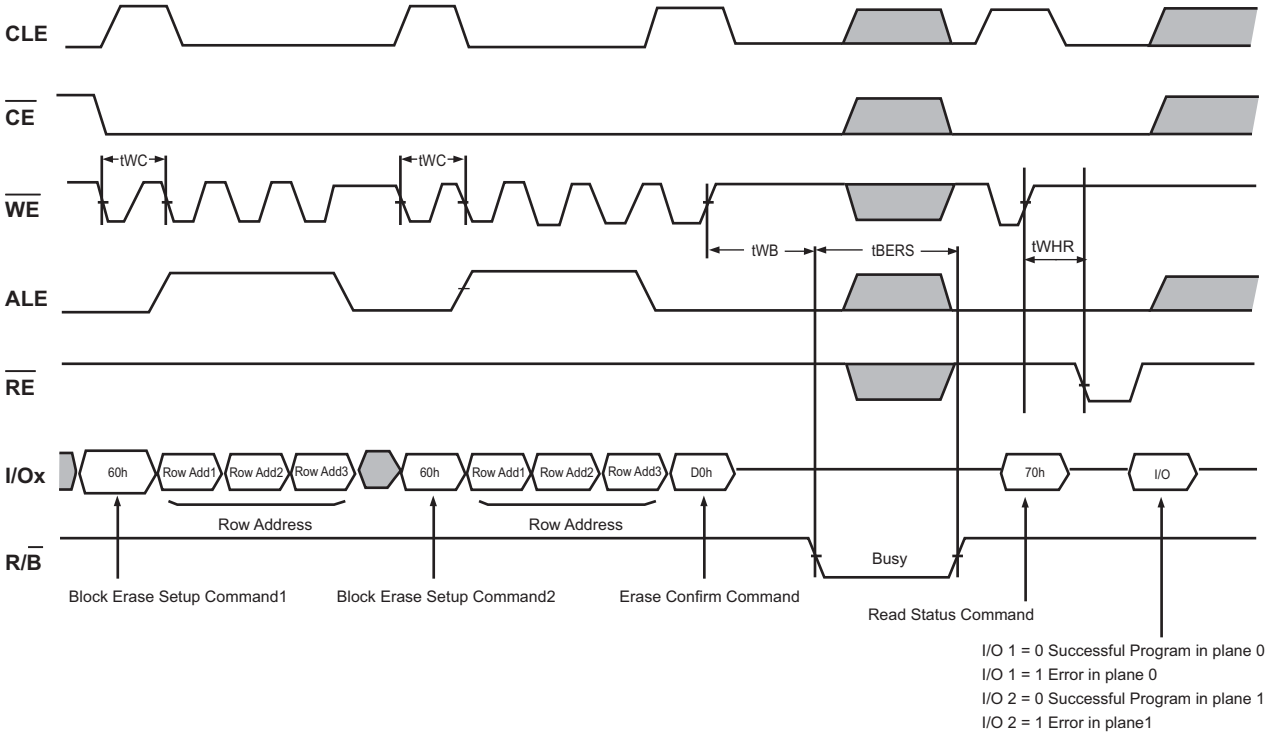

Ex.) Address Restriction for Multi-Plane Block Erase Operation

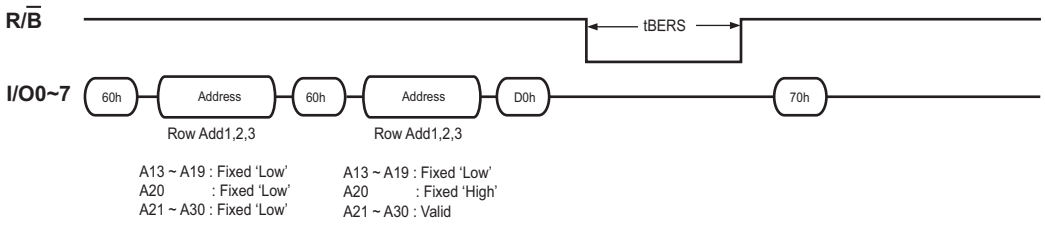

Figure 19 : Multiplane Block Erase

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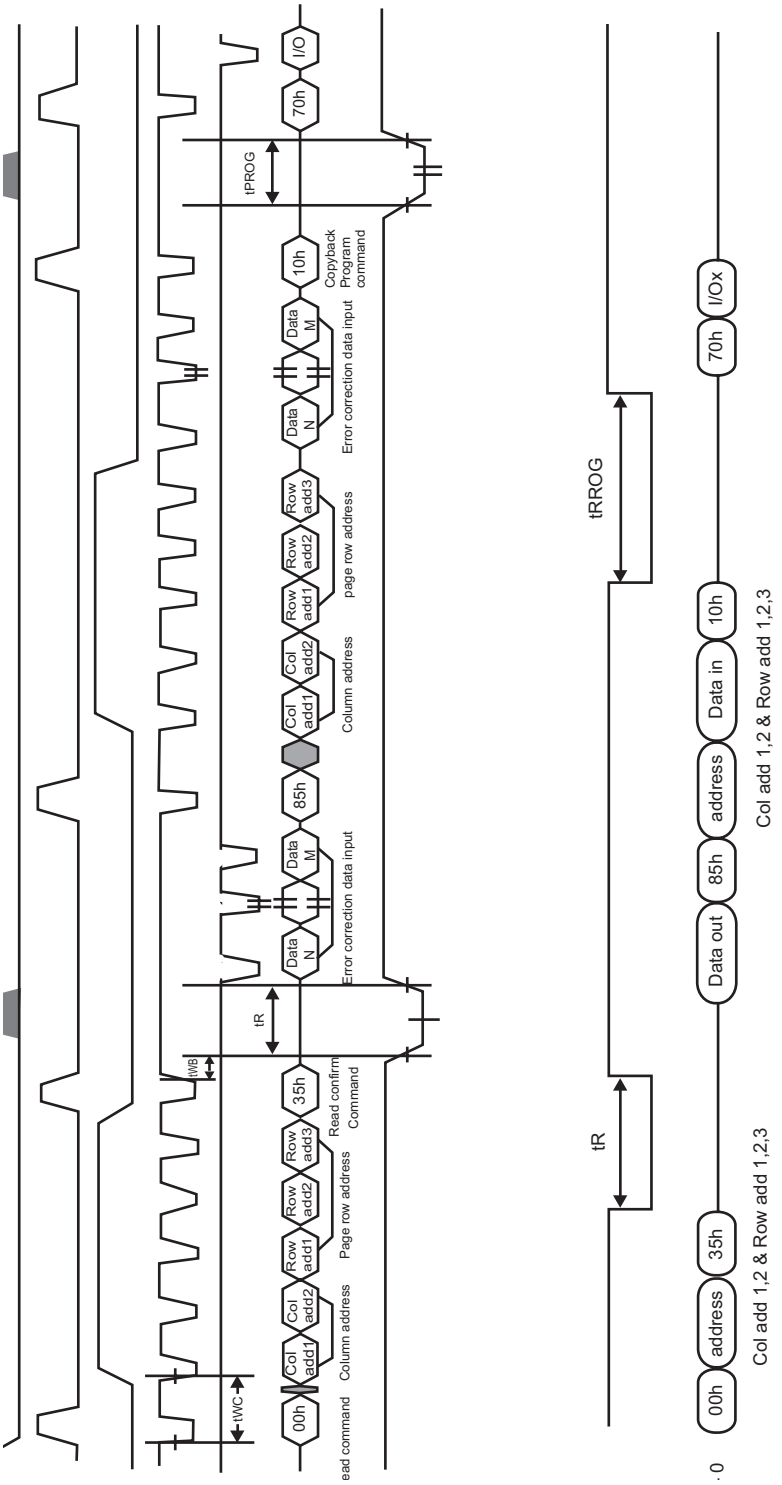

Figure 20 : Copy Back Program Operation

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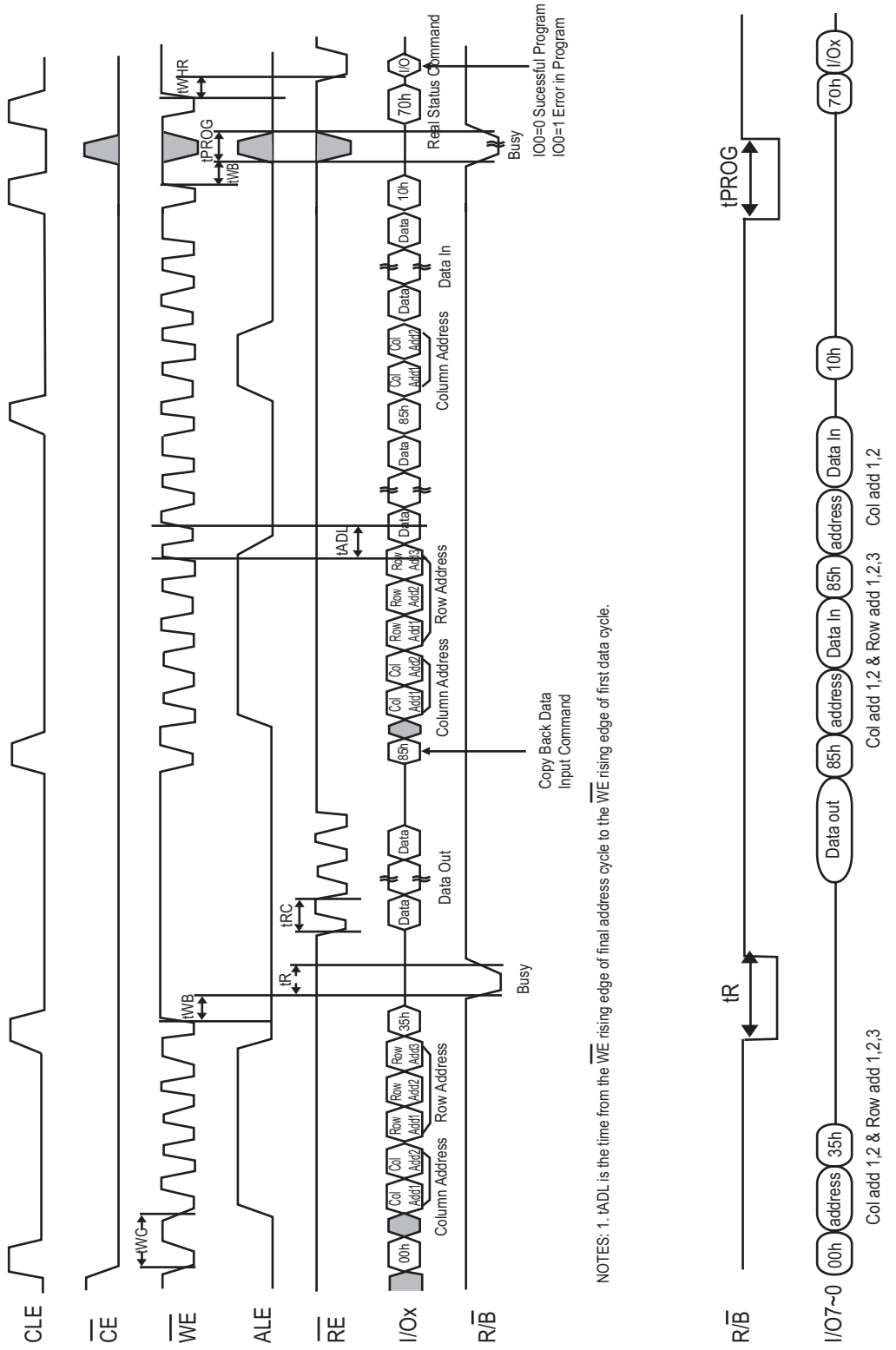

Figure 21 : Copy Back with Random Data Input

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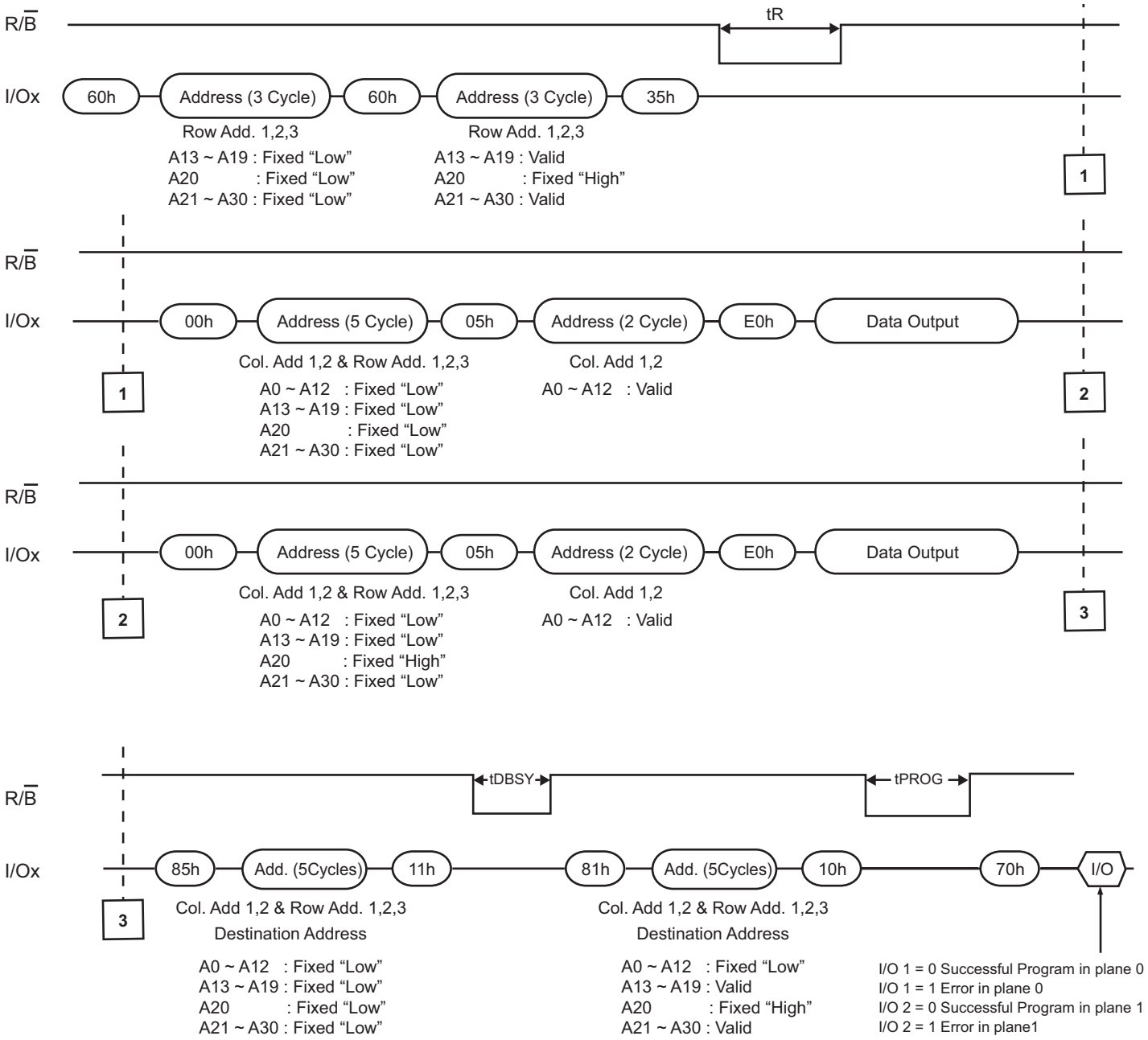

Figure 22 : Multiplane Copy Back

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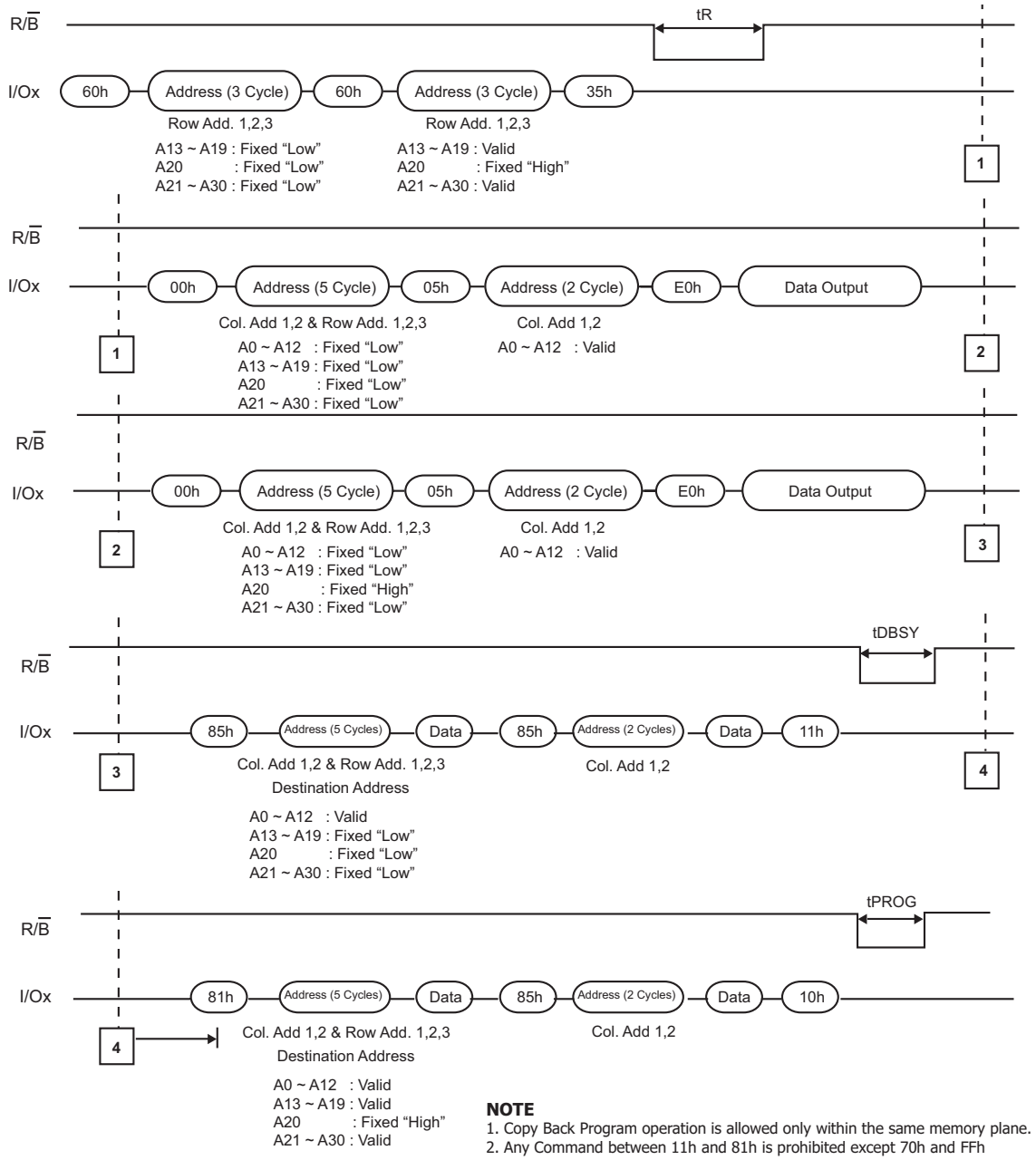

Figure 23 : Multiplane Copy Back with Random Data Input

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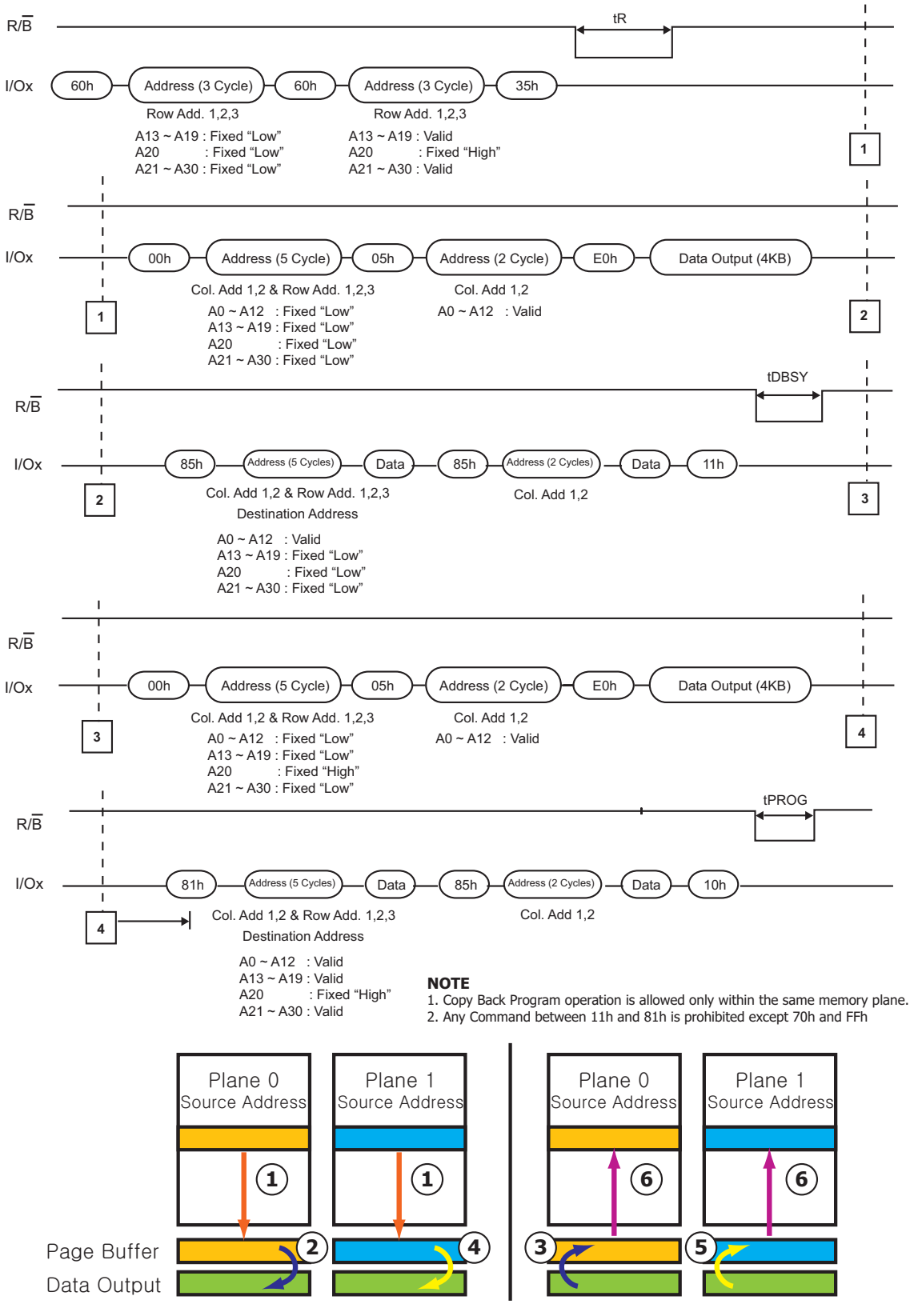

Figure 24 : Multiplane Copy Back for 4 KB buffer

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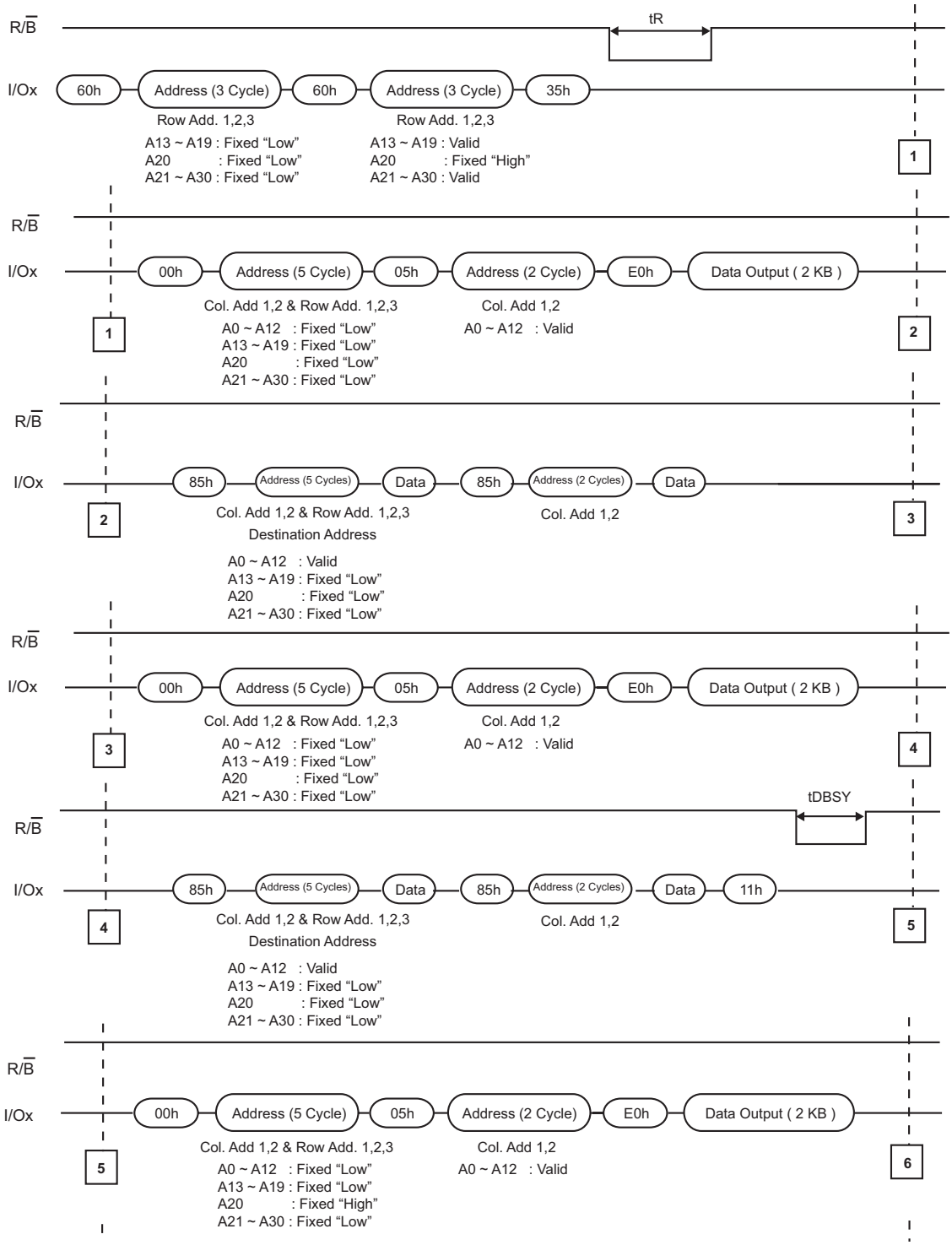

Figure 25 : Multi-Plane Copy Back for 2 KB buffer (1)

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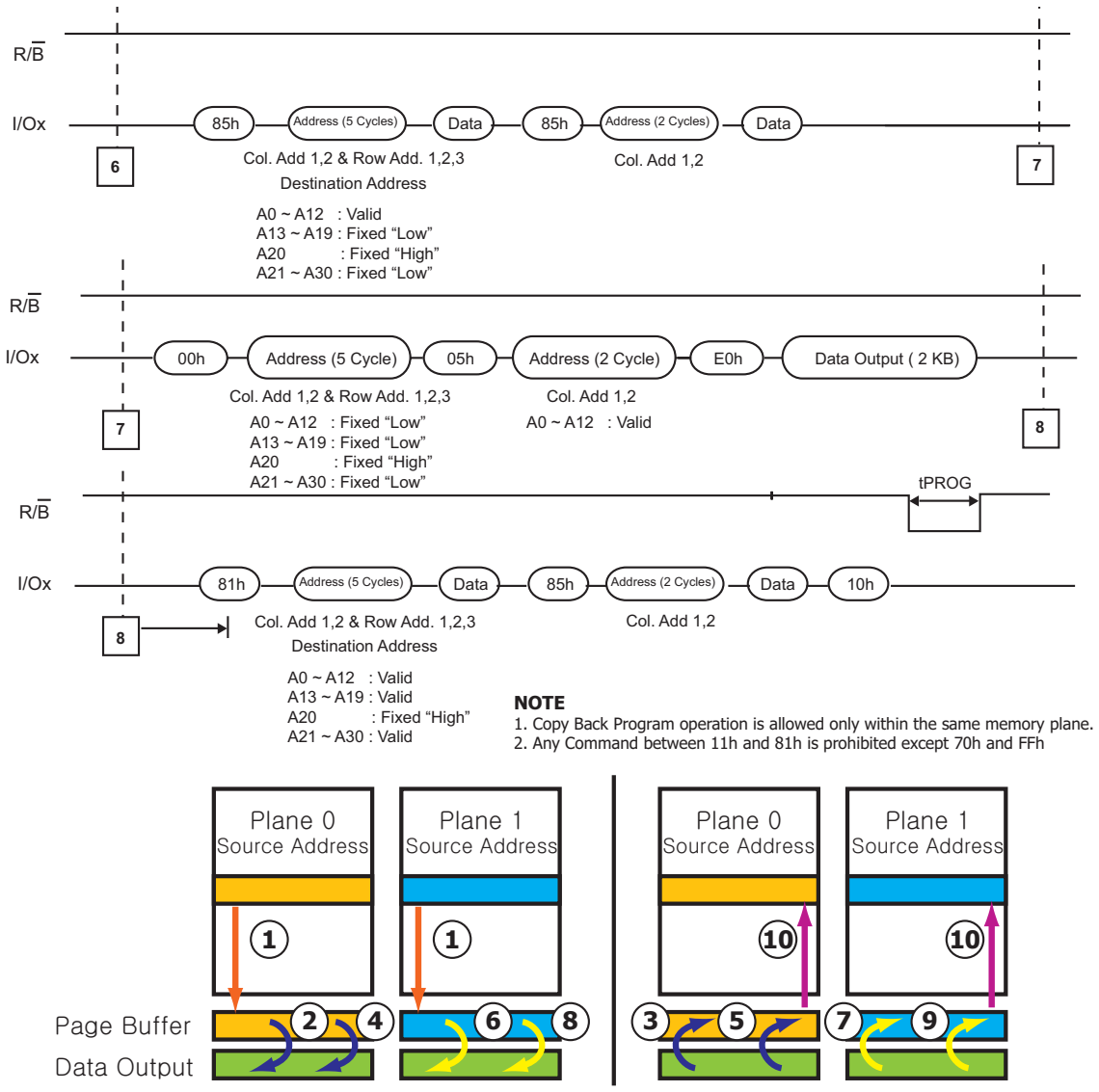

Figure 25 : Multi-Plane Copy Back for 2 KB buffer (2)

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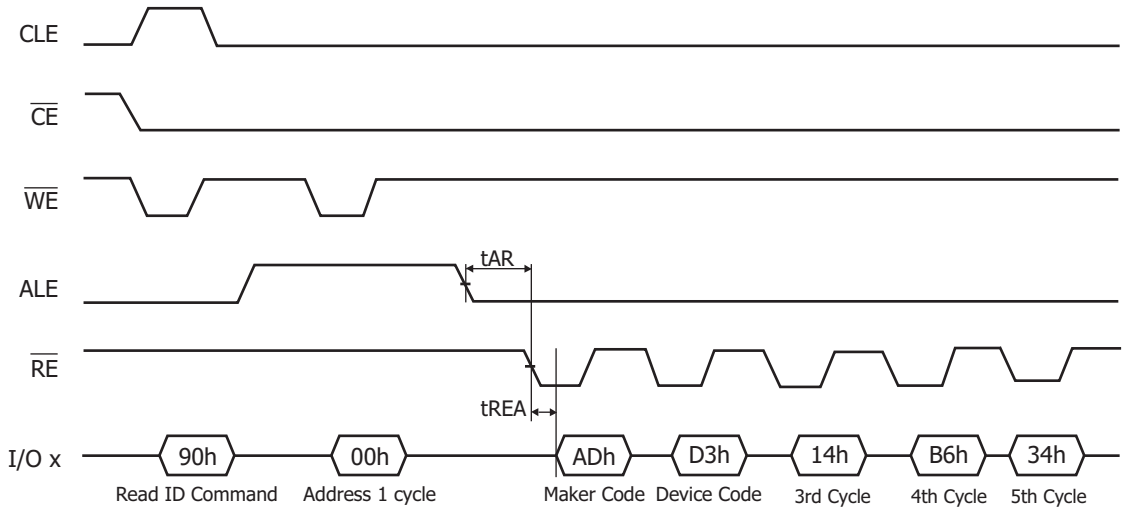

Figure 26 : Read ID

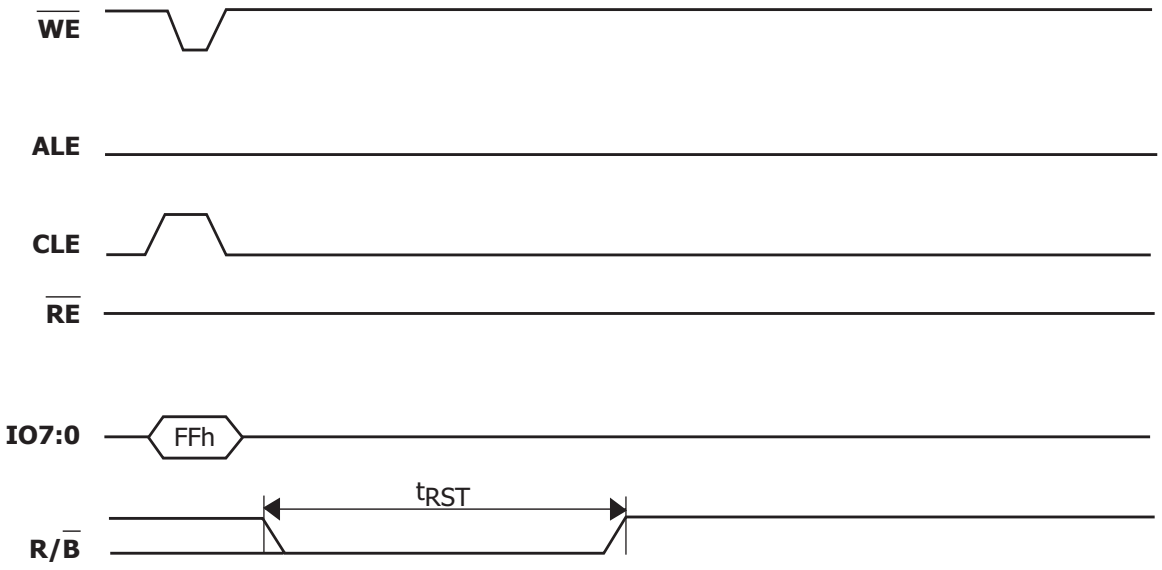

Figure 27 : Reset Operation

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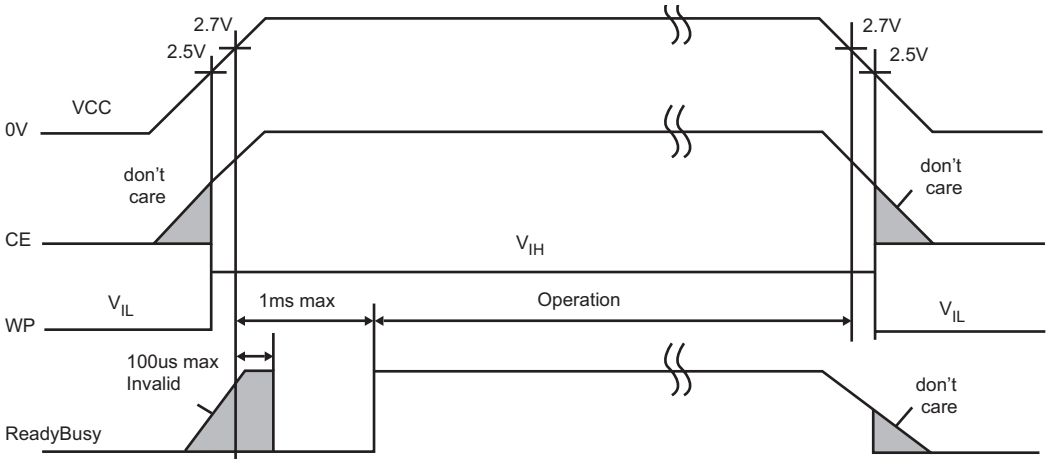

Figure 28 : Power on and Data Protection Timing

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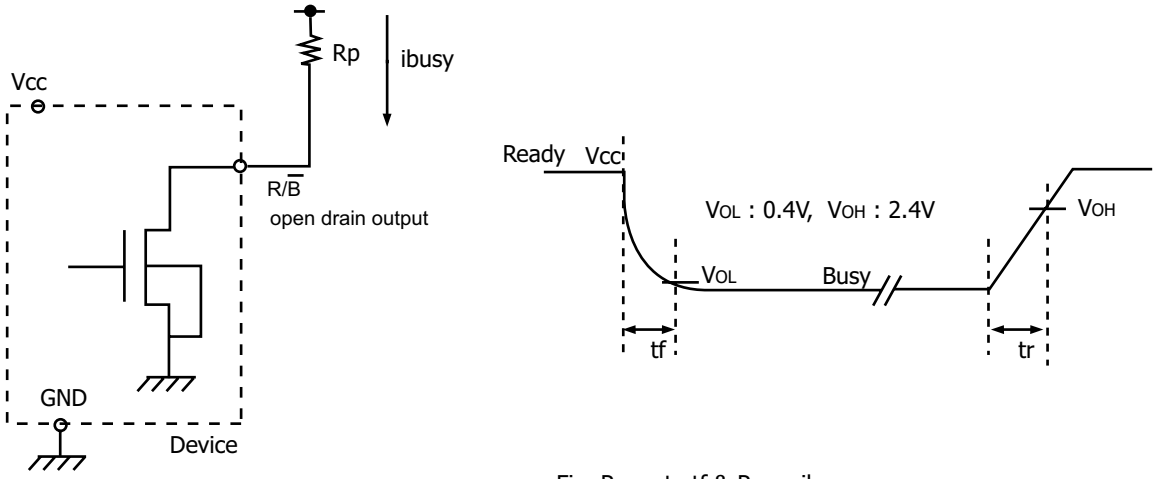
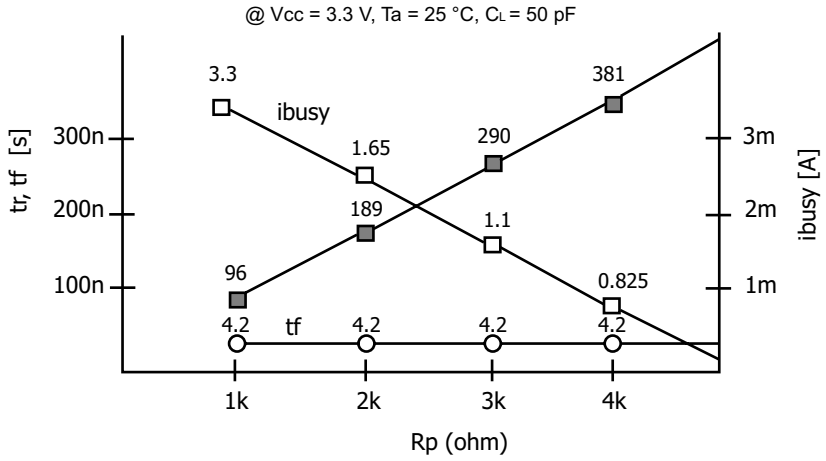


Fig. Rp vs tr, tf & Rp vs ibusy



Rp value guidence

$$Rp\ (min) = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \sum I_L} = \frac{3.2V}{8mA + \sum I_L}$$

where IL is the sum of the input currnts of all devices tied to the R/$\overline{B}$ pin.

Rp(max) is determined by maximum permissible limit of tr

Figure 29 : Ready / Busy Pin Electrical Specifications

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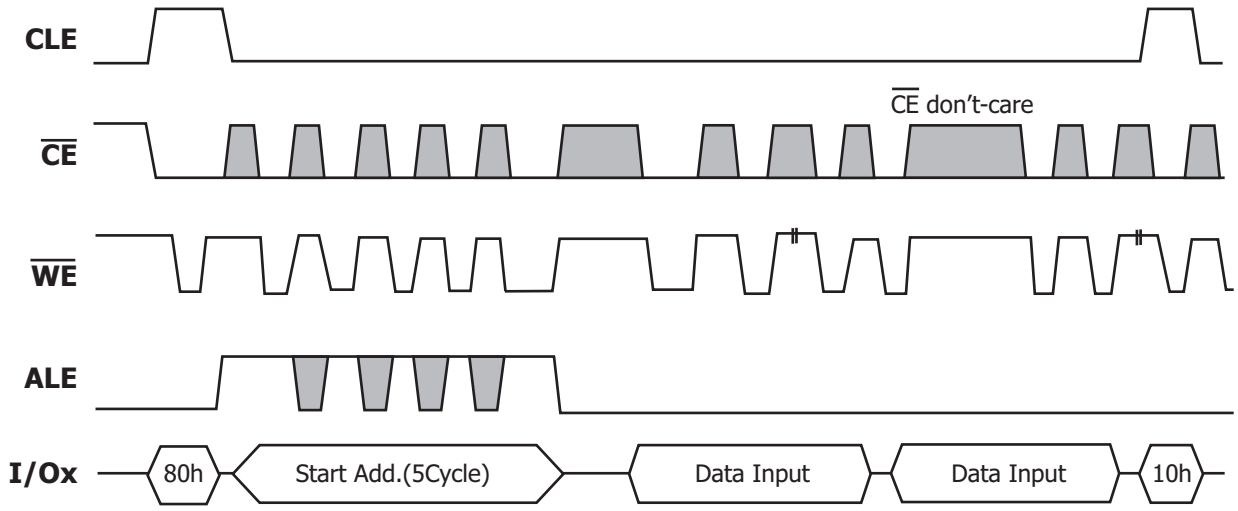

Figure 30 : Program Operation with CE don't care

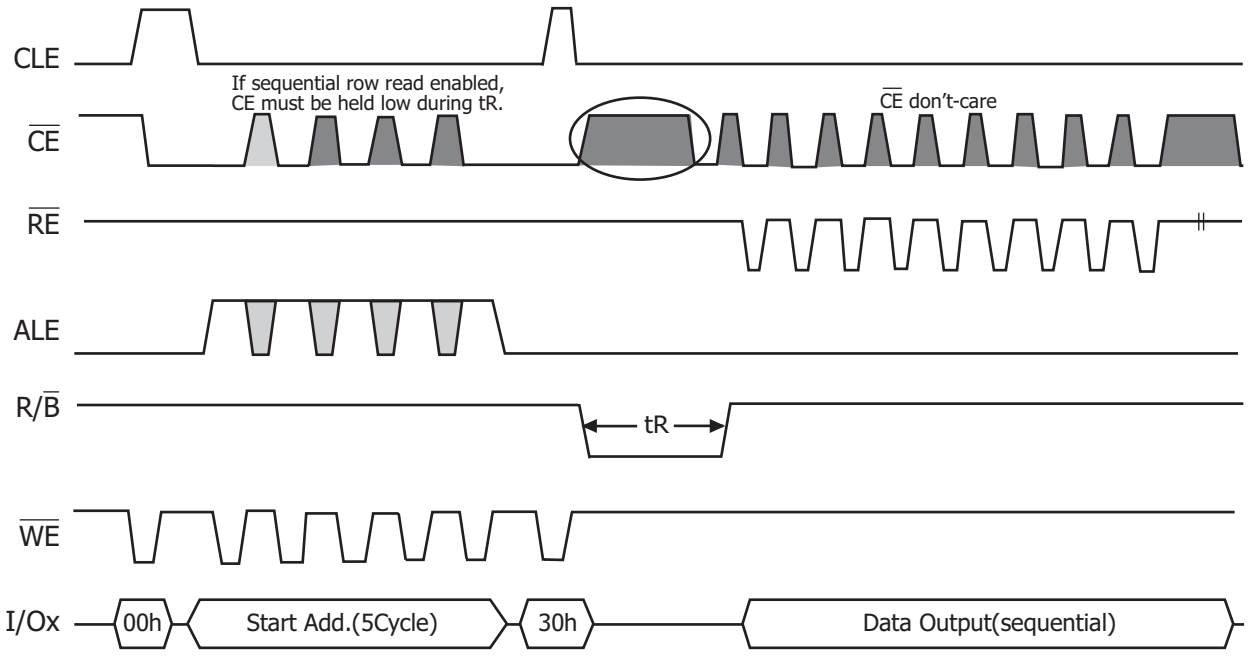

Figure 31 : Read Operation with CE don't care

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Bad Block Management

Devices with bad blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erase (FFh). The Bad Block Information is written prior to shipping. Any block where the 1st byte in the spare area of the Last or (Last-2)th page (if the last page is bad) does not contain FFh is a Bad Block. The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flowchart shown in Figure 32. The 1st block, which is placed on 00h address, is guaranteed to be a valid one.

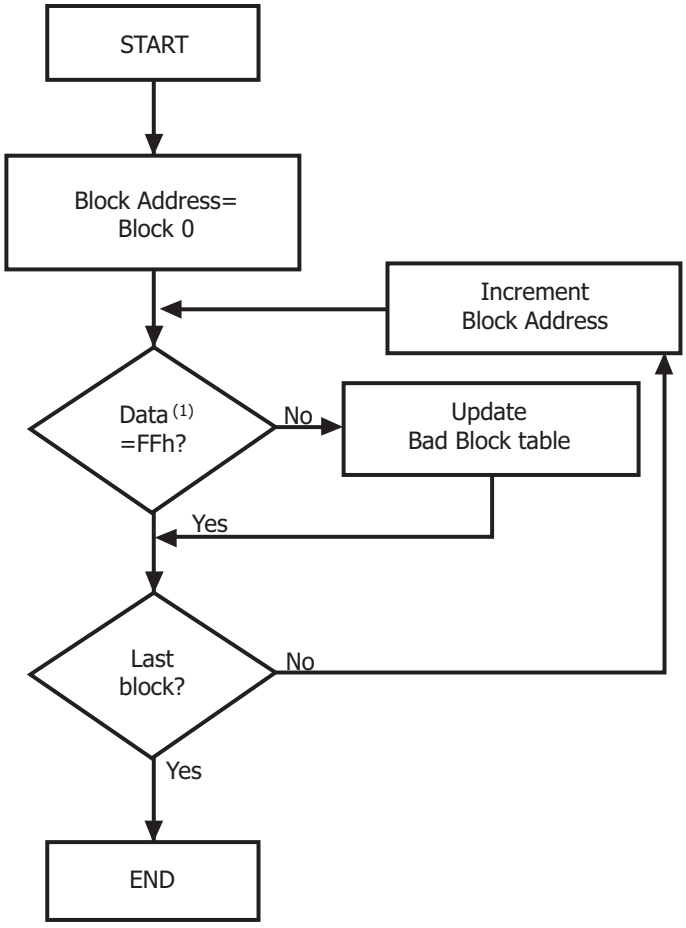

Figure 32 : Bad Block Management Flowchart

NOTE :
- Make sure that FFh at the column address 4,096 of the last page and last-2th page

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Bad Block Replacement

Over the lifetime of the device additional Bad Blocks may develop. In this case the block has to be replaced by copying the data to a valid block. These additional Bad Blocks can be identified as attempts to program or erase them will give errors in the Status Register.

The failure of a page program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block.

Refer to Table 19 and Figure 33 for the recommended procedure to follow if an error occurs during an operation.

Operation	Recommended Procedure
Erase	Block Replacement
Program	Block Replacement
Read	ECC (with 4 bits / 512 bytes)

Table 19 : Block Failure

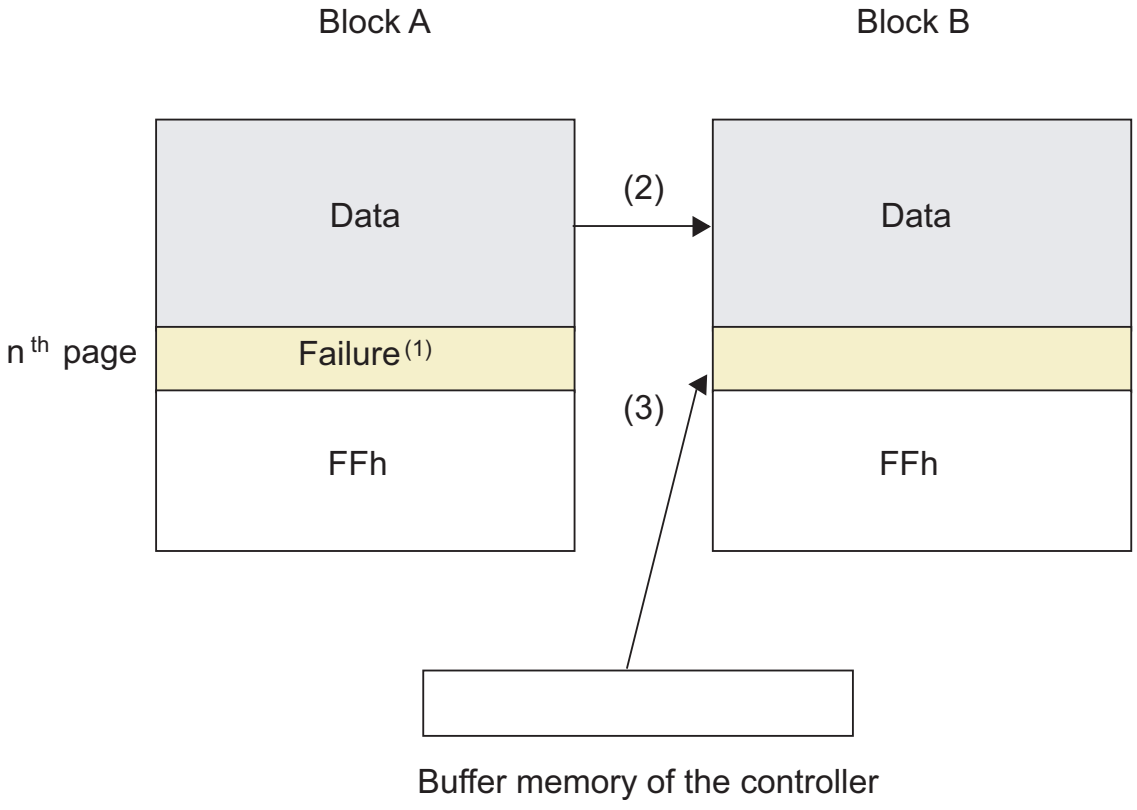

Figure 33 : Bad Block Replacement

NOTE :
1. An error occurs on the Block A during program or erase operation.
2. Data in Block A is copied to same location in Block B which is valid block.
3. N^{th} data of block A which is in controller buffer memory is copied into n^{th} page of Block B
4. Bad block table should be updated to prevent from erasing or programming Block A

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Write Protect Operation

The Erase and Program Operations are automatically reset when $\overline{WP}$ goes Low (tWW = 100ns, min). The operations are enabled and disabled as follows (Figure 34~37)

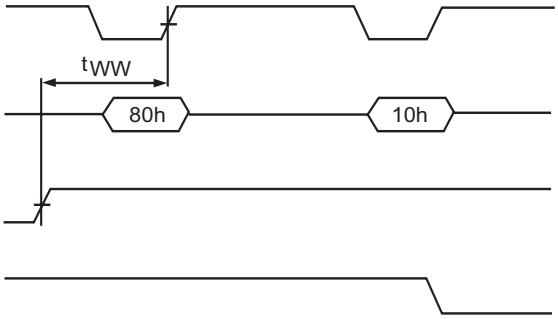

Figure 34 : Enable Programming

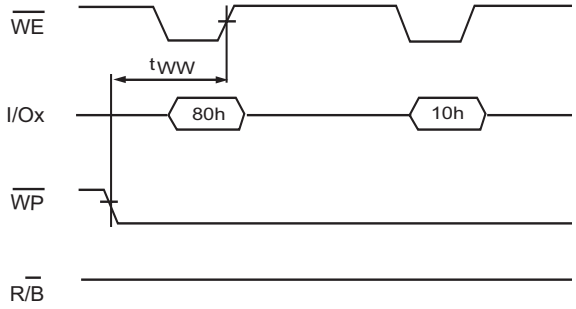

Figure 35 : Disable Programming

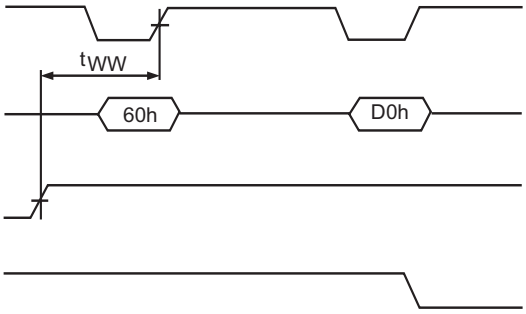

Figure 36 : Enable Erasing

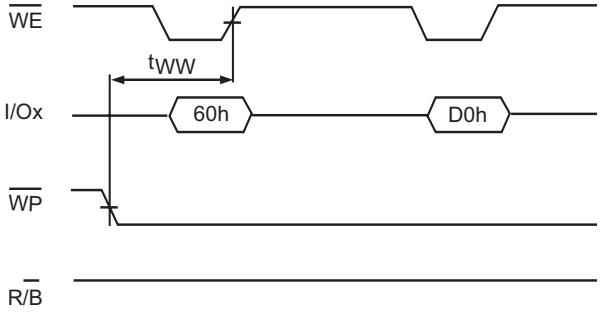

Figure 37 : Disable Erasing

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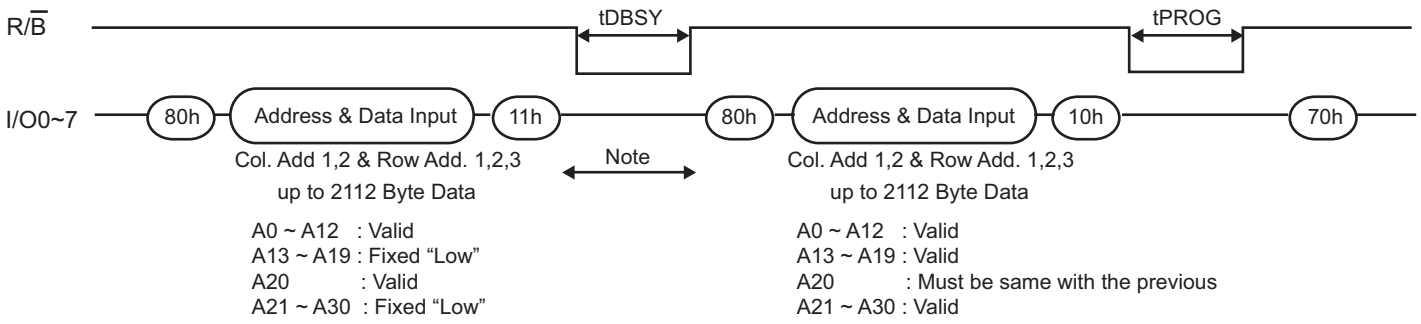
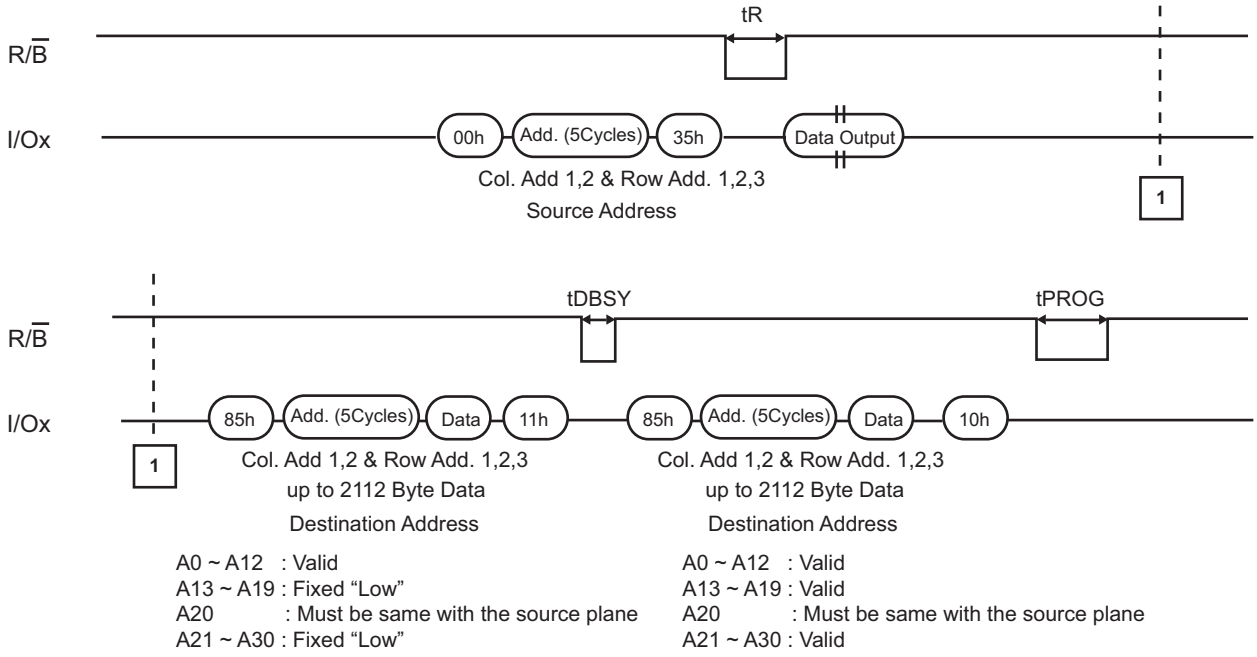
The Backward Compatibility (2KByte/page operation)

1. Page Program



Note :
Any command between 11h and 80h is prohibited except 70h and FFh.

2. Copy Back Program



Note:
1. Copy-Back Program operation is allowed only within the same memory plane.
2. Any command between 11h and 85h is prohibited except 70h/F1h and FFh.
3. On the same plane, it's prohibited to operate copy-back program from an odd address page(source page) to an even address page(target page) or from an even address page(source page) to an odd page(target page). Therefore, the copy-back program is permitted just between odd address pages or even address pages

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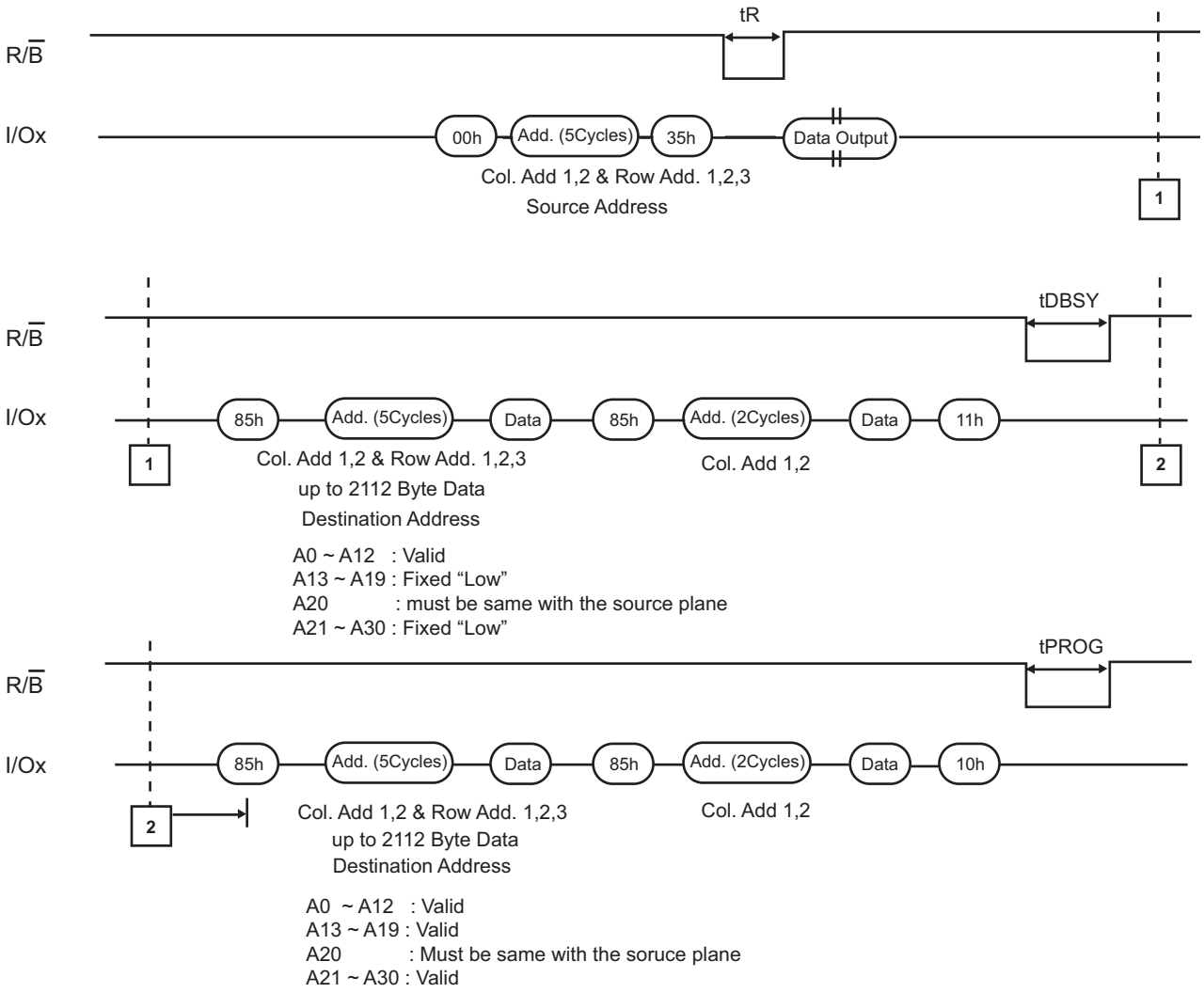
3. Copy back program with random data input



Note:

1. Copy-Back Program operation is allowed only within the same memory plane.
2. Any command between 11h and 85h is prohibited except 70h/F1h and FFh.
3. On the same plane, it's prohibited to operate copy-back program from an odd address page(source page) to an even address page(target page) or from an even address page(source page) to an odd page(target page). Therefore, the copy-back program is permitted just between odd address pages or even address pages

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Paired Page Address Information

Paired Page Address		Paired Page Address	
Group A	Group B	Group A	Group B
ooh	04h	01h	05h
02h	08h	03h	09h
06h	0Ch	07h	0Dh
0Ah	10h	0Bh	11h
0Eh	14h	0Fh	15h
12h	18h	13h	19h
16h	1Ch	17h	1Dh
1Ah	20h	1Bh	21h
1Eh	24h	1Fh	25h
22h	28h	23h	29h
26h	2Ch	27h	2Dh
2Ah	30h	2Bh	31h
2Eh	34h	2Fh	35h
32h	38h	33h	39h
36h	3Ch	37h	3Dh
3Ah	40h	3Bh	41h
3Eh	44h	3Fh	45h
42h	48h	43h	49h
46h	4Ch	47h	4Dh
4Ah	50h	4Bh	51h
4Eh	54h	4Fh	55h
52h	58h	53h	59h
56h	5Ch	57h	5Dh
5Ah	60h	5Bh	61h
5Eh	64h	5Fh	65h
62h	68h	63h	69h
66h	6Ch	67h	6Dh
6Ah	70h	6Bh	71h
6Eh	74h	6Fh	75h
72h	78h	73h	79h
76h	7Ch	77h	7Dh
7Ah	7Eh	7Bh	7Fh

Note: When program operation is abnormally aborted (ex. power-down, reset), not only page data under program but also paired page data may be damaged.

Table 20 : Paired Page Address Information

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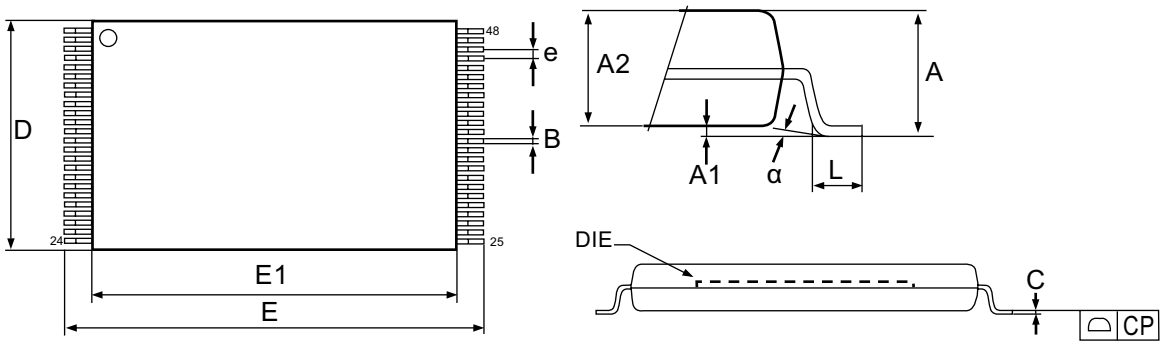

Figure 38 : 48-TSOP1 - 48-lead Plastic Thin Small Outline, 12 x 20mm, Package Outline

Symbol	millimeters		
	Min	Typ	Max
A			1.200
A1	0.050		0.150
A2	0.980		1.030
B	0.170		0.250
C	0.100		0.200
CP			0.100
D	11.910	12.000	12.120
E	19.900	20.000	20.100
E1	18.300	18.400	18.500
e		0.500	
L	0.500		0.680
alpha	0		5

Table 21 : 48-TSOP1 - 48-lead Plastic Thin Small Outline, 12 x 20mm, Package Mechanical Data

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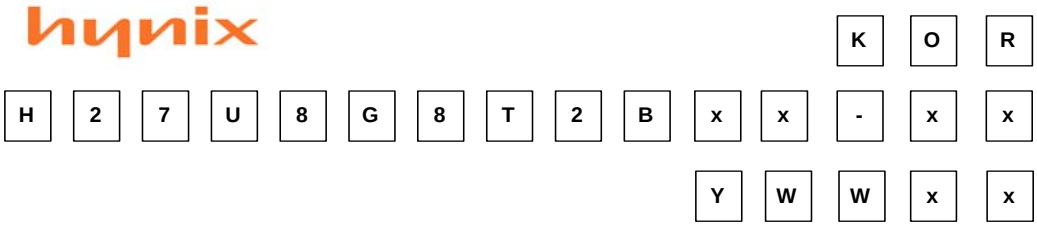
MARKING INFORMATION - TSOP1

Marking Example



- hynix	: Hynix Symbol
- KOR	: Origin Country
- H27U8G8T2Bxx-xx	: Part Number
H: Hynix	
27: NAND Flash	
U: Power Supply	: U (2.7 V~3.6 V)
8G: Density	: 8 Gbit
8 : Bit Organization	: 8(x8)
T: Classification	: Multi Level Cell+Single Die+Large Block
2: Mode	: 2(1nCE & 1R/nB; Sequential Row Read Disable)
B: Version	: 3rd Generation
x: Package Type	: T(48-TSOP1)
x: Package Material	: Blank(Normal), R(Lead & Halogen Free)
x: Bad Block	: B(Included Bad Block), S(1~5 Bad Block), P(All Good Block)
x: Operating Temperature	: C(0℃~70℃), I(-40℃~85℃)

- **Y:** Year (ex: 8=year 2008, 9= year 2009)
- **ww:** Work Week (ex: 12= work week 12)
- **xx:** Process Code

Note

- Capital Letter	: Fixed Item
- Small Letter	: Non-fixed Item

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