May 1999

National Semiconductor

LM9822 3 Channel 42-Bit Color Scanner Analog Front End

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General Description

The LM9822 is a high performance Analog Front End (AFE) for image sensor processing systems. It performs all the analog and mixed signal functions (correlated double sampling, color specific gain and offset correction, and analog to digital conversion) necessary to digitize the output of a wide variety of CIS and CCD sensors. The LM9822 has a 14 bit 6MHz ADC.

Features

- 6 million pixels/s conversion rate
- Digitally programmed gain and offset for red, green and blue color balancing
- Correlated Double Sampling for lowest noise from CCD sensors
- Compatible with CCD and CIS type image sensors
- Internal Voltage Reference Generation
- TTL/CMOS compatible input/output

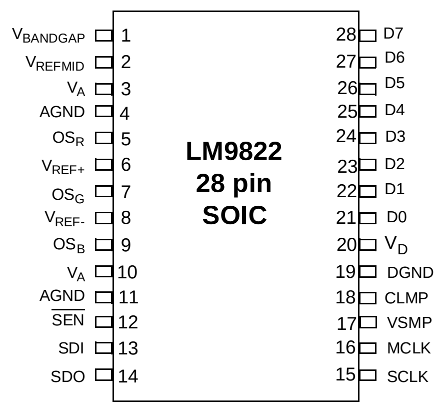
Key Specifications

Output Data Resolution	14 Bits
Pixel Conversion Rate	6MHz
Analog Supply Voltage	5V±5%
I/O Supply Voltage	3.3V±10% or 5V±5%
Power Dissipation (typical)	375mW

Applications

- Color Flatbed Document Scanners
- Color Sheetfed Scanners
- Multifunction Imaging Products
- Digital Copiers
- General Purpose Linear Array Imaging

Connection Diagram



Ordering Information

Temperature Range $0°C \le T_A \le +70°C$		NS Package Number
Order Number	Device Marking	
LM9822CCWM[1]	LM9822CCWM	M28B
LM9822CCWMX[2]	LM9822CCWM	M28B

Notes: [1] - Rail transport media, 26 parts per rail, [2] - Tape and reel transport media, 1000 parts per reel

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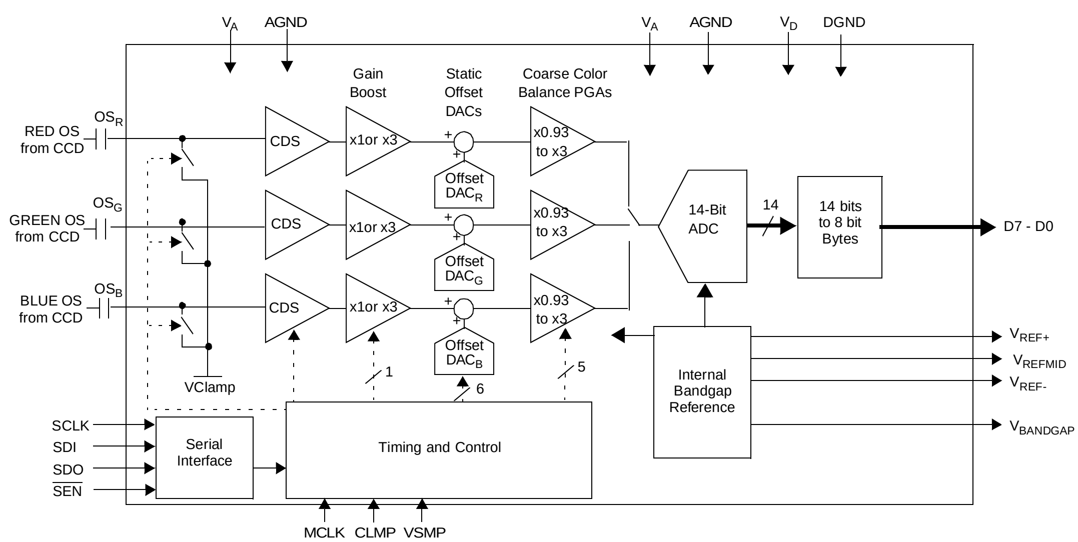
LM9822 Block Diagram



Absolute Maximum Ratings (Notes 1& 2)

Positive Supply Voltage (V^+=V_A=V_D)	
With Respect to GND=AGND=DGND	6.5V
Voltage On Any Input or Output Pin	-0.3V to V^++0.3V
Input Current at any pin (Note 3)	±25mA
Package Input Current (Note 3)	±50mA
Package Dissipation at T_A = 25°C	(Note 4)
ESD Susceptibility (Note 5)	
Human Body Model	7000V
Machine Model	450V
Soldering Information	
Infrared, 10 seconds (Note 6)	235°C
Storage Temperature	-65°C to +150°C

Operating Ratings (Notes 1& 2)

Operating Temperature Range	T_{MIN}=0°C≤T_A≤T_{MAX}=+70°C
V_A Supply Voltage	+4.75V to +5.25V
V_D Supply Voltage	+3.0V to +5.25V
V_D-V_A	≤ 100mV
OS_R, OS_G, OS_B	
Input Voltage Range	-0.05V to $_A$ + 0.05V
SCLK, SDI, $\overline{SEN}$, MCLK, VSMP, CLMP	
Input Voltage Range	-0.05V to V_D + 0.05V

Electrical Characteristics

The following specifications apply for AGND=DGND=0V, V_A=+5.0V_{DC}, V_D=+3.0 or +5.0V_{DC}, f_{MCLK}=12MHz. **Boldface limits apply for T_A=T_J=T_{MIN} to T_{MAX}**; all other limits T_A=T_J=25°C. (Notes 7, 8, 12 & 16)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
CCD/CIS Source Requirements for Full Specified Accuracy and Dynamic Range (Note 12)					
$V_{OS\ PEAK}$	Sensor's Maximum Peak Differential Signal Range	Gain = 0.933 Gain = 3.0 Gain = 9.0	2.1 0.65 0.21		V V V
Full Channel Linearity (In units of 12 bit LSBs) (Note 14)					
DNL	Differential Non-Linearity		+0.9 -0.4	**+2** **-0.9**	LSB(max)
INL	Integral Non-Linearity Error (Note 11)		±2.2	**+5** **-7**	LSB(max)
Analog Input Characteristics					
	OS_R, OS_G, OS_B Input Capacitance		5		pF
	OS_R, OS_G, OS_B Input Leakage Current	Measured with OS = 3.5V_{DC} CDS disabled	20	**25**	µA (max)
		CDS enabled	10		nA
Coarse Color Balance PGA Characteristics					
	Monotonicity			**5**	bits (min)
	G_0 (Minimum PGA Gain)	PGA Setting = 0	0.93	**.90** **.96**	V/V (min) V/V (max)
	G_{31} (Maximum PGA Gain)	PGA Setting = 31	3.0	**2.95** **3.07**	V/V (min) V/V (max)
	x3 Boost Gain	x3 Boost Setting On (Bit 5 of Gain Register is set)	3.0	**2.86** **3.08**	V/V (min) V/V (max)
	Gain Error at any gain (Note 13)		±0.3	**1.6**	% (max)
Static Offset DAC Characteristics (In units of 12 bit LSBs)					
	Monotonicity			**6**	bits (min)
	Offset DAC LSB size	PGA gain = 1	18.9	**13** **24**	LSB (min) LSB (max)
	Offset DAC Adjustment Range	PGA gain = 1	±585	**±570**	LSB (min)

Electrical Characteristics (Continued)

The following specifications apply for AGND=DGND=0V, V_A=+5.0V_{DC}, V_D=+3.0 or +5.0V_{DC}, f_{MCLK}=12MHz. **Boldface limits apply for T_A=T_J=T_{MIN} to T_{MAX}**; all other limits T_A=T_J=25°C. (Notes 7, 8, 12 & 16)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
Internal Reference Characteristics					
V_{REFMID}	Mid Reference Output Voltage		2.5		V
$V_{REF+ OUT}$	Positive Reference Output Voltage		3.5		V
$V_{REF- OUT}$	Negative Reference Output Voltage		1.5		V
ΔV_{REF}	Differential Reference Voltage $V_{REF+ OUT}$ - $V_{REF- OUT}$		2.0		V
System Characteristics (In units of 12 bit LSBs) (see section 5.1, Internal Offsets)					
C	Analog Channel Gain Constant (ADC Codes/V)	Includes voltage reference variation, gain setting = 1	2107	**1934** **2281**	LSB (min) LSB (max)
V_{OS1}	Pre-Boost Analog Channel Offset Error, CCD Mode		17.3	**-61** **+94**	LSB (min) LSB (max)
V_{OS1}	Pre-Boost Analog Channel Offset Error, CIS Mode		27	**-49** **+103**	LSB (min) LSB (max)
V_{OS2}	Pre-PGA Analog Channel Offset Error		-40	**-124** **+44**	LSB (min) LSB (max)
V_{OS3}	Post-PGA Analog Channel Offset Error		-38	**-130** **+55**	LSB (min) LSB (max)

DC and Logic Electrical Characteristics

The following specifications apply for AGND=DGND=0V, V_A=+5.0V_{DC}, V_D=+3.0 or +5.0V_{DC}, f_{MCLK}=12MHz. **Boldface limits apply for T_A=T_J=T_{MIN} to T_{MAX}**; all other limits $_A$=T_J=25°C. (Notes 7& 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
SCLK, SDI, $\overline{SEN}$, MCLK, VSMP,CLMP Digital Input Characteristics					
$V_{IN(1)}$	Logical “1” Input Voltage	V_A=5.25V		**2.0**	V (max)
$V_{IN(0)}$	Logical “0” Input Voltage	V_A=4.75V		**0.8**	V (min)
I_{IN}	Input Leakage Current	V_{IN}=V_A V_{IN}=DGND	0.1 -0.1		µA(max) µA(max)
C_{IN}	Input Capacitance		5		pF
D0-D7 Digital Output Characteristics					
$V_{OUT(1)}$	Logical “1” Output Voltage	I_{OUT}=-360µA		**0.8*V_D**	V (min)
$V_{OUT(0)}$	Logical “0” Output Voltage	I_{OUT}=1.6mA		**0.2*V_D**	V (max)
Power Supply Characteristics					
I_A	Analog Supply Current	Operating	75	**108**	mA (max)
		Power Down	675	**900**	µA (max)
I_D	Digital Supply Current (Note 15)	Operating	210	**475**	µA (max)
		Power Down	2	**25**	µA (max)

AC Electrical Characteristics

The following specifications apply for AGND=DGND=0V, V_A=+5.0V_{DC}, V_D=+3.0 or +5.0V_{DC}, f_{MCLK}=12MHz, except where noted otherwise. **Boldface limits apply for $_A$=T_J=T_{MIN} to T_{MAX}**; all other limits T_A=T_J=25°C. (Notes 7& 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
f_{MCLK}	Maximum MCLK frequency			**12**	MHz (min)
t_{MCLK}	MCLK period		83		ns (min)
	MCLK duty cycle			**40** **60**	%(min) %(max)
t_{SCLK}	Serial Clock Period			**1**	t_{MCLK}(min)
t_{SEN}	Serial Enable high time			**3**	t_{MCLK}(min)
t_{SSU}	SDI setup time			**1**	ns (min)
t_{SH}	SDI hold time			**3**	ns (min)
t_{SDDO}	SCLK edge to new valid data	V_D = 5.0V V_D = 3.3V	8.5 19	**20**	ns (max)
t_{VSU}	VSMP setup time			**1**	ns (min)
t_{VH}	VSMP hold time			**3**	ns (min)
t_{CSU}	CLMP setup time			**1**	ns (min)
t_{CH}	CLMP hold time			**3**	ns (min)
t_{DDO}	MCLK edge to new valid data	V_D = 5.0V V_D = 3.3V	16 25	**25**	ns (max) ns (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND=AGND=DGND=0V, unless otherwise specified.

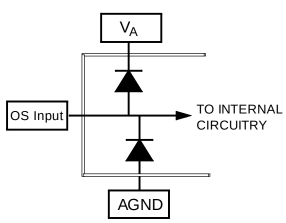
Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN}<GND or V_{IN}>V_A or V_D), the current at that pin should be limited to 25mA. The 50m maximum package input current rating limits the number of pins that can simultaneously safely exceed the power supplies with an input current of 25mA to two.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_J$max, Θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_J max - T_A) / \Theta_{JA}$. $T_J$max = 150°C for this device. The typical thermal resistance (Θ_{JA}) of this part when board mounted is 69°C/W for the M28B SOIC package.

Note 5: Human body model, 100pF capacitor discharged through a 1.5k Ω resistor. Machine model, 200 pF capacitor discharged through a 0Ω resistor.

Note 6: See AN450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in any National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Note 7: Two diodes clamp the OS analog inputs to AGND and V_A as shown below. This input protection, in combination with the external clamp capacitor and the output impedance of the sensor, prevents damage to the LM9822 from transients during power-up.



Note 8: To guarantee accuracy, it is required that V_A and V_D be connected to clean, low noise power supplies, with separate bypass capacitors at each supply pin. When both V_A and V_D are operated at 5.0V, they must be powered by the same regulator, with separate power planes or traces and separate bypass capacitors at each supply pin.

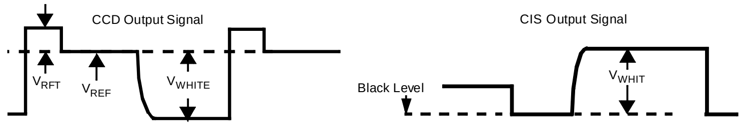
Electrical Characteristics (Continued)

Note 9: Typicals are at T_J=T_A=25°C, f_{MCLK} = 12MHz, and represent most likely parametric norm.

Note 10: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 11: Full channel integral non-linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that best fits the actual transfer function of the AFE.

Note 12: The sensor's maximum peak differential signal range is defined as the peak sensor output voltage for a white (full scale) image, with respect to the dark reference level.



Note 13: PGA Gain Error is the maximum difference between the measured gain for any PGA code and the ideal gain calculated using:

$$\text{Gain}_{PGA}\left(\frac{V}{V}\right) = G_0 + X\frac{\text{PGA code}}{32} \quad \text{where } X = (G_{31} - G_0)\frac{32}{31}.$$

Note 14: Full Channel INL and DNL are tested with CDS disabled, negative signal polarity, DOE = 0, and a single OS input with a gain register setting of 1 (000001b) and an offset register setting of 0 (000000b).

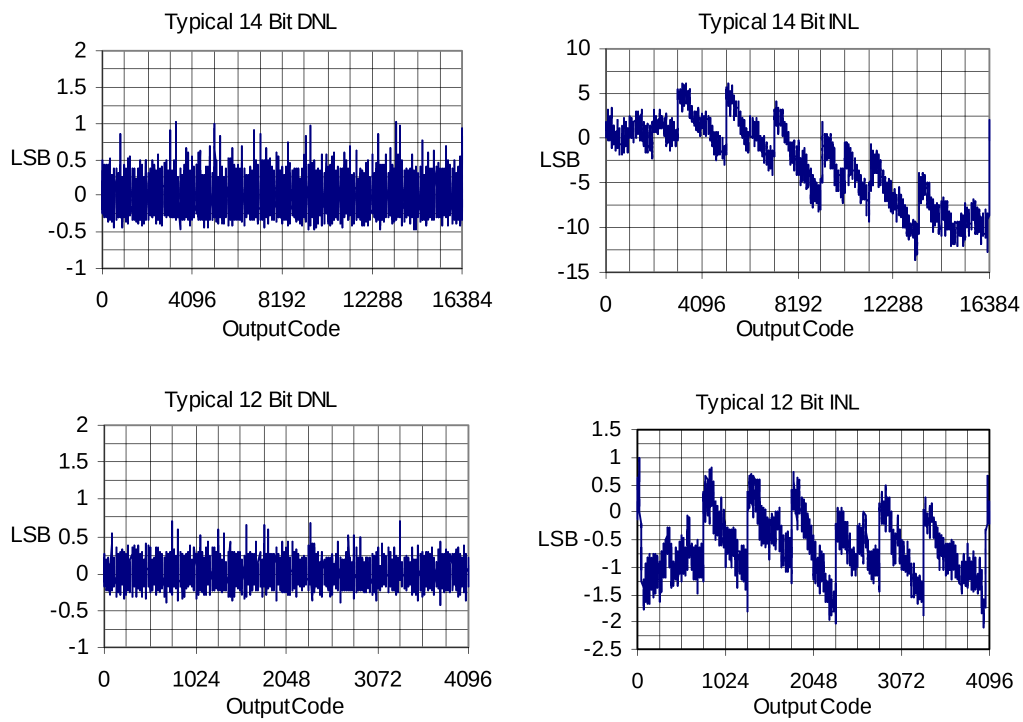
Note 15: The digital supply current (ID) does not include the load, data and switching frequency dependent current required to drive the digital output bus on pins (D7 - D0). The current required to switch the digital data bus can be calculated from: Isw = 2*Nd*Psw*CL*V_D/t_{MCLK} where Nd is total number of data pins, Psw is the probability of each data bit switching, CL is the capacitive loading on each data pin, V_D is the digital supply voltage and t_{MCLK} is the period of the MCLK input. For most applications, Nd is 8, Psw is ≈ 0.5, and V_D is 5V,and the switching current can be calculated from: Isw = 40*CL/tMCLK. (With $_D$ at 3.3V, the equation becomes: Isw = 26.4*CL/t_{MCLK}.) For example, if the capacitive load on each digital output pin (D7 - D0) is 20pF and the period of t_{MCLK} is 1/12MHz or 83ns, then the digital switching current would be 9.6mA. The calculated digital switching current will be drawn through the V_D pin and should be considered as part of the total power budget for the LM9822.

Note 16: All specifications quoted in LSBs are based on 12 bit resolution.

Typical Performance Characteristics

Full Channel DNL and INL

(Divide by 2, Monochrome Mode, 6 MHz Pixel Rate)



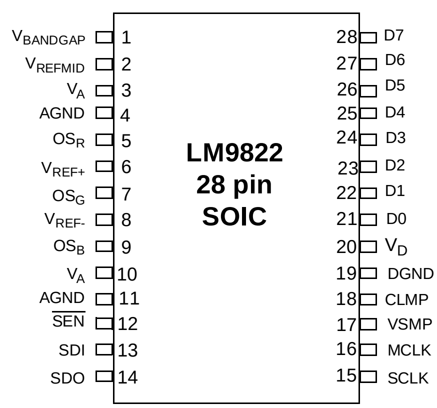
Note: The LM9822 provides 14-bit data for high resolution imaging applications. The typical full channel device performance is shown in the above graphs. In many applications, particularly those where high speed is important, or where lower cost CCD and CIS sensors are used, the signal source is only accurate to 12 bits. In these applications, only 12-bit of data may be used. 12-bit DNL and INL plots have also been provided to illustrate the performance of the LM9822 in these applications.

Pin Descriptions

Analog Power	
V_A	The two $_A$ pins are the analog supply pins. They should be connected to a voltage source of +5V and bypassed to AGND with a 0.1µF monolithic capacitor in parallel with a 10µF tantalum capacitor.
AGND	These two pins are the ground returns for the analog supplies.
V_D	This is the positive supply pin for the digital I/O pins. It should be connected to a voltage source between +3.3V and +5.0V and be bypassed to DGND with a 0.1µF monolithic capacitor in parallel with a 10µF tantalum capacitor.
DGND	This is the ground return for the digital supply.
Analog Input/Output	
OS_R, OS_G, OS_B	Analog Inputs. These inputs (for Red, Green, and Blue) should be tied to the sensor's OS (Output Signal) through DC blocking capacitors.
V_{REF+}, V_{REFMID}, V_{REF-}	Voltage reference bypass pins. V_{REF+}, V_{REFMID}, and V_{REF-} should each be bypassed to AGND through a 0.1uF monolithic capacitor.
Timing Control	
MCLK	Master clock input. The ADC conversion rate will be 1/2 of MCLK. 12MHz is the maximum frequency for MCLK.
VSMP	Sample timing input signal. If VSMP is high on the rising edge of MCLK, the input is sampled on the rising edge of the next MCLK. The reference signal for the next pixel will be sampled one to four MCLKs later, depending on the value in the CDSREF configuration bits. If CDS is not enabled, the internal reference will be sampled during the reference sample time. The number of MCLK cycles between VSMP pulses determines the pixel rate. Timing Diagrams 1 through 6 illustrate the VSMP timings for all the valid pixel rates. Note: See the applications section of the datasheet for the proper timing relationships between VSMP and MCLK.
CLMP	Clamp timing input. If CLMP and VSMP are high on the rising edge of MCLK, all three OS inputs will be internally connected to V_{CLAMP} during the next pixel. V_{CLAMP} is either VREF+ or VREF- depending on the state of the Signal Polarity bit in the Sample Mode register (Reg. 0, Bit 4).

Data Output	
D7-D0	Data Output pins. The 14 bit conversion results of the ADC are multiplexed in 8 bit bytes to D7-D0 synchronous with MCLK. The MSB consists of data bits d13-d6 on pins D7-D0 and the LSB consists of d5-d0 on pins D7-D3 with D1 and D0 low.
Serial Input/Output	
SCLK	Serial Shift Clock. Input data on SDI is valid on the rising edge of SCLK. The minimum SCLK period is 1 t_{MCLK}.
SDO	Serial Data Output. Data bits are shifted out of SDO on falling edges of SCLK. The first eight falling edges of SCLK after SEN goes low will shift out eight data bits (MSB first) from the configuration register addressed during the previous $\overline{SEN}$ low time.
SDI	Serial Data Input. A read/write bit, followed by a four address bits and eight data bits is shifted into SDI, MSB first. Data should be valid on the rising edge of SCLK. If the read/write bit is a "0" (a write), then the shifted data bits will be stored. If the read/write bit is a "1" (a read), then the data bits will be ignored, and SDO will shift out the addressed register's contents during the next $\overline{SEN}$ low time.
$\overline{SEN}$	Shift enable and load signal. When $\overline{SEN}$ is low, data is shifted into SDI. When $\overline{SEN}$ goes high, the last thirteen bits (one read/write, four address and eight data) shifted into SDI will be used to program the addressed configuration register. $\overline{SEN}$ must be high for at least 3 MCLK cycles between $\overline{SEN}$ low times.

Connection Diagram



Timing Diagrams

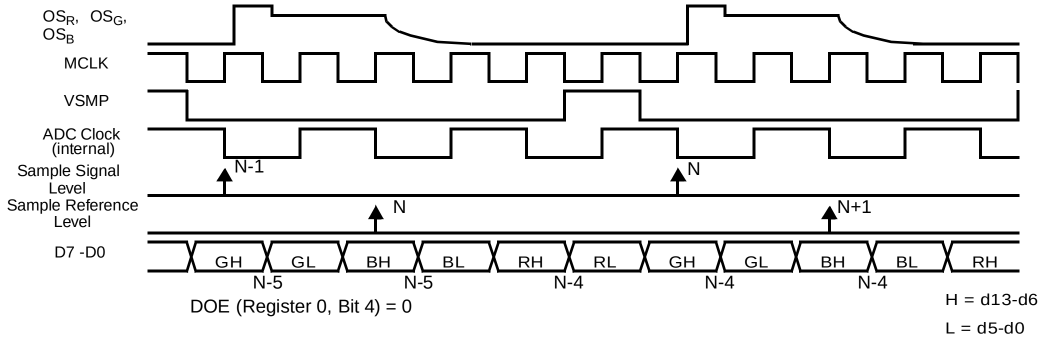


Diagram 1: Divide by 6 Color Mode Sample and Data Output Timing

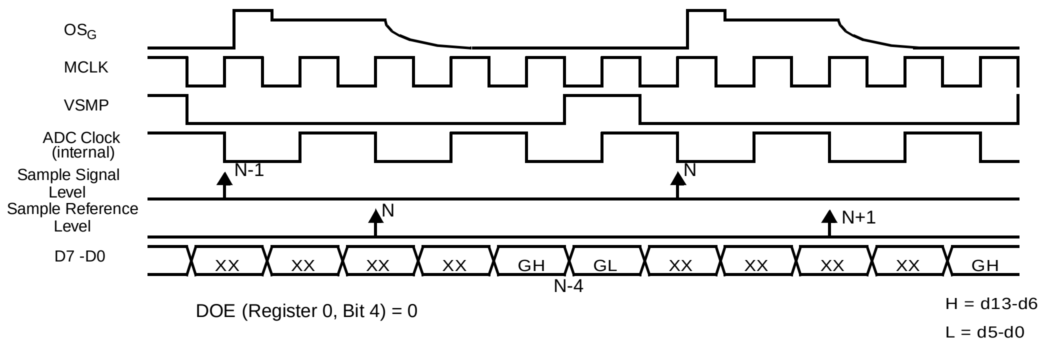


Diagram 2: Divide by 6 Monochrome Mode Sample and Data Output Timing (Green Input shown)

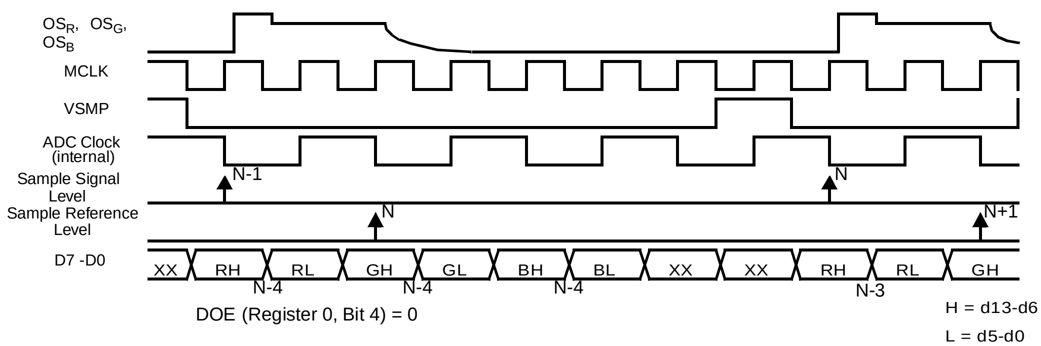


Diagram 3: Divide by 8 Color Mode Sample and Data Output Timing

Timing Diagrams (Continued)

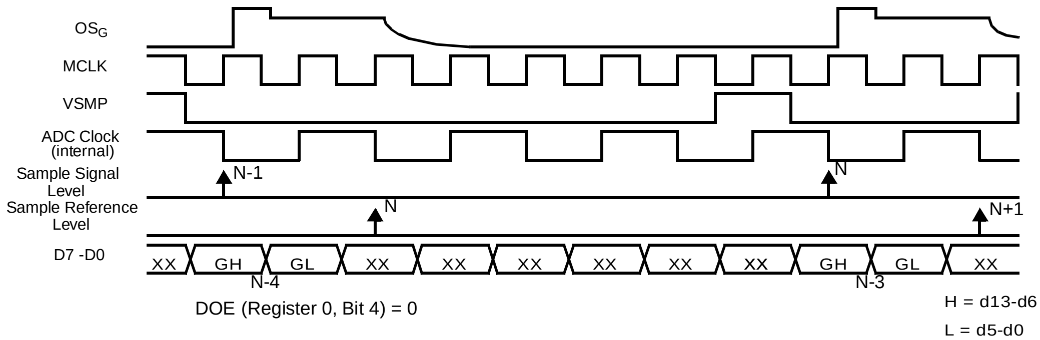


Diagram 4: Divide by 8 Monochrome Mode Sample and Data Output Timing (Green Input Shown)

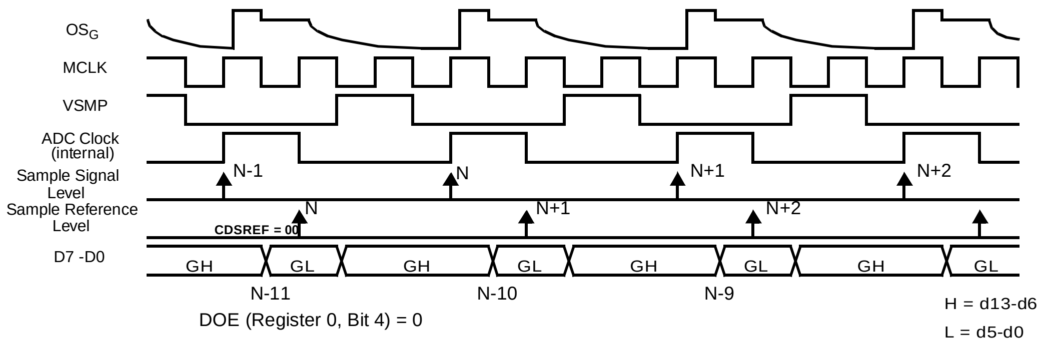


Diagram 5: Divide by 3 Monochrome Mode Sample and Data Output Timing (Green Input shown)

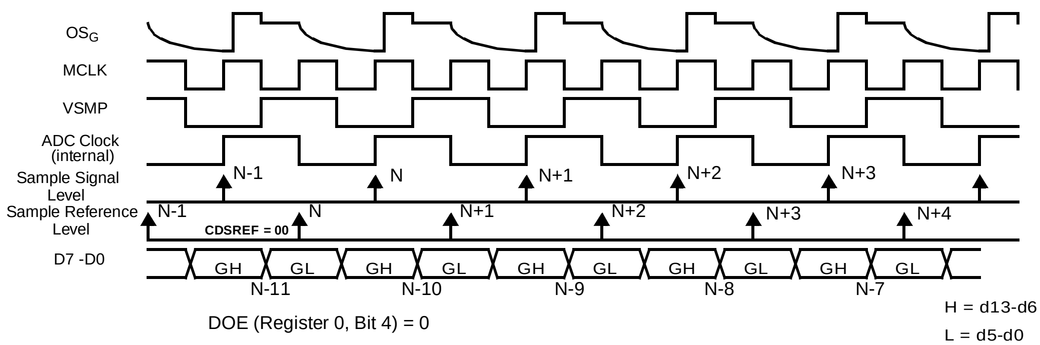


Diagram 6: Divide by 2 Monochrome Mode Sample and Data Output Timing (Green Input shown)

Timing Diagrams (Continued)

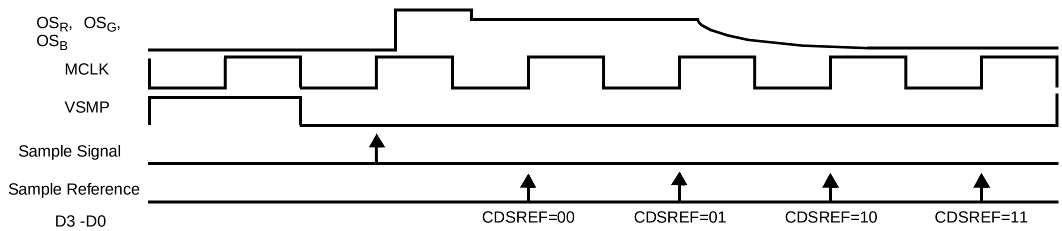


Diagram 7: Programmable Reference Sample Timing

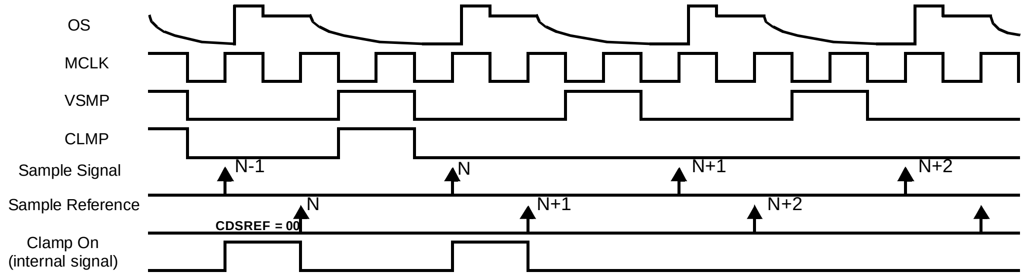


Diagram 8: Clamp Timing With SMPCL = 0

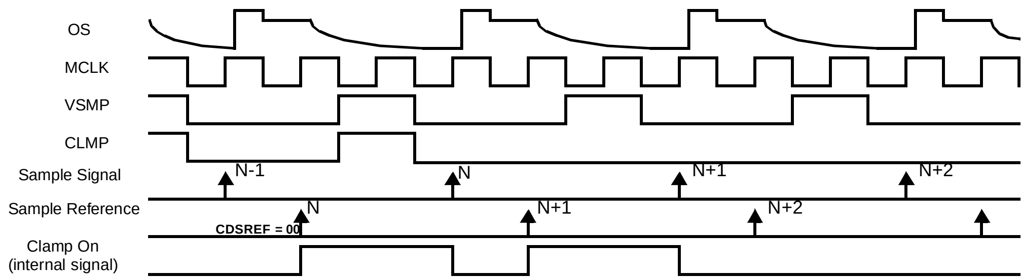


Diagram 9: Clamp Timing With SMPCL = 1

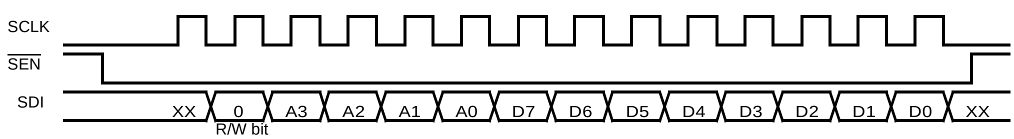


Diagram 10: Configuration Register Serial Write Timing

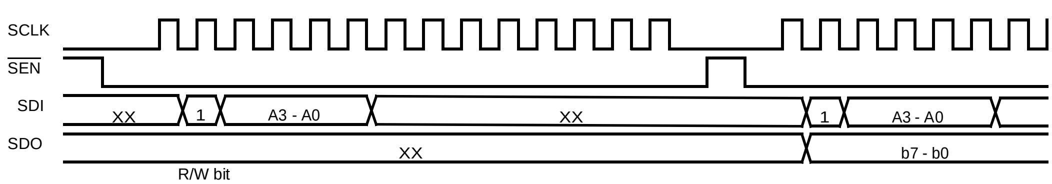


Diagram 11: Configuration Register Serial Read Timing

Timing Diagrams (Continued)

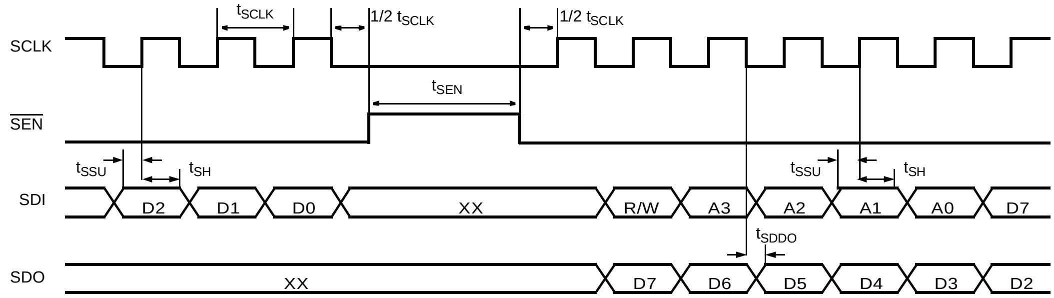


Diagram 12: Serial Input and Output Timing

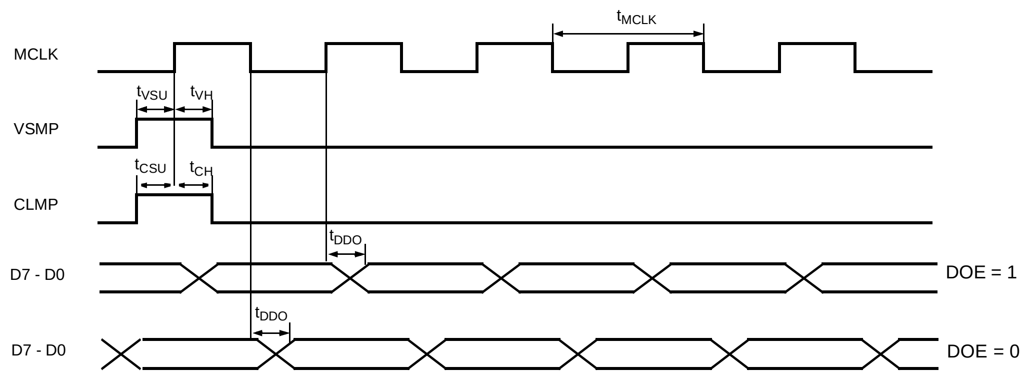


Diagram 13: MCLK, VSMP and CLMP Input Timing and Data Output Timing

Table 1: Configuration Register Address Table

Address (Binary)				Register Name and Bit Definitions							
A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	Sample Mode (Power Up Default = 62h)							
				I/O Mode	DOE	CDS	Polarity	SMPCL	CDSREF1	CDSREF0	PD
0	0	0	1	Red Offset Setting (Power Up Default = 00h)							
				N/A	N/A	Polarity	MSB				LSB
0	0	1	0	Green Offset Setting (Power Up Default = 00h)							
				N/A	N/A	Polarity	MSB				LSB
0	0	1	1	Blue Offset Setting (Power Up Default = 00h)							
				N/A	N/A	Polarity	MSB				LSB
0	1	0	0	Red Gain Setting (Power Up Default = 00h)							
				N/A	N/A	x3	MSB				LSB
0	1	0	1	Green Gain Setting (Power Up Default = 00h)							
				N/A	N/A	x3	MSB				LSB
0	1	1	0	Blue Gain Setting (Power Up Default = 00h)							
				N/A	N/A	x3	MSB				LSB
0	1	1	1	Color Mode (Power Up Default = 00h)							
				N/A	N/A	N/A	N/A	N/A	N/A	CM1	CM0
1	0	0	0	Test Register 0 (Power Up Default = 00h)							
				0	0	0	0	0	0	0	0
1	0	0	1	Test Register 1 (Power Up Default = 10h)							
				0	0	0	1	0	0	0	0
1	0	1	0	Test Register 2 (Power Up Default = 00h)							
				0	0	0	0	0	0	0	0

Table 2: Configuration Register Parameters

Power-Up Default Register Settings are shown in ***Bold Italics***

Parameter (Address)	Control Bits		Result
Sample Mode (0)			
I/O Mode (0)	**B7** ***0*** 1		**Normal Output Driver Operation** **Reduced Slew Rate Output Driver Operation**
DOE (Data Output Edge) (0)	**B6** 0 ***1***		**D7-D0 are clocked out (change) on the falling edge of MCLK - Recommended setting for lowest noise and best overall performance.** **D7-D0 are clocked out (change) on the rising edge of MCLK**
CDS (Enable) (0)	**B5** 0 ***1***		**CDS disabled (CIS)** **CDS Enabled (CCD)**
Signal Polarity (0)	**B4** ***0*** 1		**Negative Polarity (CCD) Clamping to V_{REF+}** **Positive Polarity (CIS) Clamping to V_{REF-}**
SMPCL (0)	**B3** ***0*** 1		**Clamp is on for 1 MCLK before reference sampled** **Clamp is on between the reference and the signal sample points**
CDSREF (0)	**B2** 0 ***0*** 1 1	**B1** 0 ***1*** 0 1	**Reference (for pixel N+1) sampled 1 MCLK cycle after signal (for pixel N) sampled** **Reference (for pixel N+1) sampled 2 MCLK cycle after signal (for pixel N) sampled** **Reference (for pixel N+1) sampled 3 MCLK cycle after signal (for pixel N) sampled** **Reference (for pixel N+1) sampled 4 MCLK cycle after signal (for pixel N) sampled**
PD (Power Down) (0)	**B0** ***0*** 1		**Operating** **Low Power Standby**

Table 2: Configuration Register Parameters (Continued)

Power-Up Default Register Settings are shown in ***Bold Italics***

Parameter (Address)	Control Bits						Result
Red, Green and Blue Offset DAC Settings (1, 2 & 3)							
Offset Polarity	<u>B5</u> ***0*** 1	**Positive Offset** **Negative Offset**					
Offset Value	**B4(MSB)**	**B3**	**B2**	**B1**	**B0(LSB)**	**Typical Offset = 20LSBs * Offset Value * PGA Gain**	
Typical Offset Values	<u>B5</u> (SIGN) ***0*** 0 0 ••• 0 0 1 1 1 ••• 1 1	<u>B4</u> (MSB) ***0*** 0 0 ••• 1 1 0 0 0 ••• 1 1	<u>B3</u> ***0*** 0 0 ••• 1 1 0 0 0 ••• 1 1	<u>B2</u> ***0*** 0 0 ••• 1 1 0 0 0 ••• 1 1	<u>B1</u> ***0*** 0 1 ••• 1 1 0 0 1 ••• 1 1	<u>B0</u> (LSB) ***0*** 1 0 ••• 0 1 0 1 0 ••• 0 1	**Typical Offset (with PGA Gain = 1)** <u>12 bit LSBs</u> ***0.00*** +20 +40 ••• +600 +620 0 -20 -40 ••• -600 -620
Red, Green and Blue Gain Settings (4, 5 & 6)							
Boost Gain Enable	<u>B5</u> ***0*** 1	**Boost Gain = 1V/V** **Boost Gain = 3V/V**					
PGA Gain Value	**B4(MSB)**	**B3**	**B2**	**B1**	**B0(LSB)**	**PGA Gain (V/V) =.933 + 0.0667 * (PGA Gain Value)**	
Gain	**Gain = Boost Gain * PGA Gain**						

Table 2: Configuration Register Parameters (Continued)

Power-Up Default Register Settings are shown in ***Bold Italics***

Parameter (Address)	Control Bits						Result
	B5 (x3)	B4 (MSB)	B3	B2	B1	B0 (LSB)	Typical Gain (V/V)
Typical Gain Values	***0***	***0***	***0***	***0***	***0***	***0***	***0.93***
	0	0	0	0	0	1	1.00
	0	0	0	0	1	0	1.07
	• • •	• • •	• • •	• • •	• • •	• • •	• • •
	0	1	1	1	0	1	2.87
	0	1	1	1	1	0	2.93
	0	1	1	1	1	1	3.00
	• • •	• • •	• • •	• • •	• • •	• • •	• • •
	1	0	0	0	0	0	2.79
	1	0	0	0	0	1	3.00
	1	0	0	0	1	0	3.20
	• • •	• • •	• • •	• • •	• • •	• • •	• • •
	1	1	1	1	0	1	8.60
	1	1	1	1	1	0	8.80
	1	1	1	1	1	1	9.00
Color Mode (7)							
Color Mode	B1	B0					
	0	***0***	***Color***				
	0	1	Monochrome - Red				
	1	0	Monochrome - Green				
	1	1	Monochrome - Blue				
Reserved Register 0 (8)							
Reserved Register 0	***0 0 0 0 0 0 0 0***						Reserved, always set to 00h.
Reserved Register 1 (9)							
Reserved Register 1	***0 0 0 1 0 0 0 0***						Reserved, always set to 10h.
Reserved Register 2 (A)							
Reserved Register 2	***0 0 0 0 0 0 0 0***						Reserved, always set to 00h.

Applications Information

1.0 Introduction

The LM9822 is a high performance scanner Analog Font End (AFE) for image sensor processing systems. It is designed to work with color CCD and CIS image sensors and provides a full 3 channel sampling, gain and offset correction system, coupled with a 14 bit high speed analog to digital converter. A typical application of the LM9822 is in a color flatbed document scanner. The image sensing and processing portion of the system would be configured similar to that shown in Figure 1.

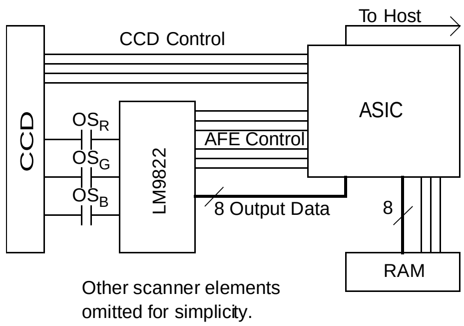


Figure 1: LM9822 in Basic Color Scanner

2.0 CDS Correlated Double Sampler

The LM9822 uses a high-performance CDS (Correlated Double Sampling) circuit to remove many sources of noise and error from the image sensor output signal. It also supports CIS image sensors with a single ended sampling mode.

Figure 2 shows the output stage of a typical CCD and the resulting output waveform:

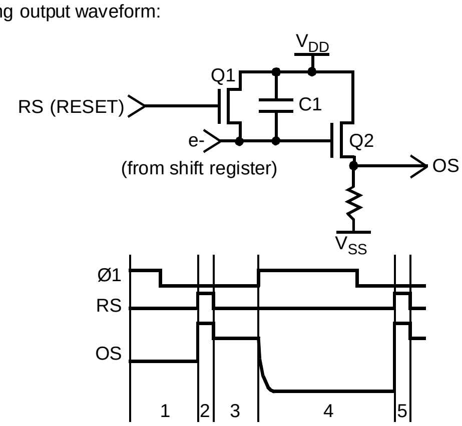


Figure 2: CDS

Capacitor C1 converts the electrons coming from the CCD's shift register to an analog voltage. The source follower output stage (Q2) buffers this voltage before it leaves the CCD. Q1 resets the voltage across capacitor C1 between pixels at intervals 2 and 5. When Q1 is on, the output signal (OS) is at its most positive voltage. After Q1 turns off (period 3), the OS level represents the residual voltage across C1 ($V_{RESIDUAL}$). $V_{RESIDUAL}$ includes charge injection from Q1, thermal noise from the ON resistance of Q1, and other sources of error. When the shift register clock (Ø1) makes a low to high transition (period 4), the electrons from the next pixel flow into C1. The charge across C1 now contains the voltage proportional to the number of electrons plus $V_{RESIDUAL}$, an error term. If OS is sampled at the end of period 3 and that voltage is subtracted from the OS at the end of period 4, the $V_{RESIDUAL}$ term is canceled and the noise on the signal is reduced ($[V_{SIGNAL}+V_{RESIDUAL}]-V_{RESIDUAL} = V_{SIGNAL}$). This is the principal of Correlated Double Sampling.

3.0 CIS Mode (CDS Off, Selectable Signal Polarity)

The also LM9822 supports CIS (Contact Image Sensor) devices. The output signal of a CIS sensor (Figure 3) differs from a CCD signal in two primary ways: its output usually increases with increasing signal strength, and it does not usually have a reference level as an integral part of the output waveform of every pixel.

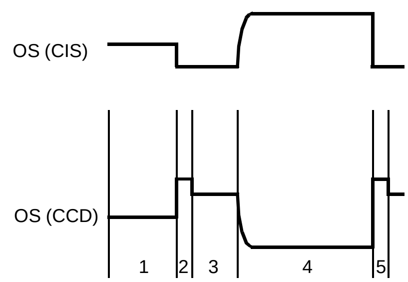


Figure 3: CIS

When the LM9822 is in CIS (CDS off) mode (Register 0, B5=1), it uses either V_{REF+} or V_{REF-} as the reference (or black) voltage for each pixel (depending on the signal polarity setting (Register 0, Bit 4)). If the signal polarity is set to one, then V_{REF-} will be sampled as the reference level. If it is set to zero, then V_{REF+} will be sampled as the reference level.

4.0 Programmable Gain

The output of the Sampler drives the input of the x3 Boost gain stage. The gain of each x3 Boost gain is 3V/V if bit B5 of that color's gain register (register 4,5, or 6) is set, or 1V/V if bit B5 is cleared. The output of each x3 gain stage is the input an offset DAC and the output of each offset DAC is the input to a PGA (Programmable Gain Amplifier). Each PGA provides 5 bits of gain correction over a 0.93V/V to 3V/V (-0.6 to 9.5dB) range. The x3 Boost gain stage and the PGA can be combined for an overall gain range of 0.93V/V to 9.0V/V (-.6 to 19dB). The gain setting for each color (registers 4, 5 and 6) should be set during calibration to bring the maximum amplitude of the strongest pixel to a level just below the desired maximum output from the ADC. The PGA gain is determined by the following equation:

$$\text{PGA Gain}\left(\frac{V}{V}\right) = 0.933 + .0667\ (\text{value in bits B4-B0})$$

Equation 1: PGA Gain

If the x3 Boost gain is enabled then the overall signal gain will be three times the PGA gain.

Applications Information (Continued)

5.0 Offset DAC

The Offset DACs remove the DC offsets generated by the sensor and the LM9822's analog signal chain (see section 5.1, Internal Offsets). The DAC value for each color (registers 1,2 and 3) should be set during calibration to the lowest value that still results in an ADC output code greater than zero for all the pixels when scanning a black line. With a PGA gain of 1V/V, each LSB of the offset DAC typically adds the equivalent of 20 ADC LSBs, providing a total offset adjustment range of ±590 ADC LSBs. The Offset DAC's output voltage is given by:

$$V_{DAC} = 9.75mV \bullet (\text{value in B4 - B0})$$

Equation 2: Offset DAC OutputVoltage

In terms of 12 bit output codes, the offset is given by:

$$Offset = \pm 20 LSBs \bullet (\text{value in B4 - B0}) \bullet \text{PGA Gain}$$

Equation 3: Offset in ADC Output Codes

The offset is positive if bit B5 is cleared and negative if B5 is set. Since the analog offset is added before the PGA gain, the value of the PGA gain must be considered when selecting the offset DAC values.

5.1 Internal Offsets

Figure 4 is a model of the LM9822's internal offsets. Equation 4 shows how to calculate the expected output code given the input voltage (V_{IN}), the LM9822 internal offsets (V_{OS1}, V_{OS2}, V_{OS3}), the programmed offset DAC voltage (V_{DAC}), the programmed gains (G_B, G_{PGA}) and the analog channel gain constant C.

C is a constant that combines the gain error through the AFE, reference voltage variance, and analog voltage to digital code conversion into one constant. Ideally, C = 2048 codes/V (4096 codes/2V) in 12 bit LSBs. Manufacturing tolerances widen the range of C (see Electrical Specifications).

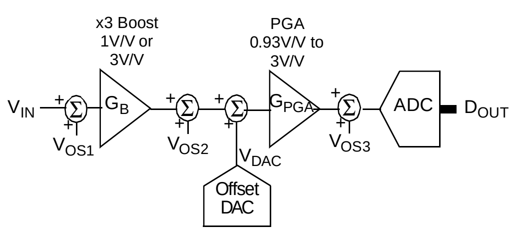


Figure 4: Internal Offset Model

$$D_{OUT} = (((V_{IN} + V_{OS1})G_B + V_{DAC} + V_{OS2})G_{PGA} + V_{OS3})C$$

Equation 4: Output code calculation with internal offsets

Equation 5 is a simplification of the output code calculation, neglecting the LM9822's internal offsets.

$$D_{OUT} = (V_{IN}G_B + V_{DAC})G_{PGA}C$$

Equation 5: Simplified output code calculation

6.0 Clamping

To perform a DC restore across the AC coupling capacitors at the beginning of every line, the LM9822 implements a clamping function. The clamping function is initiated by asserting the CLMP input. If CLMP and VSMP are both high on a rising edge of MCLK, all three OS inputs will be internally connected to V_{REF+} or V_{REF-} during the next pixel, depending on bit 4 of register 0. If bit 4 is set to one (positive signal polarity), then the OS input will be connected to V_{REF-}. If bit 4 is set to zero (negative signal polarity), then it will be connected to V_{REF+}.

6.1 Clamp Capacitor Selection

The output signal of many sensors rides on a DC offset (greater than 5V for many CCDs) which is incompatible with the LM9822's 5V operation. To eliminate this offset without resorting to additional higher voltage components, the output of the sensor is AC coupled to the LM9822 through a DC blocking capacitor, C_{CLAMP} The sensor's DOS output, if available, is not used. The value of this capacitor is determined by the leakage current of the LM9822's OS input and the output impedance of the sensor. The leakage through the OS input determines how quickly the capacitor value will drift from the clamp value of V_{REF+} or V_{REF-}, which then determines how many pixels can be processed before the droop causes errors in the conversion (±0.1V is the recommended limit for CDS operation). The output impedance of the sensor determines how quickly the capacitor can be charged to the clamp value during the black reference period at the beginning of every line.

The minimum clamp capacitor value is determined by the maximum droop the LM9822 can tolerate while converting one sensor line. The minimum clamp capacitor value is much smaller for CDS mode applications than it is for CIS mode applications.

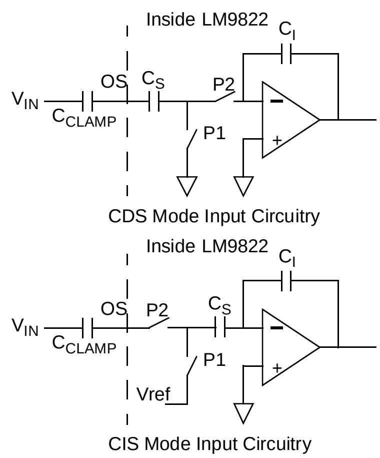


Figure 5: Input Circuitry

The LM9822 input current is considerably less when the LM9822 is operating in CDS mode. In CDS mode, the LM9822 average input current is no more than 25nA. With CDS disabled, which will likely be the case when CIS sensors are used, the LM9822 input impedance will be $1/(f_{Sample} * C_S)$. where f_{Sample} is the sample rate of the analog input and C_S is 2pF.

Applications Information (Continued)

6.1.1 CDS mode Minimum Clamp Capacitor Calculation:

The following equation takes the maximum leakage current into the OS input, the maximum allowable droop, the number of pixels on the sensor, and the pixel conversion rate, f_{VSMP}, and provides the minimum clamp capacitor value:

$$C_{CLAMP\ MIN} = \frac{i}{dV}dt$$
$$= \frac{\text{leakage current (A)}}{\text{max droop(V)}}\frac{\text{number of pixel}}{f_{VSMP}}$$

Equation 6: CDS mode $C_{CLAMP\ MIN}$ Calculation

For example, if the OS input leakage current is 25nA worst-case, the sensor has 2700 active pixels, the conversion rate is 2MHz (t_{VSMP} = 500ns), and the max droop desired is 0.1V, the minimum clamp capacitor value is:

$$C_{CLAMP\ MIN} = \frac{25n}{0.1V}\frac{270}{2MHz}$$
$$= 340p$$

Equation 7: CDS mode $C_{CLAMP\ MIN}$ Example

6.1.2 CIS mode Minimum Clamp Capacitor Calculation:

If CDS is disabled, then the maximum LM9822 OS input leakage current can be calculated from:

$$I_{leakage} = V_{SAT} f_{SampCLK} C_{SAMP}$$

Equation 8: CIS mode Input Leakage Current Calculation

where V_{SAT} is the peak pixel signal swing of the CIS OS output and C_{SAMP} is the capacitance of the LM9822 internal sampling capacitor (2pF). Inserting this into Equation 6 results in:

$$C_{CLAMP\ MIN} = \frac{i}{dV}dt$$
$$= \frac{V_{SAT}}{t_{SampCLK}} C_{SAMP} \frac{t_{SampCLK}}{\text{max droop(V)}} \text{num pixel}$$

Equation 9: CIS mode $C_{CLAMP\ MIN}$ Calculation

with C_{SAMP} equal to 2pF and V_{SAT} equal to 2V (the LM9822 maximum input signal), then Equation 9 reduces to:

$$C_{CLAMP\ MIN} = \frac{4p(F)(V)}{\text{max droop(V)}} \text{num pixels}$$

Equation 10: CIS mode $C_{CLAMP\ MIN}$ Calculation

In CIS mode (CDS disabled), the max droop limit must be much more carefully chosen, since any change in the clamp capacitor's DC value will affect the LM9822 conversion results. If a droop of one 10 bit LSB across a line is considered acceptable, then the allowed droop voltage is calculated as: 2V/1024, or approximately 2mV. If there are 2700 active pixels on a line then:

$$C_{CLAMP\ MIN} = \frac{4p(F)(V)}{2mV}270$$
$$= 5.4uF$$

Equation 11: CIS mode $C_{CLAMP\ MIN}$ Calculation Example

6.1.3 Maximum Clamp Capacitor Calculation:

The maximum size of the clamp capacitor is determined by the amount of time available to charge it to the desired value during the optical black portion of the sensor output. The internal clamp occurs when CLMP and VSMP are both high on a rising edge of MCLK. If SMPCL=0, the clamps are on immediately before the sample reference time, if SMPCL=1, the clamps are on immediately after the sample reference time. If the LM9822 is operated in Divide By 2 mode, then the clamp is on 50% of the time when CLMP is high. In this case the available charge time per line can be calculated using:

$$t_{CLAMP} = \frac{\text{Number of optical black pixels}}{2f_{VSMP}}$$

Equation 12: Clamp Time Per Line Calculation

For example, if a sensor has 18 black reference pixels and f_{VSMP} is 2MHz with a 50% duty cycle, then t_{CLAMP} is 4.5µs. Other "Divide By" modes will have lower or higher clamp duty cycles accordingly, depending on the SMPCL setting. See **Diagram 8, Clamp Timing With SMPCL = 0** and **Diagram 9, Clamp Timing With SMPCL = 1**.

The following equation takes the number of optical black pixels, the amount of time (per pixel) that the clamp is closed, the sensor's output impedance, and the desired accuracy of the final clamp voltage and provides the maximum clamp capacitor value that allows the clamp capacitor to settle to the desired accuracy within a single line:

$$C_{CLAMP\ MAX} = \frac{t}{R}\frac{1}{\ln(\text{accuracy})}$$
$$= \frac{t_{CLAMP}}{R_{CLAMP}}\frac{1}{\ln(\text{accuracy})}$$

Equation 13: $C_{CLAMP\ MAX}$ for a single line of charge time

Where t_{CLAMP} is the amount of time (per line) that the clamp is on, R_{CLAMP} is the output impedance of the CCD plus 50Ω for the LM9822 internal clamp switch, and accuracy is the ratio of the worst-case initial capacitor voltage to the desired final capacitor voltage. If t_{CLAMP} is 4.5µs, the output impedance of the sensor is 1500Ω, the worst case voltage change required across the capacitor (before the first line) is 5V, and the desired accuracy after clamping is to within 0.1V (accuracy = 5/0.1 = 50), then:

$$C_{CLAMP\ MAX} = \frac{4.5\mu s}{155\ \Omega}\frac{1}{\ln(50)}$$
$$= 728p$$

Equation 14: $C_{CLAMP\ MAX}$ Example

The final value for C_{CLAMP} should be less than or equal to $C_{CLAMP\ MAX}$, but no less than $C_{CLAMP\ MIN}$.

In some cases, depending primarily on the choice of sensor, $C_{CLAMP\ MAX}$ may actually be *less* than $C_{CLAMP\ MIN}$, meaning that the capacitor can not be charged to its final voltage during the black pixels at the beginning of a line and hold it's voltage without drooping for the duration of that line. This is usually not a problem because in most applications the sensor is clocked continuously as soon as power is applied. In this case, a larger capacitor can be used (guaranteeing that the $C_{CLAMP\ MIN}$ requirement is met), and the final clamp voltage is forced across the capacitor over multiple lines. This equation calculates how many lines are required before the capacitor settles to the desired accuracy:

$$\text{line} = \left(R_{CLAMP}\frac{C_{CLAMP}}{t_{CLAMP}}\right)\ln\left(\frac{\text{Initial Error Voltag}}{\text{Final Error Voltag}}\right)$$

Equation 15: Number of Lines Required for Clamping

Using the values shown before and a clamp capacitor value of 0.01µF, this works out to be:

$$\text{lines} = \left(155\ \frac{0.01\mu F}{4.5\mu s}\right)\ln\left(\frac{5V}{0.1V}\right) = 13.5 \text{ lines}$$

Equation 16: Clamping Lines Required Example

Applications Information (Continued)

In this example, a 0.01µF capacitor takes 14 lines after power-up to charge to its final value. On subsequent lines, the only error will be the droop across a single line which should be significantly less than the initial error. **If the LM9822 is operating in CDS mode and multiple lines are used to charge up the clamping capacitors after power-up, then a clamp capacitor value of 0.01µF should be significantly greater than the calculated $C_{CLAMP\ MIN}$ value and can virtually always be used.**

If the LM9822 is operating in CIS mode, then significantly larger clamp capacitors must be used. Fortunately, the output impedance of most CIS sensors is significantly smaller than the output impedance of CCD sensors, and R_{CLAMP} will be dominated by the 50Ω from the LM9822 internal clamp switch. With a smaller R_{CLAMP} value, the clamp capacitors will charge faster.

7.0 Power Supply Considerations

The LM9822 analog supplies ($_A$) should be powered by a single +5V source. The two analog supplies are brought out individually to allow separate bypassing for each supply input. They should *not* be powered by two or more different supplies.

Each supply input should be bypassed to its respective ground with a 0.1µF capacitor located as close as possible to the supply input pin. A single 10µF tantalum capacitor should be placed near the V_A supply pins to provide low frequency bypassing.

The V_D input can be powered at 3.3V or 5.0V. Power should be supplied by a clean, low noise linear power supply, with a 0.1 µF ceramic capacitor and a 10 µF tantalum capacitor placed near the V_D and DGND pins. If possible, a separate power and ground plane should be provided to isolate the noisy digital output signals from the sensitive analog supply pins. If the V_D voltage is lower than V_A, a separate linear regulator should be used. If V_D and $_A$ are both at 5.0V, then they should be supplied by a common linear regulator, with separate analog and digital power and ground planes.

To minimize noise, keep the LM9822 and all analog components as far as possible from noise generators, such as switching power supplies and high frequency digital busses. If possible, isolate all the analog components and signals (OS, reference inputs and outputs, $_A$, AGND) on an analog ground plane, separate from the digital ground plane. The two ground planes should be tied together at a single point, preferably the point where the power supply enters the PCB.

8.0 Serial Interface and Configuration Registers

The serial interface is used to program the configuration registers which control the operation of the LM9822. The $\overline{SEN}$, SCLK, SDI and SDO signals are used to set and verify configuration register settings. In addition, MCLK must be active during all serial interface activity. MCLK is used to register the level of the $\overline{SEN}$ input and drives the logic that process information input on the SDI line.

9.0 Sample Mode Register Settings

A brief overview of the sample mode register and the bit locations is give in **Table 2: Configuration Register Parameters** on page 14. The function of each bit is summarized in the following sections.

9.1 Output Driver Mode

The Output Driver Mode bit is normal set to 0. This bit can be set to 1 to reduce the slew rate of the output drivers.

9.2 DOE (Data Output Edge) Setting

The Data Output Edge bit selects which edge of MCLK is used to clock output data onto the output pins. For lowest noise performance, this bit should be set to 0. With this setting, new data is placed on the D7-D0 pins on every falling edge of MCLK. See Diagrams 1 through 6 and Diagram 13 for more information on data output timing for the different Divide By modes, and detailed timing of the output data signals.

The bit can be set to 1 to adjust the data output timing for some applications, but the noise performance of the LM9822 may be somewhat degraded.

9.3 CDS Enable

The CDS Enable bit determines whether the sampling section of the LM9822 operates in Correlated Double Sampling mode or in Single Ended Sampling mode. CDS mode is normally used with CCD type sensors, while Single Ended mode is normally used with CIS type sensors.

9.4 Signal Polarity

Whether the LM9822 is operating in Correlated Double Sampling Mode, or Single Ended Sampling mode, the basic sampling operation is the same. First a reference level is sampled, then a signal level is sampled. For CDS mode operation, if the signal level is lower in voltage than the reference level, the Signal Polarity bit should be set to 0. This is the normal setting for CCD type sensors. If the signal level is more positive than the reference level, the Signal Polarity bit would be set to 1 for Positive Polarity mode.

When Single Ended Mode is selected, the Signal Polarity bit determines which internal reference voltage is used to compare with the input signal. Most CIS type sensors have a positive polarity type output, and in this case the Signal Polarity Bit should be set to 1. In this case, the internal V_{REF-} is used as the reference level during the Reference Sampling period.

In addition, the Signal Polarity bit determines which internal reference voltage is used during the Clamping interval. If Signal Polarity = 0, V_{REF+} is used for clamping, if Signal Polarity = 1, V_{REF-} is used.

9.5 SMPCL

The SMPCL setting controls when the clamping action occurs during the acquisition cycle. If SMPCL is set to 0, the Clamp will be on for 1 MCLK before the reference sampling point. If SMPCL is set to 1, clamping will occur in the interval after the reference sampling point, and before the signal sampling point. In this case, the clamping time is dependent on the present “Divide By” mode, and the settings of the CDSREF bits.

9.6 CDSREF

The CDSREF setting is provided to allow adjustable sampling points for the reference sample at the higher “Divide By” modes. This may be useful to optimize the timing of the Reference Sam-

pling point for particular CCD sensors. Diagram 7 shows how the various settings of CDSREF can be used to delay the Reference Sampling point. Care must be taken to avoid setting CDSREF to an inappropriate value when operating in the lower “Divide By” modes.
Valid CDSREF settings are:

“Divide By” Mode	Valid CDSREF
/8	00,01,10,11
/6	00,01,10,11
/3	00,01
/2	00

9.7 PD (Power Down) Mode

A Power Down bit is provided to configure the LM9822 in a lower power “StandBy” mode. In this mode, typical power consumption is reduced to less than 1% of normal operating power. The serial interface is still active, but the majority of the analog and digital circuitry is powered down.

10.0 LM9822 Basic Operation

The normal operational sequence when using the LM9822 is as follows:
Immediately after applying power, all configuration registers are reset to default settings. MCLK should be applied, and the appropriate values written to the registers using the procedure discussed in section *8.0 Serial Interface and Configuration Registers* on page 20 and detailed in Diagrams 10, 11 and 12. Once the configuration registers are loaded, the timing control signals can be applied at the proper rates for the mode of conversion desired. MCLK is applied initially with VSMP and CLMP low. After at least 3 MCLKS, VSMP and CLMP signals can begin. The Divide By mode is determined by the ratio of MCLK to VSMP frequency as described in section 10.2.

14-Bit conversion results are placed on the data output pins as follows: The upper 8 bits are output first with bit 13 of the ADC on D7 and the bit 6 of the ADC on D0. The lower 6 bits are then output with bit 5 of the ADC on D7 and bit 0 of the ADC on D2. D0 and D1 are always 0 when the lower 6 bits of data are being output. The exact timing and conversion latency of the output data is affected by the settings of the DOE variable in the Sample Mode register, and the Divide By mode of operation. If DOE = 0 (recommended setting for best performance), output data will change on the falling edge of MCLK. If DOE = 1, output data is updated on the rising edge of MCLK. See Diagrams 1 through 6 and Diagram 13 for more information on data output timing.

10.1 CLMP Operation

The CLMP signal is used to engage the LM9822 internal clamp circuits at the proper time during the CCD or CIS data output cycle. If both CLMP and VSMP are high on a rising edge of MCLK, then CLMP will be applied during the next pixel. The exact timing of the internal Clamp signal is determined by the Divide By mode of operation and the setting of the SMPCL variable in the Sample Mode register. If SMPCL = 0, then the Clamp is on for 1 MCLK before the reference is sampled. If SMPCL = 1 then the clamp is on between the reference and the signal sample points. Please see Diagram 8 and Diagram 9 for a graphic example of this timing.

To clamp across multiple pixels in a row, CLMP can be set high and remain there for the entire number of pixels to be clamped, then returned to the low state for normal (signal) operation. This may simplify the timing required to generate the CLMP signal.

10.2 MCLK and VSMP Timing

The relationship between VSMP and MCLK is used to determine the 'Divide By' mode that is presently being used with the part. Valid 'Divide By' settings are:

Color - /8, /6
Monochrome - /8, /6, /3, /2

When entering a new mode, it is important to provide consistent MCLK/VSMP timing signals that meet the following condition. When switching to a new 'Divide By' mode, VSMP should be held low for a minimum of 3 MCLK cycles, then valid timing according to the datasheet diagrams for the particular mode should be started. This ensures that all internal circuitry is properly synchronized to the new conversion 'Divide By' mode being used. If the timing relationship between VSMP and MCLK is disturbed for any reason, the same procedure should be used before restarting operation in the chosen 'Divide By' mode.

For example: To change from monochrome Divide By 3 mode to monochrome Divide By 2 mode, VSMP should be held low for at least 3 MCLK cycles, then VSMP can be brought high using "Divide By 2" timing. If VSMP is not low for at least 3 MCLKs, the LM9822 may enter an unknown mode.

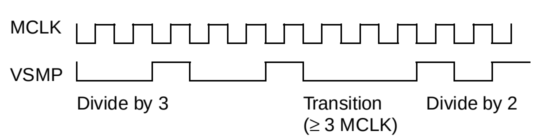
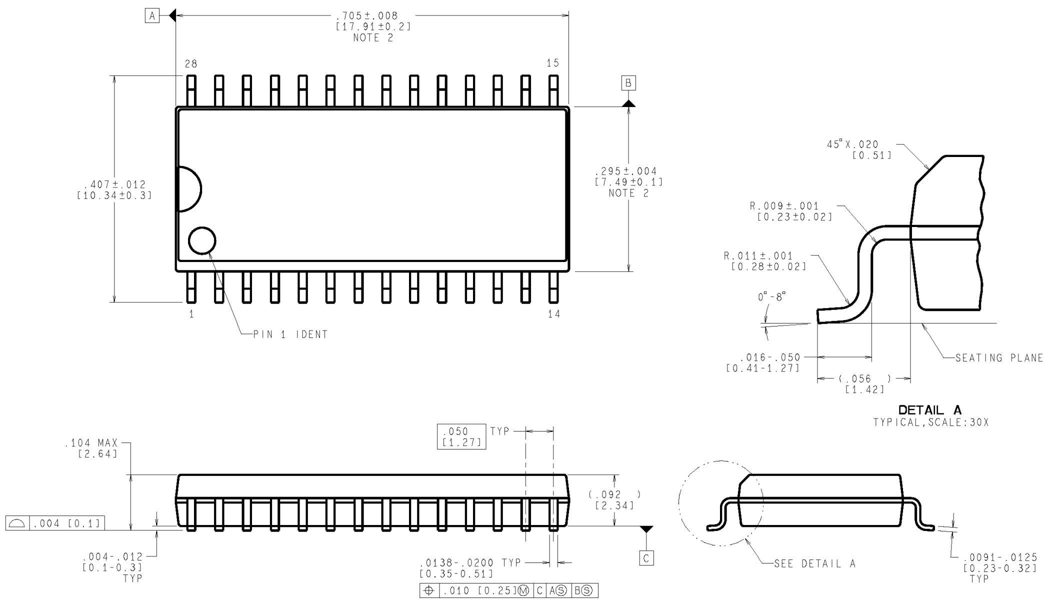


Figure 6: Timing of Transitions between ‘Divide By’ Modes

Physical Dimension inches (millimeters) unless otherwise noted



28-Lead (0.300" wide) Molded Small Outline Package (JEDEC)
Order Number LM9822CCWM
NS Package Number M28B

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