

74ABT823

9-bit D-type flip-flop with reset and enable; 3-state

Rev. 03 — 23 March 2010

Product data sheet

1. General description

The 74ABT823 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT823 is a 9-bit wide buffered register with clock enable input (\overline{CE}) and master reset input (\overline{MR}) which are ideal for parity bus interfacing in systems using many microprocessors.

The 74ABT823 is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data and address paths of buses carrying parity.

The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output Q of the flip-flop.

2. Features and benefits

- High-speed parallel registers with positive edge-triggered D-type flip-flops
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Output capability: +64 mA and –32 mA
- Power-on 3-state
- Power-on reset
- Latch-up protection exceeds 500 mA per JESD78B class II level A
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74ABT823D	–40 °C to +85 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
74ABT823DB	–40 °C to +85 °C	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
74ABT823PW	–40 °C to +85 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1



4. Functional diagram

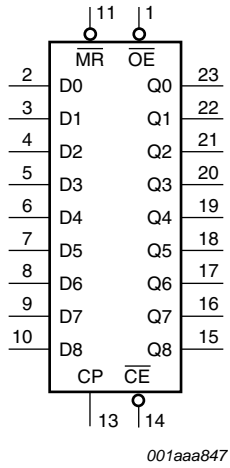


Fig 1. Logic symbol

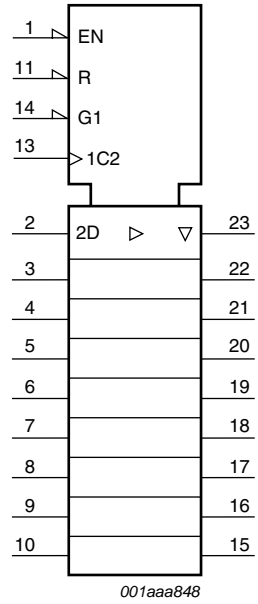


Fig 2. IEC logic symbol

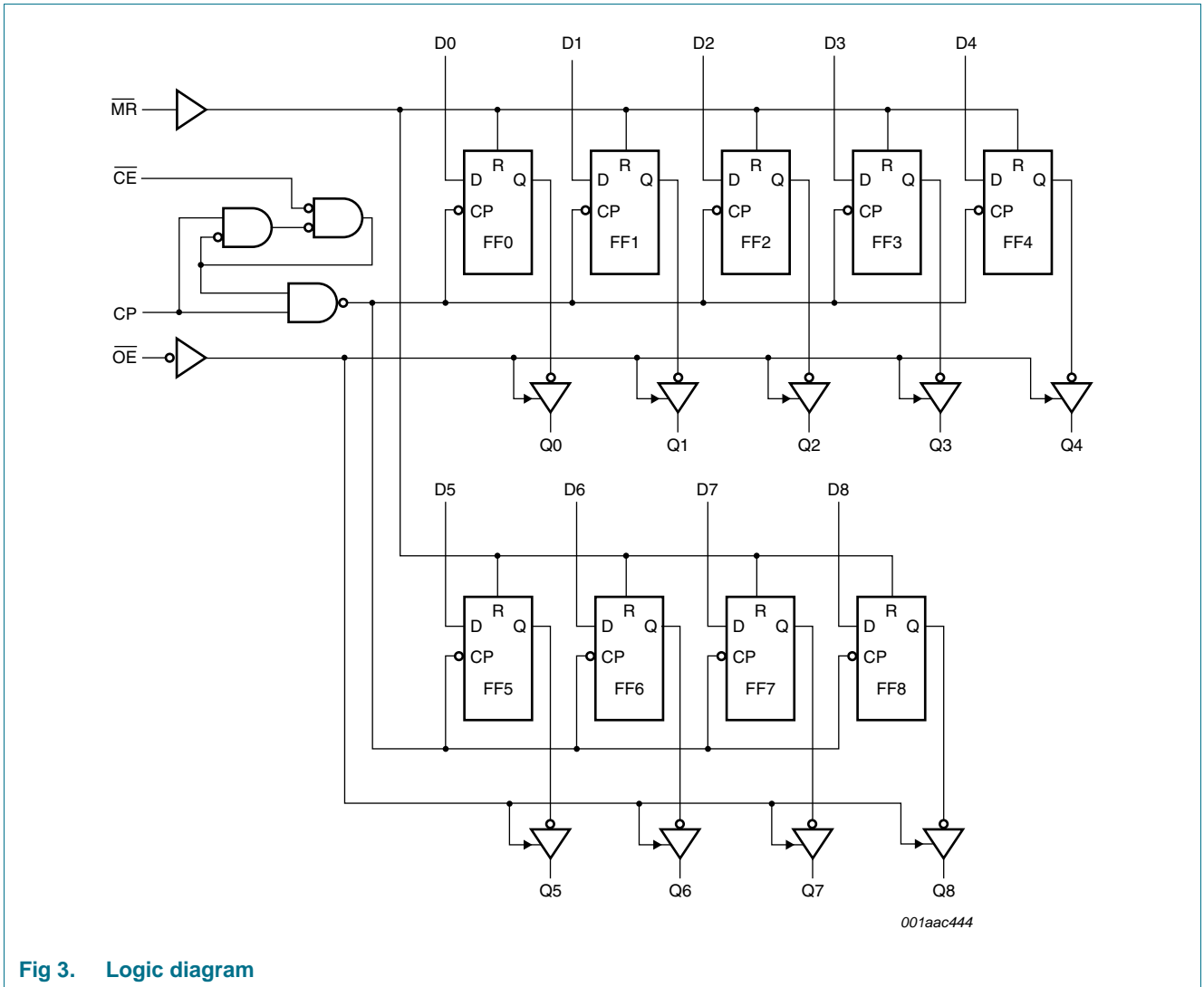
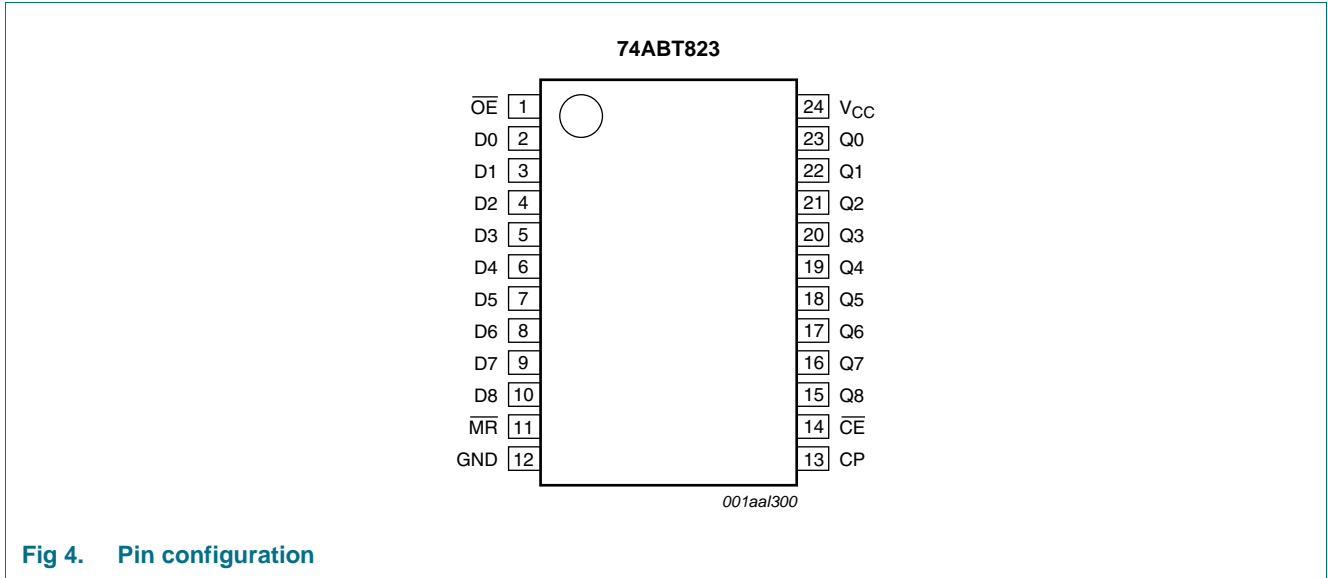


Fig 3. Logic diagram

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
\overline{OE}	1	output enable input (active LOW)
D0, D1, D2, D3, D4, D5, D6, D7, D8	2, 3, 4, 5, 6, 7, 8, 9, 10	data input
\overline{MR}	11	master reset input (active LOW)
GND	12	ground (0 V)
CP	13	clock pulse input (active rising edge)
\overline{CE}	14	clock enable input (active LOW)
Q8, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0	15, 16, 17, 18, 19, 20, 21, 22, 23	data output
V_{CC}	24	positive supply voltage

6. Functional description

6.1 Function table

Table 3. Function table^[1]

Input					Output	Operating mode
OE	MR	CE	CP	Dn	Qn	
L	L	X	X	X	L	clear
L	H	L	↑	h	H	load and read data
L	H	L	↑	l	L	
L	H	H	NC	X	NC	hold
H	X	X	X	X	Z	high-impedance

- [1] H = HIGH voltage level;
 L = LOW voltage level;
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
 ↑ = LOW-to-HIGH clock transition;
 NC = no change;
 X = don't care;
 Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
V _I	input voltage		^[1] -1.2	+7.0	V
V _O	output voltage	output in OFF-state or HIGH-state	^[1] -0.5	+5.5	V
I _{IK}	input clamping current	V _I < 0 V	-18	-	mA
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
I _O	output current	output in LOW-state	-	128	mA
T _j	junction temperature		^[2] -	150	°C
T _{stg}	storage temperature		-65	+150	°C

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 [2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

8. Recommended operating conditions

Table 5. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level Input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		-32	-	-	mA
I_{OL}	LOW-level output current		-	-	64	mA
$\Delta t/\Delta V$	input transition rise and fall rate		0	-	5	ns/V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C

9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit	
			Min	Typ	Max	Min	Max		
V_{IK}	input clamping voltage	$V_{CC} = 4.5\text{ V}; I_{IK} = -18\text{ mA}$	-1.2	-0.9	-	-1.2	-	V	
V_{OH}	HIGH-level output voltage	$V_I = V_{IL}$ or V_{IH}							
		$V_{CC} = 4.5\text{ V}; I_{OH} = -3\text{ mA}$	2.5	2.9	-	2.5	-	V	
		$V_{CC} = 5.0\text{ V}; I_{OH} = -3\text{ mA}$	3.0	3.4	-	3.0	-	V	
		$V_{CC} = 4.5\text{ V}; I_{OH} = -32\text{ mA}$	2.0	2.4	-	2.0	-	V	
V_{OL}	LOW-level output voltage	$V_{CC} = 4.5\text{ V}; I_{OL} = 64\text{ mA};$ $V_I = V_{IL}$ or V_{IH}	-	0.42	0.55	-	0.55	V	
$V_{OL(pu)}$	power-up LOW-level output voltage	$V_{CC} = 5.5\text{ V}; I_O = 1\text{ mA};$ $V_I = \text{GND}$ or V_{CC}	[1]	-	0.13	0.55	-	0.55	V
I_I	input leakage current	$V_{CC} = 5.5\text{ V}; V_I = V_{CC}$ or GND	-	± 0.01	± 1.0	-	± 1.0	μA	
I_{OFF}	power-off leakage current	$V_{CC} = 0\text{ V}; V_I$ or $V_O \leq 4.5\text{ V}$	-	± 5.0	± 100	-	± 100	μA	
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} = 2.0\text{ V}; V_O = 0.5\text{ V};$ $V_I = \text{GND}$ or $V_{CC}; \overline{\text{OE}} \text{ HIGH}$	[2]	-	± 5.0	± 50	-	± 50	μA
I_{OZ}	OFF-state output current	$V_{CC} = 5.5\text{ V}; V_I = V_{IL}$ or V_{IH}							
		$V_O = 2.7\text{ V}$	-	5.0	50	-	50	μA	
		$V_O = 0.5\text{ V}$	-	-5.0	-50	-	-50	μA	
I_{LO}	output leakage current	HIGH-state; $V_O = 5.5\text{ V};$ $V_{CC} = 5.5\text{ V}; V_I = \text{GND}$ or V_{CC}	-	5.0	50	-	50	μA	
I_O	output current	$V_{CC} = 5.5\text{ V}; V_O = 2.5\text{ V}$	[3]	-180	-50	-50	-180	-50	mA
I_{CC}	supply current	$V_{CC} = 5.5\text{ V}; V_I = \text{GND}$ or V_{CC}							
		outputs HIGH-state	-	0.5	250	-	250	μA	
		outputs LOW-state	-	27	34	-	34	mA	
		outputs disabled	-	0.5	250	-	250	μA	

Table 6. Static characteristics ...continued

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit	
			Min	Typ	Max	Min	Max		
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 5.5\text{ V}$; one input at 3.4 V; other inputs at V_{CC} or GND	[4]	-	0.5	1.5	-	1.5	mA
C_I	input capacitance	$V_I = 0\text{ V}$ or V_{CC}	-	4	-	-	-	-	pF
C_O	output capacitance	outputs disabled; $V_O = 0\text{ V}$ or V_{CC}	-	7	-	-	-	-	pF

- [1] For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- [2] This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 ms. From $V_{CC} = 2.1\text{ V}$ to $V_{CC} = 5\text{ V} \pm 10\%$ a transition time of up to 100 μs is permitted.
- [3] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- [4] This is the increase in supply current for each input at 3.4 V.

10. Dynamic characteristics

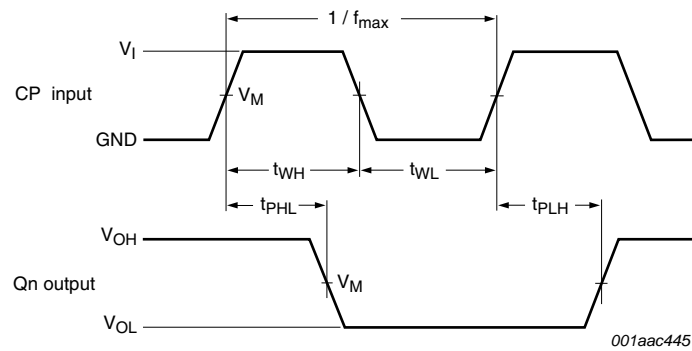
Table 7. Dynamic characteristics
GND = 0 V; for test circuit, see Figure 9.

Symbol	Parameter	Conditions	25 °C; $V_{CC} = 5.0\text{ V}$			-40 °C to +85 °C; $V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$		Unit
			Min	Typ	Max	Min	Max	
f_{max}	maximum frequency	see Figure 5	125	200	-	125	-	MHz
t_{PLH}	LOW to HIGH propagation delay	CP to Qn, see Figure 5	2.1	4.3	5.9	2.1	6.8	ns
t_{PHL}	HIGH to LOW propagation delay	CP to Qn, see Figure 5 \overline{MR} to Qn, see Figure 6	2.2	4.4	6.1	2.2	6.7	ns
t_{PZH}	OFF-state to HIGH propagation delay	\overline{OE} to Qn; see Figure 8	1.0	3.0	4.5	1.0	5.3	ns
t_{PZL}	OFF-state to LOW propagation delay	\overline{OE} to Qn; see Figure 8	2.2	4.1	5.6	2.2	6.3	ns
t_{PHZ}	HIGH to OFF-state propagation delay	\overline{OE} to Qn; see Figure 8	2.7	4.8	6.2	2.7	6.9	ns
t_{PLZ}	LOW to OFF-state propagation delay	\overline{OE} to Qn; see Figure 8	2.5	5.0	6.4	2.5	6.9	ns
$t_{su(H)}$	set-up time HIGH	Dn to CP; see Figure 7 \overline{CE} to CP; see Figure 7	2.1	0.5	-	2.1	-	ns
$t_{su(L)}$	set-up time LOW	Dn to CP; see Figure 7 \overline{CE} to CP; see Figure 7	2.1	0.2	-	2.1	-	ns
$t_{h(H)}$	hold time HIGH	CP to Dn; see Figure 7 CP to \overline{CE} ; see Figure 7	1.3	0.0	-	1.3	-	ns
$t_{h(L)}$	hold time LOW	CP to Dn; see Figure 7 CP to \overline{CE} ; see Figure 7	+1.3	-0.3	-	+1.3	-	ns
t_{WH}	pulse width HIGH	CP; see Figure 5	2.9	1.9	-	2.9	-	ns

Table 7. Dynamic characteristics ...continued
GND = 0 V; for test circuit, see Figure 9.

Symbol	Parameter	Conditions	25 °C; V _{CC} = 5.0 V			-40 °C to +85 °C; V _{CC} = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
t _{WL}	pulse width LOW	CP; see Figure 5	3.8	2.8	-	3.8	-	ns
		$\overline{\text{MR}}$; see Figure 6	5.5	4.0	-	5.5	-	ns
t _{rec}	recovery time	$\overline{\text{MR}}$ to CP; see Figure 6	2.5	0.6	-	2.5	-	ns

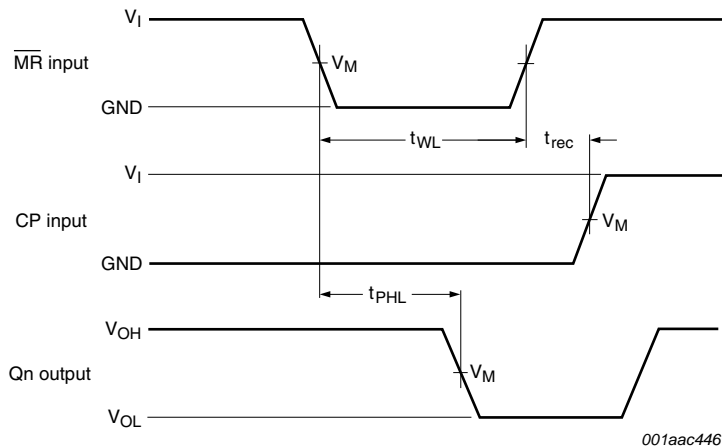
11. Waveforms



V_M = 1.5 V

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

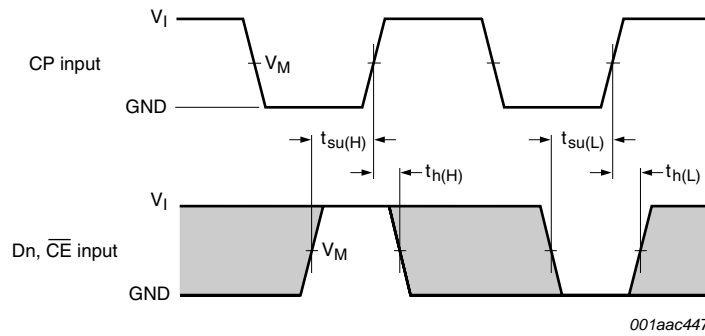
Fig 5. Propagation delay clock input (CP) to output (Qn), clock pulse (CP) width and maximum clock (CP) frequency



V_M = 1.5 V

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

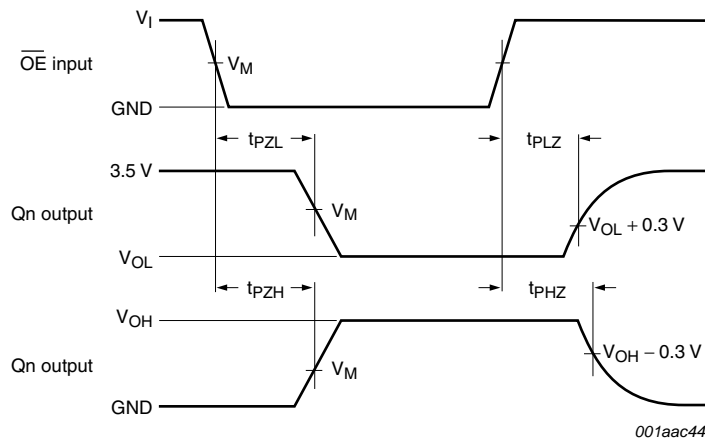
Fig 6. Master reset ($\overline{\text{MR}}$) pulse width, propagation delay master reset ($\overline{\text{MR}}$) to output (Qn) and recovery time master reset (MR) to clock (CP)



$V_M = 1.5\text{ V}$

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 7. Set-up and hold times data output (Dn) to clock (CP) and clock enable input ($\overline{\text{CE}}$) to clock (CP)



$V_M = 1.5\text{ V}$

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load

Fig 8. 3-state output (Qn) enable and disable times

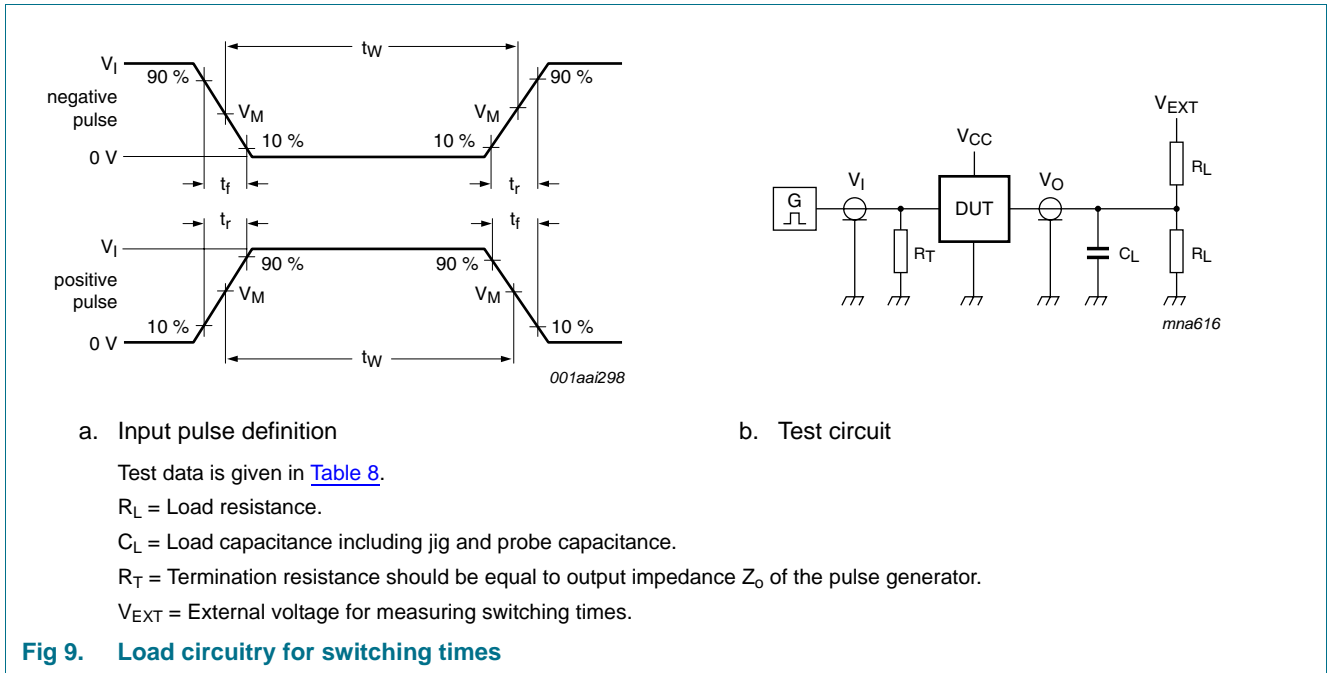


Table 8. Test data

Input				Load		V_{EXT}		
V_I	f_I	t_w	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
3.0 V	1 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	open	open	7.0 V

12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

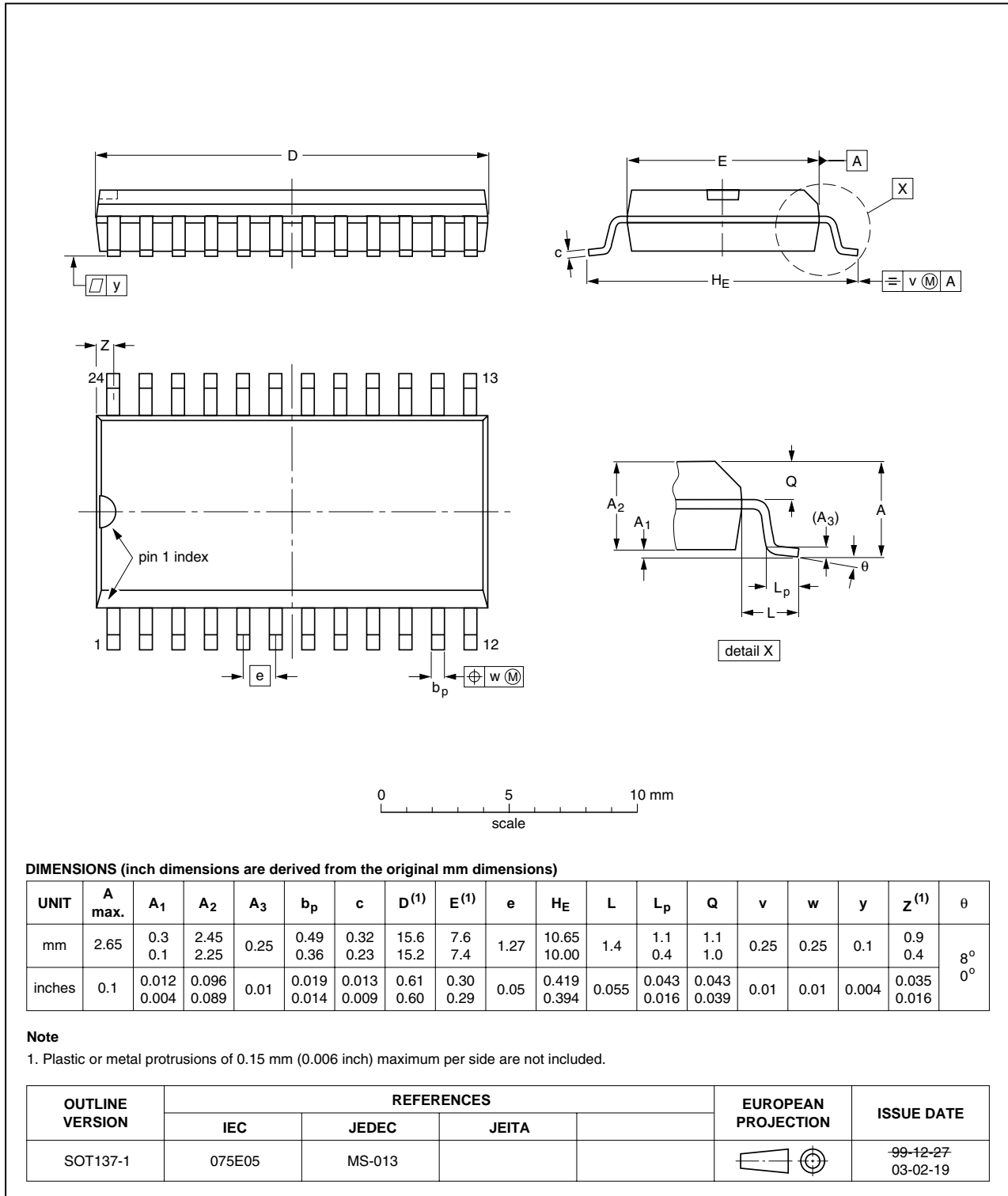


Fig 10. Package outline SOT137-1 (SO24)

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1

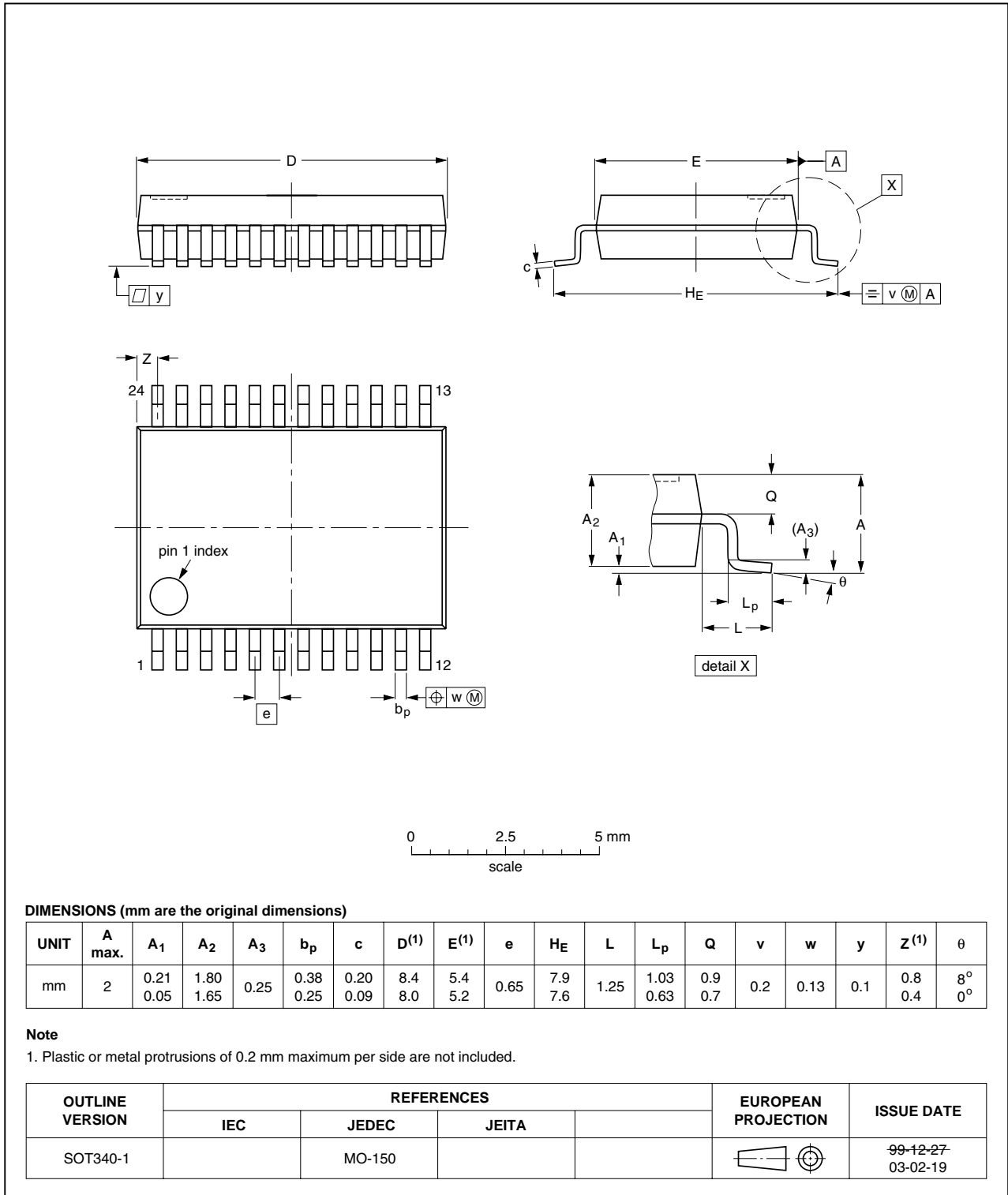


Fig 11. Package outline SOT340-1 (SSOP24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

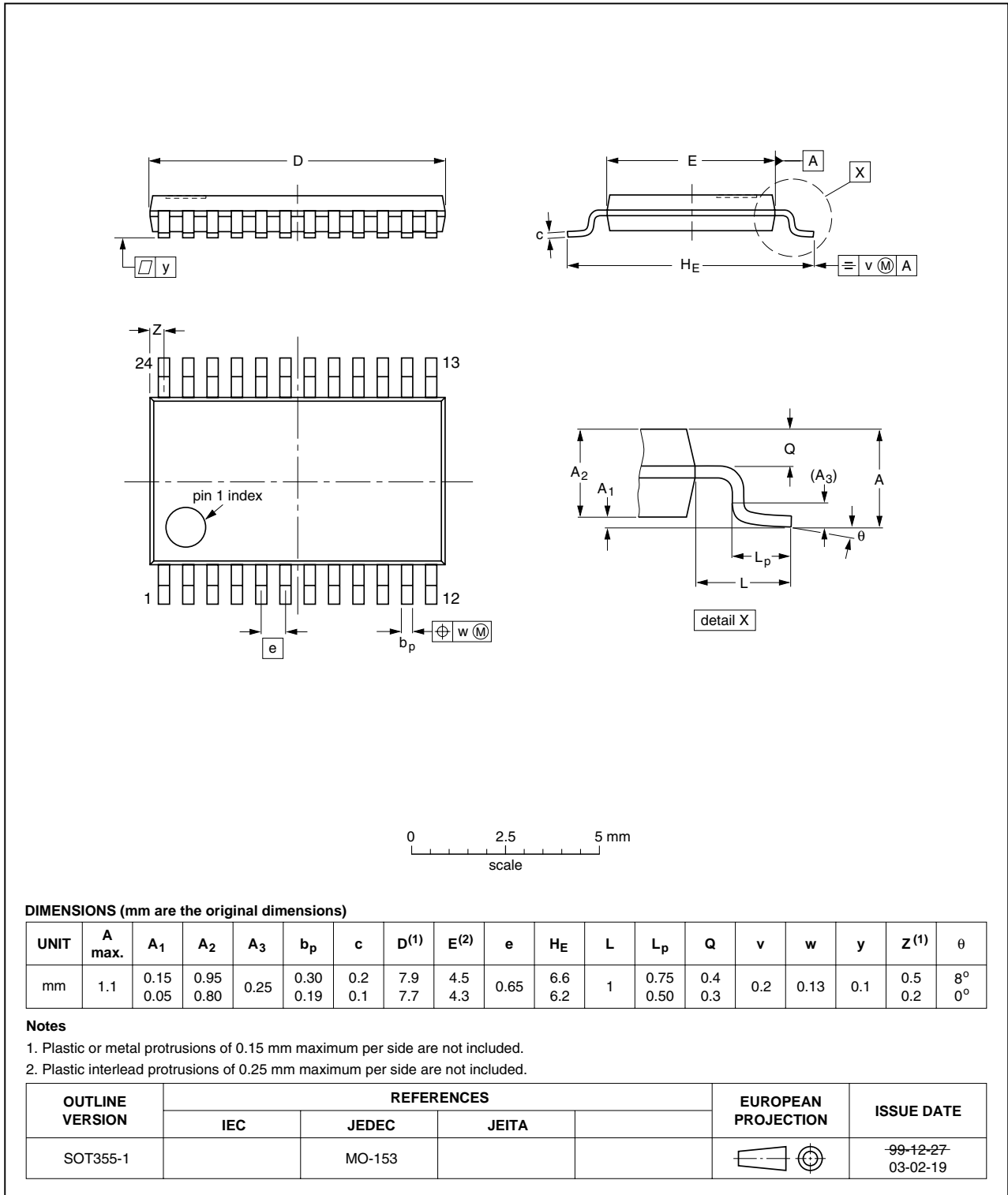


Fig 12. Package outline SOT355-1 (TSSOP24)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
BICMOS	Bipolar Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT823_3	20100323	Product data sheet	-	74ABT823_2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. DIP 24 (SOT222-1) package removed from Section 3 “Ordering information” and Section 12 “Package outline” 			
74ABT823_2	20050207	Product specification	-	74ABT823_1
74ABT823_1	19960314	Product specification	-	

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

15.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. The product is not designed, authorized or warranted to be

suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on a weakness or default in the customer application/use or the application/use of customer's third party customer(s) (hereinafter both referred to as "Application"). It is customer's sole responsibility to check whether the NXP Semiconductors product is suitable and fit for the Application planned. Customer has to do all necessary testing for the Application in order to avoid a default of the Application and the product. NXP Semiconductors does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

17. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	1
4	Functional diagram	2
5	Pinning information	4
5.1	Pinning	4
5.2	Pin description	4
6	Functional description	5
6.1	Function table	5
7	Limiting values	5
8	Recommended operating conditions	6
9	Static characteristics	6
10	Dynamic characteristics	7
11	Waveforms	8
12	Package outline	11
13	Abbreviations	14
14	Revision history	14
15	Legal information	15
15.1	Data sheet status	15
15.2	Definitions	15
15.3	Disclaimers	15
15.4	Trademarks	15
16	Contact information	16
17	Contents	17

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2010.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 23 March 2010

Document identifier: 74ABT823_3