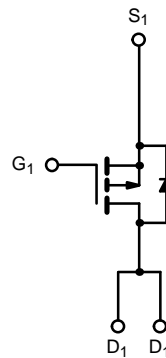
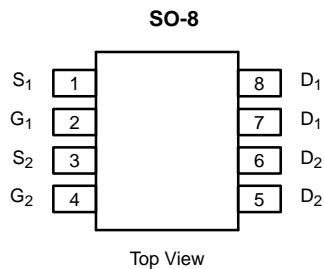
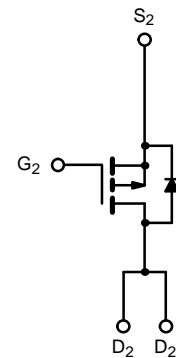


Dual P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-20	0.075 @ $V_{GS} = -4.5$ V	± 3.4
	0.105 @ $V_{GS} = -3.0$ V	± 2.9
	0.115 @ $V_{GS} = -2.7$ V	± 2.6



P-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	± 3.4
		$T_A = 70^\circ\text{C}$	± 2.7
Pulsed Drain Current	I_{DM}	± 16	A
Continuous Source Current (Diode Conduction) ^a	I_S	-2.0	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	2.0
		$T_A = 70^\circ\text{C}$	1.3
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>



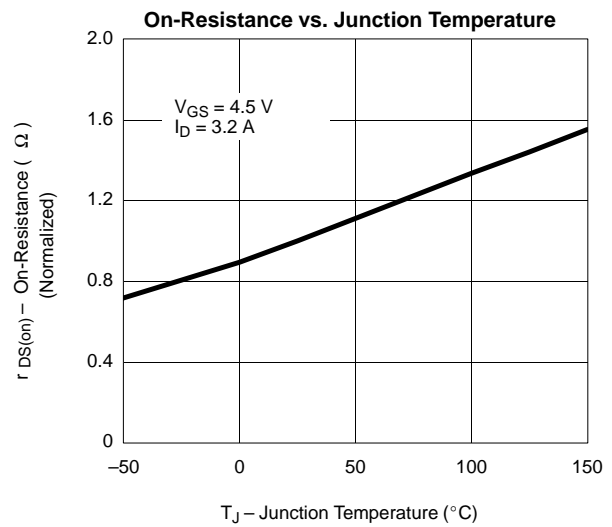
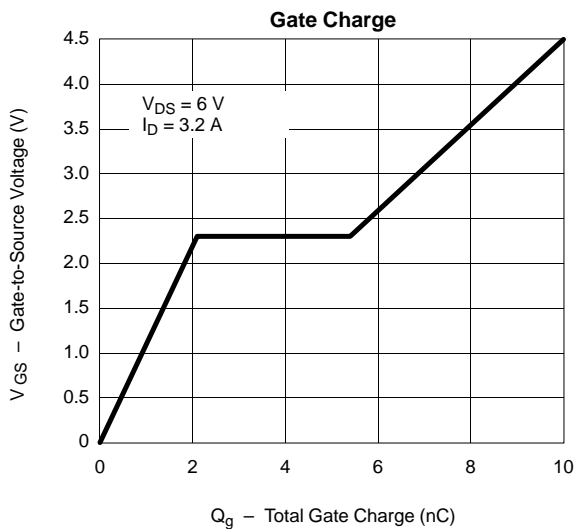
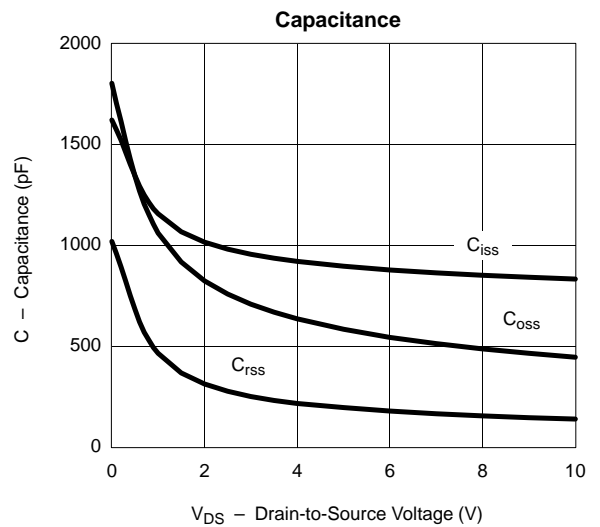
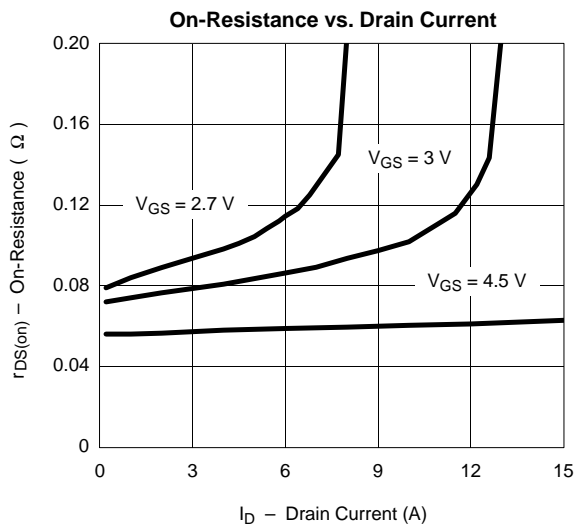
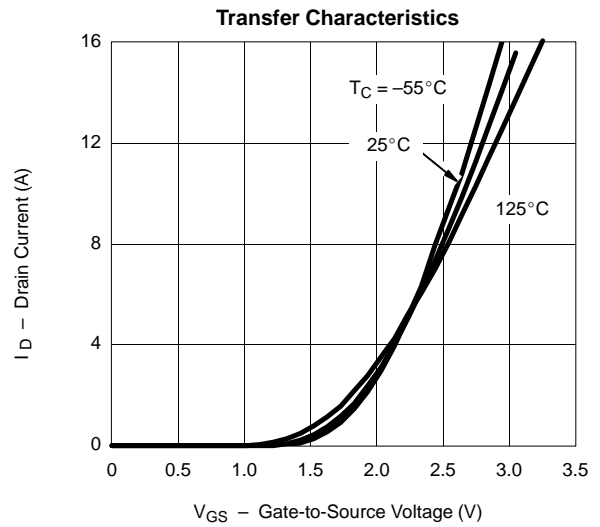
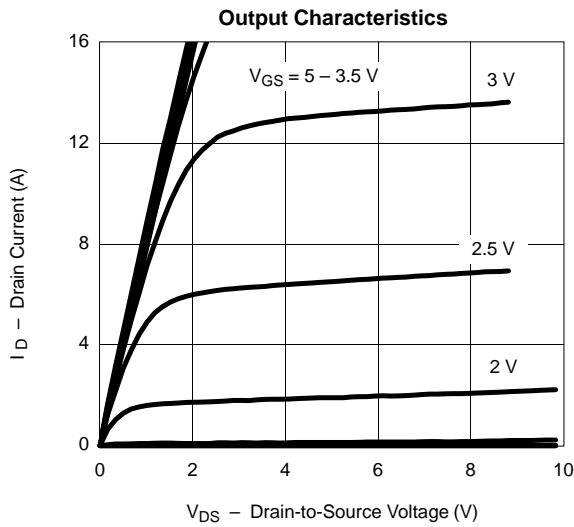
SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-0.8			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 12 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -16 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -10 V, V _{GS} = 0 V, T _J = 85 °C			-3	
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≤ -5 V, V _{GS} = -4.5 V	-16			A
		V _{DS} ≤ -5 V, V _{GS} = -2.7 V	-3			
Drain-Source On-State Resistance ^b	r _{DS(on)}	V _{GS} = -4.5 V, I _D = -3.2 A		0.06	0.075	Ω
		V _{GS} = -3.0 V, I _D = -2.0 A		0.078	0.105	
		V _{GS} = -2.7 V, I _D = -1 A		0.085	0.115	
Forward Transconductance ^b	g _{fs}	V _{DS} = -9 V, I _D = -3.4 A		8		S
Diode Forward Voltage ^b	V _{SD}	I _S = -2.0 A, V _{GS} = 0 V		-0.7	-1.2	V
Dynamic^a						
Total Gate Charge	Q _g	V _{DS} = -6 V, V _{GS} = -4.5 V, I _D = -3.2 A		10	20	nC
Gate-Source Charge	Q _{gs}			2.1		
Gate-Drain Charge	Q _{gd}			3.3		
Turn-On Delay Time	t _{d(on)}	V _{DD} = -6 V, R _L = 6 Ω I _D ≅ -1 A, V _{GEN} = -4.5 V, R _G = 6 Ω		16	40	ns
Rise Time	t _r			46	80	
Turn-Off Delay Time	t _{d(off)}			40	70	
Fall Time	t _f			25	40	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = -2.0 A, di/dt = 100 A/μs		60	100	

Notes

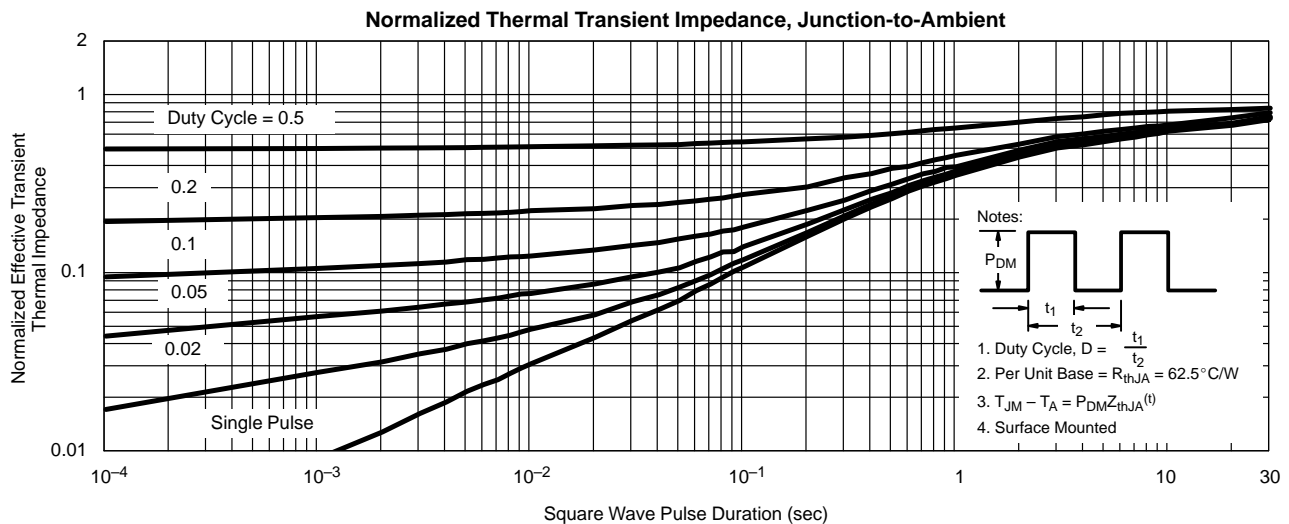
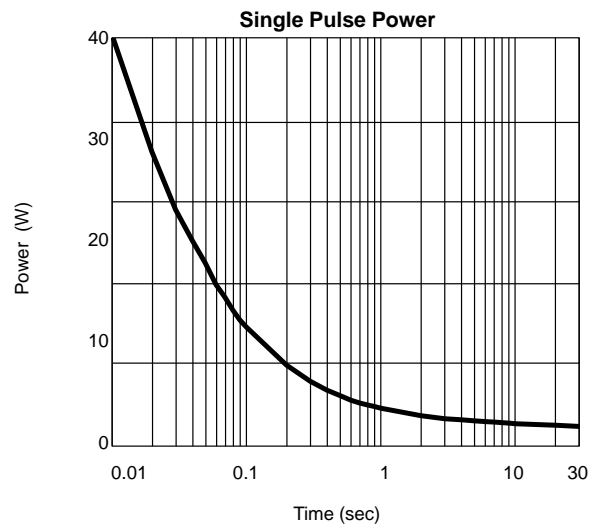
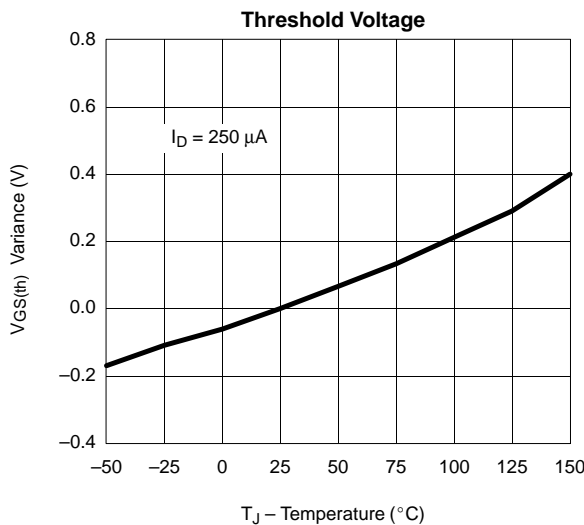
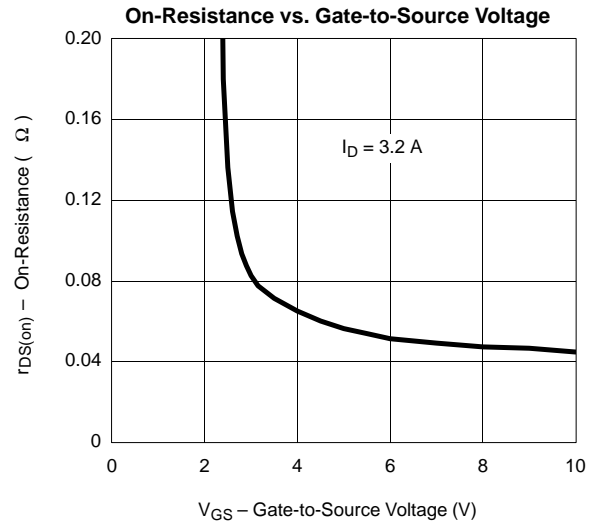
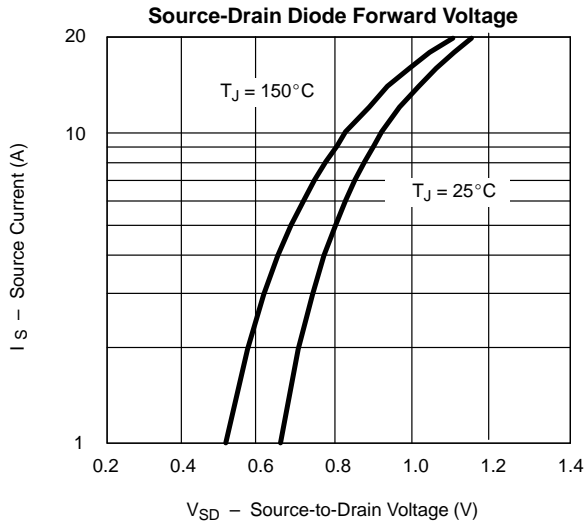
- a. For design aid only; not subject to production testing.
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





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