ACT™ 2 Field Programmable Gate Arrays

Features

- Up to 8000 Gate Array Gates (20,000 PLD equivalent gates)
- Replaces up to 200 TTL Packages
- Replaces up to eighty 20-Pin PAL® Packages
- Design Library with over 500 Macro Functions
- Single-Module Sequential Functions
- Wide-Input Combinatorial Functions
- Up to 1232 Programmable Logic Modules
- Up to 998 Flip-Flops
- Datapath Performance at 105 MHz
- 16-Bit Accumulator Performance to 42 MHz
- Two In-Circuit Diagnostic Probe Pins Support Speed Analysis to 50 MHz
- Two High-Speed, Low-Skew Clock Networks
- I/O Drive to 10 mA
- Nonvolatile, User Programmable
- Logic Fully Tested Prior to Shipment

Description

The ACT™ 2 family represents Actel's second generation of field programmable gate arrays (FPGAs). The ACT 2 family presents a two-module architecture, consisting of C-modules and S-modules. These modules are optimized for both combinatorial and sequential designs. Based on Actel's patented channeled array architecture, the ACT 2 family provides significant enhancements to gate density and performance while maintaining downward compatibility with the ACT 1 design environment and upward compatibility with the ACT 3 design environment. The devices are implemented in silicon gate, 1.0-µm, two-level metal CMOS, and employ Actel's PLICE® antifuse technology. This revolutionary architecture offers gate array design flexibility, high performance, and fast time-to-production with user programming. The ACT 2 family is supported by the Designer and Designer Advantage Systems, which offers automatic pin assignment, validation of electrical and design rules, automatic placement and routing, timing analysis, user programming, and diagnostic probe capabilities. The systems are supported on the following platforms: 386/486™ PC, Sun™, and HP™ workstations. The systems provide CAE interfaces to the following design environments: Cadence, Viewlogic®, Mentor Graphics®, and OrCAD™.

1

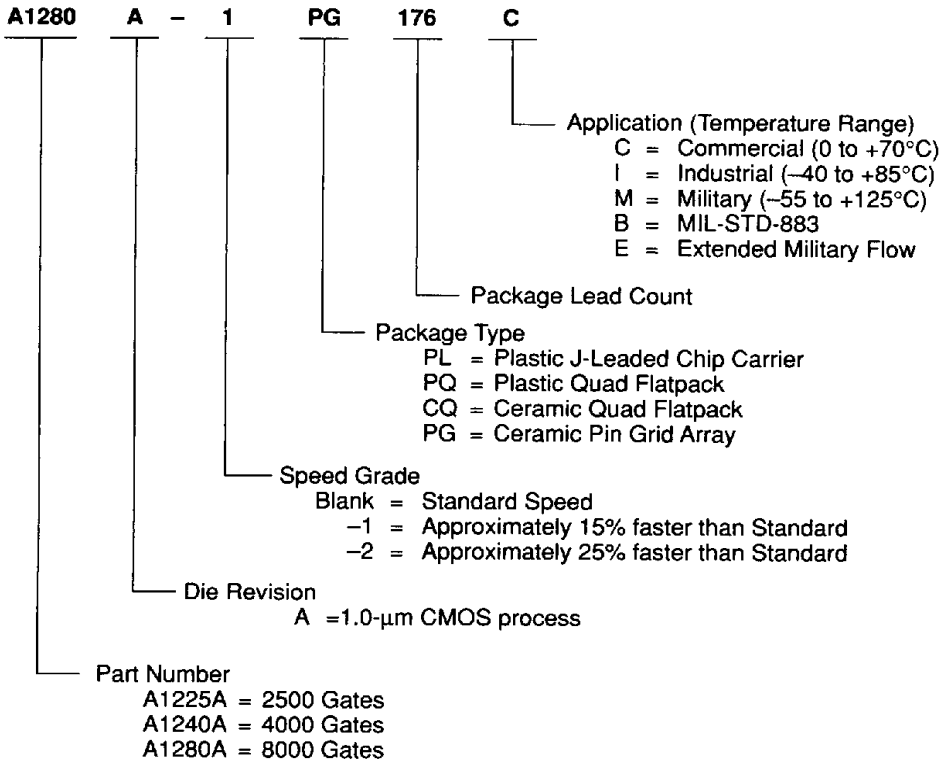
Product Family Profile

Device	A1225A	A1240A	A1280A
Capacity			
Gate Array Equivalent Gates	2,500	4,000	8,000
PLD Equivalent Gates	6,250	10,000	20,000
TTL Equivalent Packages	63	100	200
20-Pin PAL Equivalent Packages	25	40	80
Logic Modules	451	684	1,232
S-Modules	231	348	624
C-Modules	220	336	608
Flip-Flops (maximum)	382	568	998
Routing Resources			
Horizontal Tracks/Channel	36	36	36
Vertical Tracks/Channel	15	15	15
PLICE Antifuse Elements	250,000	400,000	750,000
User I/Os (maximum)	83	104	140
Packages[1]	100 CPGA 100 PQFP 84 PLCC	132 CPGA 144 PQFP 84 PLCC	176 CPGA 160 PQFP 172 CQFP
Performance[2]			
16-Bit Prescaled Counters	105 MHz	100 MHz	85 MHz
16-Bit Loadable Counters	66 MHz	63 MHz	59 MHz
16-Bit Accumulators	42 MHz	39 MHz	34 MHz
CMOS Process	1.0 µm	1.0 µm	1.0 µm

Note:

1. See product plan on page 1-33 for package availability.
2. Performance is based on '–2' speed devices at commercial worst-case operating conditions using PREP Benchmarks (mean frequency results), Suite #1, Version 1.2, dated 3-28-93, any analysis is not endorsed by PREP.

Ordering Information



Product Plan[1]

	Speed Grade*			Application				
	Std	–1	–2	C	I	M	B	E
A1225A Device								
100-pin Ceramic Pin Grid Array (PG)	✔	✔	✔	✔	—	—	—	—
100-pin Plastic Quad Flatpack (PQ)	✔	✔	✔	✔	✔	—	—	—
84-pin Plastic Leaded Chip Carrier (PL)	✔	✔	✔	✔	✔	—	—	—
A1240A Device								
132-pin Ceramic Pin Grid Array (PG)	✔	✔	✔	✔	—	✔	✔	—
144-pin Plastic Quad Flatpack (PQ)	✔	✔	✔	✔	✔	—	—	—
84-pin Plastic Leaded Chip Carrier (PL)	✔	✔	✔	✔	✔	—	—	—
A1280A Device								
176-pin Ceramic Pin Grid Array (PG)	✔	✔	✔	✔	—	✔	✔	—
160-pin Plastic Quad Flatpack (PQ)	✔	✔	✔	✔	✔	—	—	—
172-pin Ceramic Quad Flatpack (CQ)	✔	✔	✔	✔	—	✔	✔	✔

Applications: C = Commercial, I = Industrial, M = Military, B = MIL-STD-883, E = Extended Flow

Availability: ✔ = Available, P = Planned, — = Not Planned

* Speed Grade: –1 = Approx. 15% faster than Standard, –2 = Approx. 25% faster than Standard

Note:
1. Please consult Actel representatives for current availability.

Device Resources

			User I/Os							
			CPGA			PQFP			PLCC	CQFP
Device Series	Logic Modules	Gates	176-pin	132-pin	100-pin	160-pin	144-pin	100-pin	84-pin	172-pin
A1225A	451	2500	—	—	83	—	—	83	72	—
A1240A	684	4000	—	104	—	—	104	—	72	—
A1280A	1232	8000	140	—	—	125	—	—	—	140

Pin Description

CLKA **Clock A (Input)**

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKB **Clock B (Input)**

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK **Diagnostic Clock (Input)**

TTL Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND **Ground**

LOW supply voltage.

I/O **Input/Output (Input, Output)**

The I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven LOW by the ALS software.

MODE **Mode (Input)**

The MODE pin controls the use of multifunction pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os.

NC **No Connection**

This pin is not connected to circuitry within the device.

PRA **Probe A (Output)**

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

PRB **Probe B (Output)**

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDI **Serial Data Input (Input)**

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

V_{CC} **5 V Supply Voltage**

HIGH supply voltage.

V_{KS} **Programming Voltage**

Supply voltage used for device programming. This pin must be connected to GND during normal operation.

V_{PP} **Programming Voltage**

Supply voltage used for device programming. This pin must be connected to V_{CC} during normal operation.

V_{SV} **Programming Voltage**

Supply voltage used for device programming. This pin must be connected to V_{CC} during normal operation.

ACT 2 Architecture

This section of the data sheet is meant to familiarize the user with the architecture of ACT 2 family devices. A generic description of the family will be presented first, followed by a detailed description of the logic blocks, the routing structure, the antifuses, and the special function circuits. Diagrams for the ACT 2 devices are provided at the end of the data sheet. The additional circuitry required to program and test the devices will not be covered.

Array Topology

The ACT 2 family architecture is composed of five key building blocks: Logic modules, I/O modules, Routing Tracks, Global Clock Networks, and Probe Circuits. The basic structure is similar for all devices in the family, differing only in the number of rows, columns, or I/Os (see Table 1).

The logic and I/O modules are arranged in a two-dimensional array (Figure 1). There are three types of modules: Logic, I/O, and Bin. Logic and I/O modules are available as user resources. Bin modules are used during testing and are not available to users.

Table 1. Array Sizes

Device	Rows	Columns	Logic	I/O
A1225A	13	46	451	83
A1240A	14	62	684	104
A1280A	18	82	1232	140

Logic Modules

Logic modules are classified into two types: combinatorial (C-modules) and sequential (S-modules) (see Figures 2 and 3). The C-module is an enhanced version of the ACT 1 family logic module optimized to implement high fanin combinatorial macros, such as 5-input AND, and 5-input OR. The full ACT 2 combinatorial logic module is available for use as the CM8 hard macro. The S-module is designed to implement high-speed flip-flop functions within a single module. S-modules also include

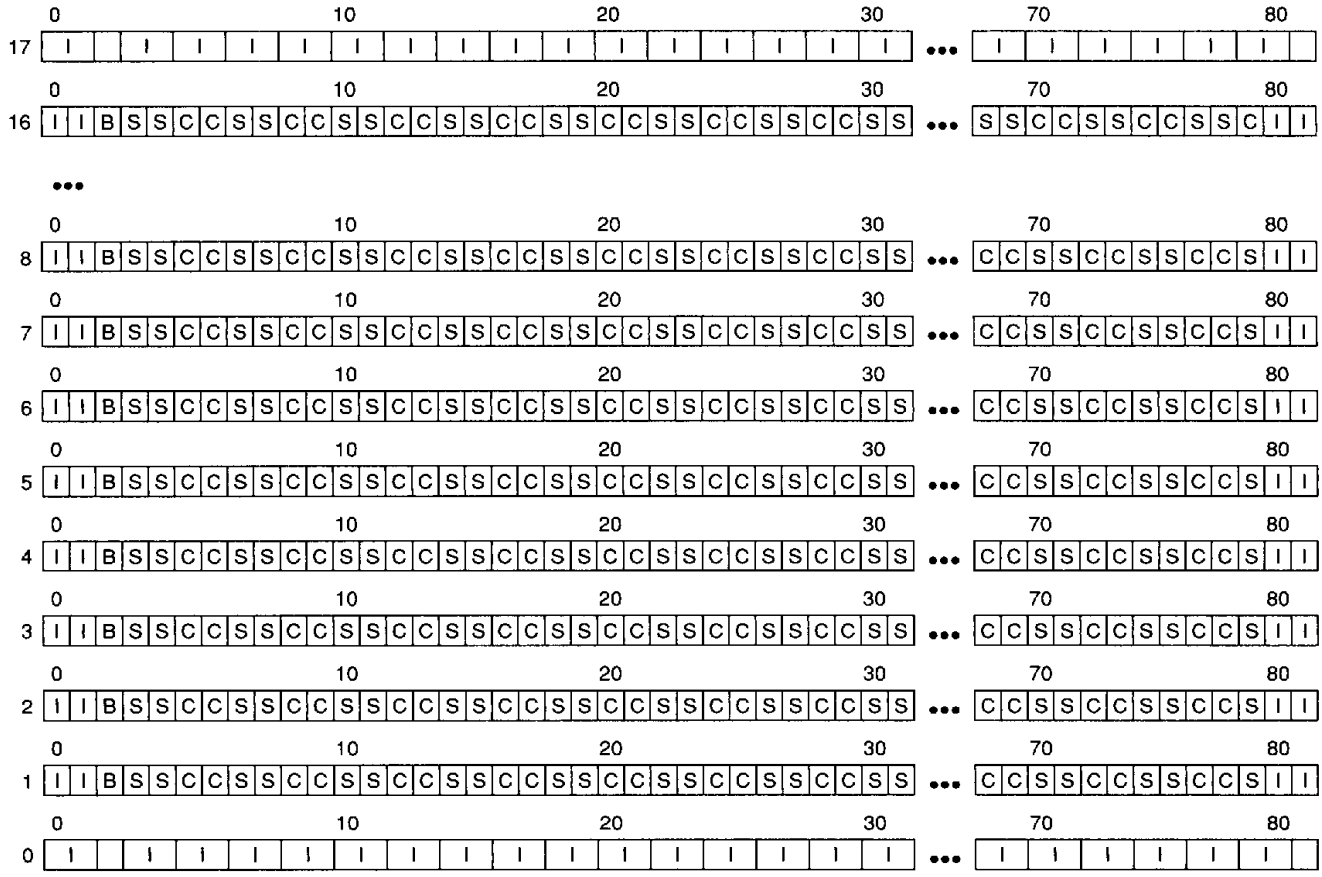


Figure 1. A1280A Simplified Floor Plan

combinatorial logic, which allows an additional level of logic to be implemented without additional propagation delay. C-modules and S-modules are arranged in pairs called module-pairs. Module-pairs are arranged in alternating pairs (shown in Figure 1) and make up the bulk of the array. This arrangement allows the placement software to support two-module macros of four types (CC, CS, SC, and SS). I/O modules are arranged around the periphery of the array.

The combinatorial module (shown in Figure 2) implements the following function:

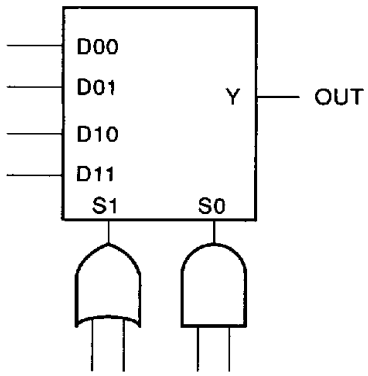
Y = !S1 * !S0 * D00 + !S1 * S0 * D01 * S1 * !S0 * D10 + S1 * S0 * D11

where:

S0 = A0 * B0

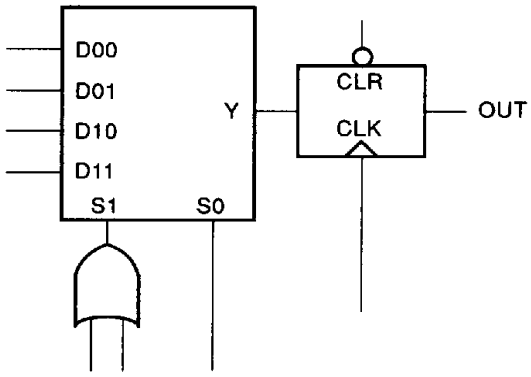
S1 = A1 + B1

The sequential module implements this same function Y (except that S0 = A0 only, since the B0 input is used for reset), followed by a sequential block. The sequential block can implement either a D-type flip-flop or a transparent latch. It can also be fully transparent so that the S-modules can be used to implement purely combinatorial functions. The function of the sequential module is determined by the macro selection from the design library of hard macros. Allowable S-module implementations are shown in Figure 3.

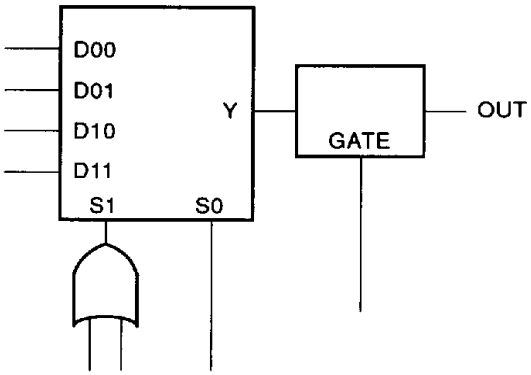


Up to 8-input function

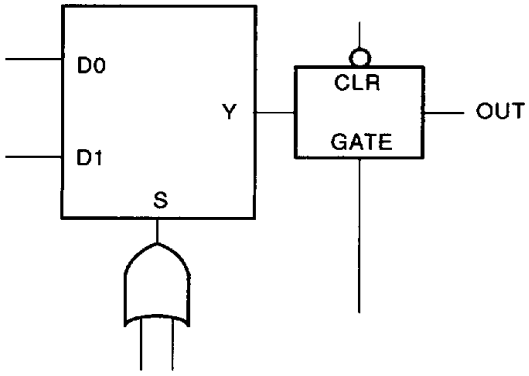
Figure 2. C-module Implementation



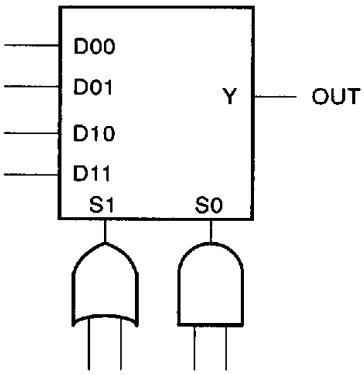
Up to 7-input function plus D-type flip-flop with clear



Up to 7-input function plus latch



Up to 4-input function plus latch with clear



Up to 8-input function (same as C-module)

Figure 3. S-module Implementations

I/Os

The I/O architecture consists of pad drivers located near the bonding pads and I/O modules located in the array. Top/bottom I/O modules are located in the top and bottom rows respectively. Side I/O modules occupy the leftmost two columns and the rightmost two columns of the array. The function of all I/O modules is identical, but the top/bottom I/O modules have a different routing interface to the array than the side I/O modules. I/Os implement a variety of user functions determined by library macro selection.

Special Purpose I/Os

Certain I/O pads are temporarily used for programming and testing the device. During normal user operation, these special I/O pads are identical to other I/O pads. The following special I/O pads and their functions are shown in Table 2.

Table 2. Special I/O Pads

SDI	Serial Data In
DCLK	Serial Data Clock In
PRA	Probe A Output
PRB	Probe B Output

Two other pads, CLKA and CLKB, also differ from normal I/Os in that they can be used to drive the global clock networks. Power, Ground, and Programming pads are not considered I/O functions. Their function is summarized as follows:

V_{CC}	Power
GND	Circuit Ground
V_{SV}, V_{KS}, V_{PP}	Programming Pads
MODE	Program/Debug Control

I/O Pads

I/O pads are located on the periphery of the die and consist of the bonding pad, the high-drive CMOS drivers, and the TTL level-shifter inputs. Each I/O pad is associated with a specific I/O module. Connections from the I/O pad to the I/O module are made using the signals DATAOUT, DATAIN, and EN (shown in Figure 4).

I/O Modules

There are two types of I/O modules: side and top/bottom. The I/O module schematic is shown in Figure 5. In the side I/O modules, there are two inputs supplying the data to be output from the chip UO1 and UO2. (UO stands for user output.) Two are used so that the router can choose to take the signal from either the routing channel above or the routing channel below the I/O module. The top/bottom I/O modules interact with only one channel and therefore have only one UO input.

The EN input enables the tristate output buffer. The global signals INEN and OUTEN (Figure 4 and Figure 5) are used to disable the inputs and outputs during certain test modes. Latches are provided in the input and output path. When GOUT is high, the latch is transparent. The latch can be used as the second stage of a rising-edge flip-flop. GIN is the reverse of GOUT. When GIN is high, the input data is latched; when it is low, the input latch becomes transparent.

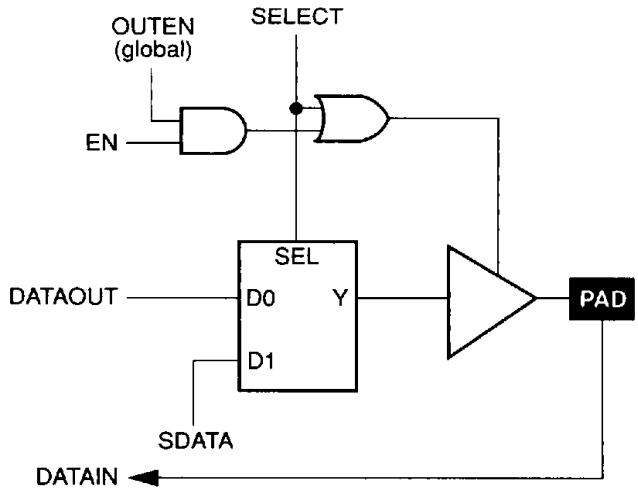


Figure 4. I/O Pad Signals

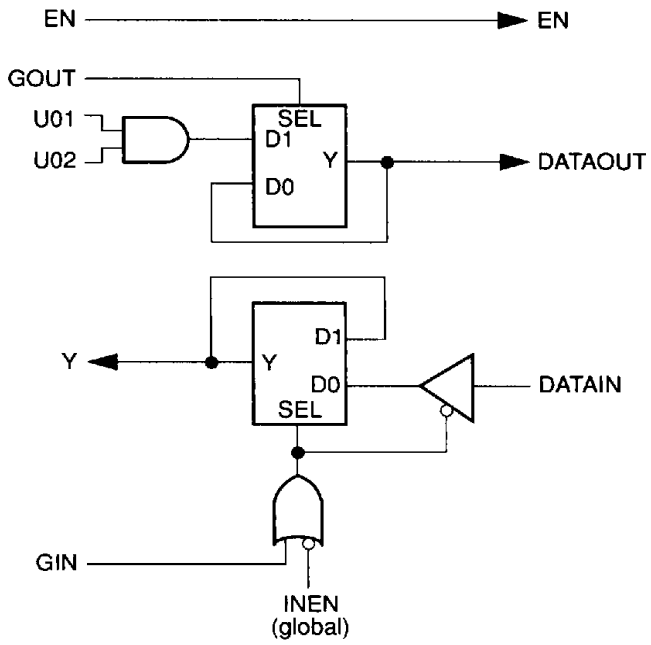


Figure 5. I/O Module

The output of the module, Y, is used for data being input to the chip. Side I/O modules have a dedicated output segment for Y extending into the routing channels above and below (similar to logic modules). Side I/O modules may also connect to the array through nondedicated Long Vertical Tracks (LVTs). Top/Bottom I/O modules have no dedicated output segment. Signals coming into the chip from the top or bottom must be routed using F-fuses and LVTs (F-fuses and LVTs are explained in detail in the routing section). I/O signals connected to I/O modules on either the top or bottom of the array may incur a delay penalty over signals connected to I/O modules on the sides.

Hard Macros

Designing within the Actel design environment is accomplished using a building block approach. Over 350 logic function macros are provided in the ACT 2 design library. Hard macro logic functions range from simple SSI gates such as AND, NOR, and Exclusive OR to more complex functions such as flip-flops with 4:1 Multiplexed Data inputs. Hard macros are implemented in the ACT 2 architecture by using one or more C-modules or S-modules. Over 200 of the macros are implemented in a single module, while several two-module macros are also available. Two-module hard macros always utilize a module-pair, either SS, CC, CS, or SC. Because one- and two-module macros have small propagation delay variances, their performances can be predicted very accurately. Hard macro propagation delays are specified in the data sheet. Soft macros comprise multiple hard macros connected together to form complex functions. These functions range from MSI functions to 16-bit counters and accumulators. A large number of TTL equivalent hard and soft macros are also provided. Soft macro delays are not specified in the data sheet.

Routing Structure

The ACT 2 architecture uses Vertical and Horizontal routing tracks to interconnect the various logic and I/O modules. These routing tracks are metal interconnects that may either be of continuous length or broken into pieces called segments. Segments can be joined together at the ends using antifuses to increase their lengths up to the full length of the track.

Horizontal Routing

Horizontal channels are located between the rows of modules and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module-pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third the row length is considered a long horizontal segment. A typical channel is shown in Figure 6. Nondedicated horizontal routing tracks are used to route signal nets. Dedicated routing tracks are used for the global clock networks and for power and ground tie-off tracks.

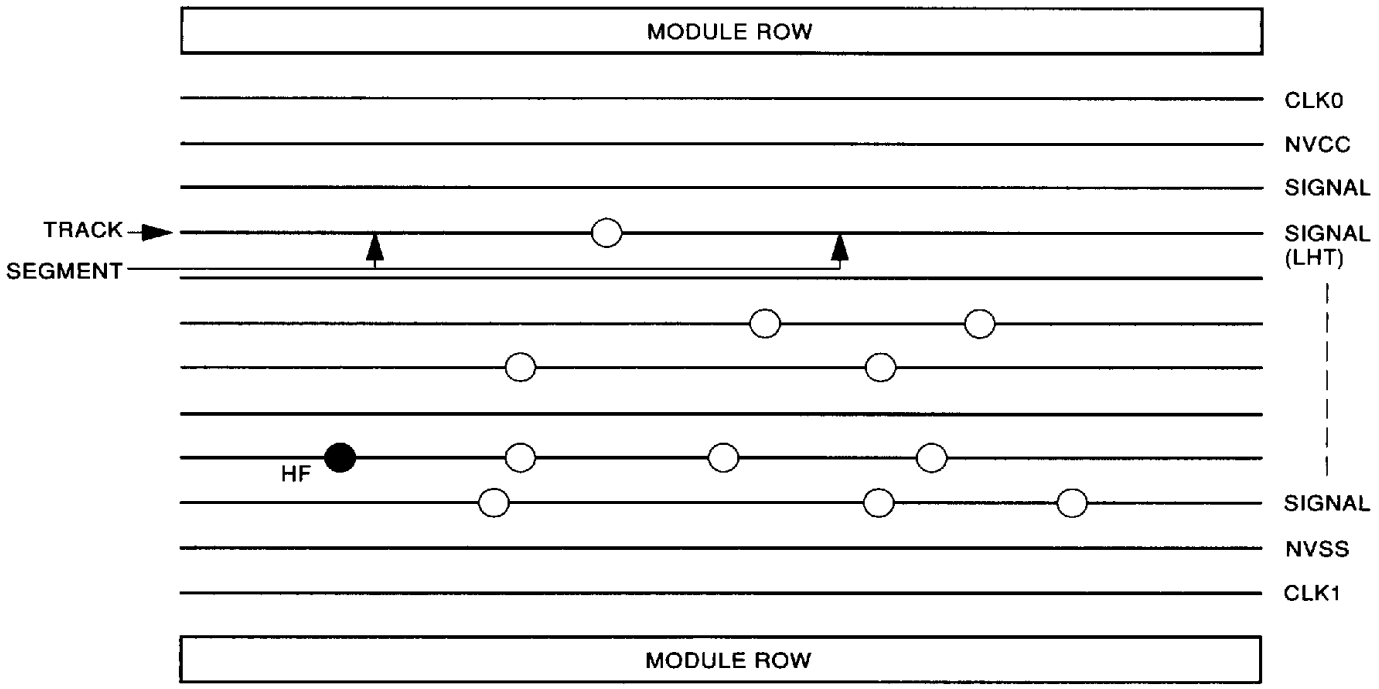


Figure 6. Horizontal Routing Tracks and Segments

Vertical Routing

Other tracks run vertically through the module. Vertical tracks are of three types: input, output, and long. Vertical tracks are also divided into one or more segments. Each segment in an input track is dedicated to the input of a particular module. Each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array where edge effects occur. LVTs contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 7.

Antifuse Structures

An antifuse is a "normally open" structure as opposed to the normally closed fuse structure used in PROMs or PALs. The use of antifuses to implement a Programmable Logic Device results in highly testable structures as well as efficient programming algorithms. The structure is highly testable because there are no preexisting connections; therefore, temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed as well as isolate individual circuit structures to be tested. This can be done both before and after programming. For example, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

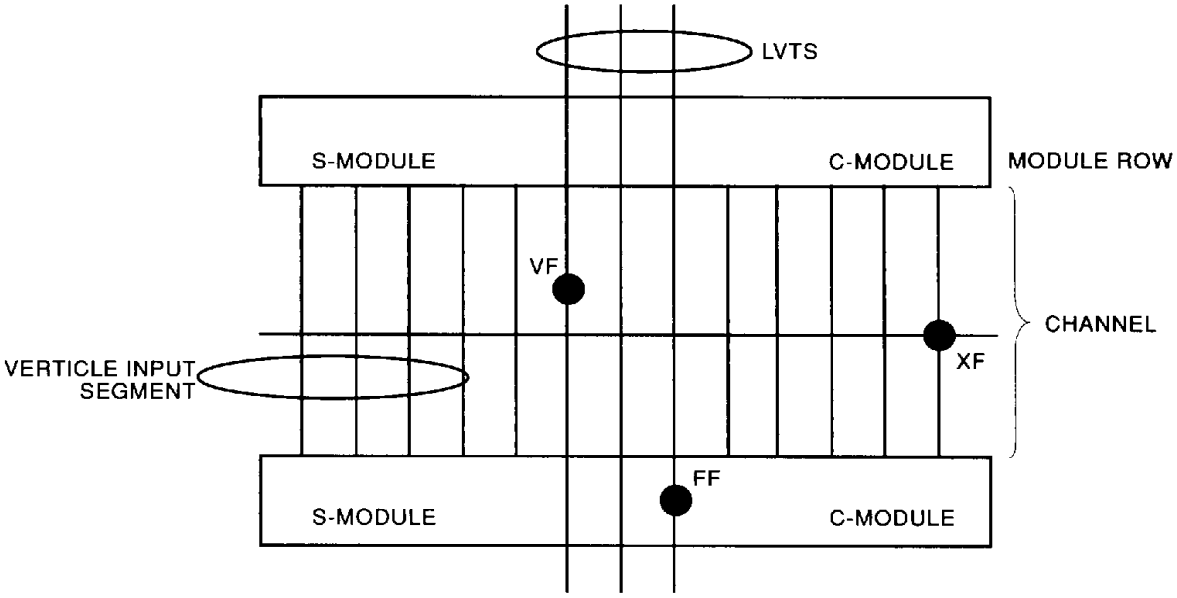


Figure 7. Vertical Routing Tracks and Segments

Antifuse Connections

Four types of antifuse connections are used in the routing structure of the ACT 2 array. (The physical structure of the antifuse is identical in each case; only the usage differs.) The four types are:

XF	Cross-connected antifuse	Most intersections of horizontal and vertical tracks have an XF that connects the perpendicular tracks.
HF	Horizontally connected antifuses	Adjacent segments in the same horizontal tracks are connected end-to-end by an HF.
VF	Vertically connected antifuse	Some long vertical tracks are divided into two segments. Adjacent long segments are connected end-to-end by a VF.
FF	"Fast-Fuse" antifuse	The FF connects a module output directly to a long vertical track.

Examples of all four antifuse connections are shown in Figures 6 and 7.

Antifuse Programming

The ACT 2 family uses the PLICE antifuse developed by Actel. The PLICE element is programmed by placing a high voltage (~17 V) across the element and supplying current (~5 mA) for a short duration (<1 ms). In the ACT 2 architecture, most antifuses are programmed to ~500 ohms resistance, except for the F-fuses which are programmed to ~250 ohms. The programming circuits are transparent to the user.

Clock Networks

Two low-skew, high fanout clock distribution networks are provided in the ACT 2 architecture (Figure 8). These networks are referred to as CLK0 and CLK1. Each network has a clock module (CLKMOD) that selects the source of the clock signal and may be driven as follows:

1. externally from the CLKA pad
2. externally from the CLKB pad
3. internally from the CLKINA input
4. internally from the CLKINB input

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel.

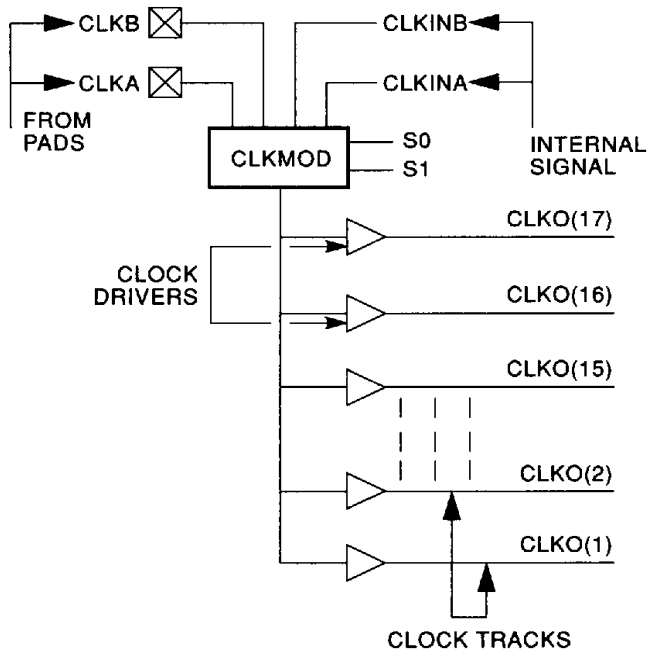


Figure 8. Clock Networks

The user controls the clock module by selecting one of two clock macros from the macro library. The macro CLKBUF is used to connect one of the two external clock pins to a clock network, and the macro CLKINT is used to connect an internally generated clock signal to a clock network. Since both clock networks are identical, the user does not care whether CLK0 or CLK1 is being used.

The clock input pads may also be used as normal I/Os, bypassing the clock networks.

Module Interface

Connections to logic and I/O modules are made through vertical segments that connect to the module inputs and outputs. These vertical segments lie on vertical tracks that span the entire height of the array.

Module Input Connections

The tracks dedicated to Module inputs are segmented by pass transistors in each module row. During normal user operation, the pass transistors are inactive (off), which isolates the inputs of a module from the inputs of the module directly above or below it. During certain test modes, the pass transistors are active (on) to verify the continuity of the metal tracks. Vertical input segments span only one channel. Inputs to the array modules come either from the channel above or the channel below. The logic modules are arranged so that half of the inputs are connected to the channel above and half of the inputs to segments in the channel below (Figure 9).

Module Output Connections

Module outputs have dedicated output segments. Output segments extend vertically two channels above and two channels below, except at the top or bottom of the array. Output segments twist, as shown in Figure 9, so that only four vertical tracks are required.

LVT Connections

Outputs may also connect to nondedicated segments (LVTs). Each module-pair in the array shares three LVTs that span the length of column as shown in Figure 9. Any module in the column pair can connect to one of the LVTs in the column using an FF connection. The FF connection uses antifuses connected directly to the driver stage of the module output, bypassing the isolation transistor. FF antifuses are programmed at a higher current level than HF, VF, or XF antifuses to produce a lower resistance value.

Antifuse Connections

In general, every intersection of a vertical segment and a horizontal segment contains an unprogrammed antifuse (XF-type). One exception is in the case of the clock networks.

Clock Connections

To minimize loading on the clock networks, only a subset of inputs has fuses on the clock tracks. Only a few of the C-module and S-module inputs can be connected to the clock networks. To further reduce loading on the clock network, only a subset of the horizontal routing tracks can connect to the clock inputs of the S-module. Both of these are illustrated in Figure 10.

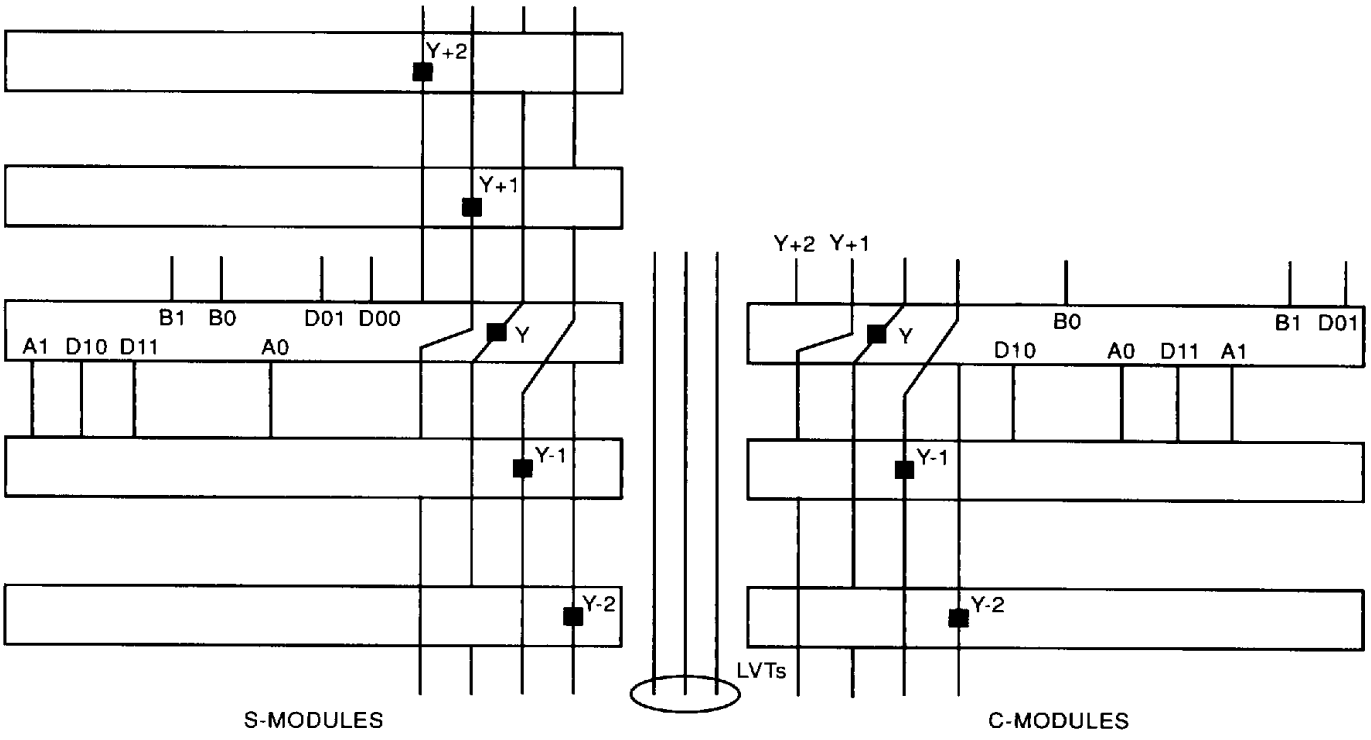


Figure 9. Logic Module Routing Interface

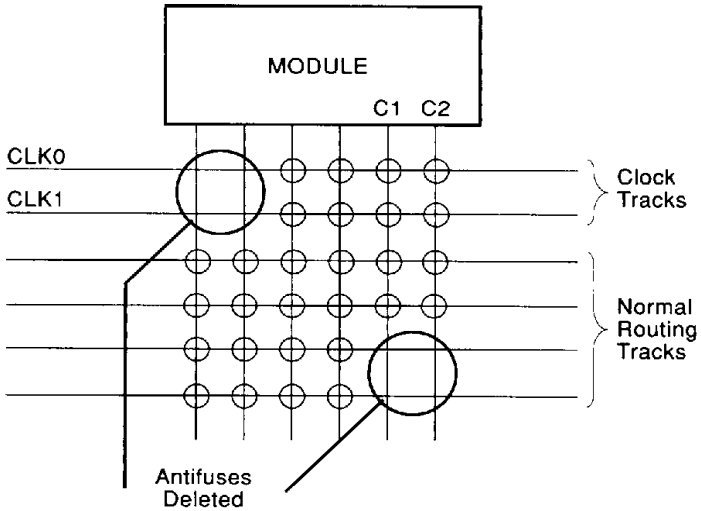


Figure 10. Fuse Deletion on Clock Networks

Programming and Test Circuits

The array of logic and I/O modules is surrounded by test and programming circuits controlled by the external pins: MODE, SDI, and DCLK. When MODE is low (GND), the device is in normal or user mode. When MODE is high (V_{CC}), the device is placed into one of several programming or test states. The SDI pin (when MODE is high) is used to input serial data to the Mode Register and various address registers surrounding the array. Data is clocked into these registers using the DCLK pin. The registers are connected as a long series of shift registers as shown in Figure 11. The Mode register determines the test or programming state of the device. Many of the test modes are used during wafer sort and final test at the factory. Other test modes are used during programming with the Activator® 2, and some of the modes are available only after programming. The Actionprobe® function is one such function available to users.

Actionprobe

If a device has been successfully programmed and the security fuse has not been programmed, any internal logic or I/O module output can be observed using the Actionprobe circuitry and the PRA and/or PRB pins. The Actionprobe diagnostic system provides the software and hardware required to perform real-time debugging. The software automatically performs the following functions.

A pattern of *ones* and *zeros* is shifted into the device from the SDI pin at each positive edge transition of DCLK. The complete sequence contains 10 bits of counter, 21 bits of Mode Register, n bits of zeros (filler of unused fields, where n depends on the particular device type), R bits of X2, C bits of Y2, R bits of X1, C bits of Y1, and a stop bit ("0" or "1"). After the stop bit has been shifted in, DCLK is left high. X1 and Y1 represent the (X,Y) location in the array for the Actionprobe output, PRA.

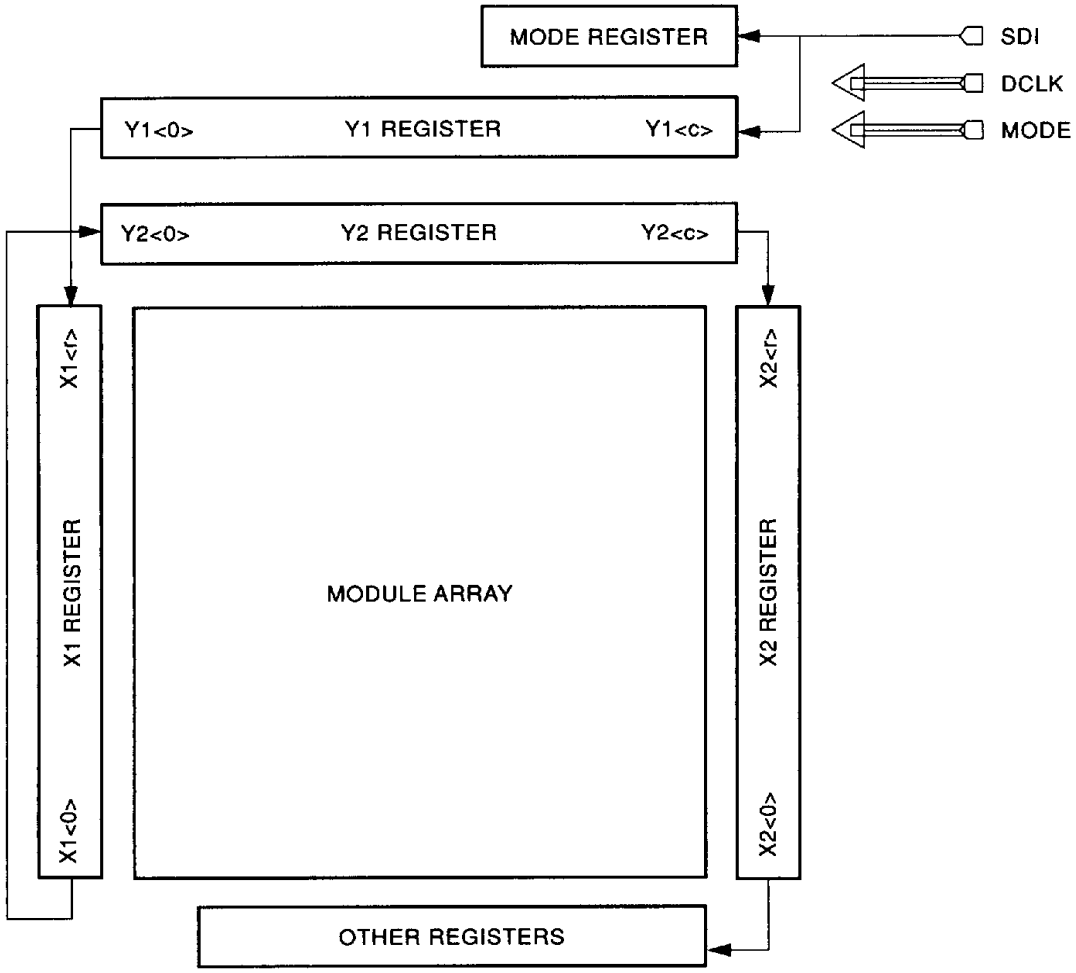


Figure 11. ACT 2 Shift Register

X2 and Y2 represent the (X,Y) location in the array for the Actionprobe output, PRB. R and C are the row and column size as defined in Table 1. The filler bits, counter pattern, and Mode Register pattern are shown in Table 3. Addressing for rows and columns is active high; that is, unselected rows and columns are "zeros" and the selected row and column is "high." The timing sequence is shown in Figure 12. The recommended frequency is 10 MHz with 10 ns setup and hold times allowing for SDI and DCLK transitions. The selected module output will be present at the PRA or PRB output approximately 20 ns after the stop-bit transition.

Table 3. Bit Stream Definitions for Actionprobe Diagnostics

Device	Probe_Mode	Filler (n)	Counter_Pattern	Mode_Register_Pattern	# of clocks
A1225A	Probe A only	308	1101011010	000000110001111100000	458
A1225A	Probe B only	308	1101011010	000000101001111100000	458
A1225A	Probe A and B	308	1101011010	000000111001111100000	458
A1240A	Probe A only	361	1111000001	000000110001111100000	545
A1240A	Probe B only	361	1111000001	000000101001111100000	545
A1240A	Probe A and B	361	1111000001	000000111001111100000	545
A1280A	Probe A only	443	0011011111	000000110001111100000	675
A1280A	Probe B only	443	0011011111	000000101001111100000	675
A1280A	Probe A and B	443	0011011111	000000111001111100000	675

For example: Selecting PRA for A1280 results in the following bit stream.
0011011111_000000110001111100000_
(433 zeros)_X2<0>...X2<17>_Y2<81>...Y2<0>_X1<0>...X1<0>...X1<17>_Y1<0>...Y1<81>_0,
where "_" is used for clarity only

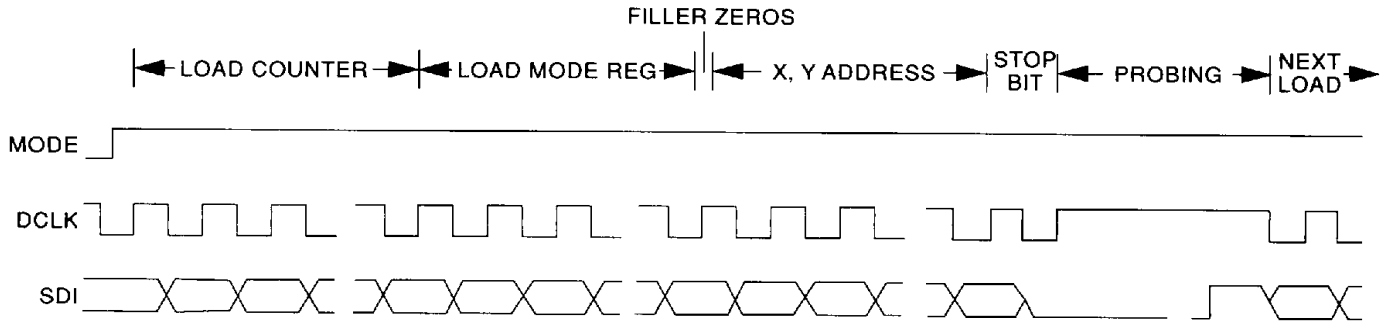


Figure 12. Timing Waveforms

Absolute Maximum Ratings[1]

Free air temperature range

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage[2,3,4]	–0.5 to +7.0	V
V_I	Input Voltage	–0.5 to V_{CC} +0.5	V
V_O	Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IO}	I/O Source/Sink Current[5]	±20	mA
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.
2. $V_{PP} = V_{CC}$, except during device programming.
3. $V_{SV} = V_{CC}$, except during device programming.
4. V_{KS} = GND, except during device programming.
5. Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5 V or less than GND – 0.5 V, the internal protection diode will be forward biased and can draw excessive current.

Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range[1]	0 to +70	–40 to +85	–55 to +125	°C
Power Supply Tolerance	±5	±10	±10	%V_{CC}

Note:

1. Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.

Electrical Specifications

Symbol	Parameter	Commercial		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}[1]	(I_{OH} = –10 mA)[2]	2.4						V
	(I_{OH} = –6 mA)	3.84						V
	(I_{OH} = –4 mA)			3.7		3.7		V
V_{OL}[1]	(I_{OL} = 10 mA)[2]		0.5					V
	(I_{OL} = 6 mA)		0.33		0.40		0.40	V
V_{IL}		–0.3	0.8	–0.3	0.8	–0.3	0.8	V
V_{IH}		2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
Input Transition Time t_R, t_F[2]			500		500		500	ns
C_{IO} I/O Capacitance[2,3]			10		10		10	pF
Standby Current, I_{CC}[4]			2		10		20	mA
Leakage Current[5]		–10	10	–10	10	–10	10	µA

Notes:

1. Only one output tested at a time. V_{CC} = min.
2. Not tested, for information only.
3. Includes worst-case 176 CPGA package capacitance. V_{OUT} = 0 V, f = 1 MHz.
4. All outputs unloaded. All inputs = V_{CC} or GND, typical I_{CC} = 1 mA. I_{CC} limit includes I_{PP} and I_{SV} during normal operation.
5. V_{OUT}, V_{IN} = V_{CC} or GND.

Package Thermal Characteristics

The device junction to case thermal characteristic is θjc, and the junction to ambient air characteristic is θja. The thermal characteristics for θja are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a PQFP 160-pin package at commercial temperature is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. commercial temp.}}{\theta ja\ (°C/W)} = \frac{150°C - 70°C}{33°C/W} = 2.4\ W$$

Package Type	Pin Count	θjc	θja Still Air	θja 300 ft/min	Units
Ceramic Pin Grid Array	100	5	35	17	°C/W
	132	5	30	15	°C/W
	176	8	23	12	°C/W
Ceramic Quad Flatpack	172	8	25	15	°C/W
Plastic Quad Flatpack[1]	100	13	55	47	°C/W
	144	15	35	26	°C/W
	160	15	33	24	°C/W
Plastic Leaded Chip Carrier[2]	84	12	44	33	°C/W

Notes:
1. Maximum Power Dissipation for PQFP packages is 2.0 Watts.
2. Maximum Power Dissipation for PLCC packages is 1.5 Watts.

Power Dissipation

$P = [I_{CC} + I_{active}] * V_{CC} + I_{OL}*V_{OL}*N + I_{OH}*(V_{CC}-V_{OH})*M$

Where:

I_{CC} is the current flowing when no inputs or outputs are changing.

I_{active} is the current flowing due to CMOS switching.

I_{OL}, I_{OH} are TTL sink/source currents.

V_{OL}, V_{OH} are TTL level output voltages.

N equals the number of outputs driving TTL loads to V_{OL}.

M equals the number of outputs driving TTL loads to V_{OH}.

An accurate determination of N and M is problematic because their values depend on the design and on the system I/O. The power can be divided into two components: static and active.

Static Power

Static power dissipation is typically a small component of the overall power. From the values provided in the Electrical Specifications, the maximum static power (commercial) dissipation is:

2 mA * 5.25 V = 10.5 mW

The static power dissipation by TTL loads depends on the number of outputs that drive high or low and the DC lead current flowing. Again, this number is typically small. For instance, a 32-bit bus driving TTL loads will generate 42 mW with all outputs driving low or 140 mW with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

Active Time

The active power component in CMOS devices is frequency dependent and is contingent on the user's logic and the external I/O. Active power dissipation results from charging internal chip capacitance such as that associated with the interconnect, unprogrammed antifuses, module inputs, and module outputs plus external capacitance due to PC board traces and load device inputs. An additional component of active power dissipation is due to totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by Equation 1.

$$\text{Power}\ (\mu W) = C_{EQ} * V_{CC}^2 * f \qquad (1)$$

Where:

C_{EQ} is the equivalent capacitance expressed in picofarads (pF).

V_{CC} is power supply in volts (V).

f is the switching frequency in megahertz (MHz).

Equivalent capacitance is calculated by measuring I_{active} at a specified frequency and voltage for each circuit component of interest. The results for ACT 2 devices are:

	C_{EQ} (pF)
Modules	7.7
Input Buffers	18.0
Output Buffers	25.0
Clock Buffer Loads	2.5

To calculate the active power dissipated from the complete design, you must solve Equation 1 for each component. To do this, you must know the switching frequency of each part of the logic. The exact equation is a piece-wise linear summation over all components, as shown in Equation 2.

$$\text{Power } (\mu W) = [(m * 7.7 \times f_1) + (n * 18.0 \times f_2) + (p * (25.0 + C_L) * f_3) + (q \times 2.5 \times f_4)] * V_{CC}^2 \quad (2)$$

Where:

m = Number of logic modules switching at frequency f_1

n = Number of input buffers switching at frequency f_2

p = Number of output buffers switching at frequency f_3

q = Number of clock loads on the global clock network

f_1 = Average logic module switching rate in MHz

f_2 = Average input buffer switching rate in MHz

f_3 = Average output buffer switching rate in MHz

f_4 = Frequency of global clock

C_L = Output load capacitance in pF

Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following rules will help you to determine average switching frequency in logic circuits. These rules are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These rules are as follows:

Module Utilization = 80% of combinatorial modules

Average Module Frequency = F/10

Inputs = 1/3 of I/O

Average Input Frequency = F/5

Outputs = 2/3 of I/Os

Average Output Frequency = F/10

Clock Net 1 Loading = 40% of sequential modules

Clock Net 1 Frequency = F

Clock Net 2 Loading = 40% of sequential modules

Clock Net 2 Frequency = F/2

Estimated Power

The results of estimating active power are displayed in Figure 13. The graphs provide a simple guideline for estimating power. The tables may be interpolated when your application has different resource utilizations or frequencies.

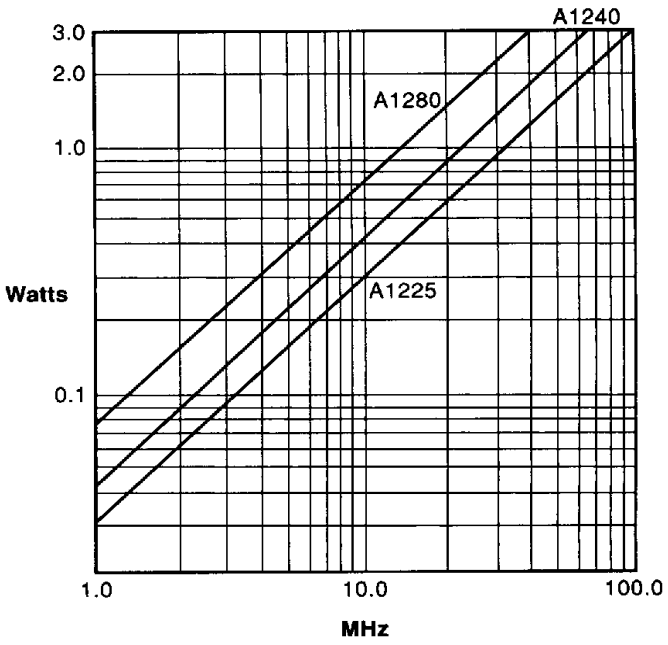
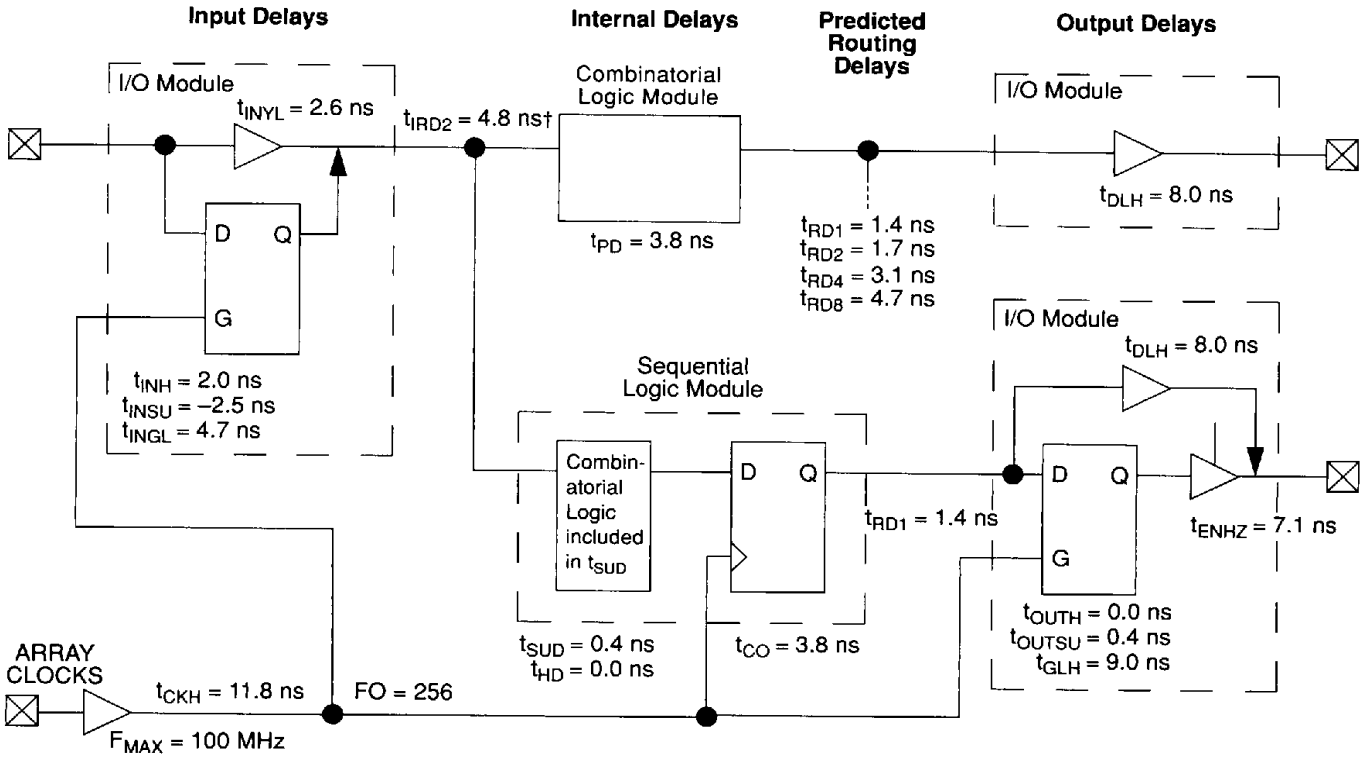


Figure 13. ACT 2 Power Estimates

ACT 2 Timing Model*

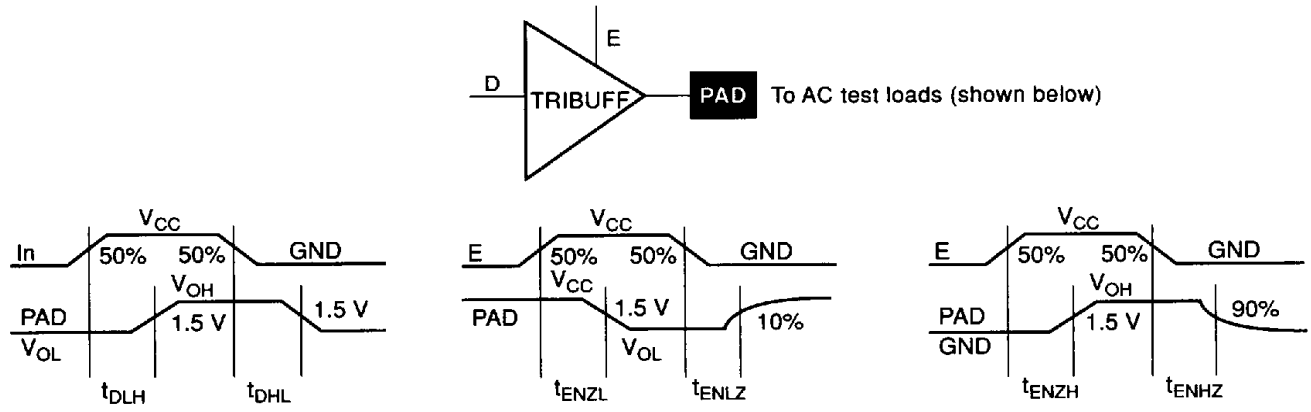


*Values shown for A1240A-2 at worst-case commercial conditions.

† Input Module Predicted Routing Delay

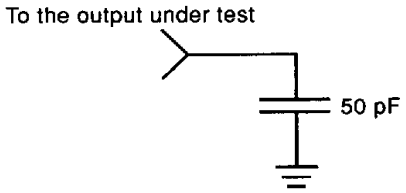
Parameter Measurement

Output Buffer Delays

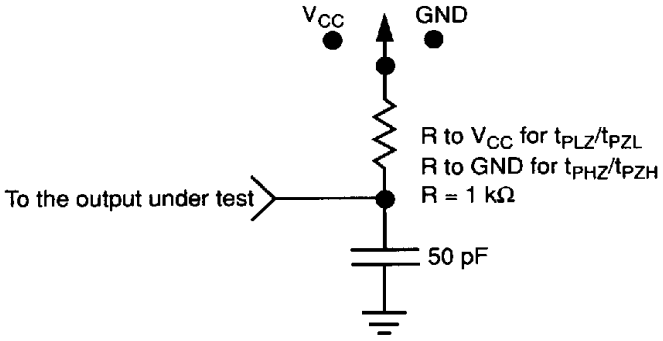


AC Test Loads

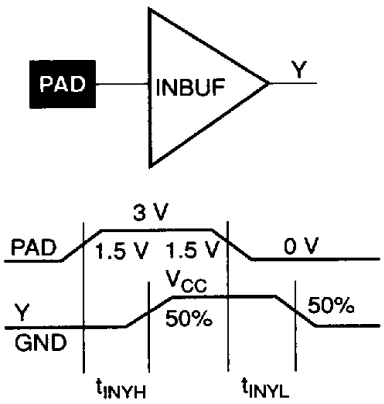
Load 1
(Used to measure propagation delay)



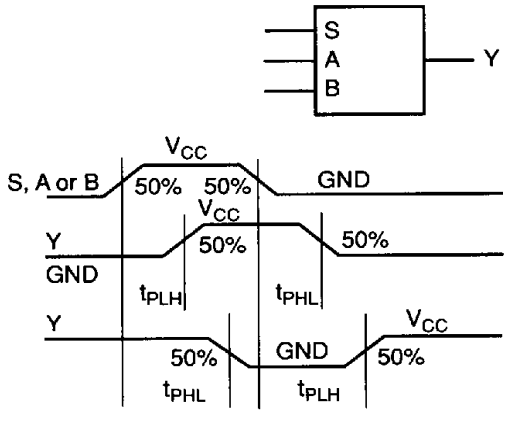
Load 2
(Used to measure rising/falling edges)



Input Buffer Delays

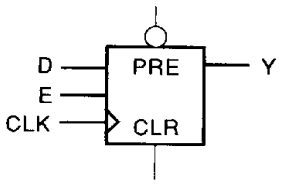


Combinatorial Macro Delays

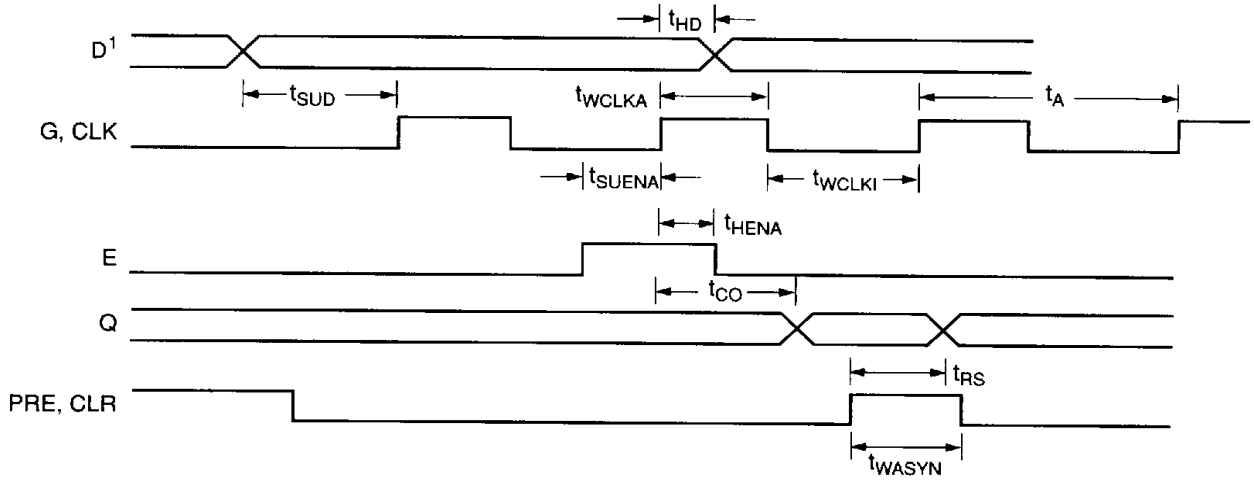


Sequential Timing Characteristics

Flip-Flops and Latches



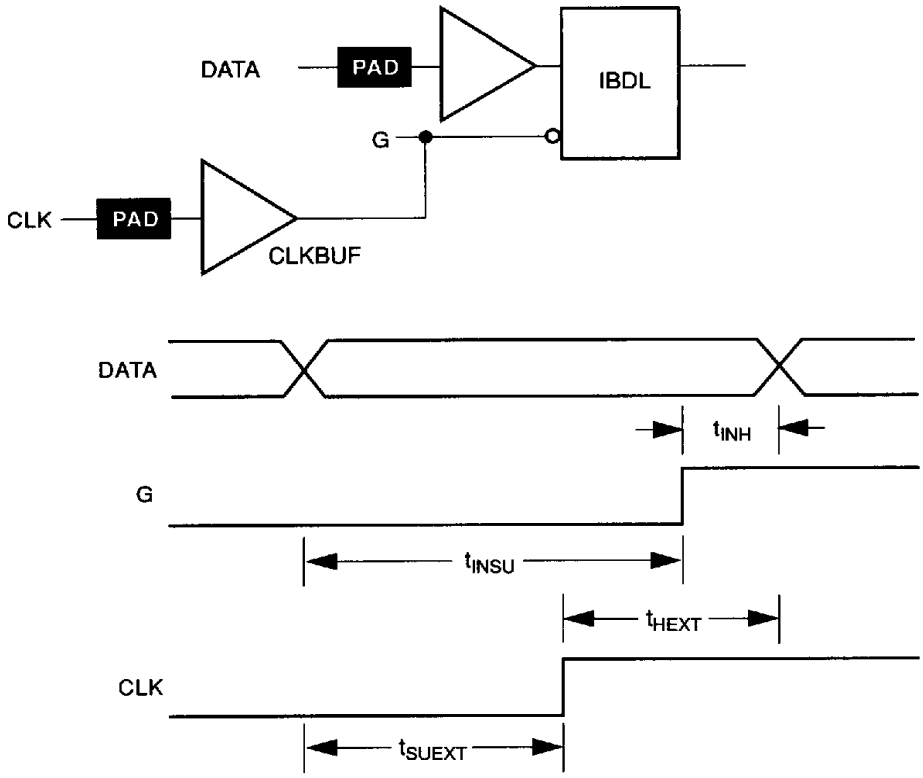
(Positive edge triggered)



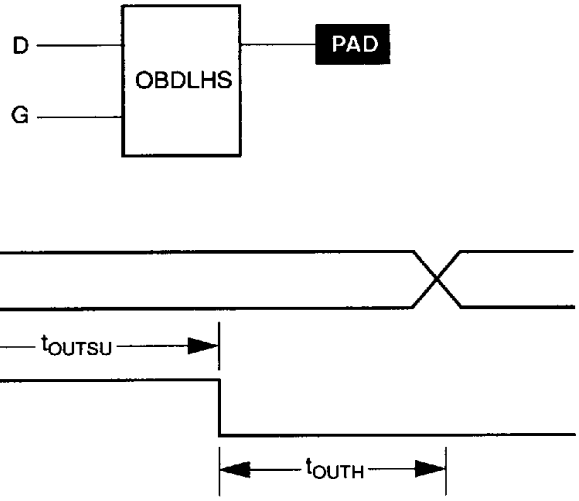
Note:
1. D represents all data functions involving A, B, and S for multiplexed flip-flops.

Sequential Timing Characteristics (continued)

Input Buffer Latches



Output Buffer Latches



Predictable Performance: Tight Delay Distributions

Propagation delay between logic modules depends on the resistive and capacitive loading of the routing tracks, the interconnect elements, and the module inputs being driven. Propagation delay increases as the length of routing tracks, the number of interconnect elements, or the number of inputs increases.

From a design perspective, the propagation delay can be statistically correlated or modeled by the fanout (number of loads) driven by a module. Higher fanout usually requires some paths to have longer routing tracks.

The ACT 2 family delivers a very tight fanout delay distribution. This tight distribution is achieved in two ways: by decreasing the delay of the interconnect elements and by decreasing the number of interconnect elements per path.

Actel's patented PLICE antifuse offers a very low resistive/capacitive interconnect. The ACT 2 family's antifuses, fabricated in 1.0 µm lithography, offer nominal levels of 500 ohms resistance and 7.5 femtofarad (fF) capacitance per antifuse.

The ACT 2 fanout distribution is also tight due to the low number of antifuses required for each interconnect path. The ACT 2 family's proprietary architecture limits the number of antifuses per path to a maximum of four, with 90% of interconnects using two antifuses.

Table 4. Logic Module + Routing Delay, by Fanout (ns) (Worst-Case Commercial Conditions)

Family	FO=1	FO=2	FO=3	FO=4	FO=8
A1225A-2	4.9	5.5	6.1	6.6	8.2
A1240A-2	5.2	5.5	6.1	6.9	8.5
A1280A-2	5.5	6.3	6.8	7.5	10.5

Timing Characteristics

Timing characteristics for ACT 2 devices fall into three categories: family dependent, device dependent, and design dependent. The input and output buffer characteristics are common to all ACT 2 family members. Internal routing delays are device dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the ALS Timer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most time-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6% of the nets in a design may be designated as critical, while 90% of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes four antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6% of nets in a fully utilized device require long tracks. Long tracks contribute approximately 6 ns to 12 ns delay. This additional delay is represented statistically in higher fanout (FO=8) routing delays in the data sheet specifications section.

Timing Derating

A best case timing derating factor of 0.45 is used to reflect best case processing. Note that this factor is relative to the "standard speed" timing parameters, and must be multiplied by the appropriate voltage and temperature derating factors for a given application.

Timing Derating Factor (Temperature and Voltage)

	Industrial		Military	
	Min.	Max.	Min.	Max.
(Commercial Minimum/Maximum Specification) x	0.69	1.11	0.67	1.23

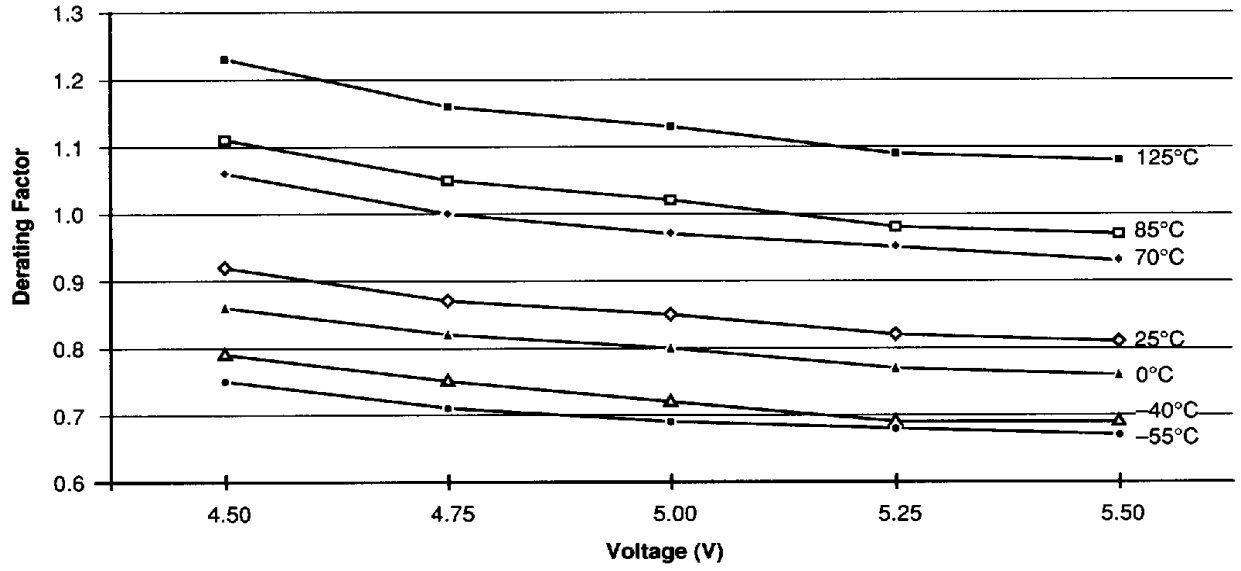
Timing Derating Factor for Designs at Typical Temperature (T_J = 25°C) and Voltage (5.0 V)

(Commercial Maximum Specification) x	0.85

Temperature and Voltage Derating Factors (normalized to Worst-Case Commercial, T_J = 4.75 V, 70°C)

	–55	–40	0	25	70	85	125
4.50	0.75	0.79	0.86	0.92	1.06	1.11	1.23
4.75	0.71	0.75	0.82	0.87	1.00	1.05	1.16
5.00	0.69	0.72	0.80	0.85	0.97	1.02	1.13
5.25	0.68	0.69	0.77	0.82	0.95	0.98	1.09
5.50	0.67	0.69	0.76	0.81	0.93	0.97	1.08

Junction Temperature and Voltage Derating Curves
(normalized to Worst-Case Commercial, T_J = 4.75 V, 70°C)



Note:
This derating factor applies to all routing and propagation delays.

A1225A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)

Logic Module Propagation Delays[1]		'Std' Speed		'–1' Speed		'–2' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		5.0		4.3		3.8	ns
t_{CO}	Sequential Clk to Q		5.0		4.3		3.8	ns
t_{GO}	Latch G to Q		5.0		4.3		3.8	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		5.0		4.3		3.8	ns
Predicted Routing Delays[2]								
t_{RD1}	FO=1 Routing Delay		1.4		1.2		1.1	ns
t_{RD2}	FO=2 Routing Delay		2.2		1.9		1.7	ns
t_{RD3}	FO=3 Routing Delay		3.0		2.6		2.3	ns
t_{RD4}	FO=4 Routing Delay		3.7		3.1		2.8	ns
t_{RD8}	FO=8 Routing Delay		5.8		4.9		4.4	ns
Sequential Timing Characteristics[3,4]								
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.4		0.4		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	1.0		1.0		1.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	6.0		5.0		4.5		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.0		5.0		4.5		ns
t_A	Flip-Flop Clock Input Period	13.0		11.0		9.4		ns
t_{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Setup	0.4		0.4		0.4		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Setup	0.4		0.4		0.4		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		75.0		90.0		105.0	MHz

Notes:

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the ALS Timer utility.
4. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

A1225A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			'Std' Speed		'–1' Speed		'–2 Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Pad to Y High			3.8		3.3		2.9	ns
t_{INYL}	Pad to Y Low			3.5		3.0		2.6	ns
t_{INGH}	G to Y High			6.6		5.7		5.0	ns
t_{INGL}	G to Y Low			6.3		5.4		4.7	ns
Input Module Predicted Routing Delays[1]									
t_{IRD1}	FO=1 Routing Delay			5.4		4.6		4.1	ns
t_{IRD2}	FO=2 Routing Delay			6.1		5.2		4.6	ns
t_{IRD3}	FO=3 Routing Delay			7.1		6.0		5.3	ns
t_{IRD4}	FO=4 Routing Delay			7.6		6.4		5.7	ns
t_{IRD8}	FO=8 Routing Delay			9.8		8.3		7.4	ns
Global Clock Network									
t_{CKH}	Input Low to High	FO = 32		12.8		11.0		10.2	ns
		FO = 256		15.7		13.0		11.8	
t_{CKL}	Input High to Low	FO = 32		12.8		11.0		10.2	ns
		FO = 256		15.9		13.2		12.0	
t_{PWH}	Minimum Pulse Width High	FO = 32	4.5		4.1		3.4		ns
		FO = 256	5.0		4.5		3.8		
t_{PWL}	Minimum Pulse Width Low	FO = 32	4.5		4.1		3.4		ns
		FO = 256	5.0		4.5		3.8		
t_{CKSW}	Maximum Skew	FO = 32		0.7		0.7		0.7	ns
		FO = 256		3.5		3.5		3.5	
t_{SUEXT}	Input Latch External Setup	FO = 32	0.0		0.0		0.0		ns
		FO = 256	0.0		0.0		0.0		
t_{HEXT}	Input Latch External Hold	FO = 32	7.0		7.0		7.0		ns
		FO = 256	11.2		11.2		11.2		
t_P	Minimum Period	FO = 32	9.1		8.3		7.7		ns
		FO = 256	10.0		8.8		8.1		
f_{MAX}	Maximum Frequency	FO = 32		110.0		120.0		130.0	MHz
		FO = 256		100.0		115.0		125.0	

Note:

1. These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1225A Timing Characteristics (continued)
(Worst-Case Commercial Conditions)

Output Module Timing		'Std' Speed		'–1' Speed		'–2 Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1, 2]								
t_{DLH}	Data to Pad High		10.6		9.0		8.0	ns
t_{DHL}	Data to Pad Low		13.4		11.4		10.1	ns
t_{ENZH}	Enable Pad Z to High		11.8		10.0		8.9	ns
t_{ENZL}	Enable Pad Z to Low		15.5		13.2		11.6	ns
t_{ENHZ}	Enable Pad High to Z		9.4		8.0		7.1	ns
t_{ENLZ}	Enable Pad Low to Z		11.1		9.5		8.3	ns
t_{GLH}	G to Pad High		11.9		10.2		8.9	ns
t_{GHL}	G to Pad Low		14.9		12.7		11.2	ns
d_{TLH}	Delta Low to High		0.09		0.08		0.07	ns/pF
d_{THL}	Delta High to Low		0.16		0.13		0.12	ns/pF
CMOS Output Module Timing[1, 2]								
t_{DLH}	Data to Pad High		13.5		11.5		10.1	ns
t_{DHL}	Data to Pad Low		11.2		9.6		8.4	ns
t_{ENZH}	Enable Pad Z to High		11.8		10.0		8.9	ns
t_{ENZL}	Enable Pad Z to Low		15.5		13.2		11.6	ns
t_{ENHZ}	Enable Pad High to Z		9.4		8.0		7.1	ns
t_{ENLZ}	Enable Pad Low to Z		11.1		9.5		8.3	ns
t_{GLH}	G to Pad High		11.9		10.2		8.9	ns
t_{GHL}	G to Pad Low		14.9		12.7		11.2	ns
d_{TLH}	Delta Low to High		0.16		0.13		0.12	ns/pF
d_{THL}	Delta High to Low		0.12		0.10		0.09	ns/pF

Notes:
1. Delays based on 50 pF loading.
2. Maximum Recommended Simultaneous Switching Outputs:

PLCC	20pF	72
	35pF	45
	50pF	32
PQFP, CPGA	20pF	80
	35pF	45
	50pF	32

A1240A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)

Logic Module Propagation Delays[1]		'Std' Speed		'–1' Speed		'–2' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		5.0		4.3		3.8	ns
t_{CO}	Sequential Clk to Q		5.0		4.3		3.8	ns
t_{GO}	Latch G to Q		5.0		4.3		3.8	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		5.0		4.3		3.8	ns
Predicted Routing Delays[2]								
t_{RD1}	FO=1 Routing Delay		1.8		1.5		1.4	ns
t_{RD2}	FO=2 Routing Delay		2.3		2.0		1.7	ns
t_{RD3}	FO=3 Routing Delay		3.0		2.6		2.3	ns
t_{RD4}	FO=4 Routing Delay		4.1		3.5		3.1	ns
t_{RD8}	FO=8 Routing Delay		6.3		5.4		4.7	ns
Sequential Timing Characteristics[3, 4]								
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.4		0.4		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	1.0		1.0		1.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	6.5		6.0		4.5		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.5		6.0		4.5		ns
t_A	Flip-Flop Clock Input Period	15.0		12.0		9.8		ns
t_{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Setup	0.4		0.4		0.4		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Setup	0.4		0.4		0.4		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		66.0		80.0		100.0	MHz

Notes:

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the ALS Timer utility.
4. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

A1240A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			'Std' Speed		'–1' Speed		'–2' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Pad to Y High			3.8		3.3		2.9	ns
t_{INYL}	Pad to Y Low			3.5		3.0		2.6	ns
t_{INGH}	G to Y High			6.6		5.7		5.0	ns
t_{INGL}	G to Y Low			6.3		5.4		4.7	ns
Input Module Predicted Routing Delays[1]									
t_{IRD1}	FO=1 Routing Delay			5.6		4.8		4.2	ns
t_{IRD2}	FO=2 Routing Delay			6.4		5.4		4.8	ns
t_{IRD3}	FO=3 Routing Delay			7.2		6.1		5.4	ns
t_{IRD4}	FO=4 Routing Delay			7.9		6.7		5.9	ns
t_{IRD8}	FO=8 Routing Delay			10.5		8.9		7.9	ns
Global Clock Network									
t_{CKH}	Input Low to High	FO = 32 FO = 256		12.8 15.7		11.0 13.0		10.2 11.8	ns
t_{CKL}	Input High to Low	FO = 32 FO = 256		12.8 15.9		11.0 13.2		10.2 12.0	ns
t_{PWH}	Minimum Pulse Width High	FO = 32 FO = 256	5.5 5.8		4.5 5.0		3.8 4.1		ns
t_{PWL}	Minimum Pulse Width Low	FO = 32 FO = 256	5.5 5.8		4.5 5.0		3.8 4.1		ns
t_{CKSW}	Maximum Skew	FO = 32 FO = 256		0.5 2.5		0.5 2.5		0.5 2.5	ns
t_{SUEXT}	Input Latch External Setup	FO = 32 FO = 256	0.0 0.0		0.0 0.0		0.0 0.0		ns
t_{HEXT}	Input Latch External Hold	FO = 32 FO = 256	7.0 11.2		7.0 11.2		7.0 11.2		ns
t_P	Minimum Period	FO = 32 FO = 256	11.1 11.7		9.1 10.0		8.1 8.8		ns
f_{MAX}	Maximum Frequency	FO = 32 FO = 256		90.0 85.0		110.0 100.0		125.0 115.0	MHz

Note:

1. These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1240A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

Output Module Timing		'Std' Speed		'–1' Speed		'–2' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1, 2]								
t_{DLH}	Data to Pad High		10.6		9.0		8.0	ns
t_{DHL}	Data to Pad Low		13.4		11.4		10.1	ns
t_{ENZH}	Enable Pad Z to High		11.8		10.0		8.9	ns
t_{ENZL}	Enable Pad Z to Low		15.5		13.2		11.7	ns
t_{ENHZ}	Enable Pad High to Z		9.4		8.0		7.1	ns
t_{ENLZ}	Enable Pad Low to Z		11.1		9.5		8.4	ns
t_{GLH}	G to Pad High		11.9		10.2		9.0	ns
t_{GHL}	G to Pad Low		14.9		12.7		11.2	ns
d_{TLH}	Delta Low to High		0.09		0.08		0.07	ns/pF
d_{THL}	Delta High to Low		0.16		0.13		0.12	ns/pF
CMOS Output Module Timing[1, 2]								
t_{DLH}	Data to Pad High		13.5		11.5		10.2	ns
t_{DHL}	Data to Pad Low		11.2		9.6		8.4	ns
t_{ENZH}	Enable Pad Z to High		11.8		10.0		8.9	ns
t_{ENZL}	Enable Pad Z to Low		15.5		13.2		11.7	ns
t_{ENHZ}	Enable Pad High to Z		9.4		8.0		7.1	ns
t_{ENLZ}	Enable Pad Low to Z		11.1		9.5		8.4	ns
t_{GLH}	G to Pad High		11.9		10.2		9.0	ns
t_{GHL}	G to Pad Low		14.9		12.7		11.2	ns
d_{TLH}	Delta Low to High		0.16		0.13		0.12	ns/pF
d_{THL}	Delta High to Low		0.12		0.10		0.09	ns/pF

Notes:

1. Delays based on 50 pF loading.
2. Maximum Recommended Simultaneous Switching Outputs:

PLCC	20pF	72
	35pF	45
	50pF	32
PQFP, CPGA	20pF	104
	35pF	68
	50pF	48

A1280A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)

Logic Module Propagation Delays[1]		'Std' Speed		'–1' Speed		'–2' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		5.0		4.3		3.8	ns
t_{CO}	Sequential Clk to Q		5.0		4.3		3.8	ns
t_{GO}	Latch G to Q		5.0		4.3		3.8	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		5.0		4.3		3.8	ns
Predicted Routing Delays[2]								
t_{RD1}	FO=1 Routing Delay		2.3		2.0		1.7	ns
t_{RD2}	FO=2 Routing Delay		3.3		2.8		2.5	ns
t_{RD3}	FO=3 Routing Delay		4.0		3.4		3.0	ns
t_{RD4}	FO=4 Routing Delay		4.9		4.2		3.7	ns
t_{RD8}	FO=8 Routing Delay		8.8		7.5		6.7	ns
Sequential Timing Characteristics[3,4]								
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.4		0.4		0.4		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	1.0		1.0		1.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	7.0		6.0		5.5		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	7.0		6.0		5.5		ns
t_A	Flip-Flop Clock Input Period	18.0		13.3		11.7		ns
t_{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Setup	0.4		0.4		0.4		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Setup	0.4		0.4		0.4		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		50.0		75.0		85.0	MHz

Notes:

1. For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the ALS Timer utility.
4. Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

A1280A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

Input Module Propagation Delays			'Std' Speed		'–1' Speed		'–2' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Pad to Y High			3.8		3.3		2.9	ns
t_{INYL}	Pad to Y Low			3.5		3.0		2.7	ns
t_{INGH}	G to Y High			6.6		5.7		5.0	ns
t_{INGL}	G to Y Low			6.3		5.4		4.8	ns
Input Module Predicted Routing Delays[1]									
t_{IRD1}	FO=1 Routing Delay			6.0		5.1		4.6	ns
t_{IRD2}	FO=2 Routing Delay			6.9		5.9		5.2	ns
t_{IRD3}	FO=3 Routing Delay			7.4		6.3		5.6	ns
t_{IRD4}	FO=4 Routing Delay			8.6		7.3		6.5	ns
t_{IRD8}	FO=8 Routing Delay			12.4		10.5		9.4	ns
Global Clock Network									
t_{CKH}	Input Low to High	FO = 32		12.8		11.0		10.2	ns
		FO = 384		17.2		14.6		13.1	
t_{CKL}	Input High to Low	FO = 32		12.8		11.0		10.2	ns
		FO = 384		17.5		14.9		13.3	
t_{PWH}	Minimum Pulse Width High	FO = 32	6.6		5.5		5.0		ns
		FO = 384	7.6		6.4		5.8		
t_{PWL}	Minimum Pulse Width Low	FO = 32	6.6		5.5		5.0		ns
		FO = 384	7.6		6.4		5.8		
t_{CKSW}	Maximum Skew	FO = 32		0.5		0.5		0.5	ns
		FO = 384		2.5		2.5		2.5	
t_{SUEXT}	Input Latch External Setup	FO = 32	0.0		0.0		0.0		ns
		FO = 384	0.0		0.0		0.0		
t_{HEXT}	Input Latch External Hold	FO = 32	7.0		7.0		7.0		ns
		FO = 384	11.2		11.2		11.2		
t_P	Minimum Period	FO = 32	13.3		11.2		9.6		ns
		FO = 384	15.3		12.6		10.6		
f_{MAX}	Maximum Frequency	FO = 32		75.0		90.0		105.0	MHz
		FO = 384		65.0		80.0		95.0	

Note:

1. These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A1280A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

Output Module Timing		'Std' Speed		'–1' Speed		'–2' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1, 2]								
t_{DLH}	Data to Pad High		10.6		9.0		8.1	ns
t_{DHL}	Data to Pad Low		13.4		11.4		10.2	ns
t_{ENZH}	Enable Pad Z to High		11.8		10.0		9.0	ns
t_{ENZL}	Enable Pad Z to Low		15.5		13.2		11.8	ns
t_{ENHZ}	Enable Pad High to Z		9.4		8.0		7.1	ns
t_{ENLZ}	Enable Pad Low to Z		11.1		9.5		8.4	ns
t_{GLH}	G to Pad High		11.9		10.2		9.0	ns
t_{GHL}	G to Pad Low		14.9		12.7		11.3	ns
d_{TLH}	Delta Low to High		0.09		0.08		0.07	ns/pF
d_{THL}	Delta High to Low		0.16		0.13		0.12	ns/pF
CMOS Output Module Timing[1, 2]								
t_{DLH}	Data to Pad High		13.5		11.5		10.3	ns
t_{DHL}	Data to Pad Low		11.2		9.6		8.5	ns
t_{ENZH}	Enable Pad Z to High		11.8		10.0		9.0	ns
t_{ENZL}	Enable Pad Z to Low		15.5		13.2		11.8	ns
t_{ENHZ}	Enable Pad High to Z		9.4		8.0		7.1	ns
t_{ENLZ}	Enable Pad Low to Z		11.1		9.5		8.4	ns
t_{GLH}	G to Pad High		11.9		10.2		9.0	ns
t_{GHL}	G to Pad Low		14.9		12.7		11.3	ns
d_{TLH}	Delta Low to High		0.16		0.13		0.12	ns/pF
d_{THL}	Delta High to Low		0.12		0.10		0.09	ns/pF

Notes:
1. Delays based on 50 pF loading.
2. Maximum Recommended Simultaneous Switching Outputs:

PQFP, CPGA, CQFP	20pF	160
	35pF	90
	50pF	64

Macro Library

Hard Macros—Combinatorial

Function	Macro	Description	Modules S	Modules C
ACT 2 Combinatorial Logic Module	CM8	Combinational Module (Full ACT 2 Logic Module)		1
ACT 2 Sequential Logic Module	DFM7A	4-input D-Type Flip-Flop with Multiplexed Data, active low Clear, and active high clock	1	
	DFM7B	4-input D-Type Flip-Flop with Multiplexed Data, active low Clear, and clock	1	
Adder	FA1A	1-bit adder, carry in and carry out active low, A-input active low		2
	FA1B	1-bit adder, carry in and carry out active low		2
	FA2A	2-bit adder, carry in and carry out active low, A0 and A1 inputs active low		2
	HA1	Half-Adder		2
	HA1A	Half-Adder with active low A-input		2
	HA1B	Half-Adder with active low carry out and sum		2
	HA1C	Half-Adder with active low carry out		2
AND	AND2	2-input AND		1
	AND2A	2-input AND with active low A-input		1
	AND2B	2-input AND with active low inputs		1
	AND3	3-input AND		1
	AND3A	3-input AND with active low A-input		1
	AND3B	3-input AND with active low A- and B-inputs		1
	AND3C	3-input AND with active low inputs		1
	AND4	4-input AND		1
	AND4A	4-input AND with active low A-input		1
	AND4B	4-input AND with active low A- and B-inputs		1
	AND4C	4-input AND with active low A-, B-, and C-inputs		1
	AND4D	4-input AND with active low inputs		2
	AND5B	5-input AND with active low A- and B-inputs		1
AND-OR	AO1	3-input AND-OR		1
	AO10	5-input AND-OR-AND		1
	AO11	3-input AND-OR		1
	AO1A	3-input AND-OR with active low A-input		1
	AO1B	3-input AND-OR with active low C-input		1
	AO1C	3-input AND-OR with active low A- and C-inputs		1
	AO1D	3-input AND-OR with active low A- and B-inputs		1
	AO1E	3-input AND-OR with active low inputs		1
	AO2	4-input AND-OR		1
	AO2A	4-input AND-OR with active low A-input		1
	AO2B	4-input AND-OR with active low A- and B-inputs		1
	AO2C	4-input AND-OR with active low A- and C-inputs		1
	AO2D	4-input AND-OR with active low A-, B-, and C-inputs		1
	AO2E	4-input AND-OR with active low inputs		1
	AO3	4-input AND-OR		1
	AO3A	4-input AND-OR		1
	AO3B	4-input AND-OR		1
	AO3C	4-input AND-OR		1
	AO4A	4-input AND-OR		1
	AO5A	4-input AND-OR		1
	AO6	2-wide 4-input AND-OR		1
	AO6A	2-wide 4-input AND-OR with active low D-input		1

Hard Macros—Combinatorial (continued)

Function	Macro	Description	Modules S	Modules C
AND-OR	AO7	5-input AND-OR		1
	AO8	5-input AND-OR with active low C- and D-inputs		1
	AO9	5-input AND-OR		1
	AOI1	3-input AND-OR-INVERT		1
	AOI1A	3-input AND-OR-INVERT with active low A-input		1
	AOI1B	3-input AND-OR-INVERT with active low C-input		1
	AOI1C	3-input AND-OR-INVERT with active low A- and B-inputs		1
	AOI1D	3-input AND-OR-INVERT with active low inputs		1
	AOI2A	4-input AND-OR-INVERT with active low A-input		1
	AOI2B	4-input AND-OR-INVERT with active low A- and C-inputs		1
	AOI3A	4-input AND-OR-INVERT with active low inputs		1
	AOI4	2-wide 4-input AND-OR-INVERT		2
	AOI4A	2-wide 4-input AND-OR-INVERT with active low C-input		1
AND-XOR	AX1	3-input AND-XOR with active low A-input		1
	AX1A	3-input AND-XOR-INVERT with active low A-input		2
	AX1B	3-input AND-XOR with active low A- and B-inputs		1
	AX1C	3-input AND-XOR		1
Buffer	BUF	Buffer with active high input and output		1
	BUFA	Buffer with active low input and output		1
Clock Net	CLKINT	Clock Net Interface	0	0
	GAND2	2-input AND Clock Net		1
	GMX4	4-to-1 Multiplexor Clock Net		1
	GNAND2	2-input NAND Clock Net		1
	GNOR2	2-input NOR Clock Net		1
	GOR2	2-input OR Clock Net		1
	GXOR2	2-input Exclusive OR Clock Net		1
Inverter	INV	Inverter with active low output		1
	INVA	Inverter with active low input		1
Majority	MAJ3	3-input complex AND-OR		1
MUX	MX2	2-to-1 Multiplexor		1
	MX2A	2-to-1 Multiplexor with active low A-input		1
	MX2B	2-to-1 Multiplexor with active low B-input		1
MUX	MX2C	2-to-1 Multiplexor with active low output		1
	MX4	4-to-1 Multiplexor		1
	MXC1	Boolean		2
	MXT	Boolean		2
NAND	NAND2	2-input NAND		1
	NAND2A	2-input NAND with active low A-input		1
	NAND2B	2-input NAND with active low inputs		1
	NAND3	3-input NAND		1
	NAND3A	3-input NAND with active low A-input		1
	NAND3B	3-input NAND with active low A- and B-inputs		1
	NAND3C	3-input NAND with active low inputs		1
	NAND4	4-input NAND		2
	NAND4A	4-input NAND with active low A-input		1
	NAND4B	4-input NAND with active low A- and B-inputs		1
	NAND4C	4-input NAND with active low A-, B-, and C-inputs		1
	NAND4D	4-input NAND with active low inputs		1
	NAND5C	5-input NAND with active low A-, B-, and C-inputs		1

Hard Macros—Combinatorial (continued)

Function	Macro	Description	Modules S	Modules C
NOR	NOR2	2-input NOR		1
	NOR2A	2-input NOR with active low A-input		1
	NOR2B	2-input NOR with active low inputs		1
	NOR3	3-input NOR		1
	NOR3A	3-input NOR with active low A-input		1
	NOR3B	3-input NOR with active low A- and B-inputs		1
	NOR3C	3-input NOR with active low inputs		1
	NOR4	4-input NOR		2
	NOR4A	4-input NOR with active low A-input		1
	NOR4B	4-input NOR with active low A- and B-inputs		1
	NOR4C	4-input NOR with active low A-, B-, and C-inputs		1
	NOR4D	4-input NOR with active low inputs		1
	NOR5C	5-input NOR with active low A-, B-, and C-inputs		1
OR	OR2	2-input OR		1
	OR2A	2-input OR with active low A-input		1
	OR2B	2-input OR with active low inputs		1
	OR3	3-input OR		1
	OR3A	3-input OR with active low A-input		1
	OR3B	3-input OR with active low A- and B-inputs		1
	OR3C	3-input OR with active low inputs		1
	OR4	4-input OR		1
	OR4A	4-input OR with active low A-input		1
	OR4B	4-input OR with active low A- and B-input		1
	OR4C	4-input OR with active low A-, B-, and C-inputs		1
	OR4D	4-input OR with active low inputs		2
	OR5B	5-input OR with active low A- and B-inputs		1
OR-AND	OA1	3-input OR-AND		1
	OA1A	3-input OR-AND with active low A-input		1
	OA1B	3-input OR-AND with active low C-input		1
	OA1C	3-input OR-AND with active low A- and C-inputs		1
	OA2	2-wide 4-input OR-AND		1
	OA2A	2 wide 4-input OR-AND with active low A-input		1
	OA3	4-input OR-AND		1
	OA3A	4-input OR-AND with active low C-input		1
	OA3B	4-input OR-AND with active low A- and C-inputs		1
	OA4	4-input OR-AND		1
	OA4A	4-input OR-AND with active low C-input		1
	OA5	4-input complex OR-AND		1
	OAI1	3-input OR-AND-INVERT		1
	OAI2A	4-input OR-AND-INVERT with active low D-input		1
	OAI3	4-input OR-AND-INVERT		1
	OAI3A	4-input OR-AND-INVERT with active low C- and D-inputs		1
XNOR	XNOR	2-input XNOR		1
XNOR-AND	XA1A	3-input XNOR-AND		1
XNOR-OR	XO1A	3-input XNOR-OR		1
XOR	XOR	2-input XOR		1
XOR-AND	XA1	3-input XOR-AND		1
XOR-OR	XO1	3-input XOR-OR		1

Hard Macros—Sequential

Function	Macro	Description	Modules S	Modules C
D-Type	DF1	D-Type Flip-Flop	1	
	DF1A	D-Type Flip-Flop with active low output	1	
	DF1B	D-Type Flip-Flop with active low clock	1	
	DF1C	D-Type Flip-Flop with active low clock and output	1	
	DFC1	D-Type Flip-Flop with active high Clear	1	1
	DFC1A	D-Type Flip-Flop with active high Clear and active low clock	1	1
	DFC1B	D-Type Flip-Flop with active low Clear	1	
	DFC1D	D-Type Flip-Flop with active low Clear and clock	1	
	DFE	D-Type Flip-Flop with active high Enable	1	
	DFE1B	D-Type Flip-Flop with active low Enable	1	
	DFE1C	D-Type Flip-Flop with active low Enable and clock	1	
	DFE3A	D-Type Flip-Flop with Enable and active low Clear	1	
	DFE3B	D-Type Flip-Flop with Enable and active low Clear and clock	1	
	DFE3C	D-Type Flip-Flop with active low Enable and Clear	1	
	DFE3D	D-Type Flip-Flop with active low Enable, Clear, and clock	1	
	DFEA	D-Type Flip-Flop with Enable and active low clock	1	
	DFM	2-input D-Type Flip-Flop with Multiplexed Data	1	
	DFM1B	2-input D-Type Flip-Flop with Multiplexed Data and active low output	1	
	DFM1C	2-input D-Type Flip-Flop with Multiplexed Data and active low clock and output	1	
	DFM3	2-input D-Type Flip-Flop with Multiplexed Data and Clear	1	1
	DFM3B	2-input D-Type Flip-Flop with Multiplexed Data and active low Clear and clock	1	
	DFM3E	2-input D-Type Flip-Flop with Multiplexed Data, Clear, and active low clock	1	1
	DFM4C	2-input D-Type Flip-Flop with Multiplexed Data and active low Preset and output	1	
	DFM4D	2-input D-Type Flip-Flop with Multiplexed Data and active low Preset, clock, and output	1	
	DFM6A	4-input D-Type Flip-Flop with Multiplexed Data, active low Clear, and active high clock	1	
	DFM6B	4-input D-Type Flip-Flop with Multiplexed Data, active low Clear, and clock	1	
	DFMA	2-input D-Type Flip-Flop with Multiplexed Data and active low clock	1	
	DFMB	2-input D-Type Flip-Flop with Multiplexed Data and active low Clear	1	
	DFME1A	2-input D-Type Flip-Flop with Multiplexed Data and active low Enable	1	
	DFP1	D-Type Flip-Flop with active high Preset		2
	DFP1A	D-Type Flip-Flop with active high Preset and active low clock		2
	DFP1B	D-Type Flip-Flop with active low Preset		2
	DFP1C	D-Type Flip-Flop with active high Preset and active low output	1	1
	DFP1D	D-Type Flip-Flop with active low Preset and clock		2
	DFP1E	D-Type Flip-Flop with active low Preset and output	1	
	DFP1F	D-Type Flip-Flop with active high Preset and active low clock and output	1	1
	DFP1G	D-Type Flip-Flop with active low Preset, clock, and output	1	
	DFPC	D-Type Flip-Flop with active high Preset, active low Clear, and active high clock		2
	DFPCA	D-Type Flip-Flop with active high Preset and active low Clear and clock		2
J-K Type	JKF	JK Flip-Flop with active low K-input	1	
	JKF1B	JK Flip-Flop with active low clock and K-input	1	
	JKF2A	JK Flip-Flop with active low Clear and K-input	1	

Hard Macros—Sequential (continued)

Function	Macro	Description	Modules S	Modules C
J-K Type	JKF2B	JK Flip-Flop with active low Clear, clock, and K-input	1	
	JKF2C	JK Flip-Flop with active high Clear and active low K-input	1	1
	JKF2D	JK Flip-Flop with active high Clear and active low clock and K-input	1	1
T-Type	TF1A	T-Type Flip-Flop with active low Clear	1	
	TF1B	T-Type Flip-Flop with active low Clear and clock	1	
Latch	DL1	Data Latch	1	
	DL1A	Data Latch with active low output	1	
	DL1B	Data Latch with active low clock	1	
	DL1C	Data Latch with active low clock and output	1	
	DLC	Data Latch with active low Clear	1	
	DLC1	Data Latch with active high Clear		1
	DLC1A	Data Latch with active high Clear and active low clock		1
	DLC1F	Data Latch with active high Clear and active low output		1
	DLC1G	Data Latch with active high Clear and active low clock and output		1
	DLCA	Data Latch with active low Clock and Clear	1	
	DLE	Data Latch with active high Enable	1	
	DLE1D	Data Latch with active high Enable and clock and active low input and output	1	
	DLE2B	Data Latch with active low Enable, Clear, and clock	1	
	DLE2C	Data Latch with active low Enable and clock and active high Clear		1
	DLE3B	Data Latch with active low Enable and clock and active low Preset		1
	DLE3C	Data Latch with active low Enable, Preset, and clock		1
	DLEA	Data Latch with active low Enable and active high clock	1	
	DLEB	Data Latch with active high Enable and active high clock	1	
	DLEC	Data Latch with active low Enable and clock	1	
	DLM	2-input Data Latch with Multiplexed Data	1	
	DLM3	4-input Data Latch with Multiplexed Data	1	
	DLM3A	4-input Data Latch with Multiplexed Data and active low clock	1	
	DLM4	Data Latch with Multiplexed Data	1	
	DLM4A	Data Latch with Multiplexed Data	1	
	DLMA	2-input Data Latch with Multiplexed Data and active low clock	1	
	DLME1A	2-input Data Latch with Multiplexed Data and Enable and active low clock	1	
	DLP1	Data Latch with active high Preset and clock		1
	DLP1A	Data Latch with active high Preset and active low clock		1
	DLP1B	Data Latch with active low Preset and active high clock		1
	DLP1C	Data Latch with active low Preset and clock		1
	DLP1D	Data Latch with active low Preset and output and active high clock	1	
	DLP1E	Data Latch with active low Preset, clock, and output	1	

Input/Output Macros

Function	Macro	Description	I/O Modules
Buffer	IBDL	Input Buffer with Latch Clock	1
	INBUF	Input Buffer	1
	OBHS	Output Buffer, High Slew	1
	OUTBUF	Output Buffer, High Slew	1
Bidirectional	BBHS	Bidirectional Buffer, High Slew	1
	BBDLHS	Bidirectional with Input Latch and Output Latch	1
	BIBUF	Bidirectional Buffer, High Slew (with hidden buffer at Y pin)	1
	CLKBIBUF	Bidirectional with Input Dedicated to Clock Network	1
Input	CLKBUF	Input for Dedicated Routed Clock Network	1
Output	DBDLKS	Output Buffer with Latch	1
	OBHS	Output Buffer	1
	TBHS	Tristate output, High Slew	1
	TRIBUFF	Tristate output, High Slew	1

Actel

Soft Macros

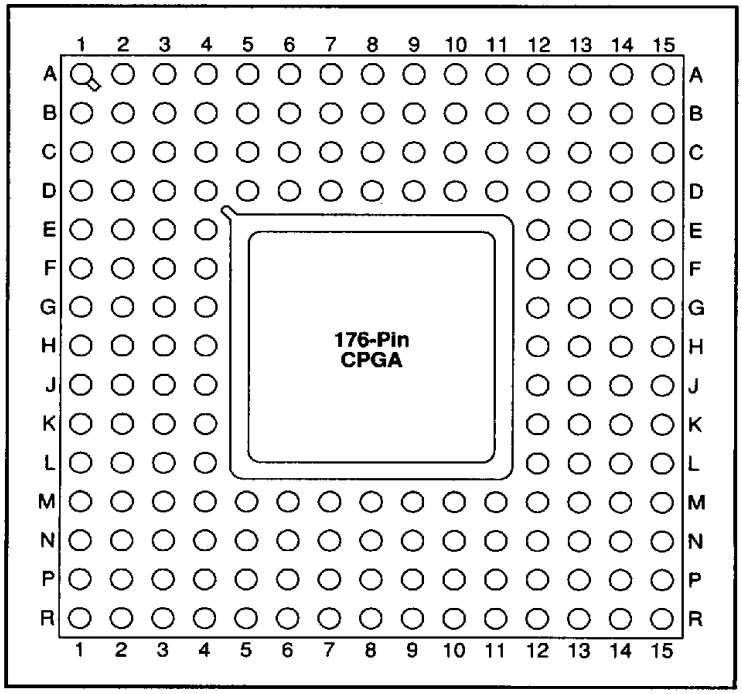
Function	Macro	Description	Maximum Logic Levels	Modules S	Modules C
Adder	FADD10	10-bit adder	3		56
	FADD12	12-bit adder	4		9
	FADD16	16-bit adder	5		97
	FADD8	8-bit adder	4		44
	FADD9	9-bit adder with active low carry out	3		49
	VAD16C	Very fast 16-bit adder, no Carry in	3		91
	VADC16C	Very fast 16-bit adder with Carry in	3		97
Comparator	ICMP4	4-bit Identity Comparator	2		5
	ICMP8	8-bit Identity Comparator	3		9
	MCMPC2	2-bit Magnitude Comparator with Enable	3		9
	MCMPC4	4-bit Magnitude Comparator with Enable	4		18
	MCMPC8	8-bit Magnitude Comparator with Enable	6		36
Counter	CNT4A	4-bit binary counter with load and clear	4	4	8
	CNT4B	4-bit binary counter with load, clear, carry-in, carry-out	4	4	7
	FCTD16C	Fast 16-bit Down Counter, parallel loadable	2	19	33
	FCTD8A	Fast 8-bit Down Counter, parallel loadable	1	10	18
	FCTD8B	Fast 8-bit Down Counter, parallel loadable	1	9	13
	FCTU16C	Fast 16-bit Up Counter, parallel loadable	2	19	31
	FCTU8A	Fast 8-bit Up Counter, parallel loadable	1	10	17
	FCTU8B	Fast 8-bit Up Counter, parallel loadable	1	9	12
	UDCNT4A	4-bit up/down counter with load, carry-in, and carry-out	5	4	13
	VCTD16C	Very fast 16-bit down counter, delay after load, registered control inputs	1	34	41
	VCTD2CP	2-bit down counter, prescaler, delay after load, used to build VCTD counters	1	5	2
	VCTD2CU	2-bit down counter, upper bits, delay after load, used to build VCTD counters	1	2	3
	VCTD4CL	4-bit down counter, lower bits, delay after load, used to build VCTD counters	1	4	7
	VCTD4CM	4-bit down counter, middle bits, delay after load, used to build VCTD counters	1	4	8
Decoder	DEC2X4	2-to-4 decoder	1		4
	DEC2X4A	2-to-4 decoder with active low outputs	1		4
	DEC3X8	3-to-8 decoder	1		8
	DEC3X8A	3-to-8 decoder with active low outputs	1		8
	DEC4X16A	4-to-16 decoder with active low outputs	2		20
	DECE2X4	2-to-4 decoder with enable	1		4
	DECE2X4A	2-to-4 decoder with enable and active low outputs	1		4
	DECE3X8	3-to-8 decoder with enable	2		11
	DECE3X8A	3-to-8 decoder with enable and active low outputs	2		11
Latch	DLC8A	Octal latch with clear active low 8-bit Data Latch with active low Clear	1	8	
	DLE8	Octal latch with enable 8-bit Data Latch with active high Enable	1	8	
	DLM8	Octal latch with multiplexed data 8-bit Data Latch with Multiplexed Data	1	8	
MUX	MX16	16-to-1 Multiplexor	2		5
	MX8	8-to-1 Multiplexor with active high output	2		3
	MX8A	8-to-1 Multiplexor with active low output	2		3
Multiplier	SMULT8	8-bit by 8-bit Multiplier			242
Shift Register	SREG4A	4-bit shift register with clear active low	1	4	
	SREG8A	8-bit shift register with clear active low	1	8	

Soft Macros—TTL Equivalent

Function	Macro	Description	Maximum Logic Levels	Modules S	Modules C
	TA00	2-input NAND	1		1
	TA02	2-input NOR	1		1
	TA04	Inverter	1		1
	TA07	Buffer	1		1
	TA08	2-input AND	1		1
	TA10	3-input NAND	1		1
	TA11	3-input AND	1		1
	TA138	3-to-8 decoder with enable and active low outputs	2		12
	TA139	2-to-4 decoder with active low enable and outputs	1		4
	TA150	16-to-1 multiplexor with active low enable	3		6
	TA151	8-to-1 multiplexor with enable and both active low and active high output	3		5
	TA153	4-to-1 multiplexor with active low enable	2		2
	TA154	4-to-16 decoder with active low outputs and select lines	2		22
	TA157	2-to-1 multiplexor with active low enable	1		1
	TA160	4-bit decade counter with active low clear and load	4	4	8
	TA161	4-bit binary counter with active low clear and load	3	4	6
	TA164	8-bit serial in, parallel out shift register, active low clear	1	8	
	TA169	4-bit Up/Down Counter	6	4	14
	TA174	hex D-type flip-flop with active low clear	1	6	
	TA175	quadruple D-type flip-flop with active low clear	1	4	
	TA181	ALU			37
	TA190	4-bit up/down decode counter with up/down mode	7	4	31
	TA191	4-bit up/down binary counter with up/down mode	7	4	30
	TA194	4-bit bidirectional universal shift register	1	4	4
	TA195	4-bit parallel-access shift register	1	4	1
	TA20	4-input NAND	1		2
	TA21	4-input AND	1		1
	TA269	8-bit up/down binary counter	8	8	28
	TA27	3-input NOR	1		1
	TA273	octal register with clear	1	8	
	TA280	9-bit odd/even parity generator and checker	4		9
	TA32	2-input OR	1		1
	TA377	octal register with active low enable	1	8	
	TA40	4-input NAND	1		2
	TA42	4 to 10 decoder	1		10
	TA51	AND-OR-Invert	1		2
	TA54	4-wide 2-input AND-OR-Invert	2		5
	TA55	2-wide 4-input AND-OR-Invert	2		3
	TA688	8-bit identity comparator	3		9
	TA86	2-input exclusive OR	1		1

Package Pin Assignments

176-Pin CPGA (Top View)



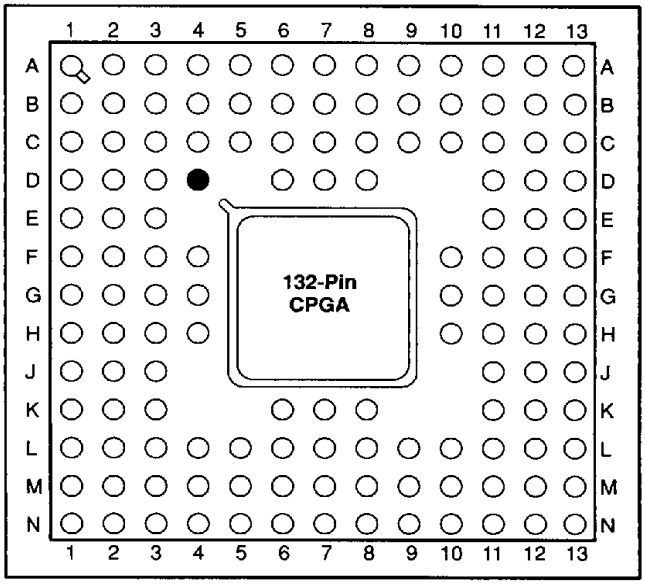
Signal	Pad Number	Location
PRA or I/O	152	C9
PRB or I/O	160	D7
MODE	2	C3
SDI or I/O	135	B14
DCLK or I/O	175	B3
CLKA or I/O	154	A9
CLKB or I/O	158	B8
GND	1, 8, 18, 23, 33, 38, 45, 57, 67, 77, 89 101, 106, 111, 121, 126, 133, 145, 156, 165	D4, E4, G4, H4, K4, L4, M4, M6, M8, M10, M12 K12, J12, H12, F12, E12, D12, D10, C8, D6
V_{CC}	13, 24, 28, 52, 68, 82, 112, 116, 140, 155, 170	F4, H3, J4, M5, N8, M11, H13, G12, D11, D8, D5
V_{PP}	110	J14
V_{SV}	25, 113	H2, H14
V_{KS}	109	J13

Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE = GND, except during device programming or debugging.
4. $V_{PP} = V_{CC}$, except during device programming.
5. $V_{SV} = V_{CC}$, except during device programming.
6. V_{KS} = GND, except during device programming.

Package Pin Assignments (continued)

132-Pin CPGA (Top View)

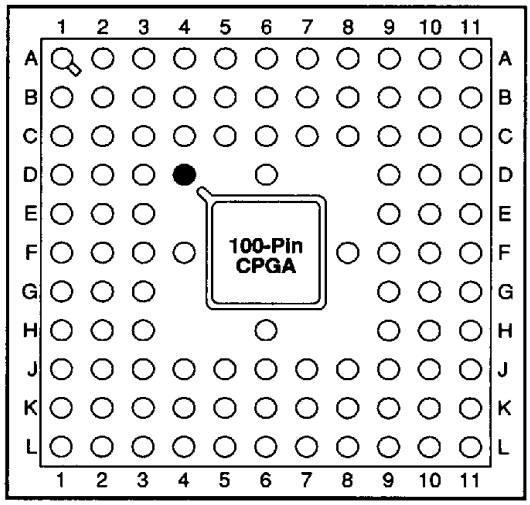


Signal	Pad Number	Location
PRA or I/O	113	B8
PRB or I/O	121	C6
MODE	2	A1
SDI or I/O	101	B12
DCLK or I/O	132	C3
CLKA or I/O	115	B7
CLKB or I/O	119	B6
GND	9, 10, 26, 27, 41, 58, 59, 73, 74, 92, 93, 107, 108, 125, 126	E3, F4, J2, J3, L5, L9, M9, K12, J11, E12, E11, C9, B9, B5, C5
V_{CC}	18, 19, 49, 50, 83, 84, 116, 117	G3, G2, L7, K7, G10, G11, D7, C7
V_{PP}	82	G13
V_{SV}	17, 85	G4, G12
V_{KS}	81	H13

Notes:
1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE = GND, except during device programming or debugging.
4. $V_{PP} = V_{CC}$, except during device programming.
5. $V_{SV} = V_{CC}$, except during device programming.
6. V_{KS} = GND, except during device programming.

Package Pin Assignments (continued)

100-Pin CPGA (Top View)

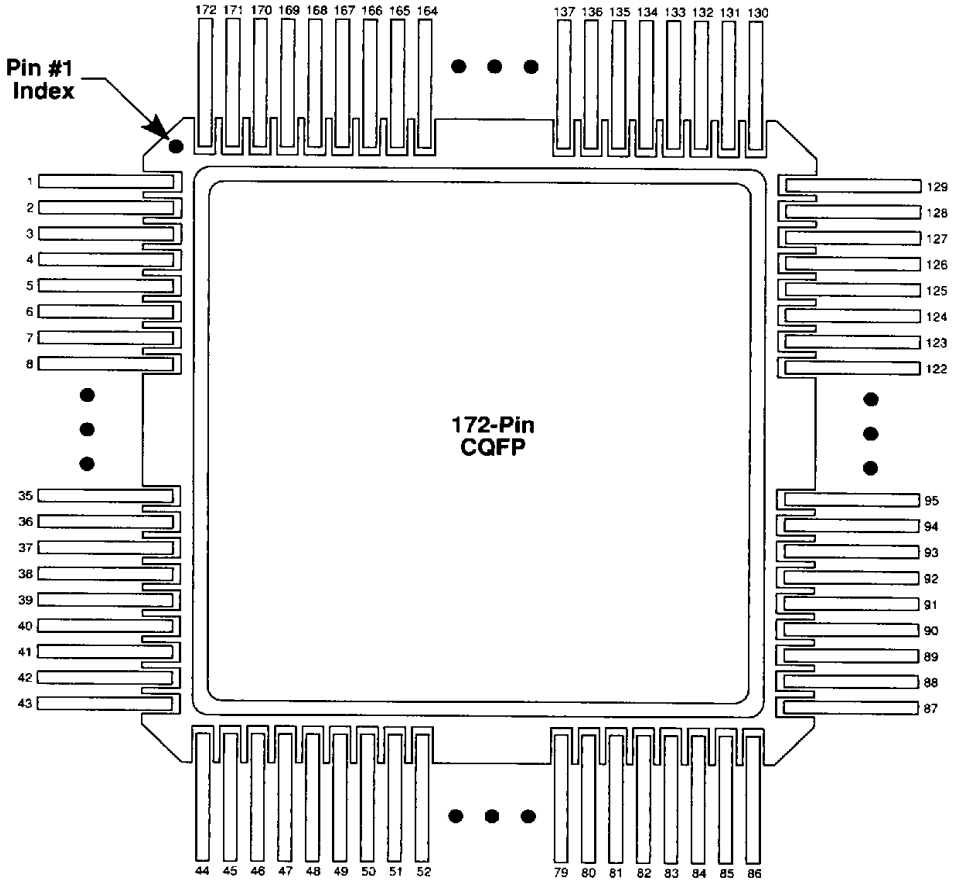


Signal	Pad Number	Location
PRA or I/O	85	A7
PRB or I/O	92	A4
MODE	2	C2
SDI or I/O	77	C8
DCLK or I/O	100	C3
CLKA or I/O	87	C6
CLKB or I/O	90	D6
GND	7, 20, 32, 44, 55, 70, 82, 94	E3, G3, J5, J7, G9, D10, C7, C5
V_{CC}	15, 38, 64, 88	F3, K6, F9, B6
V_{PP}	63	F10
V_{SV}	14, 65	G1, E11
V_{KS}	62	F11

Notes:
1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE = GND, except during device programming or debugging.
4. $V_{PP} = V_{CC}$, except during device programming.
5. $V_{SV} = V_{CC}$, except during device programming.
6. V_{KS} = GND, except during device programming.

Package Pin Assignments (continued)

172-Pin CQFP (Top View)

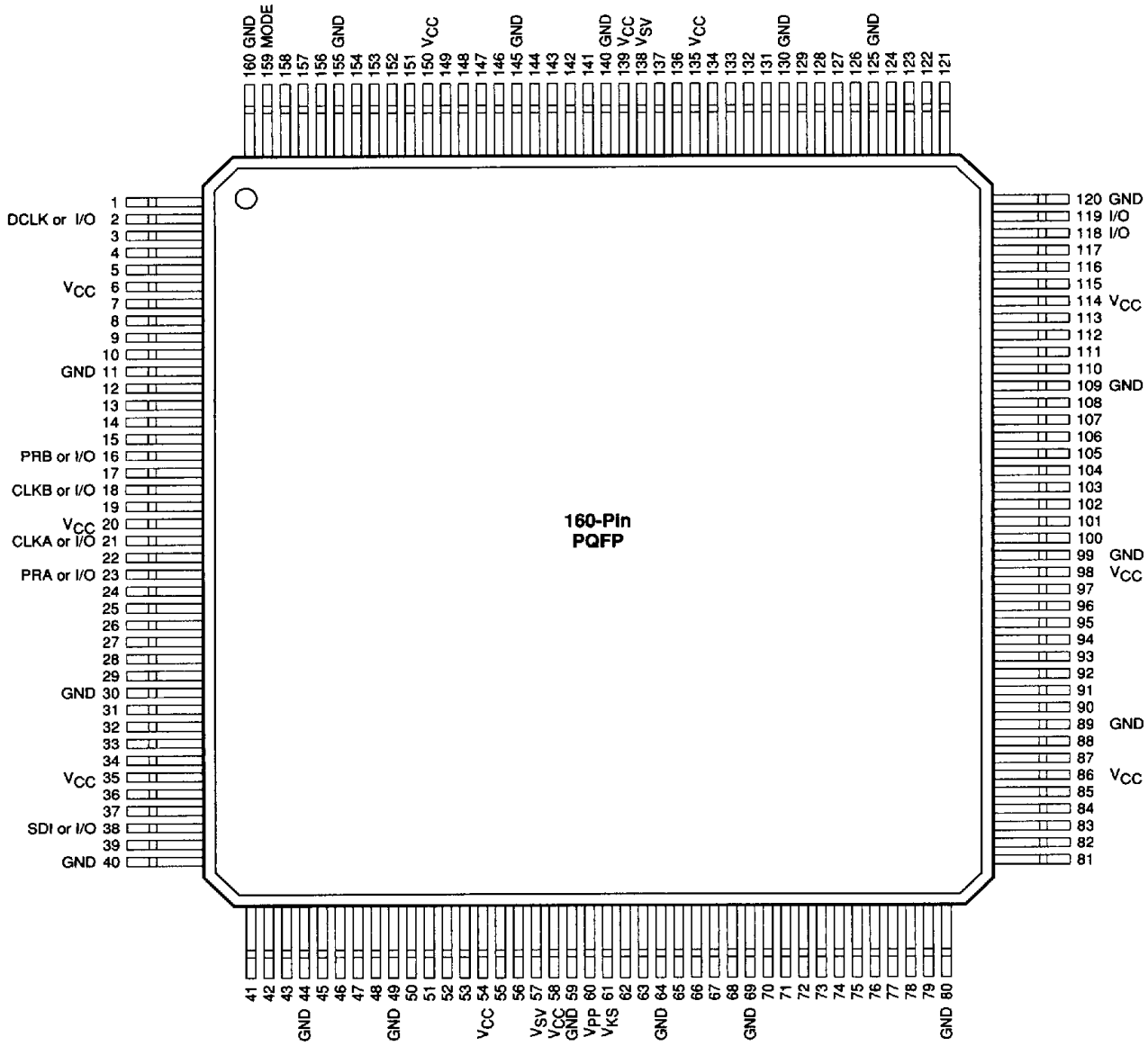


Signal	PIN Number
MODE	1
GND	7, 17, 22, 32, 37, 55, 65, 75, 98, 103, 108, 118, 123, 141, 152, 161
V_{CC}	12, 23, 27, 50, 66, 80, 109, 113, 136, 151, 166
V_{SV}	24, 110
V_{KS}	106
V_{PP}	107
SDI or I/O	131
PRA or I/O	148
PRB or I/O	156
CLKA or I/O	150
CLKB or I/O	154
DCLK or I/O	171

Notes:
1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE = GND, except during device programming or debugging.
4. $V_{PP} = V_{CC}$, except during device programming.
5. $V_{SV} = V_{CC}$, except during device programming.
6. V_{KS} = GND, except during device programming.

Package Pin Assignments (continued)

160-Pin PQFP (Top View)

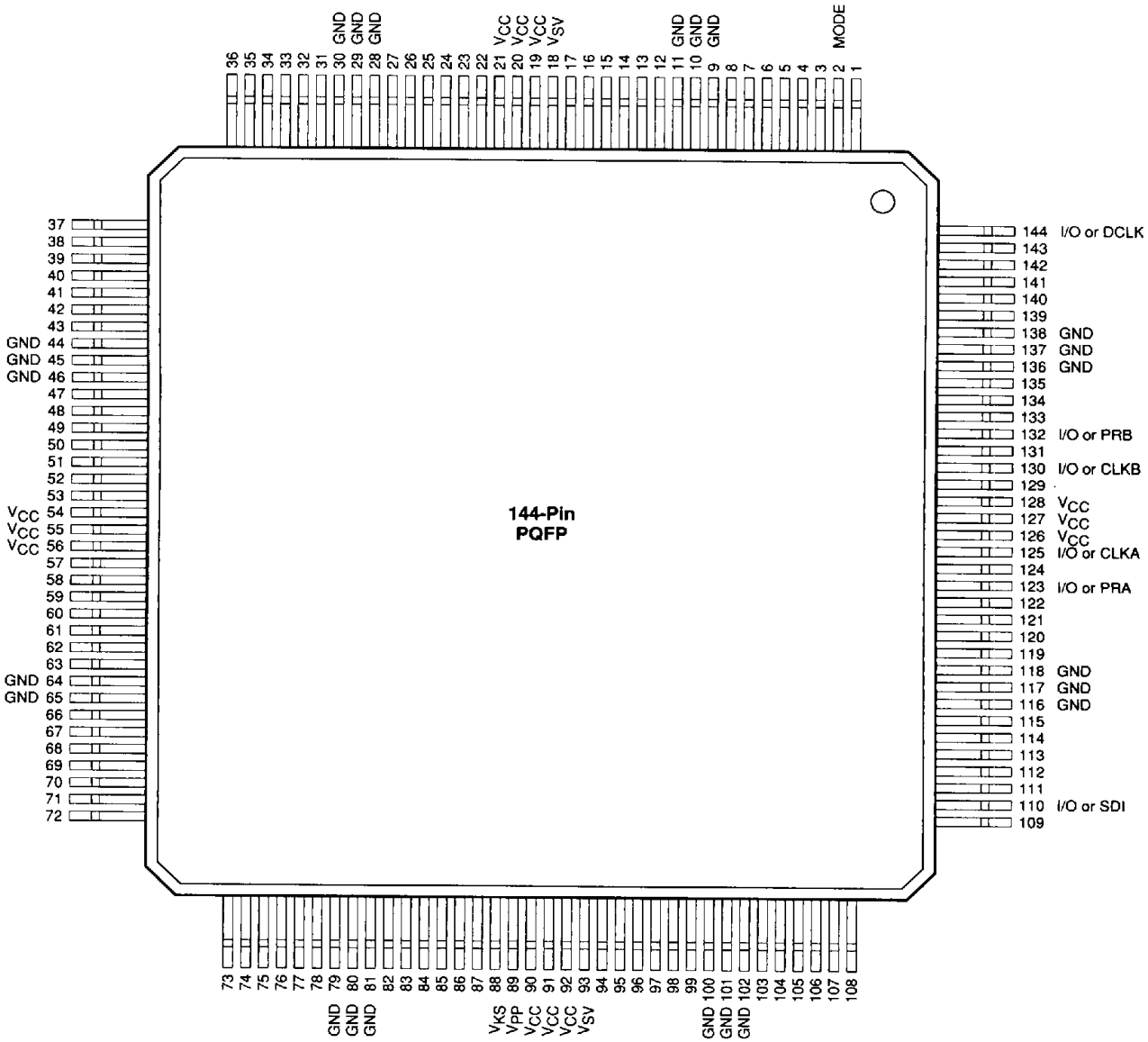


Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE = GND, except during device programming or debugging.
4. $V_{PP} = V_{CC}$, except during device programming.
5. $V_{SV} = V_{CC}$, except during device programming.
6. V_{KS} = GND, except during device programming.

Package Pin Assignments (continued)

144-Pin PQFP (Top View)

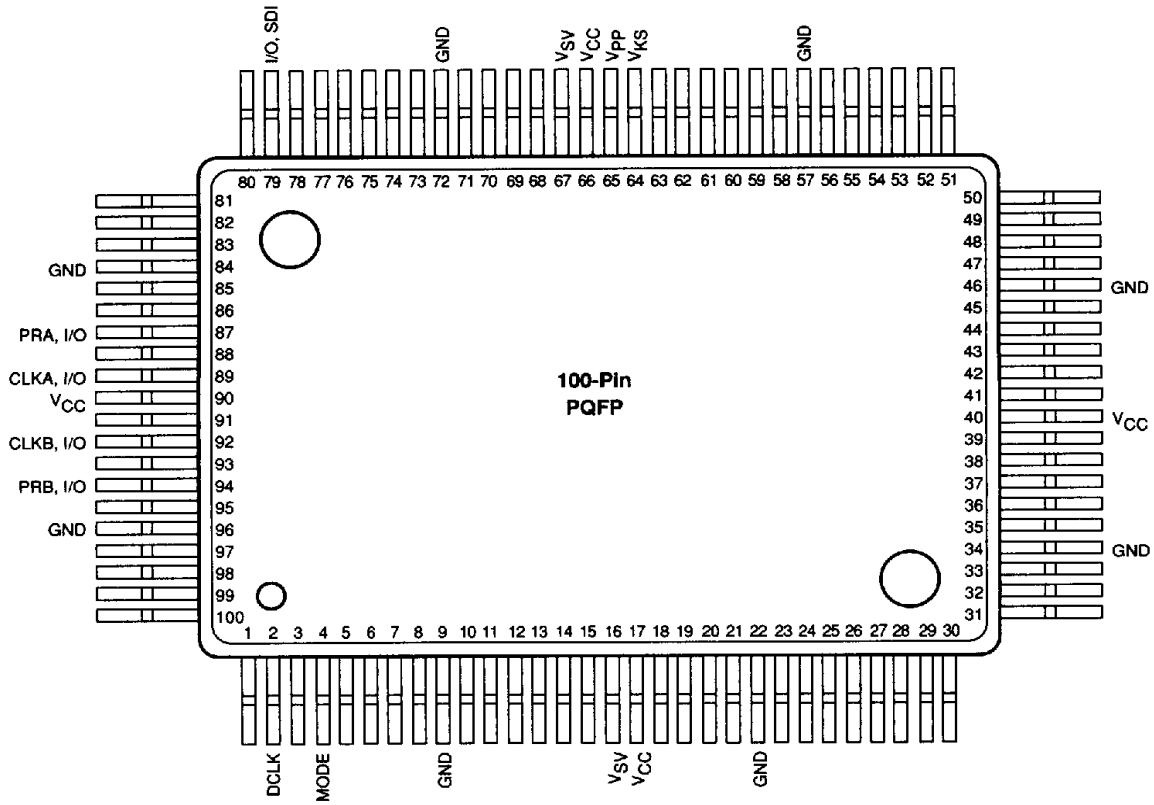


Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE = GND, except during device programming or debugging.
4. $V_{PP} = V_{CC}$, except during device programming.
5. $V_{SV} = V_{CC}$, except during device programming.
6. V_{KS} = GND, except during device programming.

Package Pin Assignments (continued)

100-Pin PQFP (Top View)

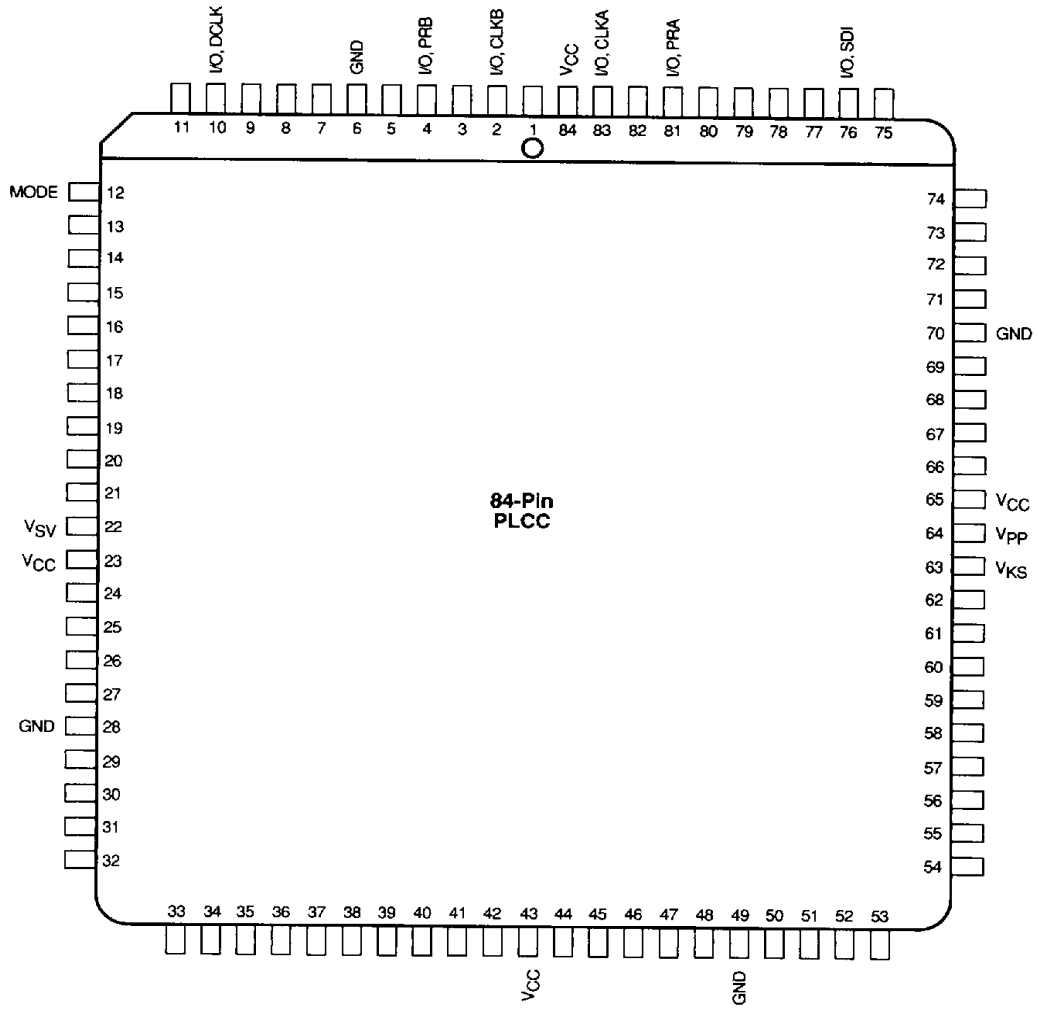


Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE = GND, except during device programming or debugging.
4. $V_{PP} = V_{CC}$, except during device programming.
5. $V_{SV} = V_{CC}$, except during device programming.
6. V_{KS} = GND, except during device programming.

Package Pin Assignments (continued)

84-Pin PLCC (Top View)



Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE = GND, except during device programming or debugging.
4. $V_{PP} = V_{CC}$, except during device programming.
5. $V_{SV} = V_{CC}$, except during device programming.
6. V_{KS} = GND, except during device programming.