NEC

MOS INTEGRATED CIRCUIT
μPD78F0233

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD78F0233 is a member of the μPD780232 Subseries that belongs to the 78K/0 Series. It replaces the internal ROM[Note] of the μPD780232 with a flash memory.

Since the μPD78F0233 can be written/erased electrically while mounted on a board, it is suitable for applications involving system evaluation during system development, small-scale production, and for systems that are expected to be frequently upgraded.

Note The internal ROM capacity varies (refer to **4. DIFFERENCES BETWEEN μPD78F0233 AND MASK ROM VERSION** for details).

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD780232 Subseries User's Manual: U13364E
78K/0 Series User's Manual – Instructions: U12326E

FEATURES

- Pin-compatible with mask ROM versions (except V_{PP} pin)
- Flash memory: 24 KB[Note]
- Internal high-speed RAM: 768 bytes
- Internal buffer RAM: 32 bytes
- VFD display RAM: 112 bytes
- Operable in the same supply voltage as mask ROM version (V_{DD} = 4.5 to 5.5 V)

Note The flash memory capacity can be changed with the internal memory size switching register (IMS).

Remark Refer to **4. DIFFERENCES BETWEEN μPD78F0233 AND MASK ROM VERSION** for the differences between the flash memory version and mask ROM versions.

APPLICATIONS

Monolithic mini components, separated mini components, tuners, cassette decks, CD/MD players, audio amplifiers, etc.

ORDERING INFORMATION

Part Number	Package	Internal ROM
μPD78F0233GC-8BT	80-pin plastic QFP (14 × 14)	Flash memory

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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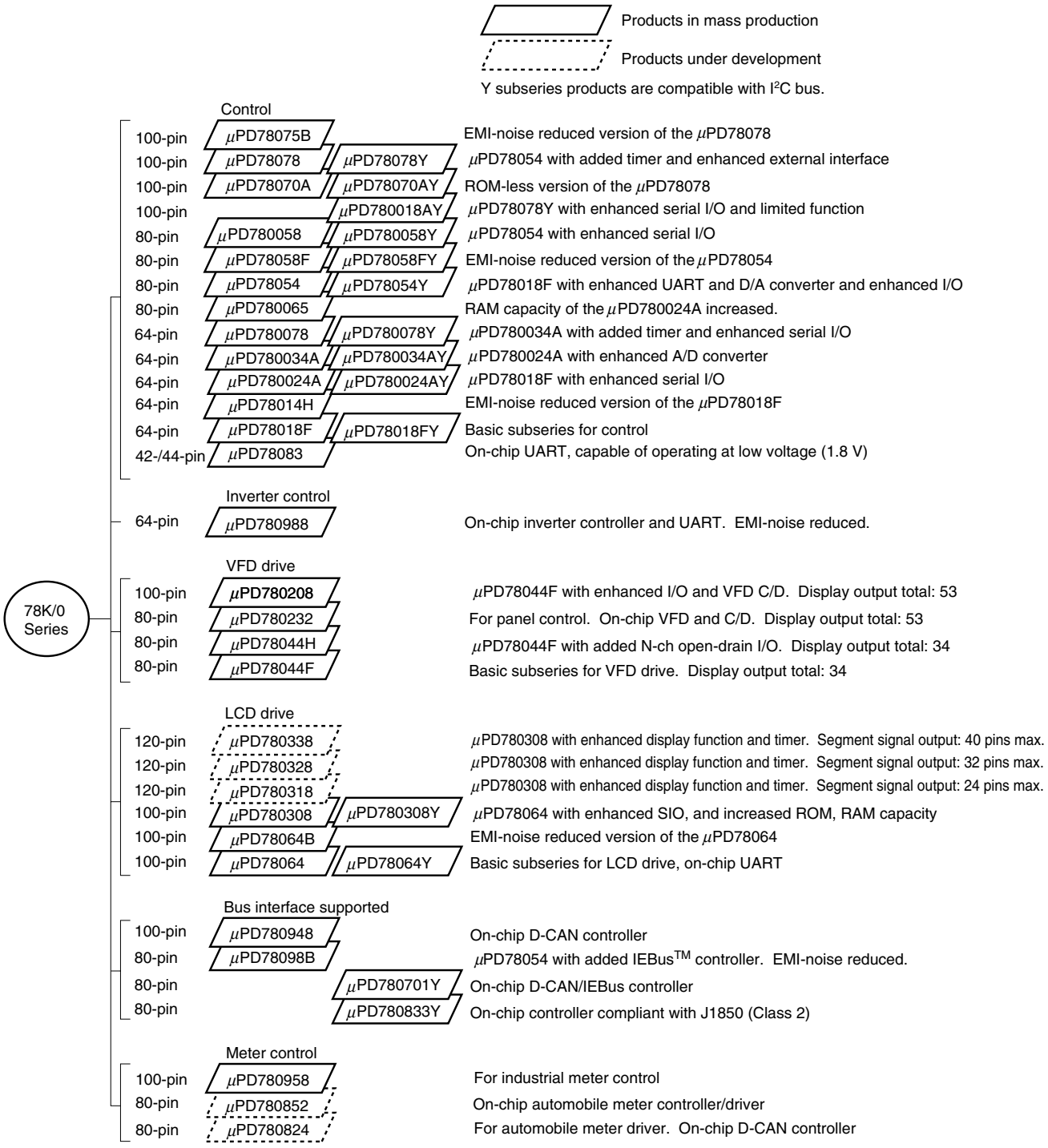
The mark ★ shows major revised points.

★ 78K/0 SERIES LINEUP

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries names.



Remark VFD (Vacuum Fluorescent Display) is referred to as FIP™ (Fluorescent Indicator Panel) in some documents, but the functions of the two are the same.

The major functional differences among the subseries are shown below.

Subseries Name \ Function		ROM Capacity	Timer				8-Bit A/D	10-Bit A/D	8-Bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-Bit	16-Bit	Watch	WDT							
Control	μPD78075B	32 K to 40 K	4 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1 ch)	88	1.8 V	√
	μPD78078	48 K to 60 K											
	μPD78070A	–									61	2.7 V	
	μPD780058	24 K to 60 K	2 ch							3 ch (time-division UART: 1 ch)	68	1.8 V	
	μPD78058F	48 K to 60 K								3 ch (UART: 1 ch)	69	2.7 V	
	μPD78054	16 K to 60 K										2.0 V	
	μPD780065	40 K to 48 K							–	4 ch (UART: 1 ch)	60	2.7 V	
	μPD780078	48 K to 60 K		2 ch			–	8 ch		3 ch (UART: 2 ch)	52	1.8 V	
	μPD780034A	8 K to 32 K		1 ch						3 ch (UART: 1 ch)	51		
	μPD780024A						8 ch	–					
	μPD78014H									2 ch	53		
	μPD78018F	8 K to 60 K											
	μPD78083	8 K to 16 K		–	–					1 ch (UART: 1 ch)	33		–
Inverter control	μPD780988	16 K to 60 K	3 ch	**Note**	–	1 ch	–	8 ch	–	3 ch (UART: 2 ch)	47	4.0 V	√
VFD drive	μPD780208	32 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	2 ch	74	2.7 V	–
	μPD780232	16 K to 24 K	3 ch	–	–		4 ch				40	4.5 V	
	μPD78044H	32 K to 48 K	2 ch	1 ch	1 ch		8 ch			1 ch	68	2.7 V	
	μPD78044F	16 K to 40 K								2 ch			
LCD drive	μPD780338	48 K to 60 K	3 ch	2 ch	1 ch	1 ch	–	10 ch	1 ch	2 ch (UART: 1 ch)	54	1.8 V	–
	μPD780328										62		
	μPD780318										70		
	μPD780308	48 K to 60 K	2 ch	1 ch			8 ch	–	–	3 ch (time-division UART: 1 ch)	57	2.0 V	
	μPD78064B	32 K								2 ch (UART: 1 ch)			
	μPD78064	16 K to 32 K											
Bus interface supported	μPD780948	60 K	2 ch	2 ch	1 ch	1 ch	8 ch	–	–	3 ch (UART: 1 ch)	79	4.0 V	√
	μPD78098B	40 K to 60 K		1 ch					2 ch		69	2.7 V	–
Meter control	μPD780958	48 K to 60 K	4 ch	2 ch	–	1 ch	–	–	–	2 ch (UART: 1 ch)	69	2.2 V	–
Dash board control	μPD780852	32 K to 40 K	3 ch	1 ch	1 ch	1 ch	5 ch	–	–	3 ch (UART: 1 ch)	56	4.0 V	–
	μPD780824	32 K to 60 K								2 ch (UART: 1 ch)	59		

Note 16-bit timer: 2 channels
10-bit timer: 1 channel

OVERVIEW OF FUNCTIONS

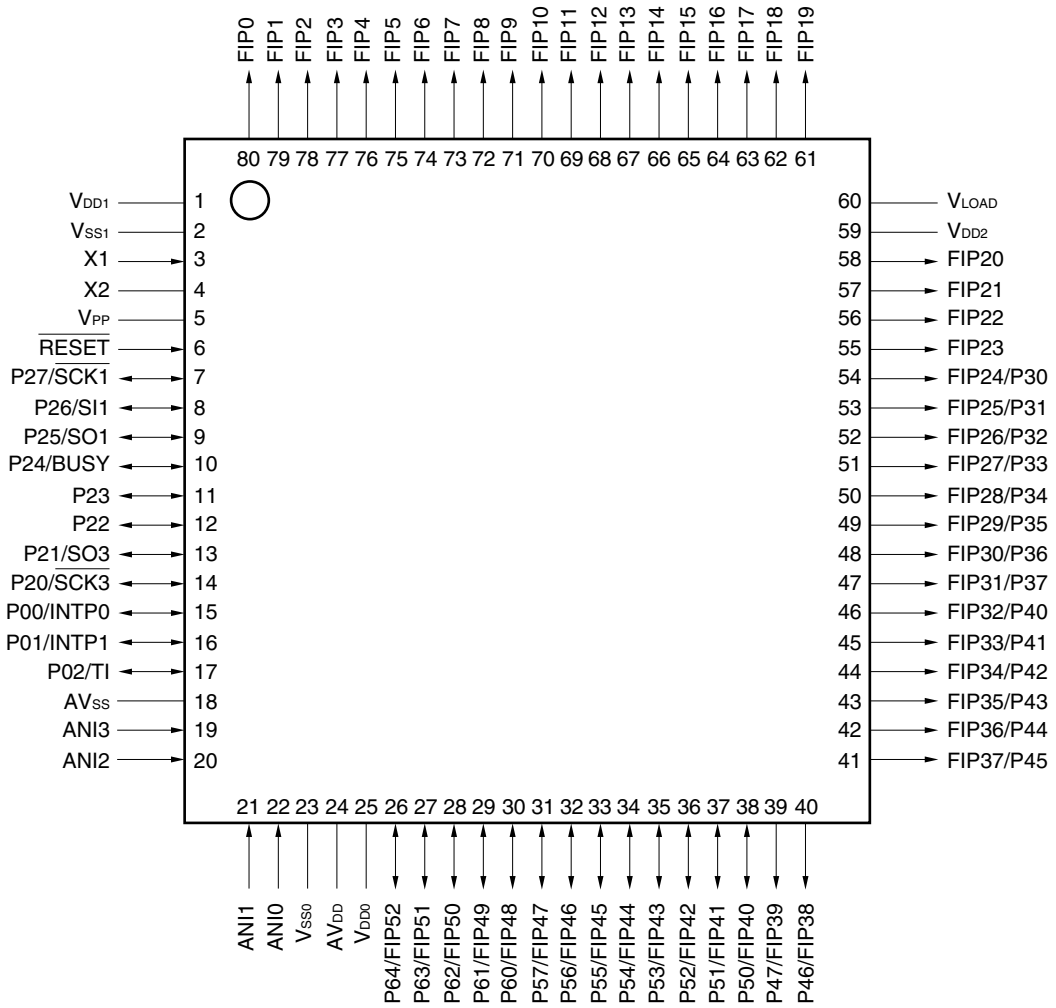
Item		Function
Internal memory	Flash memory	24 KB[Note]
	High-speed RAM	768 bytes
	Buffer RAM	32 bytes
	VFD display RAM	112 bytes
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Minimum instruction execution time		• On-chip minimum instruction execution time variable function • 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (@ 5.0 MHz operation with system clock)
Instruction set		• Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulate (set, reset, test, Boolean operation)
I/O ports (including alternate-function pins for VFD)		Total: 40 • CMOS I/Os: 11 • P-ch open-drain I/Os: 13 • P-ch open-drain outputs: 16
VFD controller/driver		Total of display outputs: 53 • 15 mA display current: 20 • 5 mA display current: 33
A/D converter		• 8-bit resolution × 4 channels • Power supply voltage: AV_{DD} = 4.5 to 5.5 V
Serial interface		• 2-wire serial mode (transmit only): 1 channel • 3-wire serial mode (with automatic transmit/receive function): 1 channel
Timer		• 8-bit remote control timer: 1 channel • 8-bit timer: 2 channels • Watchdog timer: 1 channel
Vectored interrupt sources	Maskable	Internal: 10, external: 2
	Non-maskable	Internal: 1
	Software	1
Power supply voltage		V_{DD} = 4.5 to 5.5 V
Package		80-pin plastic QFP (14 × 14)

Note The flash memory capacity can be changed with the internal memory size switching register (IMS).

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

- **80-pin plastic QFP (14 × 14)**
  μPD78F0233GC-8BT



Cautions 1. Connect directly V_{PP} pin to V_{SS1} in normal operation mode.

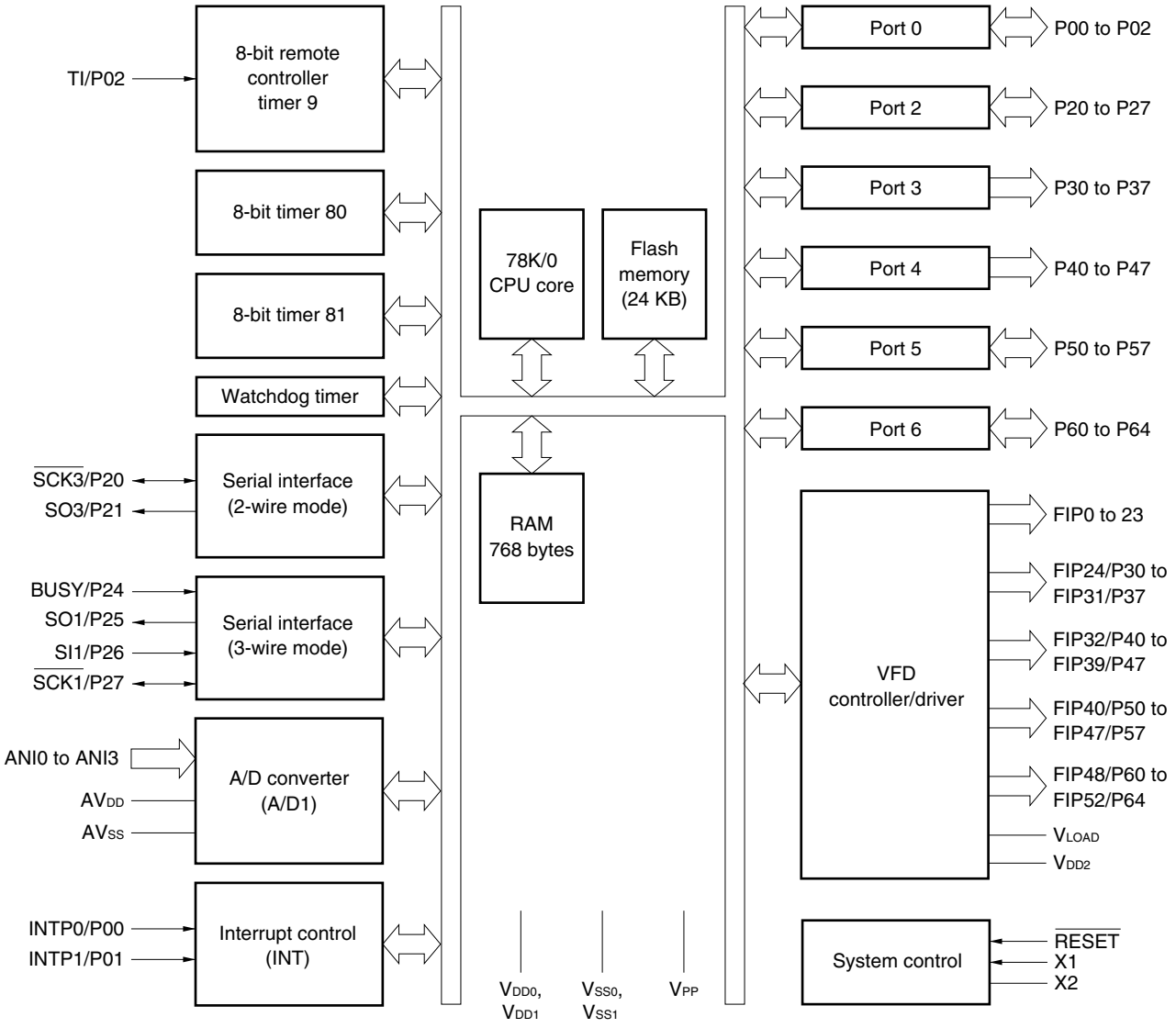
2. Connect AV_{DD} pin to V_{DD1}.

3. Connect AV_{SS} pin to V_{SS1}.

Remark When the μPD78F0233 is used in applications where the noise generated inside the microcontroller needs to be reduced, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

ANI0 to ANI3:	Analog input	P60 to P64:	Port 6
AV_{DD}:	Analog power supply	$\overline{RESET}$:	Reset
AV_{SS}:	Analog ground	$\overline{SCK1}$ and $\overline{SCK3}$:	Serial clock
BUSY:	Busy	SI1:	Serial input
FIP0 to FIP52:	Fluorescent indicator panel	SO1 and SO3:	Serial output
INTP0 and INTP1:	External interrupt input	TI:	Timer input
P00 to P02:	Port 0	V_{DD0} to V_{DD2}:	Power supply
P20 to P27:	Port 2	V_{LOAD}:	Negative power supply
P30 to P37:	Port 3	V_{PP}:	Programming power supply
P40 to P47:	Port 4	V_{SS0} and V_{SS1}:	Ground
P50 to P57:	Port 5	X1 and X2:	Crystal

2. BLOCK DIAGRAM



3. PIN FUNCTION LIST

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 3-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be connected by software.	Input	INTP0
P01				INTP1
P02				TI
P20	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be connected by software.	Input	$\overline{SCK3}$
P21				SO3
P22, P23				—
P24				BUSY
P25				SO1
P26				SI1
P27				$\overline{SCK1}$
P30 to P37	Output	Port 3. 8-bit output-dedicated port.	Output	FIP24 to FIP31
P40 to P47	Output	Port 4. 8-bit output-dedicated port.	Output	FIP32 to FIP39
P50 to P57	I/O	Port 5. 8-bit I/O port. Input/output can be specified in 1-bit units.	Input	FIP40 to FIP47
P60 to P64	I/O	Port 6. 5-bit I/O port. Input/output can be specified in 1-bit units.	Input	FIP48 to FIP52

3.2 Non-Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	Valid edge (rising edge, falling edge, or both rising and falling edges) can be specified. External interrupt request input.	Input	P00
INTP1				P01
TI	Input	8-bit remote control timer 9 (TM9) timer input	Input	P02
$\overline{SCK3}$	I/O	Serial interface serial clock I/O	Input	P20
SO3	Output	Serial interface serial data output	Input	P21
BUSY	Input	Serial interface automatic transmit/receive busy signal output	Input	P24
SO1	Output	Serial interface serial data output	Input	P25
SI1	Input	Serial interface serial data input	Input	P26
$\overline{SCK1}$	I/O	Serial interface serial clock I/O	Input	P27
FIP0 to FIP23	Output	VFD controller/driver high-voltage tolerant large current output. On-chip pull-down resistor	Output	—
FIP24 to FIP31		VFD controller/driver high-voltage tolerant large current output		P30 to P37
FIP32 to FIP39				P40 to P47
FIP40 to FIP47			Input	P50 to P57
FIP48 to FIP52				P60 to P64
V_{LOAD}	—	VFD controller/driver pull-down resistor connection	—	—
$\overline{RESET}$	Input	System reset input	—	—
X1	Input	Crystal connection for system clock oscillation	—	—
X2	—		—	—
ANI0 to ANI3	Input	A/D converter analog input	Input	—
AV_{DD}	—	A/D converter analog power supply/reference voltage input; Keep the same potential with V_{DD1}.	—	—
AV_{SS}	—	A/D converter ground potential; Keep the same potential with V_{SS1}.	—	—
V_{DD0}	—	Positive power supply for ports	—	—
V_{DD1}	—	Positive power supply except for ports, analog, and VFD controller/driver	—	—
V_{DD2}	—	Positive power supply for VFD controller/driver	—	—
V_{SS0}	—	Ground potential for ports	—	—
V_{SS1}	—	Ground potential except for ports and analog	—	—
V_{PP}	—	High-voltage applied during program writing/verifying; Connect directly to V_{SS1} pin in normal operation mode.	—	—

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

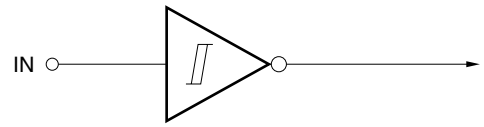
The I/O circuit type of each pin and the recommended connection of unused pins are shown in Table 3-1. For the I/O circuit configuration of each type, see Figure 3-1.

★ **Table 3-1. Types of Pin I/O Circuits**

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/INTP0	8-C	I/O	Input: Independently connect to V_{SS0} via a resistor. Output: Leave open.
P01/INTP1			
P02/TI			
P20/$\overline{SCK3}$	8-C	I/O	Input: Independently connect to V_{DD0} or V_{SS0} via a resistor. Output: Leave open.
P21/SO3			
P22, P23			
P24/BUSY			
P25/SO1			
P26/SI1			
P27/$\overline{SCK1}$			
P30/FIP24 to P37/FIP31	14-E	Output	Leave open.
P40/FIP32 to P47/FIP39			
P50/FIP40 to P57/FIP47	15-E	I/O	Input: Independently connect to V_{DD0} or V_{SS0} via a resistor. Output: Leave open.
P60/FIP48 to P64/FIP52			
FIP0 to FIP23	14-C	Output	Leave open.
$\overline{RESET}$	2	Input	—
ANI0 to ANI3	7	Input	Connect to V_{DD0} or V_{SS0}.
AV_{DD}	—	—	Connect to V_{DD1}.
AV_{SS}			Connect to V_{SS1}.
V_{LOAD}			
V_{PP}			Connect to V_{SS1} directly.

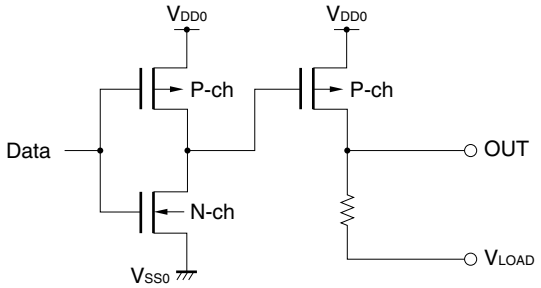
Figure 3-1. Pin I/O Circuits

Type 2

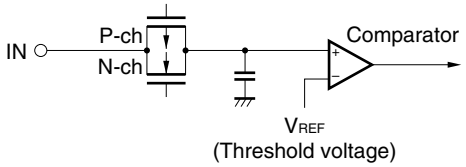


Schmitt trigger input with hysteresis characteristics

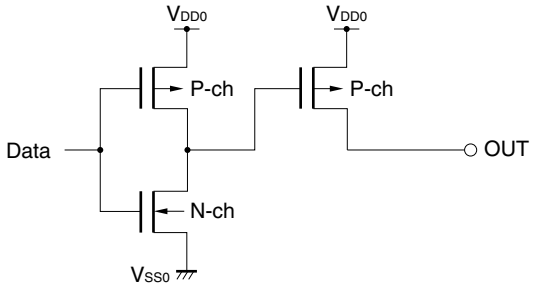
Type 14-C



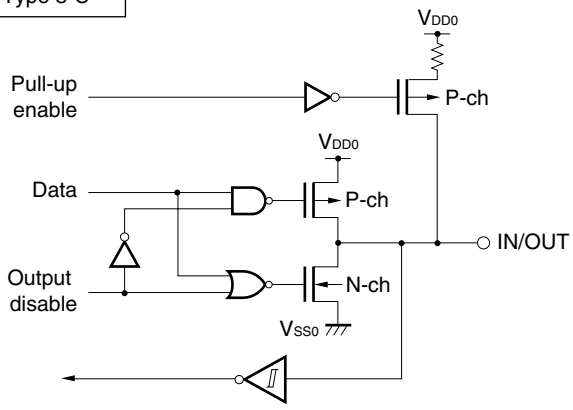
Type 7



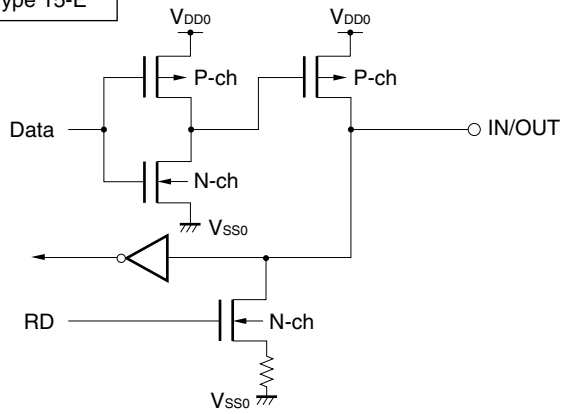
Type 14-E



Type 8-C



Type 15-E



4. DIFFERENCES BETWEEN μPD78F0233 AND MASK ROM VERSION

The μPD78F0233 is a product provided with an internal flash memory that enables on-board electrical writing/erasing/rewriting.

The functions of the μPD78F0233, except those specified for flash memory, can be made the same as those of the mask ROM versions by setting the memory size switching register (IMS).

Table 4-1 shows the differences between the flash memory version (μPD78F0233) and the mask ROM version (μPD780232).

Table 4-1. Differences Between μPD78F0233 and Mask ROM Versions

Item	μPD78F0233	Mask ROM Version
Internal ROM structure	Flash memory	Mask ROM
Internal ROM capacity	24 KB	16 KB
IC pin	Not provided	Provided
V_{PP} pin	Provided	Not provided
Pull-down resistor in FIP0 to FIP23	Provided	Selected by mask option
Pull-down resistor in P30/FIP24 to P37/FIP31, P40/FIP32 to P47/FIP39, P50/FIP40 to P57/FIP47, P60/FIP48 to P64/FIP52	Not provided	
Electrical specifications and recommended soldering conditions	Refer to the data sheets of individual products.	

Caution There are differences in noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass producing it with the mask ROM version, be sure to conduct sufficient evaluations on the commercial samples (CS) (not engineering samples (ES)) of the mask ROM versions.

5. INTERNAL MEMORY SIZE SWITCHING REGISTER (IMS)

IMS is a register that is set by software and is used to specify a part of the internal memory that is not to be used. By setting IMS, the internal memory of the uPD78F0233 can be mapped identically to that of a mask ROM version.

IMS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets IMS to CFH.

Figure 5-1. Format of Internal Memory Size Switching Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	R/W

ROM3	ROM2	ROM1	ROM0	Selection of internal ROM capacity
0	1	0	0	16 KB
0	1	1	0	24 KB
Other than above				Setting prohibited

RAM2	RAM1	RAM0	Selection of internal high-speed RAM capacity
0	0	0	768 bytes
Other than above			Setting prohibited

Caution $\overline{\text{RESET}}$ input set IMS to CFH. After $\overline{\text{RESET}}$ input, always set IMS as follows.

- **μPD78F0233: 06H**
- **When μPD78F0233 is used with the same memory map as the one used in the mask ROM version (μPD780232): 04H**

6. FLASH MEMORY PROGRAMMING

The flash memory of the μPD78F0233 can be written while the microcontroller is mounted on the target system board. Rewriting is possible by using the dedicated flash programmer (Flashpro III (FL-PR3, PG-FP3)) or a program.

When using Flashpro III, connect it to both the host machine and the target system.

In addition, the flash memory can be written on the flash-programming adapter connected to Flashpro III.

Remark FL-PR3 is a product of Naito Densei Machida Mfg. Co., Ltd.

6.1 Selection of Communication Mode

Write operations to the flash memory are performed using Flashpro III in the serial communication mode. Choose a proper communication mode out of the ones listed in Table 6-1 to perform write operations. When selecting the communication mode, use the format illustrated in Figure 6-1. Select the communication mode according to the number of V_{PP} pulses shown in Table 6-1.

Table 6-1. List of Communication Modes

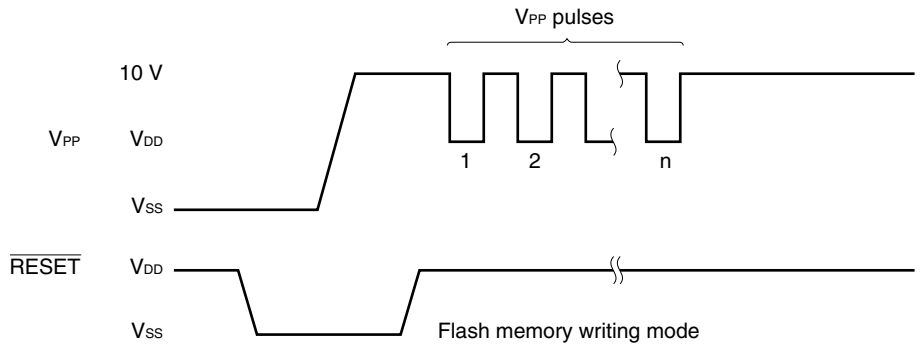
Communication Modes	No. of Channels	Pins[Note 1]	V_{PP} Pulses
3-wire serial I/O	1	$\overline{SCK1}$/P27 SI1/P26 SO1/P25	0
Pseudo 3-wire serial I/O[Note 2]	1	P20/$\overline{SCK3}$ (serial clock I/O) P21/SO3 (serial data output) P22 (serial data input)	12

Notes 1. Shifting to the flash memory programming mode sets all pins not used for flash memory programming to the same state as immediately after reset. Therefore, all ports enter an output high-impedance state. If the external device does not acknowledge an output high-impedance state, handling such as connecting to V_{DD0} via a resistor or connecting to V_{SS0} via a resistor is required.

2. Performs serial transmission by controlling ports with software.

Caution Be sure to select the communication mode according to the number of V_{PP} pulses shown in Table 6-1.

Figure 6-1. Format of Communication Mode Selection



6.2 Flash Memory Programming Functions

Operations such as writing to the flash memory are performed by various commands/data transmission and reception operations according to the selected communication mode. Table 6-2 describes the main flash memory programming functions.

Table 6-2. Main Flash Memory Programming Functions

Function	Description
Reset	Used in cancellation of writing and transmission synchronization detection.
Batch verify	Compares the contents of the entire memory and the input data.
Batch erase	Erases the contents of the entire memory.
Batch blank check	Checks that the entire memory has been deleted.
High-speed writing	Writes to the flash memory based on writing-starting address and the number of writing data (bytes)
Continuous writing	Writes continuously based on information input at high-speed writing.
Status	Used to check the current operation mode and the end of operation.
Oscillation frequency setting	Inputs information of frequency of resonator.
Erase time setting	Inputs the time-length to erase the contents of the memory.
Silicon signature reading	Outputs the device name, memory capacity, and information of device block.

6.3 Connection to Flashpro III

The connection of the Flashpro III and the μPD78F0233 differs according to the communication mode. The connection for each communication mode is shown in Figure 6-2 and 6-3.

Figure 6-2. Connection to Flashpro III in 3-Wire Serial I/O Mode

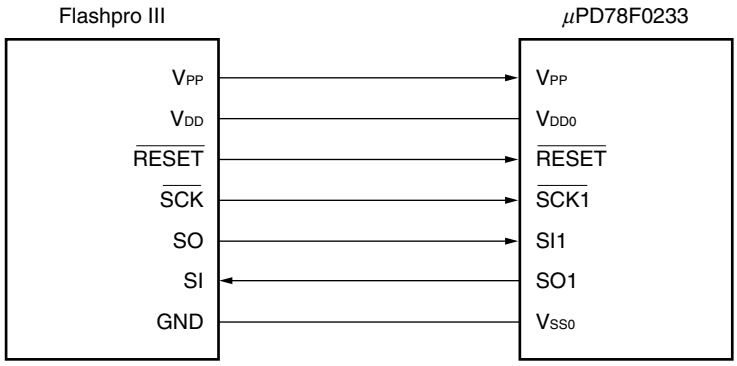
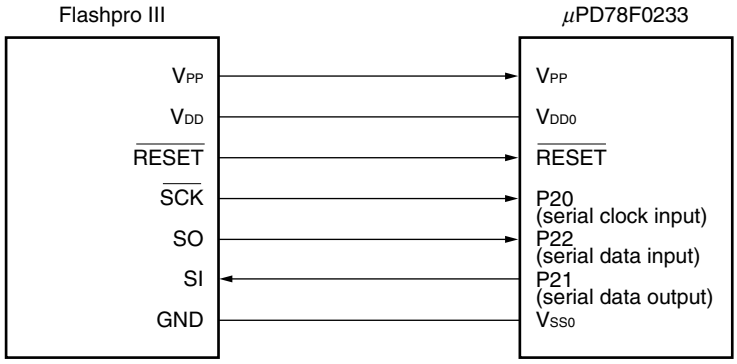


Figure 6-3. Connection to Flashpro III in Pseudo 3-Wire Serial I/O Mode



★ 7. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

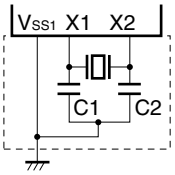
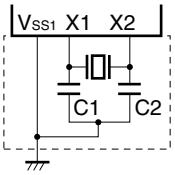
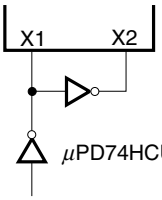
Parameter	Symbol	Conditions		Rating	Unit
Supply voltage	V_{DD}			–0.3 to +6.5	V
	V_{PP}			–0.3 to +10.5	V
	V_{LOAD}			V_{DD} – 45 to V_{DD} + 0.3	V
	AV_{DD}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P02, P20 to P27, X1, X2, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P50 to P57, P60 to P64	P-ch open drain	V_{DD} – 45 to V_{DD} + 0.3	V
Output voltage	V_{O1}			–0.3 to V_{DD} + 0.3	V
	V_{O2}			V_{DD} – 45 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	ANI0 to ANI3	Analog input pins	AV_{SS} to AV_{DD}	V
Output current, high	I_{OH}	1 pin among P00 to P02 and P20 to P27		–10	mA
		Total of P00 to P02 and P20 to P27		–30	mA
		1 pin among FIP0 to FIP23, P30 to P37, P40 to P47, P50 to P57, and P60 to P64		–30	mA
		Total of FIP0 to FIP23, P30 to P37, P40 to P47, P50 to P57, and P60 to P64	Peak value	–300	mA
			rms	–120	mA
Output current, low	I_{OL}**Note**	1 pin among P00 to P02 and P20 to P27	Peak value	10	mA
			rms	5	mA
		Total of P00 to P02 and P20 to P27	Peak value	20	mA
			rms	10	mA
Total loss	P_T	T_A = –40 to +60°C		700	mW
		T_A = –60 to +85°C		500	mW
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–40 to +125	°C

Note The rms value should be calculated as follows: [rms value] = [peak value] × $\sqrt{\text{Duty}}$

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)**Note 1**	V_{DD} = Oscillation voltage range	1		5	MHz
		Oscillation stabilization time**Note 2**	After V_{DD} reaches the minimum value of oscillation voltage range			4	ms
Crystal resonator		Oscillation frequency (f_X)**Note 1**		1		5	MHz
		Oscillation stabilization time**Note 2**				10	ms
External clock		X1 input frequency (f_X)**Note 1**		1		5	MHz
		X1 input high-/low-level width (t_{XH}/t_{XL})		85		450	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release.

Caution When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

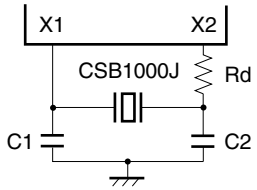
- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Recommended Oscillator Constant

System clock: Ceramic resonator (T_A = –40 to +85°C)

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant		Oscillation Voltage Range		Remark
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)	
Murata Mfg. Co., Ltd.	CSB1000J[Note]	1.00	100	100	4.5	5.5	Rd = 2.2 kΩ
	CSA2.00MG040	2.00	100	100			
	CST2.00MG040		On-chip	On-chip			
	CSA3.58MG	3.58	30	30			
	CST3.58MGW		On-chip	On-chip			
	CSA4.19MG	4.19	30	30			
	CST4.19MGW		On-chip	On-chip			
	CSA5.00MG	5.00	30	30			
	CST5.00MGW		On-chip	On-chip			

Note When using the CSB1000J (1.0 MHz) of Murata Mfg. Co., Ltd. as a ceramic resonator, a limiting resistor (Rd = 2.2 kΩ) is necessary (refer to the figure below). A limiting resistor is not necessary when another recommended resonator is used.



Caution The oscillator constant and oscillation voltage range indicate conditions of stable oscillation. Oscillation frequency precision is not guaranteed. For applications requiring oscillation frequency precision, the oscillation frequency must be adjusted on the implementation circuit. For details, please contact directly the manufacturer of the resonator you will use.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V	P00 to P02, P20 to P27			15	pF
			P50 to P57, P60 to P64			35	pF
Output capacitance	C_{OUT}	f = 1 MHz Unmeasured pins returned to 0 V	P00 to P02, P20 to P27			15	pF
			P30 to P37, P40 to P47, P50 to P57, P60 to P64, FIP0 to FIP23			35	pF
I/O capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V	P00 to P02, P20 to P27			15	pF
			P50 to P57, P60 to P64			35	pF

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P02, P20 to P27, $\overline{\text{RESET}}$		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	P50 to P57, P60 to P64		0.7 V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2		V_{DD} – 0.5		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P02, P20 to P27, $\overline{\text{RESET}}$		0		0.2 V_{DD}	V
	V_{IL2}	X1, X2		0		0.4	V
Output voltage, high	V_{OH}	I_{OH} = –1 mA		V_{DD} – 1.0		V_{DD}	V
		I_{OH} = –100 μA		V_{DD} – 0.5		V_{DD}	V
Output voltage, low	V_{OL}	P00 to P02, P20 to P27	I_{OL} = 400 μA			0.5	V
Input leakage current, high	I_{LIH1}	P00 to P02, P20 to P27, P50 to P57, P60 to P64, $\overline{\text{RESET}}$	V_{IN} = V_{DD}			3	μA
	I_{LIH2}	X1, X2				20	μA
Input leakage current, low	I_{LIL1}	P00 to P02, P20 to P27, $\overline{\text{RESET}}$	V_{IN} = 0 V			–3	μA
	I_{LIL2}	X1, X2				–20	μA
	I_{LIL3}	P50 to P57, P60 to P64	V_{IN} = V_{LOAD} = V_{DD} – 40 V			–10	μA
Output leakage current, high	I_{LOH}	P00 to P02, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P64	V_{OUT} = V_{DD}			3	μA
Output leakage current, low	I_{LOL1}	P00 to P02, P20 to P27	V_{OUT} = 0 V			–3	μA
	I_{LOL2}	P30 to P37, P40 to P47, P50 to P57, P60 to P64	V_{OUT} = V_{LOAD} = V_{DD} – 40 V			–10	μA
VFD output current	I_{OD}	FIP0 to FIP19	V_{OD} = V_{DD} – 2 V			–15	mA
		FIP20 to FIP52				–5	mA
Software pull-up resistor	R_1	P00 to P02, P20 to P27	V_{IN} = 0 V	10	30	100	kΩ
On-chip pull-down resistor	R_2	FIP0 to FIP23	V_{OD} – V_{LOAD} = 40 V	30	60	135	kΩ
Power supply current[Note]	I_{DD1}	5 MHz crystal oscillation operation mode	PCC = 00H		9	18	mA
	I_{DD2}	5 MHz crystal oscillation HALT mode			2.5	7.5	mA
	I_{DD3}	STOP mode			1	30	μA

Note Refers to current flowing to the V_{DD} pin. The current flowing to the on-chip pull-up and pull-down resistors is not included.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

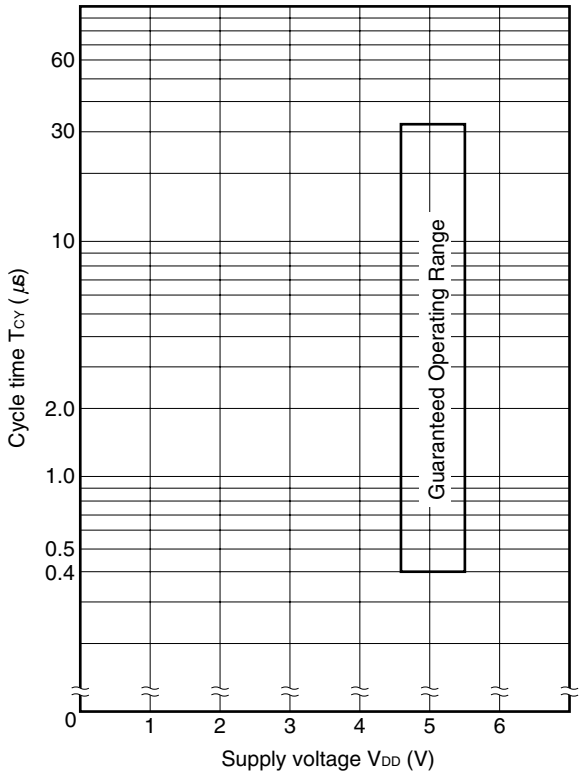
2. PCC: Processor clock control register

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operated with main system clock	0.4		32	μs
Interrupt request input high-/low-level width	t_{INTH} t_{INTL}	INTP0, INTP1	10			μs
$\overline{RESET}$ low-level width	t_{RSL}		10			μs

T_{CY} vs V_{DD}



(2) Timer/counter (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TI input high-/low-level width	t_{TIH} t_{TIL}		$2/F_{count}$ +0.2 **Note**			μs

Note F_{count} is the frequency of the count clock selected by TM9 (the frequency can be selected from $f_X/2^6$, $f_X/2^7$, $f_X/2^8$, and $f_X/2^9$).

(3) Serial interface (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

(a) Serial interface (3-wire serial mode)

(i) 3-wire serial mode ($\overline{SCK1}$...Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY1}		800			ns
$\overline{SCK1}$ high-/low-level width	t_{KH1} t_{KL1}		$t_{KCY1}/2 - 50$			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK1}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI1}		400			ns
Delay time from $\overline{SCK1}\downarrow$ to SO1 output	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the $\overline{SCK1}$ and SO1 output lines.

(ii) 3-wire serial mode ($\overline{SCK1}$...External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY2}		800			ns
$\overline{SCK1}$ high-/low-level width	t_{KH2} t_{KL2}		400			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK2}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI2}		400			ns
Delay time from $\overline{SCK1}\downarrow$ to SO1 output	t_{KSO2}	C = 100 pF[Note]			300	ns
$\overline{SCK1}$ rise/fall time	t_{R2} t_{F2}				1	μs

Note C is the load capacitance of the SO1 output line.

(b) Serial interface (2-wire serial mode)

(i) 2-wire serial mode ($\overline{SCK3}$...Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY3}		800			ns
$\overline{SCK3}$ high-/low-level width	t_{KH3} t_{KL3}		$t_{KCY3}/2 - 50$			ns
Delay time from $\overline{SCK3}\downarrow$ to SO3 output	t_{KSO3}	C = 100 pF**Note**			300	ns

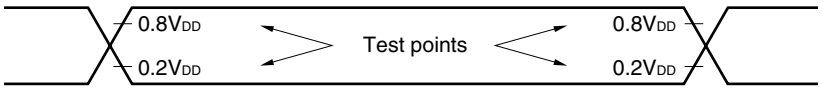
Note C is the load capacitance of the $\overline{SCK3}$ and SO3 output lines.

(ii) 2-wire serial mode ($\overline{SCK3}$...External clock input)

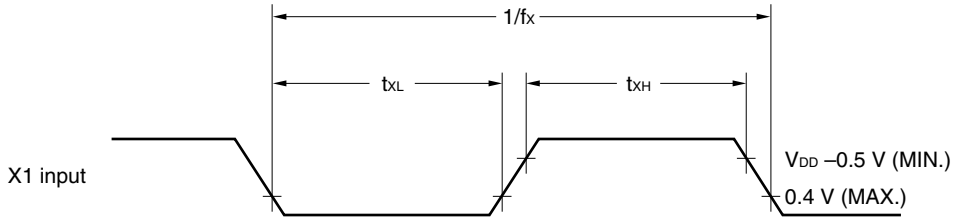
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY4}		800			ns
$\overline{SCK3}$ high-/low-level width	t_{KH4} t_{KL4}		400			ns
Delay time from $\overline{SCK3}\downarrow$ to SO3 output	t_{KSO4}	C = 100 pF**Note**			300	ns
$\overline{SCK3}$ rise/fall time	t_{R4} t_{F4}				1	μs

Note C is the load capacitance of the SO3 output line.

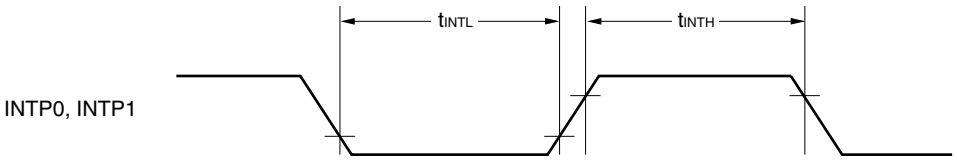
AC Timing Test Points (Excluding X1 input)



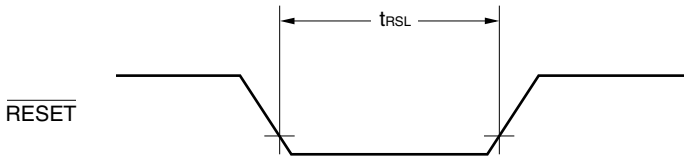
Clock Timing



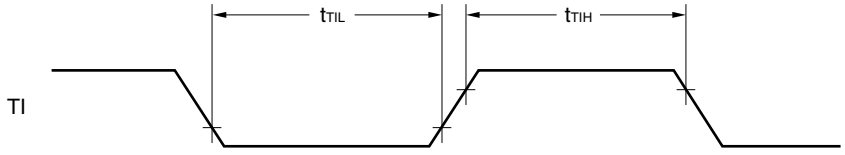
Interrupt Request Input Timing



$\overline{\text{RESET}}$ Input Timing

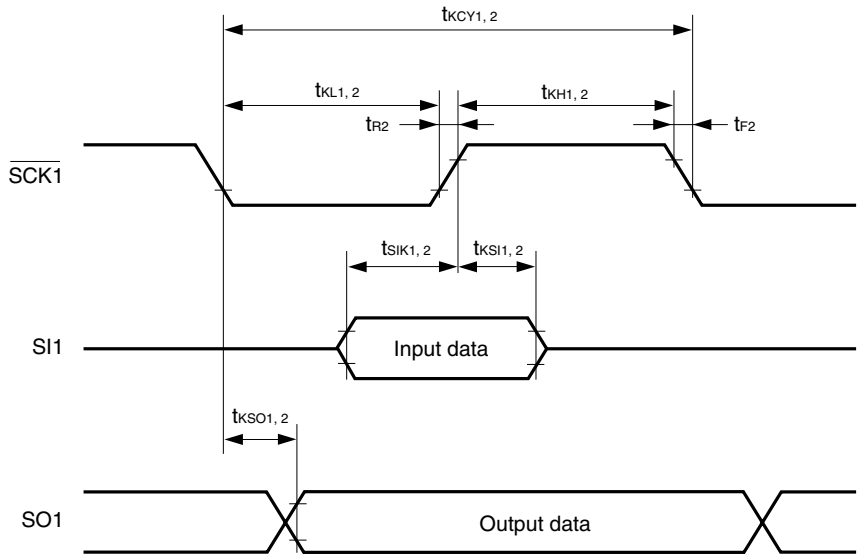


TI Timing

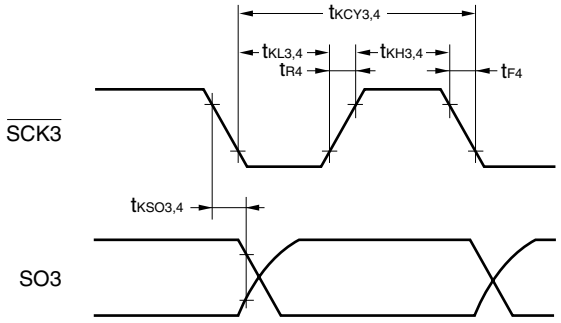


Serial Transfer Timing

3-wire serial mode:



2-wire serial mode:



A/D Converter Characteristics (T_A = –40 to +85°C, AV_{DD} = V_{DD} = 4.0 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					8	bit
Overall error**Note 1**					±1.0	%
Conversion time**Note 2**	t_{CONV}		14			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{DD}	V

Notes 1. Excludes quantization error (±1/2LSB). It is indicated as a ratio to the full-scale value.

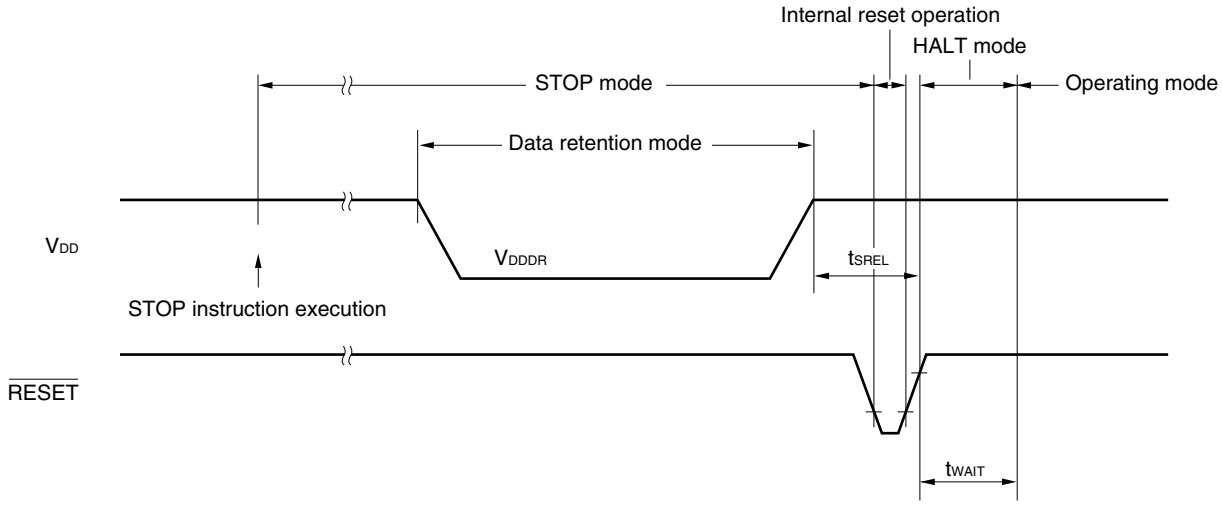
2. Set the A/D conversion time to 14 μs or more.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

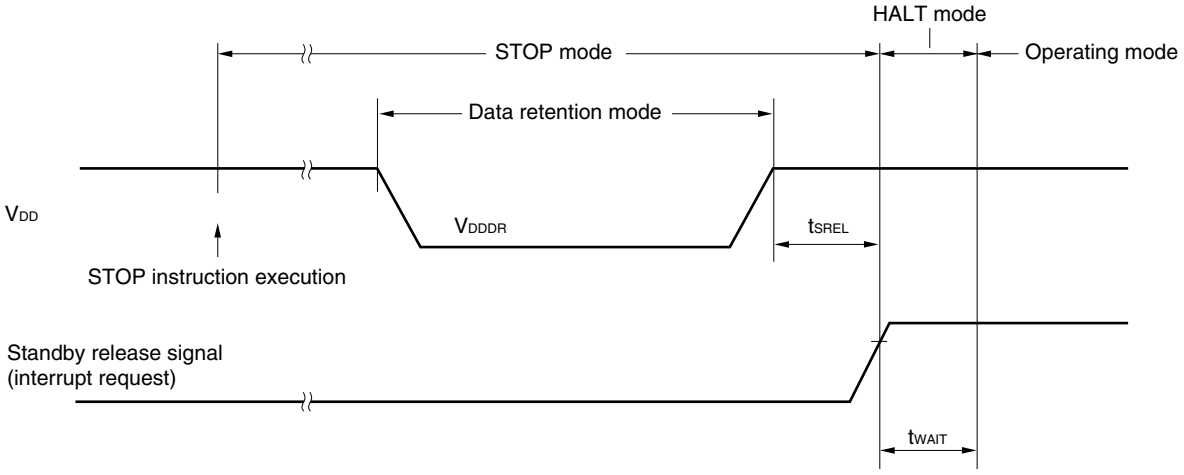
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.0		5.5	V
Data retention supply current	I_{DDDR}			0.1	30	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{17}/f_X$		ms
		Release by interrupt request		**Note**		ms

Note Selection of $2^{12}/f_X$ and $2^{14}/f_X$ to $2^{17}/f_X$ is possible with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time selection register (OSTS).

Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



Flash Memory Programming Characteristics (V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, V_{PP} = 9.7 to 10.3 V)

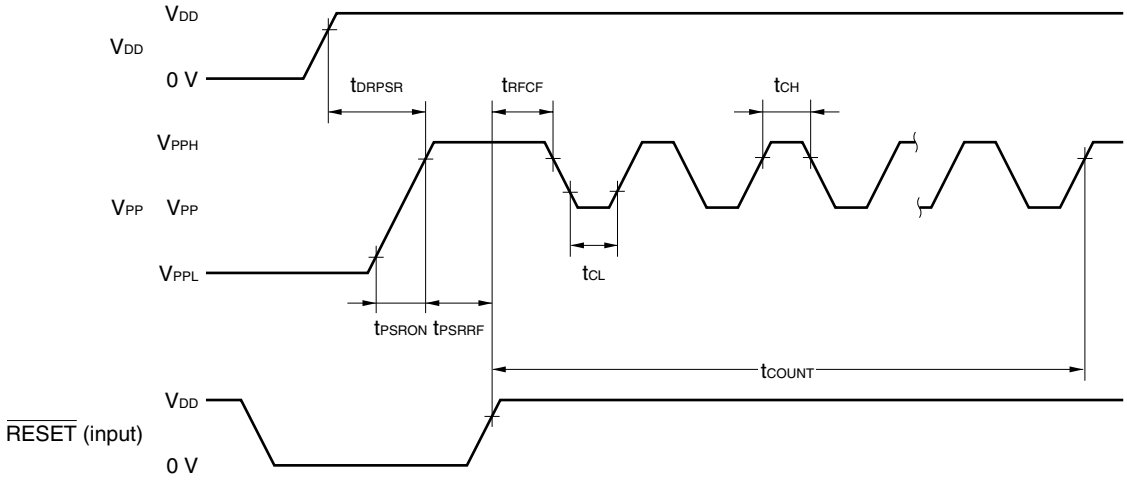
(1) Basic characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_X		1.0		5.0	MHz
Supply voltage	V_{DD}	Operation voltage when writing	4.5		5.5	V
	V_{PP}	Upon V_{PP} high-level detection	$0.8V_{DD}$	V_{DD}	$1.2V_{DD}$	V
	V_{PPH}	Upon V_{PP} high-voltage detection	9.7	10.0	10.3	V
V_{DD} supply current	I_{DD}				10	mA
V_{PP} supply current	I_{PP}	V_{PP} =10.0 V		75	100	mA
Write time (per byte)	T_{WRT}		50		500	μs
Number of rewrites	C_{WRT}				20	Times
Erase time	T_{ERASE}		1		20	s
Programming temperature	T_{PRG}		+10		+40	°C

(2) Serial write operation characteristics

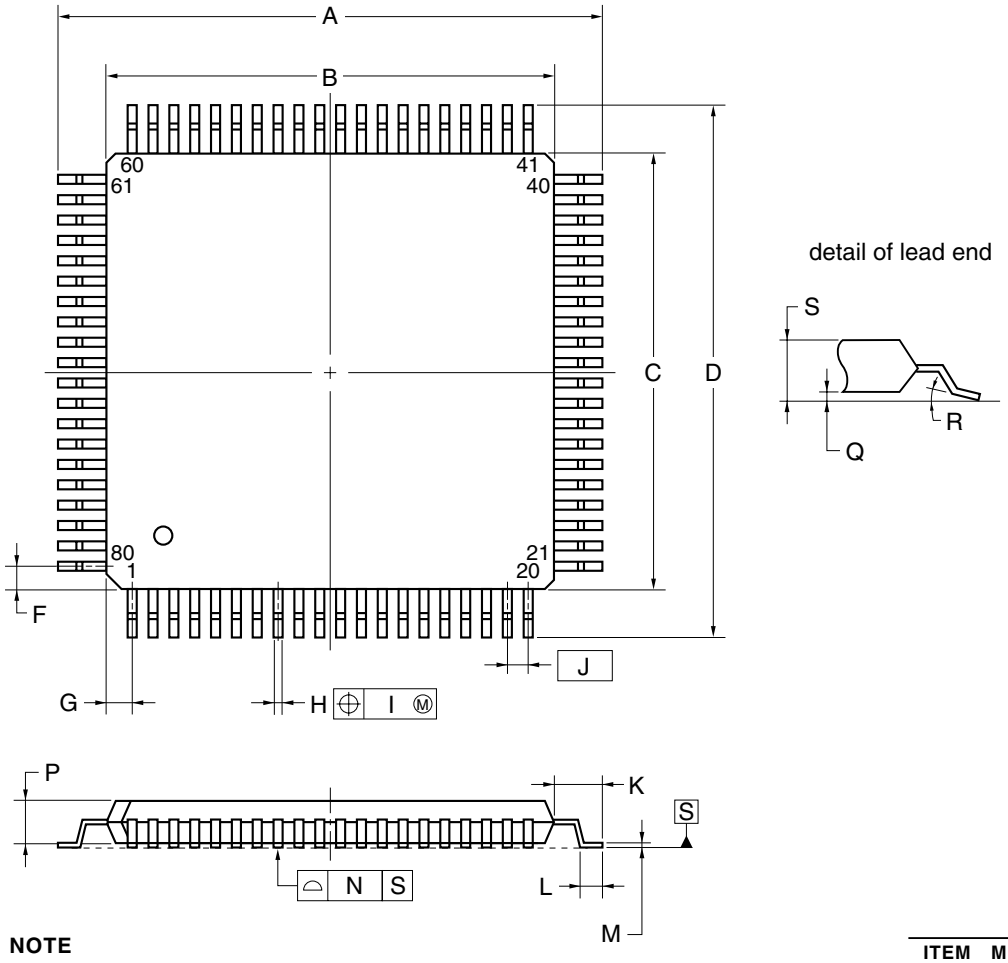
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{PP} set time	t_{PSRON}	V_{PP} high voltage	1.0			μs
Set time from V_{DD}↑ to V_{PP}↑	t_{DRPSR}	V_{PP} high voltage	1.0			μs
Set time from V_{PP}↑ to $\overline{RESET}$↑	t_{PSRRF}	V_{PP} high voltage	1.0			μs
V_{PP} count start time from $\overline{RESET}$↑	t_{RFCF}		1.0			μs
Count execution time	t_{COUNT}				2.0	ms
V_{PP} counter high-level width	t_{CH}		8.0			μs
V_{PP} counter low-level width	t_{CL}		8.0			μs
V_{PP} counter noise elimination width	t_{NFW}			40		ns

Flash Memory Write Mode Set Timing



8. PACKAGE DRAWING

80-PIN PLASTIC QFP (14x14)



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	17.20±0.20
B	14.00±0.20
C	14.00±0.20
D	17.20±0.20
F	0.825
G	0.825
H	0.32±0.06
I	0.13
J	0.65 (T.P.)
K	1.60±0.20
L	0.80±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.10
P	1.40±0.10
Q	0.125±0.075
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.70 MAX.

P80GC-65-8BT-1

★ 9. RECOMMENDED SOLDERING CONDITIONS

The μPD78F0233 should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 9-1. Surface Mounting Type Soldering Conditions

μPD78F0233GC-8BT: 80-pin plastic QFP (14 × 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Two times or less	VP15-00-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Twice Preheating temperature: 120°C max. (package surface temperature)	WS60-00-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78F0233.
Also refer to **(6) Notes on using development tools**.

(1) Software Package

SP78K0	78K/0 Series common software package

(2) Language Processing Software

RA78K0	78K/0 Series common assembler package
CC78K0	78K/0 Series common C compiler package
★ DF780233	μPD780232 Subseries device file
CC78K0-L	78K/0 Series common C compiler library source file

(3) Flash Memory Writing Tools

★ Flashpro III (FL-PR3, GP-FP3)	Dedicated flash programmer for on-chip flash memory microcontrollers
FA-80GC	Adapter for flash memory writing Used by connecting to Flashpro III • For 80-pin plastic QFP (GC-8BT type)

(4) Debugging Tools

- **When in-circuit emulator IE-78K0-NS (-A) is used**

IE-78K0-NS (-A)	In-circuit emulator common to 78K/0 Series
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
★ IE-78K0-NS-PA	Performance board that enhances and expands the IE-78K0-NS functions
IE-70000-98-IF-C	Adapter required when PC-9800 series (except notebook type) is used as host machine (C bus supported)
★ IE-70000-CD-IF-A	PC card and interface cable required when notebook type PC is used as host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Adapter required when IBM PC/AT™ or compatible is used as host machine
★ IE-70000-PCI-IF-A	Adapter required when PC incorporating PCI bus is used as host machine
★ IE-780233-NS-EM4, IE-78K0-NS-P01	Emulation board and I/O board to emulate the μPD780232 Subseries
NP-80GC ★ NP-80GC-TQ ★ NP-H80GC-TQ	Emulation probe for 80-pin plastic QFP (GC-8BT type)
EV-9200GC-80	Conversion socket to connect the NP-80GC and the target system board on which 80-pin plastic QFP (GC-8BT type) can be mounted
★ TGC-080SBP	Conversion adapter to connect the NP-80GC-TQ or NP-H80GC-TQ and a target system board on which an 80-pin plastic QFP (GC-8BT type) can be mounted
ID78K0-NS	Integrated debugger for IE-78K0-NS
SM78K0	System simulator common to 78K/0 Series
★ DF780233	Device file for μPD780232 Subseries

- **When in-circuit emulator IE-78001-R-A is used**

IE-78001-R-A	In-circuit emulator common to 78K/0 Series
★ IE-70000-98-IF-C	Adapter required when PC-9800 series (except notebook type) is used as host machine (C bus supported)
★ IE-70000-PC-IF-C	Adapter required when IBM PC/AT or compatible is used as host machine (ISA bus supported)
★ IE-70000-PCI-IF-A	Adapter required when PC incorporating PCI bus is used as host machine
IE-70000-R-SV3	Interface adapter and cable required when EWS is used as host machine
★ IE-780233-NS-EM4, IE-78K0-NS-P01	Emulation board and I/O board to emulate the μPD780232 Subseries
IE-78K0-R-EX1	Emulation probe conversion board required when using IE-780232-NS-EM1 on IE-78001-R-A
EP-78230GC-R	Emulation probe for 80-pin plastic QFP (GC-8BT type)
EV-9200GC-80	Conversion socket to connect the EP-78230GC-R and the target system board on which 80-pin plastic QFP (GC-8BT type) can be mounted
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	System simulator common to 78K/0 Series
★ DF780233	Device file for μPD780232 Subseries

(5) Real-Time OSs

RX78K0	Real-time OS for 78K/0 Series
MX78K0	OS for 78K/0 Series

★ (6) Notes on using development tools

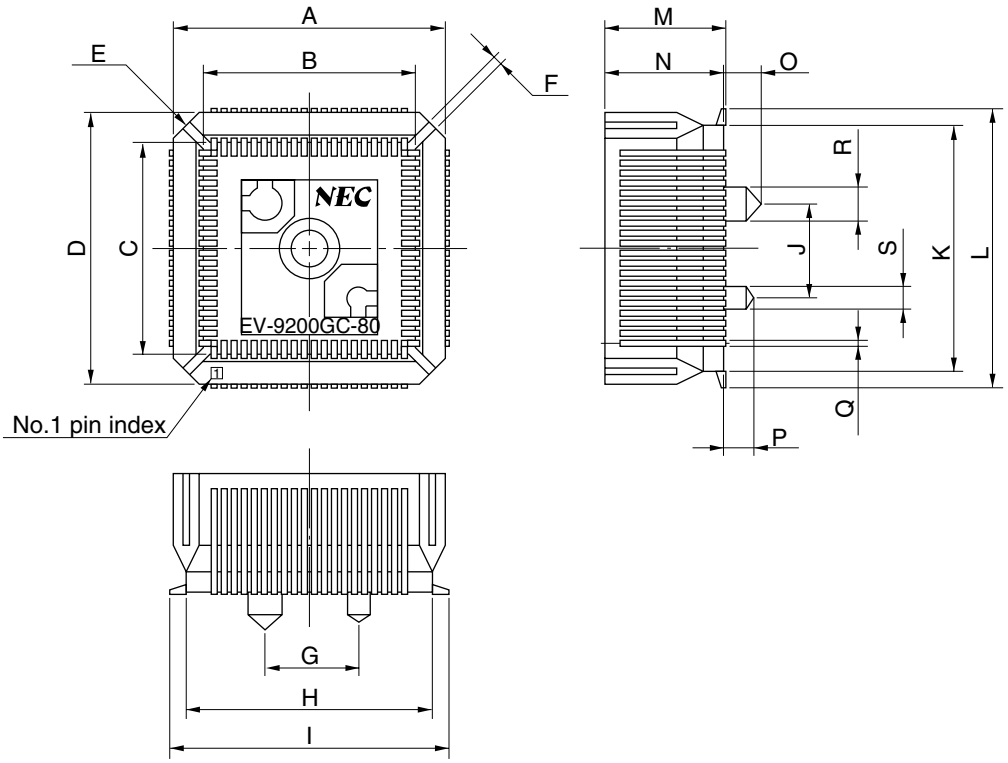
- The ID78K0-NS, ID78K0, and SM78K0 in combination with the DF780233.
- The CC78K0 and RX78K0 are used in combination with the RA78K0 and DF780233.
- FL-PR3, FA-80GC, NP-80GC, NP-80GC-TQ, and NP-H80GC-TQ are products made by Naito Densei Machida Mfg. Co., Ltd. (+81-45-475-4191).
- TGK-080SBP is a product made by TOKYO ELETECH CORPORATION.
  For further information, contact Daimaru Kogyo, Ltd.
  Tokyo Electronics Department (+81-3-3820-7112)
  Osaka Electronics Department (+81-6-6244-6672)
- For third-party development tools, refer to **Single-Chip Microcontroller Selection Guide (U11069E)**.
- The host machines and OS suitable for each software are as follows:

Host Machine [OS] / Software	PC PC-9800 series [Windows™] IBM PC/AT or compatibles [Japanese/English Windows]	EWS HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™]
RA78K0	√Note	√
CC78K0	√Note	√
ID78K0-NS	√	—
ID78K0	√	—
SM78K0	√	—
RX78K0	√Note	√
MX78K0	√Note	√

Note DOS-based software

CONVERSION SOCKET (EV-9200GC-80) DRAWING AND RECOMMENDED BOARD MOUNTING PATTERN

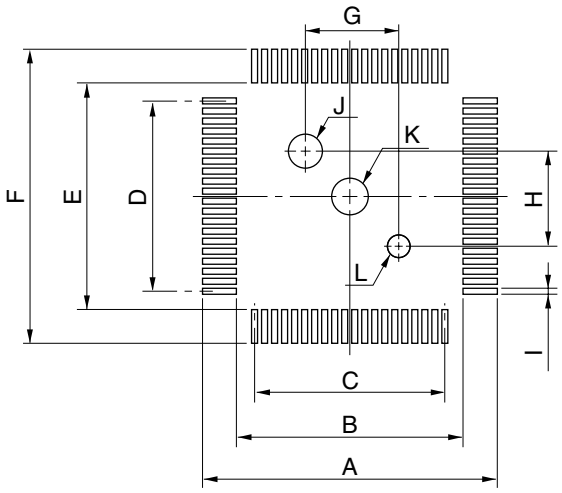
Figure A-1. EV-9200GC-80 Drawing (for reference only)



EV-9200GC-80-G1E

ITEM	MILLIMETERS	INCHES
A	18.0	0.709
B	14.4	0.567
C	14.4	0.567
D	18.0	0.709
E	4-C 2.0	4-C 0.079
F	0.8	0.031
G	6.0	0.236
H	16.0	0.63
I	18.7	0.736
J	6.0	0.236
K	16.0	0.63
L	18.7	0.736
M	8.2	0.323
N	8.0	0.315
O	2.5	0.098
P	2.0	0.079
Q	0.35	0.014
R	ϕ2.3	ϕ0.091
S	ϕ1.5	ϕ0.059

Figure A-2. EV-9200GC-80 Recommended Board Mounting Pattern (for reference only)



EV-9200GC-80-P1E

ITEM	MILLIMETERS	INCHES
A	19.7	0.776
B	15.0	0.591
C	$0.65\pm0.02\times19=12.35\pm0.05$	$0.026^{+0.001}_{-0.002}\times0.748=0.486^{+0.003}_{-0.002}$
D	$0.65\pm0.02\times19=12.35\pm0.05$	$0.026^{+0.001}_{-0.002}\times0.748=0.486^{+0.003}_{-0.002}$
E	15.0	0.591
F	19.7	0.776
G	6.0 ± 0.05	$0.236^{+0.003}_{-0.002}$
H	6.0 ± 0.05	$0.236^{+0.003}_{-0.002}$
I	0.35 ± 0.02	$0.014^{+0.001}_{-0.001}$
J	$\phi2.36\pm0.03$	$\phi0.093^{+0.001}_{-0.002}$
K	$\phi2.3$	$\phi0.091$
L	$\phi1.57\pm0.03$	$\phi0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

APPENDIX B. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

★ **Documents Related to Device**

Document Name	Document No.
μPD780232 Subseries User's Manual	U13364E
μPD780232 Data Sheet	U13415E
μPD78F0233 Data Sheet	This manual
78K/0 Series User's Manual - Instructions	U12326E

★ **Documents Related to Development Tool (User's Manual)**

Document Name		Document No.
RA78K0 Assembler Package	Operation	U14445E
	Language	U14446E
	Structured Assembly Language	U11789E
CC78K0 C Compiler	Operation	U14297E
	Language	U14298E
IE-78K0-NS In-Circuit Emulator		U13731E
IE-78K0-NS-A In-Circuit Emulator		U14889E
IE-78001-R-A In-Circuit Emulator		U14142E
IE-78K0-R-EX1 In-Circuit Emulator		To be prepared
IE-780233-NS-EM4 Emulation Board		U14666E
EP-78230 Emulation Probe		EEU-1515
SM78K0S, SM78K0 System Simulator Ver. 2.10 or Later Windows Based	Operation	U14611E
SM78K Series System Simulator Ver. 2.10 or Later	External Part User Open Interface Specifications	U15006E
ID78K0-NS Integrated Debugger Ver. 2.00 or Later Windows Based	Operation	U14379E
ID78K0-NS, ID78K0S-NS Integrated Debugger Ver. 2.20 or Later Windows Based	Operation	U14910E
ID78K0 Integrated Debugger Windows Based	Reference	U11539E
	Guide	U11649E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Documents Related to Embedded Software (User's Manuals)

Document Name		Document No.
78K/0 Series Real-Time OS	Fundamental	U11537E
	Installation	U11536E
78K/0 Series OS MX78K0	Fundamental	U12257E

Other Related Documents

Document Name	Document No.
★ SEMICONDUCTOR SELECTION GUIDE - Products & Packages - (CD-ROM)	X13769E
Semiconductor Device Mounting Technology Manual	C10535E
Quality Guides on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability and Quality Control	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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