

Data Sheet



Lead (Pb) Free
RoHS 6 fully
compliant



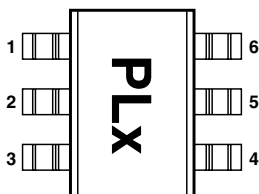
Description

Avago's HSMS-285x family of zero bias Schottky detector diodes has been designed and optimized for use in small signal (Pin < -20 dBm) applications at frequencies below 1.5 GHz. They are ideal for RF/ID and RF Tag applications where primary (DC bias) power is not available.

Important Note: For detector applications with input power levels greater than -20 dBm, use the HSMS-282x series at frequencies below 4.0 GHz, and the HSMS-286x series at frequencies above 4.0 GHz. The HSMS-285x series IS NOT RECOMMENDED for these higher power level applications.

Available in various package configurations, these detector diodes provide low cost solutions to a wide variety of design problems. Avago's manufacturing techniques assure that when two diodes are mounted into a single package, they are taken from adjacent sites on the wafer, assuring the highest possible degree of match.

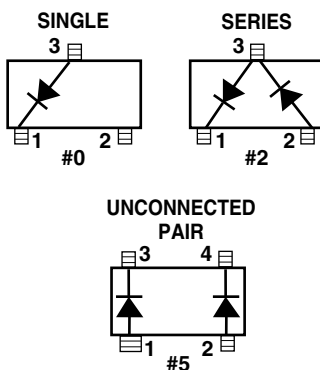
Pin Connections and Package Marking



Notes:

1. Package marking provides orientation and identification.
2. See "Electrical Specifications" for appropriate package marking.

SOT-23/SOT-143 Package Lead Code Identification (top view)



Features

- Surface Mount SOT-23/SOT-143 Packages
- Miniature SOT-323 and SOT-363 Packages
- High Detection Sensitivity:
up to 50 mV/μW at 915 MHz
- Low Flicker Noise:
-162 dBV/Hz at 100 Hz
- Low FIT (Failure in Time) Rate*
- Tape and Reel Options Available
- Matched Diodes for Consistent Performance
- Better Thermal Conductivity for Higher Power Dissipation
- Lead-free

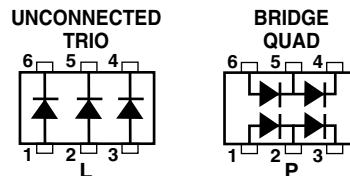
* For more information see the Surface Mount Schottky Reliability Data Sheet.



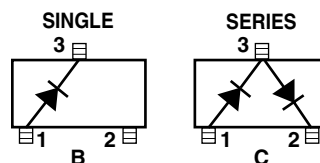
Attention: Observe precautions for handling electrostatic sensitive devices.

ESD Machine Model (Class A)
ESD Human Body Model (Class 0)
Refer to Avago Application Note A004R:
Electrostatic Discharge Damage and Control.

SOT-363 Package Lead Code Identification (top view)



SOT-323 Package Lead Code Identification (top view)



SOT-23/SOT-143 DC Electrical Specifications, $T_c = +25^\circ\text{C}$, Single Diode

Part Number HSMS-	Package Marking Code	Lead Code	Configuration	Maximum Forward Voltage		Maximum Reverse Leakage,	Typical Capacitance C_T (pF)
				V_F (mV)		I_R (μA)	
2850	P0	0	Single	150	250	175	0.30
2852	P2	2	Series Pair ^[1,2]				
2855	P5	5	Unconnected Pair ^[1,2]				
Test Conditions				$I_F = 0.1 \text{ mA}$	$I_F = 1.0 \text{ mA}$	$V_R = 2\text{V}$	$V_R = -0.5 \text{ V to } -1.0\text{V}$ $f = 1 \text{ MHz}$

Notes:

1. ΔV_F for diodes in pairs is 15.0 mV maximum at 1.0 mA.
2. ΔC_T for diodes in pairs is 0.05 pF maximum at -0.5V .

SOT-323/SOT-363 DC Electrical Specifications, $T_c = +25^\circ\text{C}$, Single Diode

Part Number HSMS-	Package Marking Code	Lead Code	Configuration	Maximum Forward Voltage		Maximum Reverse Leakage,	Typical Capacitance C_T (pF)
				V_F (mV)		I_R (μA)	
285B	P0	B	Single	150	250	175.	0.30
285C	P2	C	Series Pair				
285L	PL	L	Unconnected Trio				
285P	PP	P	Bridge Quad				
Test Conditions				$I_F = 0.1 \text{ mA}$	$I_F = 1.0 \text{ mA}$	$V_R = 2\text{V}$	$V_R = 0.5 \text{ V to } -1.0\text{V}$ $f = 1 \text{ MHz}$

Notes:

1. ΔV_F for diodes in pairs is 15.0 mV maximum at 1.0 mA.
2. ΔC_T for diodes in pairs is 0.05 pF maximum at -0.5V .

RF Electrical Specifications, $T_c = +25^\circ\text{C}$, Single Diode

Part Number HSMS-	Typical Tangential Sensitivity TSS (dBm) @ $f = 915 \text{ MHz}$	Typical Voltage Sensitivity g (mV/ μW) @ $f = 915 \text{ MHz}$	Typical Video Resistance R_V (K Ω)
2850	-57	40	8.0
2852			
2855			
285B			
285C			
285L			
285P			
Test Conditions	Video Bandwidth = 2 MHz Zero Bias	Power in = -40 dBm $R_L = 100 \text{ K}\Omega$, Zero Bias	Zero Bias

Absolute Maximum Ratings, $T_C = +25^\circ\text{C}$, Single Diode

Symbol	Parameter	Unit	Absolute Maximum ^[1]	
			SOT-23/143	SOT-323/363
P_{IV}	Peak Inverse Voltage	V	2.0	2.0
T_J	Junction Temperature	$^\circ\text{C}$	150	150
T_{STG}	Storage Temperature	$^\circ\text{C}$	-65 to 150	-65 to 150
T_{OP}	Operating Temperature	$^\circ\text{C}$	-65 to 150	-65 to 150
θ_{jc}	Thermal Resistance ^[2]	$^\circ\text{C}/\text{W}$	500	150

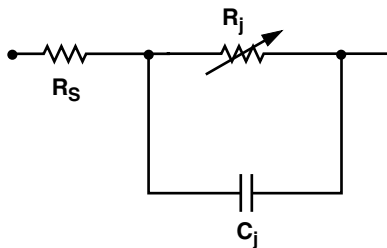
ESD WARNING:
Handling Precautions Should Be Taken
To Avoid Static Discharge.

Notes:

1. Operation in excess of any one of these conditions may result in permanent damage to the device.
2. $T_C = +25^\circ\text{C}$, where T_C is defined to be the temperature at the package pins where contact is made to the circuit board.

Equivalent Linear Circuit Model

HSMS-285x chip



R_S = series resistance (see Table of SPICE parameters)

C_j = junction capacitance (see Table of SPICE parameters)

$$R_j = \frac{8.33 \times 10^{-5} nT}{I_b + I_s}$$

where

I_b = externally applied bias current in amps

I_s = saturation current (see table of SPICE parameters)

T = temperature, $^\circ\text{K}$

n = ideality factor (see table of SPICE parameters)

Note:

To effectively model the packaged HSMS-285x product, please refer to Application Note AN1124.

SPICE Parameters

Parameter	Units	HSMS-285x
B_V	V	3.8
C_{J0}	pF	0.18
E_G	eV	0.69
I_{BV}	A	3 E-4
I_S	A	3 E-6
N		1.06
R_S	Ω	25
$P_B (V_J)$	V	0.35
$P_T (XTI)$		2
M		0.5

Typical Parameters, Single Diode

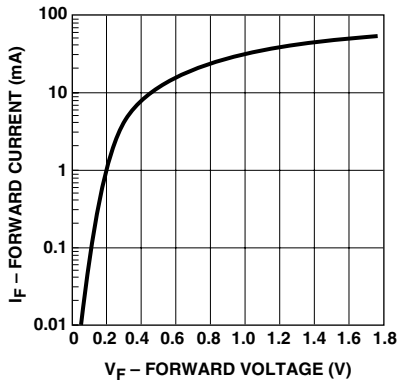


Figure 1. Typical Forward Current vs. Forward Voltage.

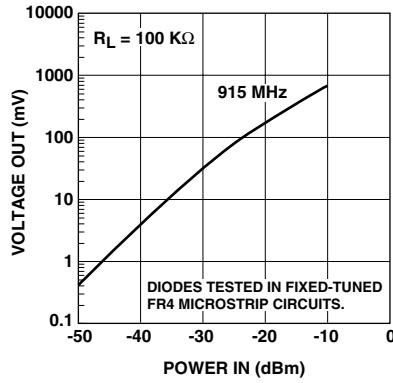


Figure 2. +25°C Output Voltage vs. Input Power at Zero Bias.

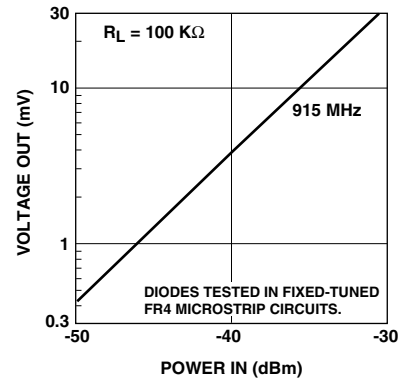


Figure 3. +25°C Expanded Output Voltage vs. Input Power. See Figure 2.

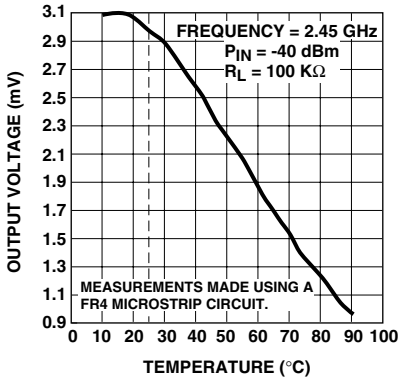


Figure 4. Output Voltage vs. Temperature.

Applications Information

Introduction

Avago's HSMS-285x family of Schottky detector diodes has been developed specifically for low cost, high volume designs in small signal ($P_{in} < -20$ dBm) applications at frequencies below 1.5 GHz. At higher frequencies, the DC biased HSMS-286x family should be considered.

In large signal power or gain control applications ($P_{in} > -20$ dBm), the HSMS-282x and HSMS-286x products should be used. The HSMS-285x zero bias diode is not designed for large signal designs.

Schottky Barrier Diode Characteristics

Stripped of its package, a Schottky barrier diode chip consists of a metal-semiconductor barrier formed by deposition of a metal layer on a semiconductor. The most common of several different types, the passivated diode, is shown in Figure 5, along with its equivalent circuit.

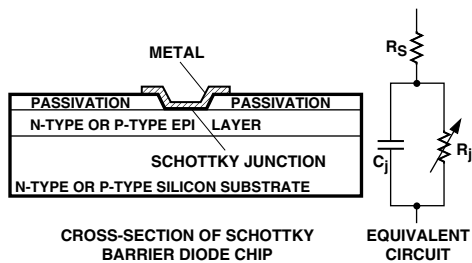


Figure 5. Schottky Diode Chip.

R_s is the parasitic series resistance of the diode, the sum of the bondwire and leadframe resistance, the resistance of the bulk layer of silicon, etc. RF energy coupled into R_s is lost as heat — it does not contribute to the rectified output of the diode. C_j is parasitic junction capacitance of the diode, controlled by the thickness of the epitaxial layer and the diameter of the Schottky contact. R_j is the junction resistance of the diode, a function of the total current flowing through it.

$$R_j = \frac{8.33 \times 10^{-5} n T}{I_s + I_b} = R_V - R_s$$

$$= \frac{0.026}{I_s + I_b} \text{ at } 25^\circ\text{C}$$

where

n = ideality factor (see table of SPICE parameters)

T = temperature in $^\circ\text{K}$

I_s = saturation current (see table of SPICE parameters)

I_b = externally applied bias current in amps

I_s is a function of diode barrier height, and can range from picoamps for high barrier diodes to as much as 5 μA for very low barrier diodes.

The Height of the Schottky Barrier

The current-voltage characteristic of a Schottky barrier diode at room temperature is described by the following equation:

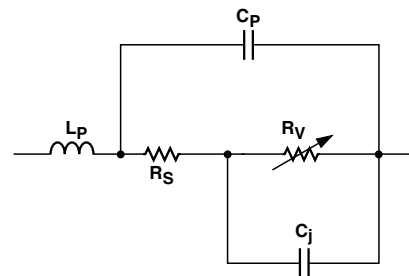
$$I = I_s \left(\exp\left(\frac{V - IR_s}{0.026}\right) - 1 \right)$$

On a semi-log plot (as shown in the Avago catalog) the current graph will be a straight line with inverse slope $2.3 \times 0.026 = 0.060$ volts per cycle (until the effect of R_s is seen in a curve that droops at high current). All Schottky diode curves have the same slope, but not necessarily the same value of current for a given voltage. This is determined by the saturation current, I_s , and is related to the barrier height of the diode.

Through the choice of p-type or n-type silicon, and the selection of metal, one can tailor the characteristics of a Schottky diode. Barrier height will be altered, and at the same time C_j and R_s will be changed. In general, very low barrier height diodes (with high values of I_s , suitable for zero bias applications) are realized on p-type silicon. Such diodes suffer from higher values of R_s than do the n-type. Thus, p-type diodes are generally reserved for small signal detector applications (where very high values of R_V swamp out high R_s) and n-type diodes are used for mixer applications (where high L.O. drive levels keep R_V low).

Measuring Diode Parameters

The measurement of the five elements which make up the low frequency equivalent circuit for a packaged Schottky diode (see Figure 6) is a complex task. Various techniques are used for each element. The task begins with the elements of the diode chip itself.



FOR THE HSMS-285x SERIES

$C_p = 0.08$ pF

$L_p = 2$ nH

$C_j = 0.18$ pF

$R_s = 25$ Ω

$R_V = 9$ $\text{K}\Omega$

Figure 6. Equivalent Circuit of a Schottky Diode.

R_s is perhaps the easiest to measure accurately. The V-I curve is measured for the diode under forward bias, and the slope of the curve is taken at some relatively high value of current (such as 5 mA). This slope is converted into a resistance R_d .

$$R_s = R_d - \frac{0.026}{I_f}$$

R_V and C_J are very difficult to measure. Consider the impedance of $C_J = 0.16$ pF when measured at 1 MHz — it is approximately 1 M Ω . For a well designed zero bias Schottky, R_V is in the range of 5 to 25 K Ω , and it shorts out the junction capacitance. Moving up to a higher frequency enables the measurement of the capacitance, but it then shorts out the video resistance. The best measurement technique is to mount the diode in series in a 50 Ω microstrip test circuit and measure its insertion loss at low power levels (around -20 dBm) using an HP8753C network analyzer. The resulting display will appear as shown in Figure 7.

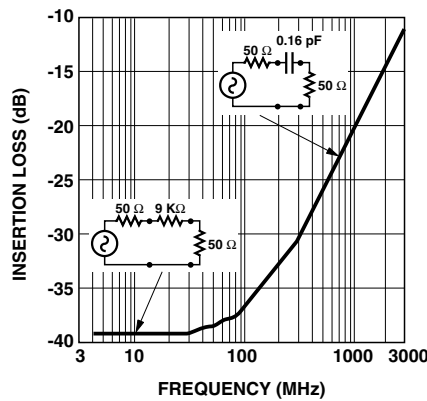


Figure 7. Measuring C_J and R_V .

At frequencies below 10 MHz, the video resistance dominates the loss and can easily be calculated from it. At frequencies above 300 MHz, the junction capacitance sets the loss, which plots out as a straight line when frequency is plotted on a log scale. Again, calculation is straightforward.

L_p and C_p are best measured on the HP8753C, with the diode terminating a 50 Ω line on the input port. The resulting tabulation of S_{11} can be put into a microwave linear analysis program having the five element equivalent circuit with R_V , C_J and R_s fixed. The optimizer can then adjust the values of L_p and C_p until the calculated S_{11} matches the measured values. Note that extreme care must be taken to de-embed the parasitics of the 50 Ω test fixture.

Detector Circuits

When DC bias is available, Schottky diode detector circuits can be used to create low cost RF and microwave receivers with a sensitivity of -55 dBm to -57 dBm.^[1] These circuits can take a variety of forms, but in the most simple case they appear as shown in Figure 8. This is the basic detector circuit used with the HSMS-285x family of diodes.

In the design of such detector circuits, the starting point is the equivalent circuit of the diode, as shown in Figure 6.

Of interest in the design of the video portion of the circuit is the diode's video impedance—the other four elements of the equivalent circuit disappear at all reasonable video frequencies. In general, the lower the diode's video impedance, the better the design.

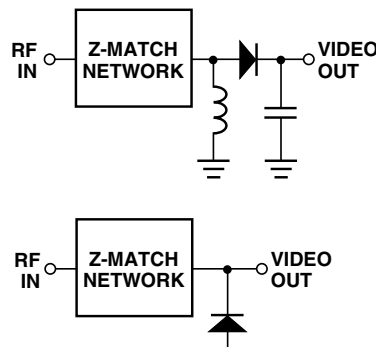


Figure 8. Basic Detector Circuits.

The situation is somewhat more complicated in the design of the RF impedance matching network, which includes the package inductance and capacitance (which can be tuned out), the series resistance, the junction capacitance and the video resistance. Of these five elements of the diode's equivalent circuit, the four parasitics are constants and the video resistance is a function of the current flowing through the diode.

$$R_V \approx \frac{26,000}{I_s + I_b}$$

where

I_s = diode saturation current in μ A

I_b = bias current in μ A

Saturation current is a function of the diode's design,^[2] and it is a constant at a given temperature. For the HSMS-285x series, it is typically 3 to 5 μ A at 25°C.

Saturation current sets the detection sensitivity, video resistance and input RF impedance of the zero bias Schottky detector diode. Since no external bias is used with the HSMS-285x series, a single transfer curve at any given frequency is obtained, as shown in Figure 2.

^[1] Avago Application Note 923, Schottky Barrier Diode Video Detectors.

The most difficult part of the design of a detector circuit is the input impedance matching network. For very broadband detectors, a shunt $60\ \Omega$ resistor will give good input match, but at the expense of detection sensitivity.

When maximum sensitivity is required over a narrow band of frequencies, a reactive matching network is optimum. Such networks can be realized in either lumped or distributed elements, depending upon frequency, size constraints and cost limitations, but certain general design principals exist for all types.^[3] Design work begins with the RF impedance of the HSMS-285x series, which is given in Figure 9.

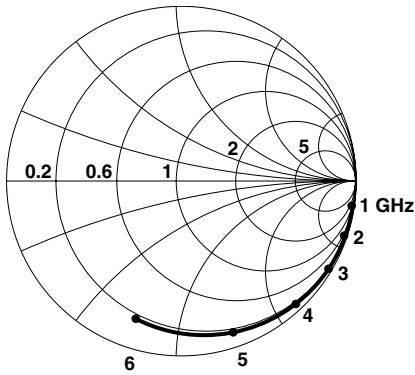


Figure 9. RF Impedance of the HSMS-285x Series at -40 dBm.

915 MHz Detector Circuit

Figure 10 illustrates a simple impedance matching network for a 915 MHz detector.

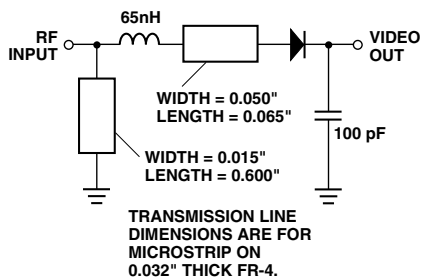
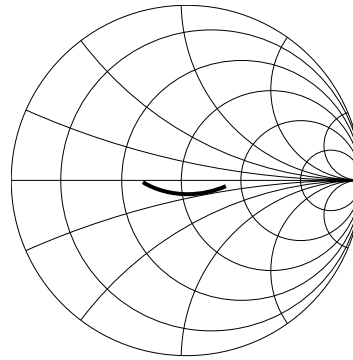


Figure 10. 915 MHz Matching Network for the HSMS-285x Series at Zero Bias.

A 65 nH inductor rotates the impedance of the diode to a point on the Smith Chart where a shunt inductor can pull it up to the center. The short length of 0.065" wide microstrip line is used to mount the lead of the diode's SOT-323 package. A shorted shunt stub of length $<\lambda/4$ provides the necessary shunt inductance and simultaneously provides the return circuit for the current generated in the diode. The impedance of this circuit is given in Figure 11.



FREQUENCY (GHz): 0.9-0.93

Figure 11. Input Impedance.

The input match, expressed in terms of return loss, is given in Figure 12.

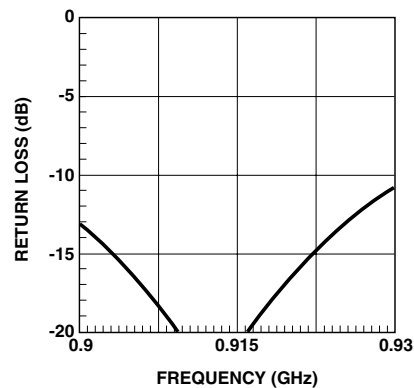


Figure 12. Input Return Loss.

As can be seen, the band over which a good match is achieved is more than adequate for 915 MHz RFID applications.

Voltage Doublers

To this point, we have restricted our discussion to single diode detectors. A glance at Figure 8, however, will lead to the suggestion that the two types of single diode detectors be combined into a two diode voltage doubler^[4] (known also as a full wave rectifier). Such a detector is shown in Figure 13.

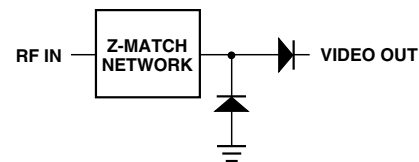


Figure 13. Voltage Doubler Circuit.

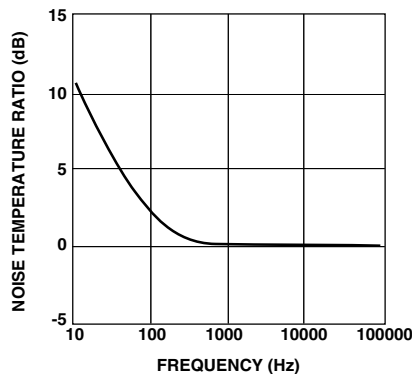
^[2] Avago Application Note 969, An Optimum Zero Bias Schottky Detector Diode.

^[3] Avago Application Note 963, Impedance Matching Techniques for Mixers and Detectors.

Such a circuit offers several advantages. First the voltage outputs of two diodes are added in series, increasing the overall value of voltage sensitivity for the network (compared to a single diode detector). Second, the RF impedances of the two diodes are added in parallel, making the job of reactive matching a bit easier. Such a circuit can easily be realized using the two series diodes in the HSMS-285C.

Flicker Noise

Reference to Figure 5 will show that there is a junction of metal, silicon, and passivation around the rim of the Schottky contact. It is in this three-way junction that flicker noise^[5] is generated. This noise can severely reduce the sensitivity of a crystal video receiver utilizing a Schottky detector circuit if the video frequency is below the noise corner. Flicker noise can be substantially reduced by the elimination of passivation, but such diodes cannot be mounted in non-hermetic packages. p-type silicon Schottky diodes have the least flicker noise at a given value of external bias (compared to n-type silicon or GaAs). At zero bias, such diodes can have extremely low values of flicker noise. For the HSMS-285x series, the noise temperature ratio is given in Figure 14.



Diode Burnout

Figure 14. Typical Noise Temperature Ratio.

Noise temperature ratio is the quotient of the diode's noise power (expressed in dBV/Hz) divided by the noise power of an ideal resistor of resistance $R = R_v$.

For an ideal resistor R , at 300°K, the noise voltage can be computed from

$$v = 1.287 \times 10^{-10} \sqrt{R} \text{ volts/Hz}$$

which can be expressed as

$$20 \log_{10} v \text{ dBV/Hz}$$

Thus, for a diode with $R_v = 9\text{K}\Omega$, the noise voltage is 12.2 nV/Hz or -158 dBV/Hz. On the graph of Figure 14, -158 dBV/Hz would replace the zero on the vertical scale to convert the chart to one of absolute noise voltage vs. frequency.

Any Schottky junction, be it an RF diode or the gate of a MESFET, is relatively delicate and can be burned out with excessive RF power. Many crystal video receivers used in RFID (tag) applications find themselves in poorly controlled environments where high power sources may be present. Examples are the areas around airport and FAA radars, nearby ham radio operators, the vicinity of a broadcast band transmitter, etc. In such environments, the Schottky diodes of the receiver can be protected by a device known as a limiter diode.^[6] Formerly available only in radar warning receivers and other high cost electronic warfare applications, these diodes have been adapted to commercial and consumer circuits.

Avago offers a complete line of surface mountable PIN limiter diodes. Most notably, our HSMP-4820 (SOT-23) can act as a very fast (nanosecond) power-sensitive switch when placed between the antenna and the Schottky diode, shorting out the RF circuit temporarily and reflecting the excessive RF energy back out the antenna.

Assembly Instructions

SOT-323 PCB Footprint

A recommended PCB pad layout for the miniature SOT-323 (SC-70) package is shown in Figure 15 (dimensions are in inches). This layout provides ample allowance for package placement by automated assembly equipment without adding parasitics that could impair the performance. Figure 16 shows the pad layout for the six-lead SOT-363.

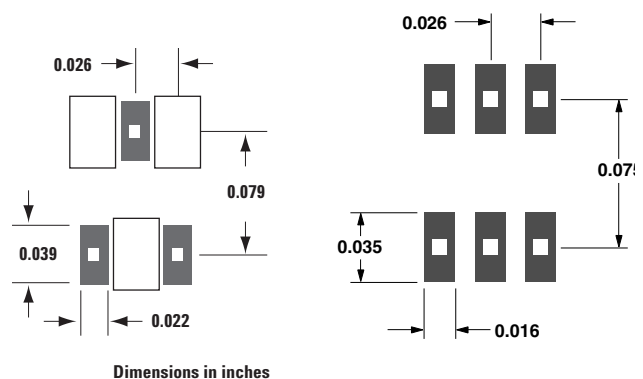


Figure 15. Recommended PCB Pad Layout for Avago's SC70 3L/SOT-323 Products.

Figure 16. Recommended PCB Pad Layout for Avago's SC70 6L/SOT-363 Products.

^[4] Avago Application Note 956-4, Schottky Diode Voltage Doubler.

^[5] Avago Application Note 965-3, Flicker Noise in Schottky Diodes.

^[6] Avago Application Note 1050, Low Cost, Surface Mount Power Limiters.

SMT Assembly

Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g., IR or vapor phase reflow, wave soldering, etc.) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the SOT packages, will reach solder reflow temperatures faster than those with a greater mass.

Avago's diodes have been qualified to the time-temperature profile shown in Figure 17. This profile is representative of an IR reflow type of surface mount assembly process.

After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat

zones. The preheat zones increase the temperature of the board and components to prevent thermal shock and begin evaporating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

The rates of change of temperature for the ramp-up and cool-down zones are chosen to be low enough to not cause deformation of the board or damage to components due to thermal shock. The maximum temperature in the reflow zone (T_{MAX}) should not exceed 260°C.

These parameters are typical for a surface mount assembly process for Avago diodes. As a general guideline, the circuit board and components should be exposed only to the minimum temperatures and times necessary to achieve a uniform reflow of solder.

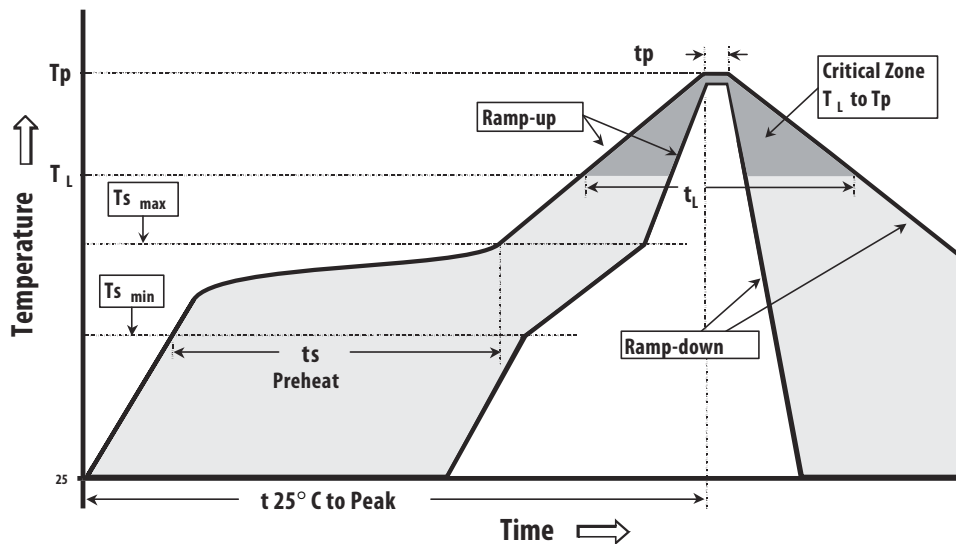


Figure 17. Surface Mount Assembly Profile.

Lead-Free Reflow Profile Recommendation (IPC/JEDEC J-STD-020C)

Reflow Parameter	Lead-Free Assembly
Average ramp-up rate (Liquidus Temperature ($T_{S(max)}$) to Peak)	3°C/second max
Preheat	Temperature Min ($T_{S(min)}$)
	Temperature Max ($T_{S(max)}$)
	Time (min to max) (t_s)
$T_{S(max)}$ to T_L Ramp-up Rate	3°C/second max
Time maintained above:	Temperature (T_L)
	Time (t_L)
Peak Temperature (T_P)	260 +0/-5°C
Time within 5 °C of actual Peak temperature (t_p)	20-40 seconds
Ramp-down Rate	6°C/second max
Time 25 °C to Peak Temperature	8 minutes max

Note 1: All temperatures refer to topside of the package, measured on the package body surface

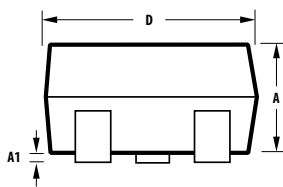
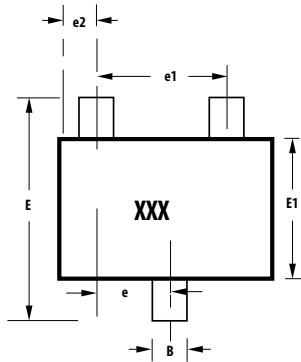
Part Number Ordering Information

Part Number	No. of Devices	Container
HSMS-285x-TR2G	10000	13" Reel
HSMS-285x-TR1G	3000	7" Reel
HSMS-285x-BLK G	100	antistatic bag

where x = 0, 2, 5, B, C, L and P for HSMS-285x.

Package Dimensions

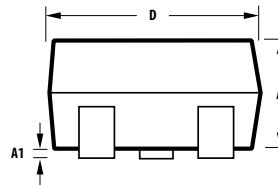
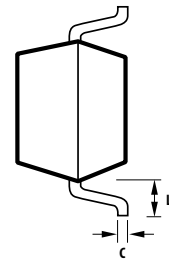
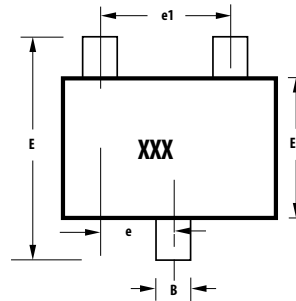
Outline 23 (SOT-23)



Notes:
XXX-package marking
Drawings are not to scale

SYMBOL	DIMENSIONS (mm)	
	MIN.	MAX.
A	0.79	1.20
A1	0.000	0.100
B	0.30	0.54
C	0.08	0.20
D	2.73	3.13
E1	1.15	1.50
e	0.89	1.02
e1	1.78	2.04
e2	0.45	0.60
E	2.10	2.70
L	0.45	0.69

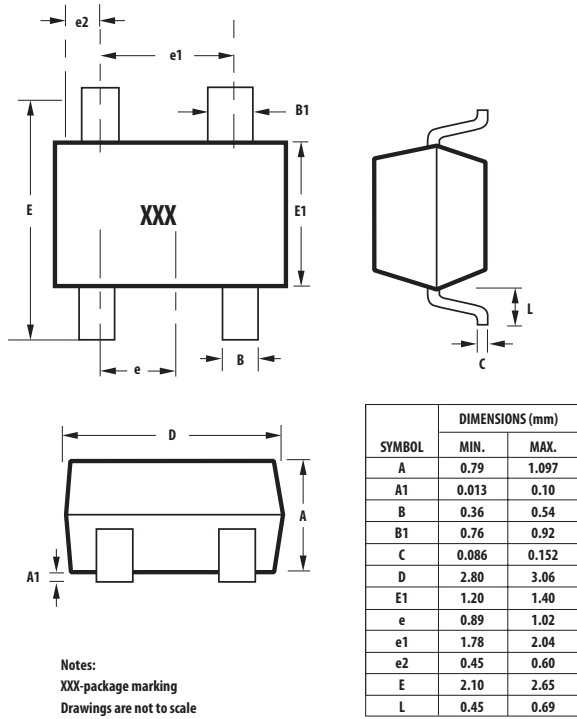
Outline SOT-323 (SC-70 3 Lead)



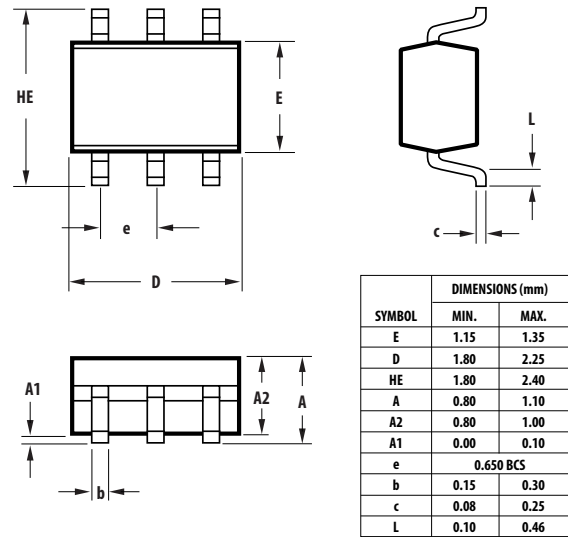
Notes:
XXX-package marking
Drawings are not to scale

SYMBOL	DIMENSIONS (mm)	
	MIN.	MAX.
A	0.80	1.00
A1	0.00	0.10
B	0.15	0.40
C	0.08	0.25
D	1.80	2.25
E1	1.10	1.40
e	0.65 typical	
e1	1.30 typical	
E	1.80	2.40
L	0.26	0.46

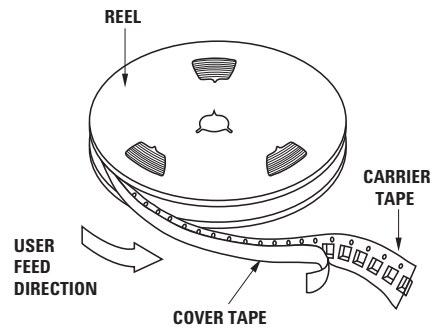
Outline 143 (SOT-143)



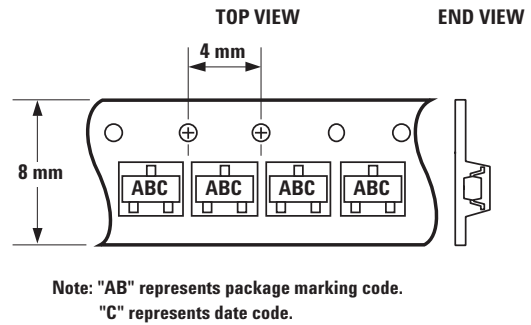
Outline SOT-363 (SC-70 6 Lead)



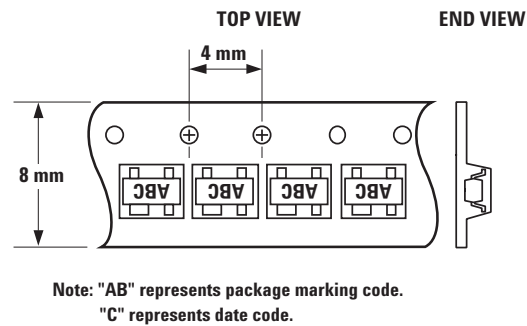
Device Orientation



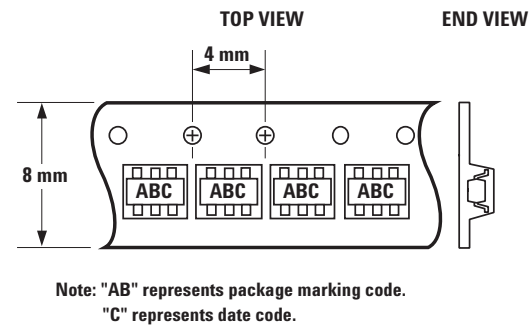
For Outlines SOT-23, -323



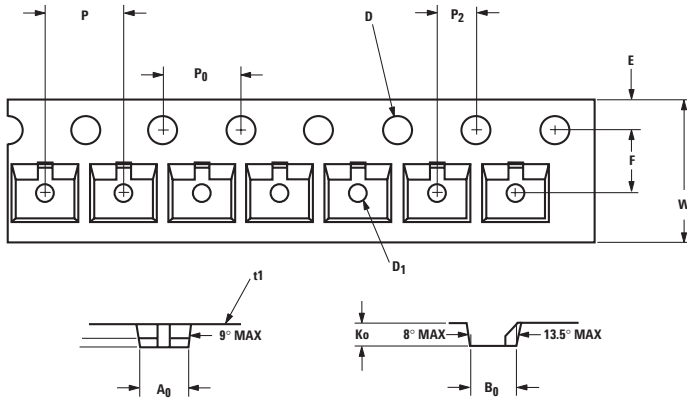
For Outline SOT-143



For Outline SOT-363

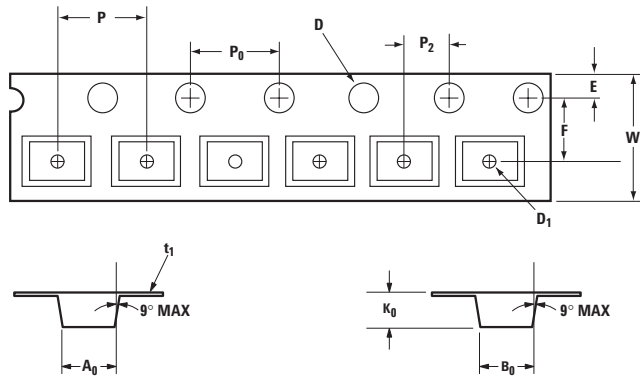


Tape Dimensions and Product Orientation For Outline SOT-23



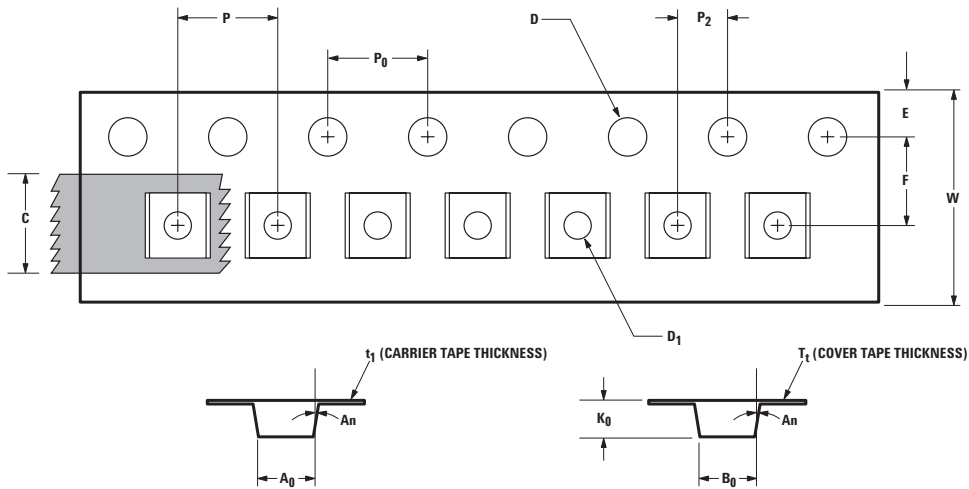
DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	3.15 ± 0.10	0.124 ± 0.004
	WIDTH	B_0	2.77 ± 0.10	0.109 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 ± 0.05	0.039 ± 0.002
PERFORATION	DIAMETER	D	1.50 ± 0.10	0.059 ± 0.004
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	$8.00 \pm 0.30 - 0.10$	$0.315 \pm 0.012 - 0.004$
	THICKNESS	t_1	0.229 ± 0.013	0.009 ± 0.0005
DISTANCE BETWEEN CENTERLINE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

For Outline SOT-143



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	3.19 ± 0.10	0.126 ± 0.004
	WIDTH	B_0	2.80 ± 0.10	0.110 ± 0.004
	DEPTH	K_0	1.31 ± 0.10	0.052 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 ± 0.25	0.039 ± 0.010
PERFORATION	DIAMETER	D	1.50 ± 0.10	0.059 ± 0.004
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	$8.00 \pm 0.30 - 0.10$	$0.315 \pm 0.012 - 0.004$
	THICKNESS	t_1	0.254 ± 0.013	0.0100 ± 0.0005
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

Tape Dimensions and Product Orientation For Outlines SOT-323, -363



	DESCRIPTION	SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.40 ± 0.10	0.094 ± 0.004
	WIDTH	B_0	2.40 ± 0.10	0.094 ± 0.004
	DEPTH	K_0	1.20 ± 0.10	0.047 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	$1.00 + 0.25$	$0.039 + 0.010$
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.254 ± 0.02	0.0100 ± 0.0008
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_1	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002
ANGLE	FOR SOT-323 (SC70-3 LEAD) FOR SOT-363 (SC70-6 LEAD)	A_n	8°C MAX 10°C MAX	

For product information and a complete list of distributors, please go to our web site: www.avagotech.com

Avago, Avago Technologies, and the A logo are trademarks of Avago Technologies in the United States and other countries. Data subject to change. Copyright © 2005-2009 Avago Technologies. All rights reserved. Obsoletes 5989-4022EN AV02-1377EN - May 29, 2009

AVAGO
TECHNOLOGIES