STLC2411

BLUETOOTH™ BASEBAND

PRELIMINARY DATA

1 FEATURES

- Pin to pin compatible with the previous version STLC2410B
- Ericsson Technology Licensing Baseband Core (EBC)
- Bluetooth™ specification compliance: V1.1 and V1.2
- Point-to-point, point-to-multi-point (up to 7 slaves) and scatternet capability
- Asynchronous Connection Oriented (logical transport) link
- Synchronous Connection Oriented (SCO) links: 2 simultaneous SCO channels
- Supports Pitch-Period Error Concealment (PPEC)
  - Improves speech quality in the vicinity of interference
  - Improves coexistence with WLAN
  - Works at receiver, no Bluetooth implication
- Adaptive Frequency Hopping (AFH): hopping kernel, channel assessment as Master and as Slave
- Faster Connection: Interlaced scan for Page and Inquiry scan, first FHS without random backoff, RSSI used to limit range
- Extended SCO (eSCO) links
- Standard BlueRF bus interface
- QoS Flush
- Clock support
  - System clock input: any integer value from 12 … 33 MHz
  - LPO clock input at 3.2 and 32 kHz or via the embedded 32 kHz crystal oscillator cell
- ARM7TDMI 32-bit CPU
- Memory organization
  - 64KByte on-chip RAM
  - 4KByte on-chip boot ROM
  - Programmable external memory interface (EMI)
    - Supports byte and half word access
    - Supports up to 3 external RAM banks (1 Mbyte/ bank)
    - Supports up to 2 Mbyte external flash memory
- Low power architecture with 2 different low power levels:
  - Sleep Mode
  - Deep Sleep Mode
- HW support for packet types
  - ACL: DM1, 3, 5 and DH1, 3, 5
  - SCO: HV1, 3 and DV
  - eSCO: EV3, 5
- Communication interfaces
  - Synchronous Serial Interface, supporting up to 32 bit data and different industry standards
  - Two enhanced 16550 UARTs with 128 byte FIFO depth
  - 12Mbps USB interface
  - Fast master I2C bus interface
  - Multi slot PCM interface
  - 16 programmable GPIOs
  - 2 external interrupts and various interrupt possibilities through other interfaces
- Ciphering support for up to 128-bit key
- Efficient support for WLAN coexistence in collocated scenario
- Receiver Signal Strength Indication (RSSI) support for power-controlled links
- Separate control for external power amplifier (PA) for class1 power support.
- Software support
  - Low level (up to HCI) stack or embedded stack with profiles
  - Support of UART and USB HCI transport layers
- Compliant to automotive specification AEC-Q100

Figure 1. Package

TFBGA132 (8x8x1.2mm)

Table 1. Order Codes

Part Number	Package	Temp. Range
STLC2411	TFBGA132	-40 to +85 °C

1.1 Applications Features

Typical applications in which the STLC2411 can be used are:

- Portable computers, PDA
- Modems
- Handheld data transfer devices
- Cameras
- Computer peripherals
- Other type of devices that require the wireless communication provided by Bluetooth™
- Cable replacement

2 DESCRIPTION

The STLC2411 offers a compact and complete solution for short-range wireless connectivity. It incorporates all the lower layer functions of the Bluetooth™ protocol. The microcontroller allows the support of all data packets of Bluetooth™ in addition to voice. The embedded controller can be used to run the Bluetooth™ protocol and application layers if required. The software is located in an external memory accessed through the external memory interface.

3 QUICK REFERENCE DATA

3.1 Absolute Maximum Ratings

Operation of the device beyond these conditions is not guaranteed.
Sustained exposure to these limits will adversely affect device reliability.

Table 2. Absolute Maximum Ratings

Symbol	Conditions	Min	Max	Unit
V_{DD}	Supply voltage core	V_{SS} - 0.5	2.5	V
V_{DDIO}	Supply voltage I/O		4	V
V_{IN}	Input voltage on any digital pin	V_{SS} - 0.5	V_{DDIO} + 0.3	V
T_{stg}	Storage temperature	-65	+150	°C
T_{lead}	Lead temperature < 10s		+250	°C

3.2 Operating Ranges

Operating ranges define the limits for functional operation and parametric characteristics of the device. Functionality outside these limits is not implied.

Table 3. Operating Ranges

Symbol	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage digital core and emi pads	1.55	1.8	1.95	V
V_{DDIO_RADIO}	Supply voltage radio interface (Values are given for the STLC2150 BT radio.)	2.7	3.3	3.6	V
V_{DDIO}	Supply voltage digital IO	1.65	3.3	3.6	V
T_{amb}	Operating ambient temperature	-40		+85	°C

3.3 I/O specifications

Depending on the interface, the I/O voltage is typical 1.8V (interface to the flash memory) or typical 3.3V (all the other interfaces). These I/Os comply with the EIA/JEDEC standard JESD8-B.

3.3.1 Specifications for 3.3V I/Os

Table 4. LVTTL DC Input Specification (3V<V_{DDIO}<3.6V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{il}	Low level input voltage				0.8	V
V_{ih}	High level input voltage		2			V
V_{hyst}	Schmitt trigger hysteresis		0.4			V

Table 5. LVTTL DC Output Specification (3V<V_{DDIO}<3.6V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ol}	Low level output voltage	I_{ol} = X mA			0.15	V
V_{oh}	High level output voltage	I_{oh} =-X mA	V_{DDIO}-0.15			V

Note: X is the source/sink current under worst-case conditions according to the drive capability. (See table 8, pad information for value of X).

3.3.2 Specifications for 1.8V I/Os

Table 6. DC Input Specification (1.55V<V_{DD}<1.95V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{il}	Low level input voltage				0.35*V_{DD}	V
V_{ih}	High level input voltage		0.65*V_{DD}			V
V_{hyst}	Schmitt trigger hysteresis		0.2	0.3	0.5	V

Table 7. DC Output Specification (1.55V<V_{DD}<1.95V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ol}	Low level output voltage	I_{ol} = X mA			0.15	V
V_{oh}	High level output voltage	I_{oh} =-X mA	V_{DD}-0.15			V

Note: X is the source/sink current under worst-case conditions according to the drive capability. (See table 8, pad information for value of X).

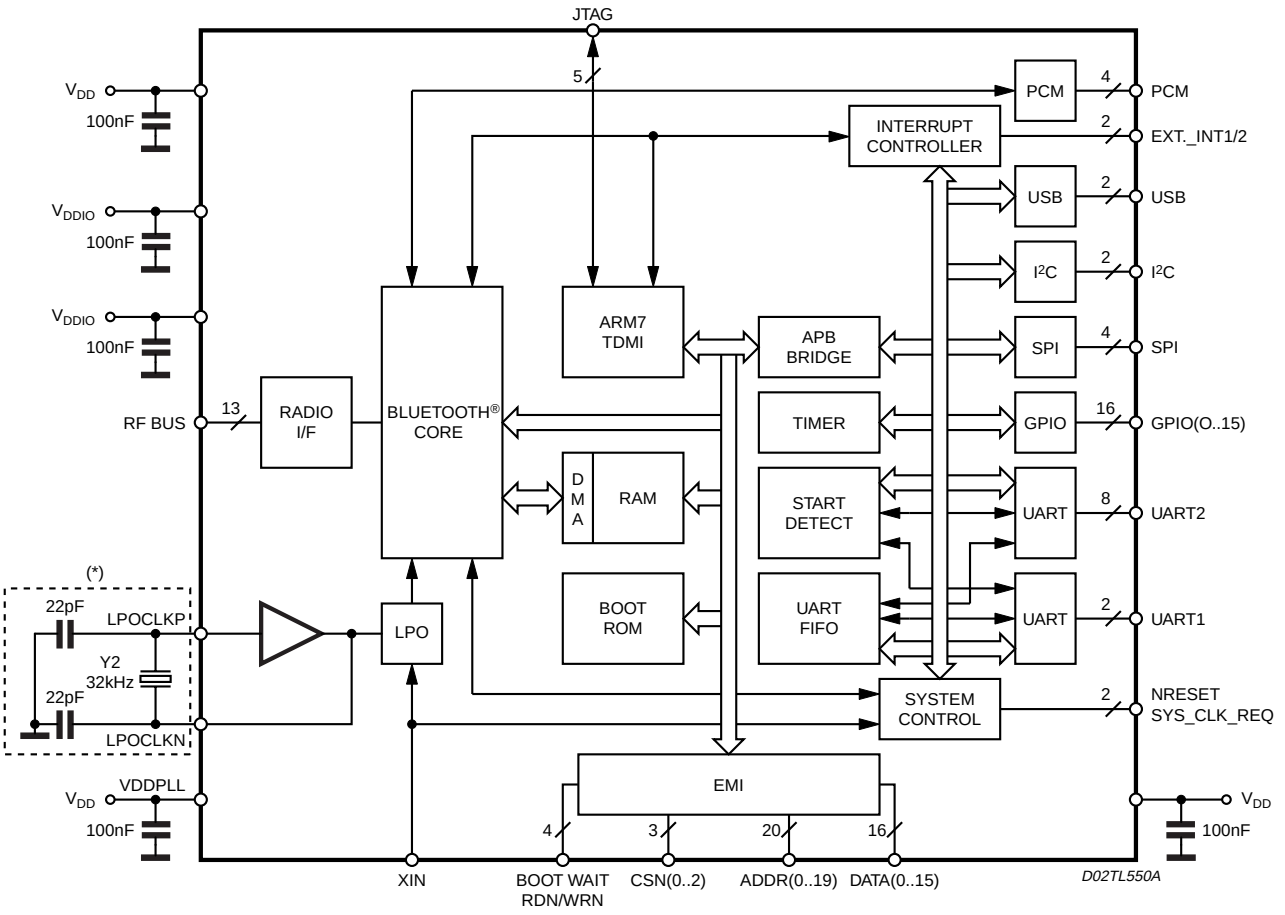
3.4 Current Consumption

Table 8. Typical power consumption of the STLC2411 and External STM Flash (M28R400CB) using UART (VDD = VDD Flash = PLLVDD = 1.8V, VDDIO = 3.3V) (Indicative only)

STLC2411 State	Core		IO	Unit
	Slave	Master		
Standby (no low power mode)	5.10	5.10	0.13	mA
Standby (low power mode enabled)	0.94	0.94	0.13	mA
ACL connection (no transmission)	7.60	6.99	0.13	mA
ACL connection (data transmission)	7.90	7.20	0.13	mA
SCO connection (no codec connected)	8.70	7.90	0.14	mA
Inquiry and Page scan (low power mode enabled)	127	n.a.	5	µA
Low Power mode (32 kHz crystal)	20	20	0	µA

4 BLOCK DIAGRAM AND ELECTRICAL SCHEMA

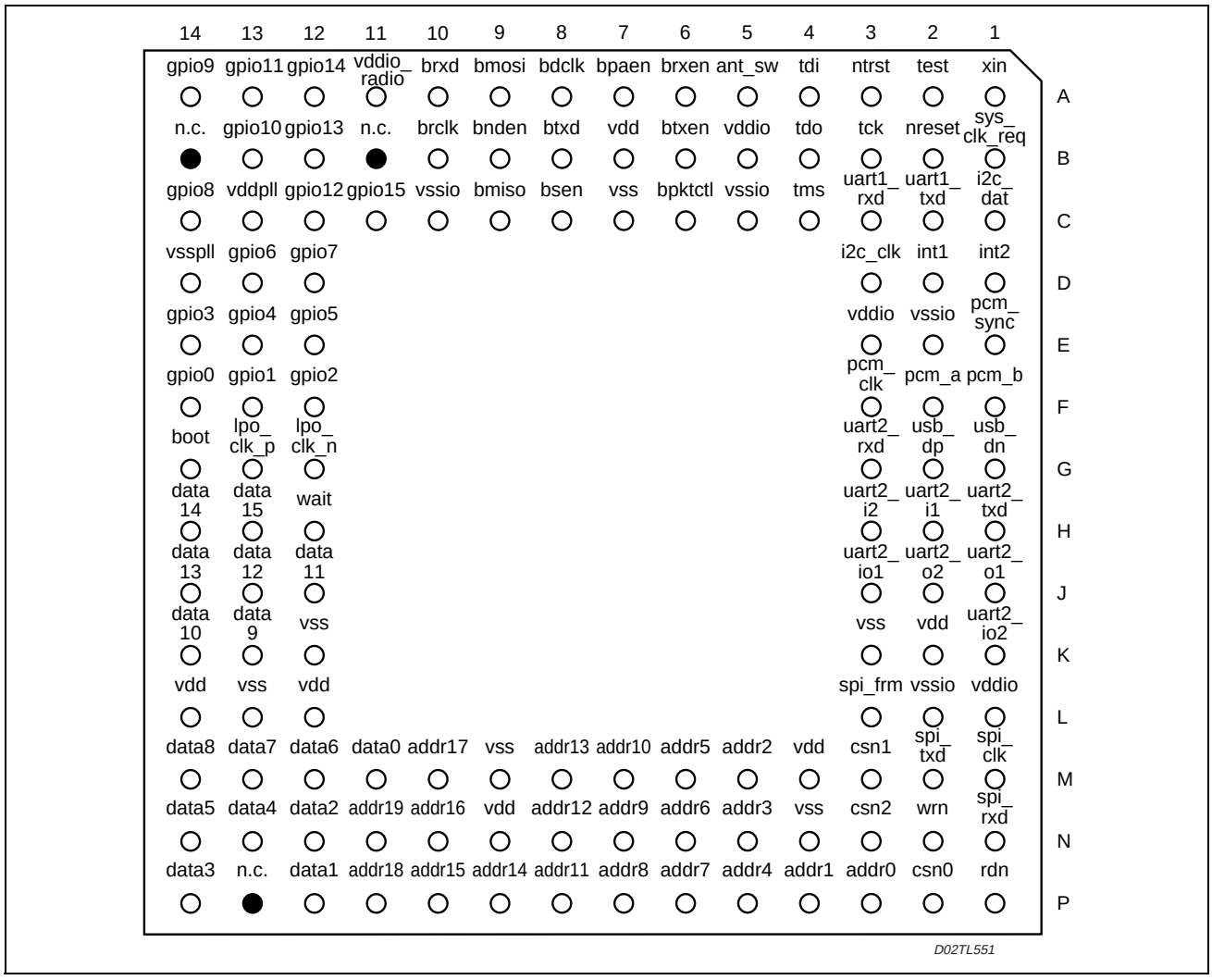
Figure 2. Block Diagram and Electrical Schematic



(*) If a low-power clock is available, it can be connected to the LPOCLKP pin in stead of using a crystal

5 PINOUT

Figure 3. Pin out (Bottom view)



5.1 Pin Description and Assignment

Table 9 shows the pin list of the STLC2411. There are 107 digital functional pins and 22 supply pins. The column "PU/PD" shows the pads implementing an internal weak pull-up/down, to fix value if the pin is left open. This cannot replace an external pull-up/down.

The pads are grouped according to three different power supply values, as shown in column "VDD":

- V1 for 3.3 V typical 1.65 - 3.6 V range
- V1_radio for 3.3 V typical 2.7 - 3.6 V range (for STLC2150 BT radio)
- V2 for 1.8 V typical 1.55 - 1.95 V range

Note:
V1 and V1_radio can be connected together to the same 3.3 V typical supply for STLC2150 BT radio.

Finally the column "DIR" describes the pin directions:

- I for Inputs
- O for Outputs
- I/O for Input/Outputs
- O/t for tri-state outputs

Table 9. STLC2411 Pin List

Name	Pin #	Description	DIR	PU/PD	VDD	PAD
Interface to external memory (supports up to 2 Mbyte Flash and byte access for up to1 Mbyte RAM.)						
int1	D2	External Interrupt used also as external wakeup	I	(1)	V1	CMOS, 3.3V TTL compatible schmitt trigger
int2	D1	Second external interrupt	I	(1)		
boot	G14	Select external boot from EMI or internal from ROM	I	(1)	V2	CMOS 1.8V
wait	H12	EMI external wait signal (left open)	I	PD		
rdn	P1	External read	O		V2	CMOS 1.8V 4mA slew rate control
wrn	N2	External write	O			
csn0	P2	External chip select bank 0	O			
csn1	M3	External chip select bank 1	O			
csn2	N3	External chip select bank 2	O			
addr0	P3	External address bit 0	O			
addr1	P4	External address bit 1	O			
addr2	M5	External address bit 2	O			
addr3	N5	External address bit 3	O			
addr4	P5	External address bit 4	O			
addr5	M6	External address bit 5	O			
addr6	N6	External address bit 6	O			
addr7	P6	External address bit 7	O			
addr8	P7	External address bit 8	O			
addr9	N7	External address bit 9	O			
addr10	M7	External address bit 10	O			
addr11	P8	External address bit 11	O			
addr12	N8	External address bit 12	O			
addr13	M8	External address bit 13	O			
addr14	P9	External address bit 14	O			
addr15	P10	External address bit 15	O			
addr16	N10	External address bit 16	O			
addr17	M10	External address bit 17	O			
addr18	P11	External address bit 18	O			
addr19	N11	External address bit 19	O			
data0	M11	External data bit 0	I/O	PD	V2	CMOS 1.8V 4mA slew rate control
data1	P12	External data bit 1	I/O	PD		
data2	N12	External data bit 2	I/O	PD		
data3	P14	External data bit 3	I/O	PD		
data4	N13	External data bit 4	I/O	PD		
data5	N14	External data bit 5	I/O	PD		

Table 9. STLC2411 Pin List (continued)

Name	Pin #	Description	DIR	PU/PD	VDD	PAD
data6	M12	External data bit 6	I/O	PD	V2	CMOS 1.8V 4mA slew rate control
data7	M13	External data bit 7	I/O	PD		
data8	M14	External data bit 8	I/O	PD		
data9	K13	External data bit 9	I/O	PD		
data10	K14	External data bit 10	I/O	PD		
data11	J12	External data bit 11	I/O	PD		
data12	J13	External data bit 12	I/O	PD		
data13	J14	External data bit 13	I/O	PD		
data14	H14	External data bit 14	I/O	PD		
data15	H13	External data bit 15	I/O	PD		
SPI interface						
spi_frm	L3	Synchronous Serial Interface frame sync	I/O		V1	CMOS, 3.3V TTL compatible, 2mA tri-state slew rate control schmitt trigger
spi_clk	M1	Synchronous Serial Interface clock	I/O			
spi_txd	M2	Synchronous Serial Interface transmit data	O/t		V1	CMOS, 3.3V TTL compatible, 2mA slew rate control
spi_rxd	N1	Synchronous Serial Interface receive data	I	(1)	V1	CMOS, 3.3V TTL compatible schmitt trigger
UART interface						
uart1_txd	C2	Uart1 transmit data	O/t		V1	CMOS, 3.3V TTL compatible, 2mA slew rate control
uart1_rxd	C3	Uart1 receive data	I	(2)	V1	CMOS, 3.3V TTL compatible schmitt trigger
uart2_o1	J1	Uart2 modem output	O		V1	CMOS, 3.3V TTL compatible, 2mA slew rate control
uart2_o2	J2	Uart2 modem output	O/t		V1	CMOS, 3.3V TTL compatible, 2mA slew rate control
uart2_i1	H2	Uart2 modem input	I	(2)	V1	CMOS, 3.3V TTL compatible
uart2_i2	H3	Uart2 modem input	I	(2)	V1	
uart2_io1	J3	Uart2 modem input/output	I/O	(2)	V1	CMOS, 3.3V TTL compatible, 2mA tri-state slew rate control
uart2_io2	K1	Uart2 modem input/output	I/O	(2)	V1	
uart2_txd	H1	Uart2 transmit data	O/t		V1	CMOS, 3.3V TTL compatible, 2mA slew rate control

Table 9. STLC2411 Pin List (continued)

Name	Pin #	Description	DIR	PU/PD	VDD	PAD
uart2_rxd	G3	Uart2 receive data	I	(2)	V1	CMOS, 3.3V TTL compatible
I2C interface						
i2c_dat	C1	I2C data pin	I/O	(3)	V1	CMOS, 3.3V TTL compatible, 2mA tri-state slew rate control
i2c_clk	D3	I2C clock pin	I/O	(3)	V1	
USB interface						
usb_dn	G1	USB - pin (Needs a series resistor of 27 Ω ±5%)	I/O	(1)	V1	
usb_dp	G2	USB + pin (Needs a series resistor of 27 Ω ±5%)	I/O	(1)	V1	
GPIO interface						
gpio0	F14	Gpio port 0	I/O	PU	V1	CMOS, 3.3V TTL compatible, 4mA tri-state slew rate control
gpio1	F13	Gpio port 1	I/O	PU		
gpio2	F12	Gpio port 2	I/O	PU		
gpio3	E14	Gpio port 3	I/O	PU	V1	CMOS, 3.3V TTL compatible, 4mA tri-state slew rate control schmitt trigger
gpio4	E13	Gpio port 4	I/O	PU	V1	CMOS, 3.3V TTL compatible, 4mA tri-state slew rate control
gpio5	E12	Gpio port 5	I/O	PU		
gpio6	D13	Gpio port 6	I/O	PU		
gpio7	D12	Gpio port 7	I/O	PU		
gpio8	C14	Gpio port 8	I/O	PU	V1	CMOS, 3.3V TTL compatible, 2mA tri-state slew rate control
gpio9	A14	Gpio port 9	I/O	PU		
gpio10	B13	Gpio port 10	I/O	PU		
gpio11	A13	Gpio port 11	I/O	PU		
gpio12	C12	Gpio port 12	I/O	PU		
gpio13	B12	Gpio port 13	I/O	PU		
gpio14	A12	Gpio port 14	I/O	PU		
gpio15	C11	Gpio port 15	I/O	PU		
Clock and test pins						
xin	A1	System clock	I		V1	CMOS, 3.3V TTL compatible schmitt trigger
nreset	B2	Reset	I			
sys_clk_req	B1	System clock request	I/O		V1	CMOS, 3.3V TTL compatible, 2mA tri-state slew rate control
lpo_clk_p	G13	Low power oscillator + / Slow clock input	I	(1)	V2	
lpo_clk_n	G12	Low power oscillator -	O			

Table 9. STLC2411 Pin List (continued)

Name	Pin #	Description	DIR	PU/PD	VDD	PAD
test	A2	Test mode	I	PD	V1	CMOS, 3.3V TTL compatible
JTAG interface						
ntrst	A3	JTAG pin	I	PD	V1	CMOS, 3.3V TTL compatible
tck	B3	JTAG pin	I	(1)	V1	CMOS, 3.3V TTL compatible schmitt trigger
tms	C4	JTAG pin	I	PU	V1	CMOS, 3.3V TTL compatible
tdi	A4	JTAG pin	I	PU		
tdo	B4	JTAG pin (should be left open)	O/t		V1	CMOS, 3.3V TTL compatible, 2mA slew rate control
PCM interface						
pcm_a	F2	PCM data	I/O	PD	V1	CMOS, 3.3V TTL compatible, 2mA tri-state slew rate control
pcm_b	F1	PCM data	I/O	PD		
pcm_sync	E1	PCM 8kHz sync	I/O	PD		
pcm_clk	F3	PCM clock	I/O	PD	V1	CMOS, 3.3V TTL compatible, 2mA tri-state slew rate control schmitt trigger
Radio interface						
brclk	B10	Transmit clock	I	(1)	V1_radio	CMOS, 3.3V TTL compatible schmitt trigger
brxd	A10	Receive data	I			
bmiso	C9	RF serial interface input data	I	(1)	V1_radio	CMOS, 3.3V TTL compatible
bnden	B9	RF serial interface control	O		V1_radio	CMOS, 3.3V TTL compatible, 2mA slew rate control
bmosi	A9	RF serial interface output data	O			
bdclk	A8	RF serial interface clock	O			
btxd	B8	Transmit data	O			
bsen	C8	Synthesizer ON	O			
bpaen	A7	Open PLL	O			
brxen	A6	Receive ON	O			
btxen	B6	Transmit ON	O			
bpktctl	C6	Packet ON	O			
ant_sw	A5	Antenna switch	O		V1_radio	CMOS, 3.3V TTL compatible, 8mA slew rate control

(1) Should be strapped to vssio if not used
(2) Should be strapped to vddio if not used
(3) Must have a 10 kOhm pull-up.

Table 9. Pin List (continued)

Name	Pin #	Description
Power Supply		
vsspll	D14	PLL ground
vddpll	C13	1.8V supply for PLL
vdd	B7	1.8V Digital supply
vdd	K2	1.8V Digital supply
vdd	L12	1.8V Digital supply
vdd	L14	1.8V Digital supply
vdd	M4	1.8V Digital supply
vdd	N9	1.8V Digital supply
vddio_radio	A11	3.3V Supply voltage radio interface
vddio	B5	3.3V Supply voltage digital IO
vddio	E3	
vddio	L1	
vss	C7	Digital ground
vss	K3	Digital ground
vss	K12	Digital ground
vss	L13	Digital ground
vss	M9	Digital ground
vss	N4	Digital ground
vssio	C5	I/O's ground
vssio	C10	I/O's ground
vssio	E2	I/O's ground
vssio	L2	I/O's ground

6 FUNCTIONAL DESCRIPTION

6.1 Baseband

– WLAN coexistence. See also 7.12. WLAN.

6.1.1 Baseband 1.1 Features

The baseband is based on Ericsson Technology Licensing Baseband Core (EBC) and it is compliant with the Bluetooth specification 1.1:

– Point to multipoint (up to 7 Slaves)
– Asynchronous Connection Less (ACL) link support giving data rates up to 721 kbps
– Synchronous Connection Oriented (SCO) link with support for 2 voice channels over the air interface.
– Flexible voice format to host and over the air (CVSD, PCM 13/16 bits, A-law, μ-law)
– HW support for packet types: DM1, 3, 5; DH1, 3, 5; HV1, 3; DV
– Scatternet capabilities (Master in one piconet and Slave in the other one; Slave in two piconets). All scatternet v.1.1 errata supported.
– Ciphering support up to 128 bits key
– Paging modes R0, R1, R2
– Channel Quality Driven Data Rate
– Full Bluetooth software stack available
– Low-level link controller

6.1.2 Baseband 1.2 Features

The baseband part is also compliant with the Bluetooth specification 1.2:

– Extended SCO (eSCO) links: supports EV3 and EV5 packets. See also 7.6. eSCO.
– Adaptive Frequency Hopping (AFH): hopping kernel, channel assessment as Master and as Slave. See also 7.7. AFH.
– Faster Connection: Interlaced scan for Page and Inquiry scan, answer FHS at first reception, RSSI used to limit range. See also 7.8. Faster Connection.
– QoS Flush. See also 7.9. QoS.
– Synchronization: the local and the master BT clock are available via HCI commands for synchronization of parallel applications on different slaves.
– L2CAP Flow & Error control
– LMP Improvements
– LMP SCO handling
– Parameter Ranges update

7 GENERAL SPECIFICATION

7.1 SYSTEM CLOCK

The STLC2411 works with a single clock provided on the XIN pin. The value of this external clock should be any integer value from 12 … 33 MHz ±20ppm (overall).

7.1.1 SLOW CLOCK

The slow clock is used by the baseband as reference clock during the low power modes. The slow clock requires an accuracy of ±250ppm (overall).
Several options are foreseen in order to adjust the STLC2411 behaviour according to the features of the radio used:

– If the system clock (e.g. 13MHz) is not provided at all times (power consumption saving) and no slow clock is provided by the system, a 32 kHz crystal must be used by the STLC2411 (default mode).
– If the system clock (e.g. 13MHz) is not provided at all times (power consumption saving) and the system provides a slow clock at 32kHz or 3.2kHz, this signal is simply connected to the STLC2411 (lpo_clk_p).
– If the system clock (e.g. 13MHz) is provided at all times, the STLC2411 generates from the reference clock an internal 32kHz clock. This mode is not an optimized mode for power consumption.

7.2 BOOT PROCEDURE

The boot code instructions are the first that ARM7TDMI executes after a HW reset. All the internal device's registers are set to their default value.

There are 2 types of boot:

– External memory boot.

When boot pin is set to `1` (connected to VDD), the STLC2411 boots on its external memory

– UART download boot from ROM.

When boot pin is set to `0` (connected to GND), the STLC2411 boots on its internal ROM (needed to download the new firmware in the external memory).

When booting on the internal ROM, the STLC2411 will monitor the UART interface for approximately 1.4 second. If there is no request for code downloading during this period, the ROM jumps to external memory.

7.3 CLOCK DETECTION

The STLC2411 has an automatic slow clock frequency detection (32kHz, 3.2kHz or none).

7.4 MASTER RESET

When the device's reset is held active (nreset is low), uart1_txd and uart2_txd are set to input state. When the nreset returns high, the device starts to boot.

Remark: The device should be held in active reset for minimum 20ms in order to guarantee a complete reset of the device.

7.5 INTERRUPTS/WAKE-UP

All GPIOs can be used both as external interrupt source and as wake-up source. In addition, the chip can be woken-up by USB, uart1_rxd, uart2_rxd, int1, int2.

7.6 V1.2 detailed functionality - Extended SCO

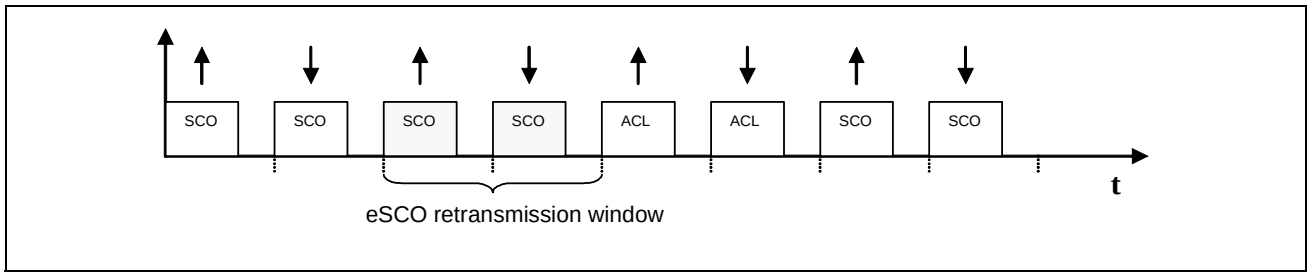
User Perspective - Extended SCO

This function gives improved voice quality since it enables the possibility to retransmit lost or corrupted voice packets in both directions.

Technical perspective - Extended SCO

eSCO incorporates CRC, negotiable data rate, negotiable retransmission window and multi-slot packets. Retransmission of lost or corrupted packets during the retransmission window guarantees on-time delivery.

Figure 4. eSCO



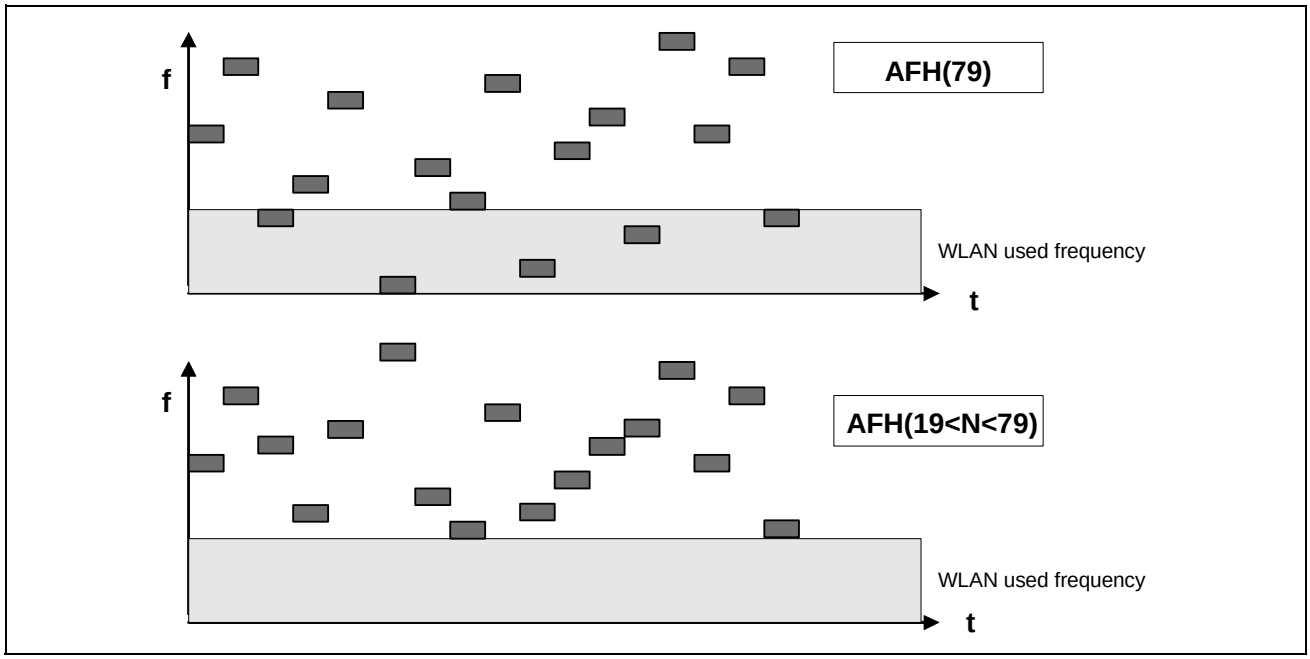
7.7 V1.2 detailed functionality - Adaptive Frequency Hopping

User Perspective - Adaptive Frequency Hopping

In the Bluetooth spec 1.1 the Bluetooth devices hop in the 2.4 GHz band over 79-channels. Since WLAN 802.11 has become popular, there are specification improvements in the 1.2-SIG spec for Bluetooth where the Bluetooth units can avoid the jammed bands and thereby provide an improved co-existence with WLAN.

Technical perspective - Adaptive Frequency Hopping

Figure 5. AFH



First the Master and/or the Slaves identify the jammed channels. The Master decides on the channel distribution and informs the involved slaves. The Master and the Slaves, at a predefined instant, switch to the new channel distribution scheme.

No longer jammed channels are re-inserted into the channel distribution scheme. AFH uses the same hop frequency for transmission as for reception.

7.8 V1.2 detailed functionality - Faster Connection

User Perspective - Faster Connection

This feature gives the User about 65% faster connection on average when enabled compared to Bluetooth spec 1.1 connection procedure.

Technical perspective - Faster Connection

The faster Inquiry functionality is based on a removed/shortened random back off and also a new Interlaced Inquiry scan scheme.

The faster Page functionality is based on Interlaced Page Scan.

7.9 V1.2 detailed functionality - Quality of Service

User Perspective - Quality of Service

Small changes to the BT1.1 spec regarding Quality of Service makes a large difference by allowing all QoS parameters to be communicated over HCI to the link manager that enables efficient BW management. Here after a short list of user perspectives:

1) Flush timeout: enables time-bounded traffic such as video streaming to become more robust when the channel degrades. It sets the maximum delay of an L2CAP frame. It does not enable multiple streams in one piconet, or heavy data transfer at the same time.
2) Simple latency control: allows the host to set the poll interval. Provides enough support for HID devices mixed with other traffic in the piconet.

7.10 Low power modes

To save power, two low power modes are supported. Depending of the Bluetooth and of the Host's activity, the STLC2411 autonomously decides to use Sleep Mode or Deep Sleep Mode.

Table 10. Low power modes

Low power mode	Description
Sleep Mode	The STLC2411: - Accepts HCI commands from the Host. - Supports page- and inquiry scans. - Supports Bluetooth links that are in Sniff, Hold or Park. - Can transfer data over Bluetooth links. - The system clock is still active in part of the design.
Deep Sleep Mode	The STLC2411: - Does not accept HCI commands from the Host. - Keeps track of page- and inquiry scan activities. Switches between sleep and active mode when it is time to scan. - Supports Bluetooth links that are in Sniff, Hold or Park. - Does not transfer data over Bluetooth links. - The system clock is not active in any part of the design. Note: Deep Sleep mode is not compatible with a USB transport layer.

Some examples of the low power modes usage:

7.10.1 SNIFF OR PARK

The STLC2411 is in active mode with a Bluetooth connection, once the connection is concluded the SNIFF or the PARK is programmed. Once one of these two states is entered the STLC2411 goes in Sleep Mode. After that, the Host may decide to place the STLC2411 in Deep Sleep Mode by putting the UART LINK in low power mode. The Deep Sleep Mode allows smaller power consumption. When the STLC2411 needs to send or receive a packet (e.g. at T_{SNIFF} or at the beacon instant) it will require the clock and it will go in active mode for the needed transmission/reception. Immediately afterwards it will go back to the Deep

Sleep Mode. If some HCI transmission is needed, the UART link will be reactivated, using one of the two ways explained in 7.5, and the STLC2411 will move from the Deep Sleep Mode to the Sleep Mode.

7.10.2 INQUIRY/PAGE SCAN

When only inquiry scan or page scan is enabled, the STLC2411 will go in Sleep Mode or Deep Sleep Mode outside the receiver activity. The selection between Sleep Mode and Deep Sleep Mode depend on the UART activity like in SNIFF or PARK.

7.10.3 NO CONNECTION

If the Host places the UART in low power and there is no activity, then the STLC2411 can be placed in Deep Sleep Mode.

7.10.4 ACTIVE LINK

When there is an active link (SCO or ACL), the STLC2411 cannot go in Deep Sleep Mode whatever the UART state is. But the STLC2411 baseband is made such that whenever it is possible, depending on the scheduled activity (number of link, type of link, amount of data exchanged), it goes in Sleep Mode.

7.11 SW initiated low power mode

A wide set of wake up mechanisms are supported.

7.12 Bluetooth - WLAN coexistence in collocated scenario

The coexistence interface uses 4 GPIO pins, when enabled.

Bluetooth and WLAN 802.11 b/g technologies occupy the same 2.4 GHz ISM band. STLC2411 implements a set of mechanisms to avoid interference in a collocated scenario.

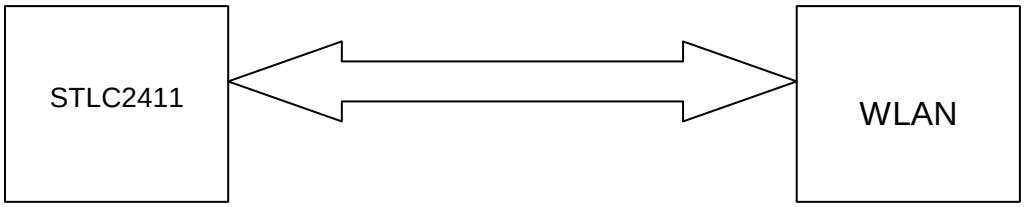
The STLC2411 supports 5 different algorithms in order to provide efficient and flexible simultaneous functionality between the two technologies in collocated scenarios:

- **Algorithm 1:** PTA (Packet Traffic Arbitration) based coexistence algorithm defined in accordance with the IEEE 802.15.2 recommended practice.
- **Algorithm 2:** the WLAN is the master and it indicates to the STLC2411 when not to operate in case of simultaneous use of the air interface.
- **Algorithm 3:** the STLC2411 is the master and it indicates to the WLAN chip when not to operate in case of simultaneous use of the air interface.
- **Algorithm 4:** Two-wire mechanism
- **Algorithm 5:** Alternating Wireless Medium Access (AWMA), defined in accordance with the WLAN 802.11 b/g technologies.

The algorithm is selected via HCI command. The default algorithm is algorithm 1.

7.12.1 Algorithm 1: PTA (Packet Traffic Arbitration)

The Algorithm is based on a bus connection between the STLC2411 and the WLAN chip:



By using this coexistence interface it's possible to dynamically allocate bandwidth to the two devices when simultaneous operations are required while the full bandwidth can be allocated to one of them in case the other one does not require activity. The algorithm involves a priority mechanism, which allows preserving the quality of certain types of link. A typical application would be to guarantee optimal quality to the Blue-

tooth voice communication while an intensive WLAN communication is ongoing.

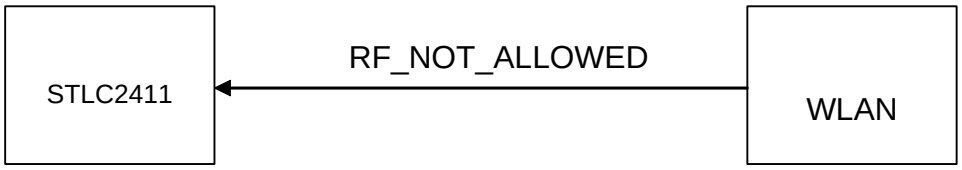
Several algorithms have been implemented in order to provide a maximum of flexibility and efficiency for the priority handling. Those algorithms can be activated via specific HCI commands.

The combination of a time division multiplexing techniques to share the bandwidth in case of simultaneous operations and of the priority mechanism avoid the interference due to packet collision and it allows the maximization of the 2.4 GHz ISM bandwidth usage for both devices while preserving the quality of some critical types of link.

7.12.2 Algorithm 2: WLAN master

In case the STLC2411 has to cooperate, in a collocated scenario, with a WLAN chip not supporting a PTA based algorithm, it's possible to put in place a simpler mechanism.

The interface is reduced to 1 line:

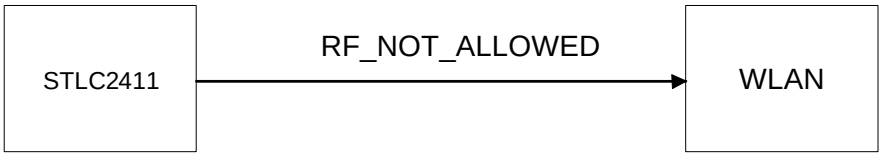


When the WLAN has to operate, it alerts HIGH the RF_NOT_ALLOWED signal and the STLC2411 will not operate while this signals stays HIGH.

This mechanism permits to avoid packet collision in order to make an efficient use of the bandwidth but cannot provide guaranteed quality over the Bluetooth links.

7.12.3 Algorithm 3: Bluetooth master

This algorithm represents the symmetrical case of section 7.12.2. Also in this case the interface is reduced to 1 line:



When the STLC2411 has to operate it alerts HIGH the RF_NOT_ALLOWED signal and the WLAN will not operate while this signals stays HIGH.

This mechanism permits to avoid packet collision in order to make an efficient use of the bandwidth, it provides high quality for all Bluetooth links but cannot provide guaranteed quality over the WLAN links.

7.12.4 Algorithm 4: Two-wire mechanism

Based on algorithm 2 and 3, the Host decides, on a case-by-case basis, whether WLAN or Bluetooth is master.

7.12.5 Algorithm 5: Alternating Wireless Medium Access (AWMA)

AWMA utilizes a portion of the WLAN beacon interval for Bluetooth operations. From a timing perspective, the medium assignment alternates between usage following WLAN procedures and usage following Bluetooth procedures.

The timing synchronization between the WLAN and the STLC2411 is done by the HW signal MEDIUM_FREE.

Table 11. WLAN HW signal assignment

WLAN	Scenario 1: PTA	Scenario 2: WLAN master	Scenario 3: BT master	Scenario 4: 2-wire	Scenario 5: AWMA
WLAN 1	TX_ CONFIRM	BT_RF_NOT_ ALLOWED	Not used	BT_RF_NOT_ ALLOWED	MEDIUM_FREE
WLAN 2	TX_ REQUEST	Not used	WLAN_RF_ NOT_ ALLOWED	WLAN_RF_ NOT_ ALLOWED	Not used
WLAN 3	STATUS	Not used	Not used	Not used	Not used
WLAN 4	OPTIONAL_ SIGNAL	Not used	Not used	Not used	Not used

8 INTERFACES

8.1 UART Interface

The chip contains two enhanced (128 byte transmit FIFO and 128 byte receive FIFO, sleep mode, 127 Rx and 128 Tx interrupt thresholds) UARTs named UART1 and UART2 compatible with the standard M16550 UART.

For UART1, only Rx and Tx signals are available (used for debug purposes).

UART2 features:

– standard HCI UART transport layer:
  – all HCI commands as described in the Bluetooth™ specification 1.1
  – ST specific HCI command (check STLC2411 Software Interface document for more information)
– RXD, TXD, CTS, RTS on permanent external pins
– 128-byte FIFOs, for transmit and for receive
– Default configuration: 57.600 kbps
– Specific HCI command to change to the following baud rates:

Table 12. List of supported baud rates

Baud rate		
–	**57.600 kbps (default)**	4800
921.6k	38.4 k	2400
460.8 k	28.8 k	1800
230.4 k	19.2 k	1200
153.6 k	14.4 k	900
115.2 k	9600	600
76.8 k	7200	300

8.2 Synchronous Serial Interface

The Synchronous Serial Interface (SSI) (or the Synchronous Peripheral Interface (SPI)) is a flexible module supporting full-duplex and half-duplex synchronous communications with external devices in Master and Slave mode. It enables a microcontroller unit to communicate with peripheral devices or allows interprocessor communications in a multiple-master environment. This Interface is compatible with the Motorola SPI standard, with the Texas Instruments Synchronous Serial frame format and with National Semiconductor Microwire standard.

Special extensions are implemented to support the Agilent SPI interface for optical mouse applications and the 32 bit data SPI for stereo codec applications.

8.2.1 Feature description: Agilent mode

One application is a combination of a Bluetooth device with an AGILENT optical mouse sensor to build a Bluetooth Mouse. The AGILENT chip has an SPI interface with one bi-directional data port.

When spi_io from ADNS_2030 is driving, spi_rxd should be active, while spi_txd is set as a tri-state high

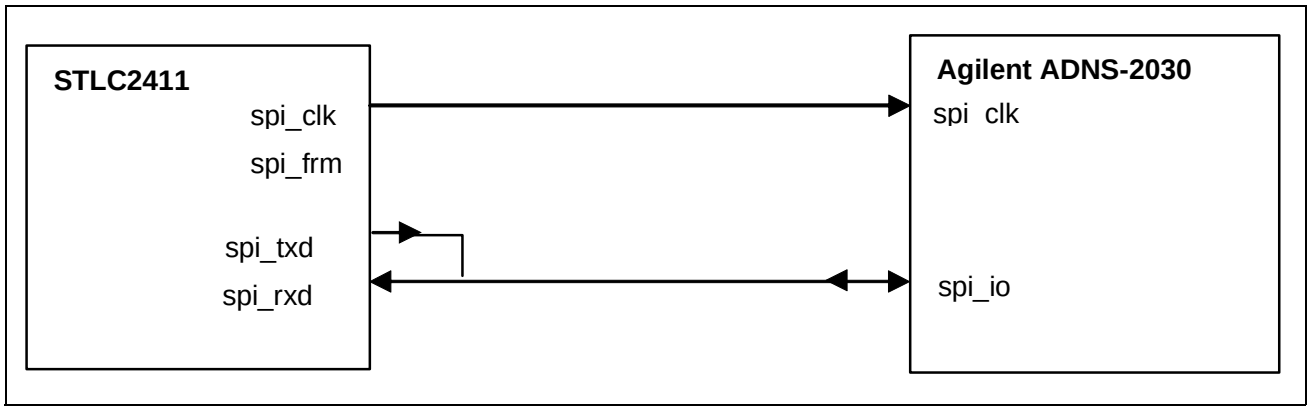
impedance input.

For a read operation, the Bluetooth spi_txd is put in high impedance state after the reception of the address.

Note that this feature works independently of the SPI mode, supporting other combinations.

In this case, the devices are connected as described in the figure below.

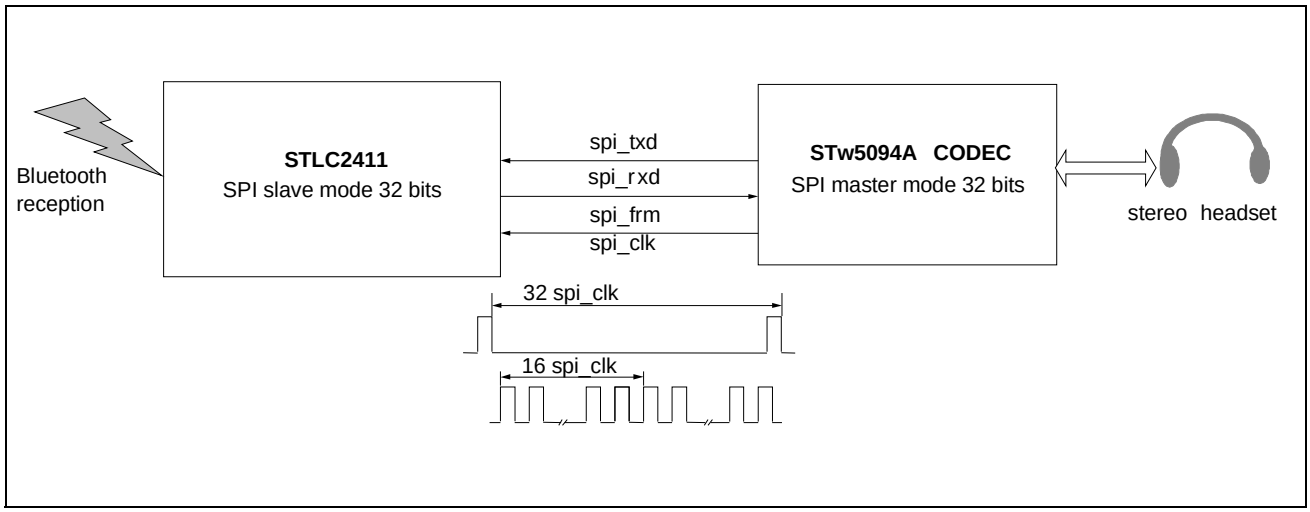
Figure 6.



8.2.2 Feature description: 32 bit SPI

One application is a Bluetooth stereo headset. In this application, the audio samples are received from the emitter through the air using the Bluetooth baseband with ACL packets. The samples are decoded by the embedded ARM CPU (the samples were encoded, for compression, in SBC or MP3 format) and then sent to a stereo codec though the SPI interface. The application is described in the figure below.

Figure 7.



To support this application, the data size is 32 bits. The 32 bits support is implemented for both transmit and receive.

8.3 I2C Interface

Used to access I2C peripherals.

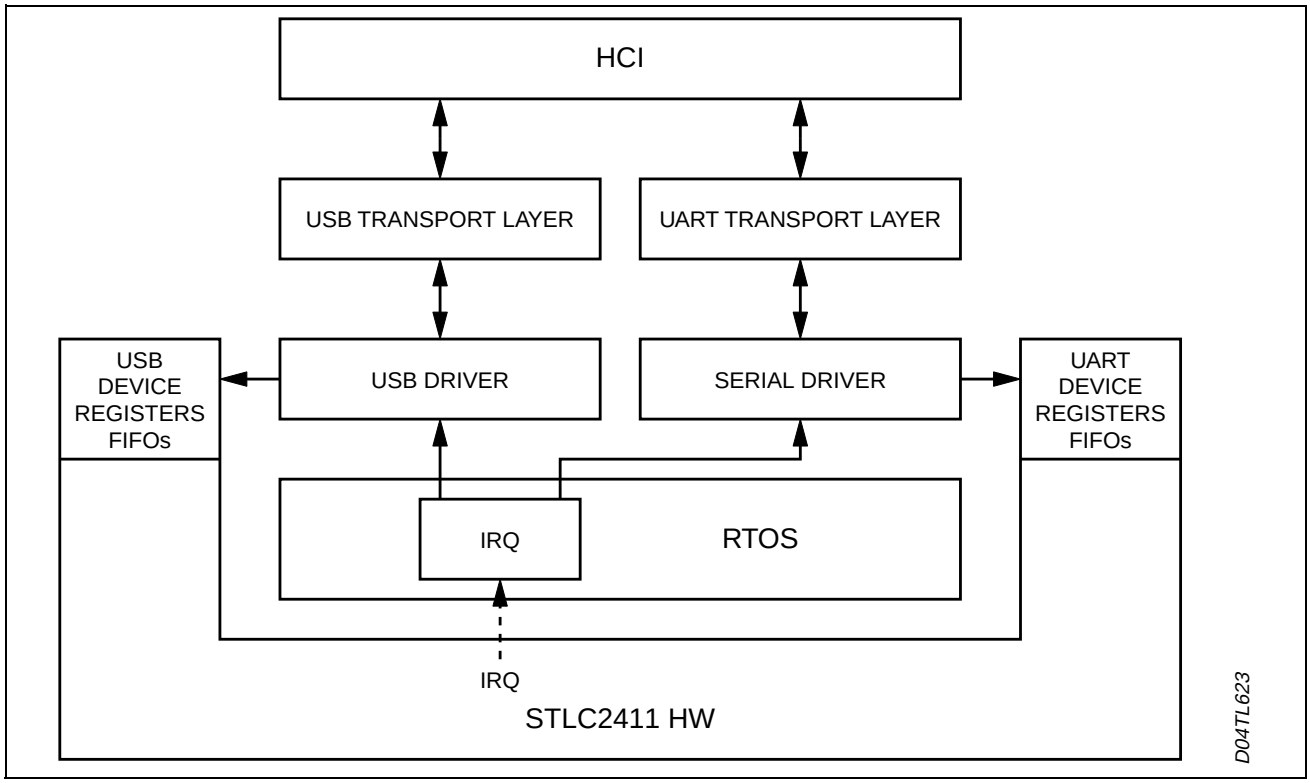
The interface is a fast master I2C; it has full control of the interface at all times. I2C slave functionality is not supported.

8.4 USB Interface

The USB interface is compliant with the USB 2.0 full speed specification. Max throughput on the USB interface is 12 Mbit/s.

Figure 8 gives an overview of the main components needed for supporting the USB interface, as specified in the Bluetooth™ Core Specification. For clarity, the serial interface (including the UART Transport Layer) is also shown.

Figure 8. USB Interface



The USB device registers and FIFOs are memory mapped. The USB Driver will use these registers to access the USB interface. The equivalent exists for the HCI communication over UART.

For transmission to the host, the USB & Serial Drivers interface with the HW via a set of registers and FIFOs, while in the other direction, the hardware may trigger the Drivers through a set of interrupts (identified by the RTOS, and directed to the appropriate Driver routines).

8.5 JTAG Interface

The JTAG interface is compliant with the JTAG IEEE Std 1149.1. Its allows both the boundary scan of the digital pins and the debug of the ARM7TDMI application when connected with the standard ARM7 development tools.

8.6 RF Interface

The STLC2411 radio interface is compatible to BlueRF (unidirectional RxMode2 for data and unidirectional serial interface for control).

8.7 PCM voice interface

The voice interface is a direct PCM interface to connect to a standard CODEC (e.g. STw5093 or STw5094) including internal decimator and interpolator filters. The data can be linear PCM (13-16bit), µ-Law (8bit) or A-Law (8bit). By default the codec interface is configured as master. The encoding on the air

interface is programmable to be CVSD, A-Law or µ-Law.

The PCM block is able to manage the PCM bus with up to 3 timeslots.

PCM clock and data are in master mode available at 2 MHz or at 2.048 MHz to allow interfacing of standard codecs.

The four signals of the PCM interface are:

- PCM_CLK : PCM clock
- PCM_SYNC : PCM 8kHz sync
- PCM_A : PCM data
- PCM_B : PCM data

Directions of PCM_A and PCM_B are software configurable.

Three additional PCM_SYNC signals can be provided via the GPIOs. See section 12 for more details.

Figure 9. PCM (A-law, µ-law) standard mode

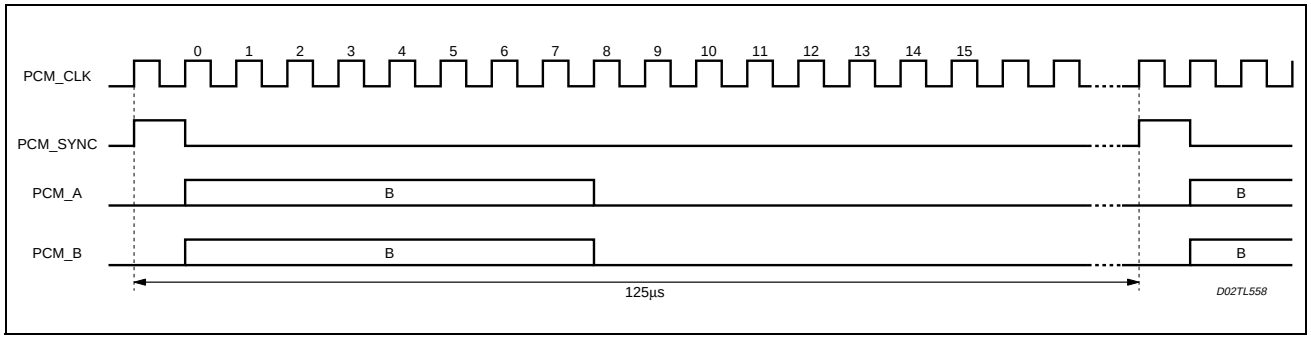


Figure 10. Linear mode

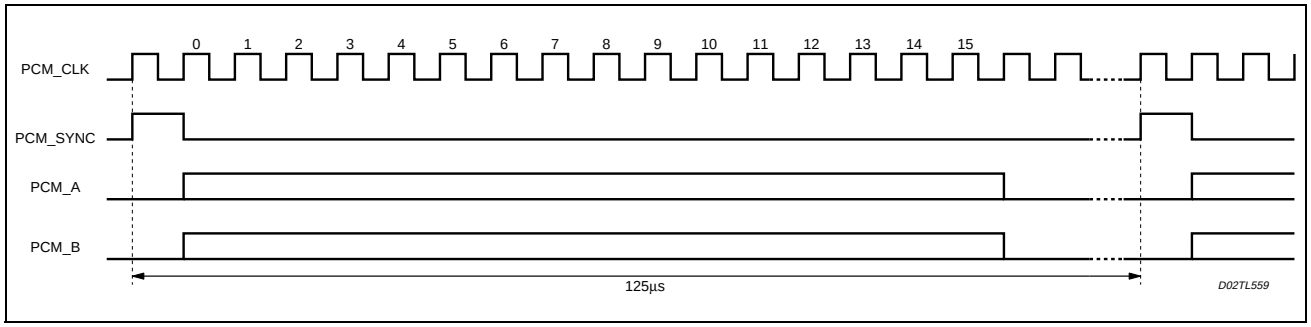
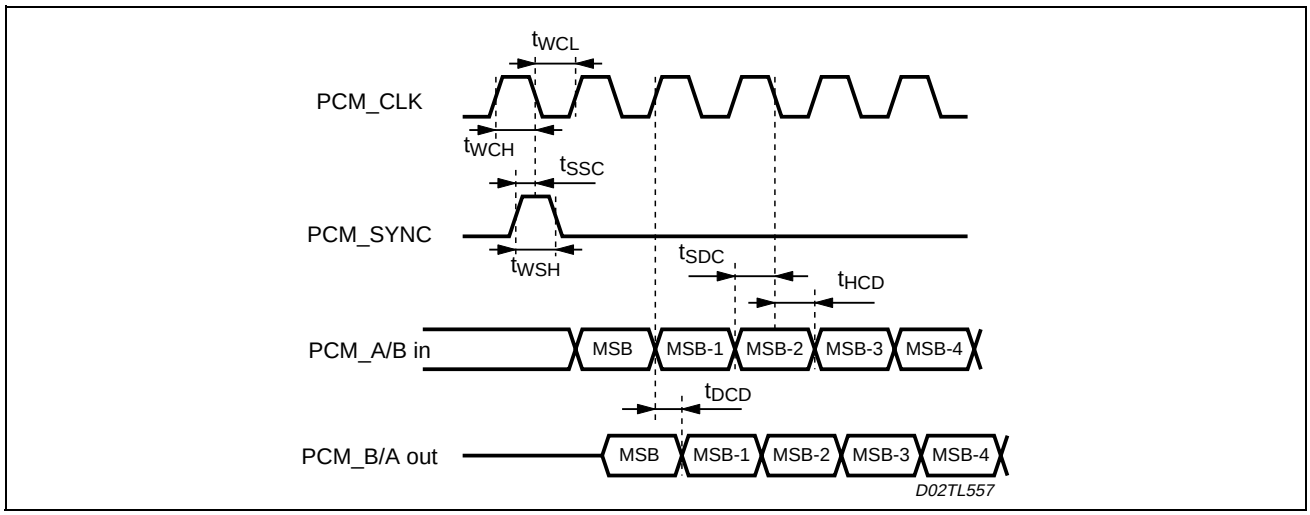


Table 13. PCM interface timing.

Symbol	Description	Min	Typ	Max	Unit
PCM Interface					
F_{pcm_clk}	Frequency of PCM_CLK (master)		2048		kHz
F_{pcm_sync}	Frequency of PCM_SYNC		8		kHz
t_{WCH}	High period of PCM_CLK	200			ns
t_{WCL}	Low period of PCM_CLK	200			ns
t_{WSH}	High period of PCM_SYNC	200			ns
t_{SSC}	Setup time, PCM_SYNC high to PCM_CLK low	100			ns
t_{SDC}	Setup time, PCM_A/B input valid to PCM_CLK low	100			ns
t_{HCD}	Hold time, PCM_CLK low to PCM_A/B input invalid	100			ns
t_{DCD}	Delay time, PCM_CLK high to PCM_A/B output valid			150	ns

Figure 11. PCM interface timing



9 HCI UART TRANSPORT LAYER

The UART Transport Layer is specified by the Bluetooth™ SIG, and allows HCI level communication between a host controller (STLC2411) and a host (e.g. PC), via a serial line.

The objective of this HCI UART Transport Layer is to make it possible to use the Bluetooth™ HCI over a serial interface between two UARTs on the same PCB. The HCI UART Transport Layer assumes that the UART communication is free from line errors.

9.1 UART Settings

The HCI UART Transport Layer uses the following settings for RS232:

- Baud rate: Configurable (Default baud rate: 57.600 kbps)
- Number of data bits: 8
- Parity bit: no parity
- Stop bit: 1 stop bit
- Flow control: RTS/CTS
- Flow-off response time: 3 ms

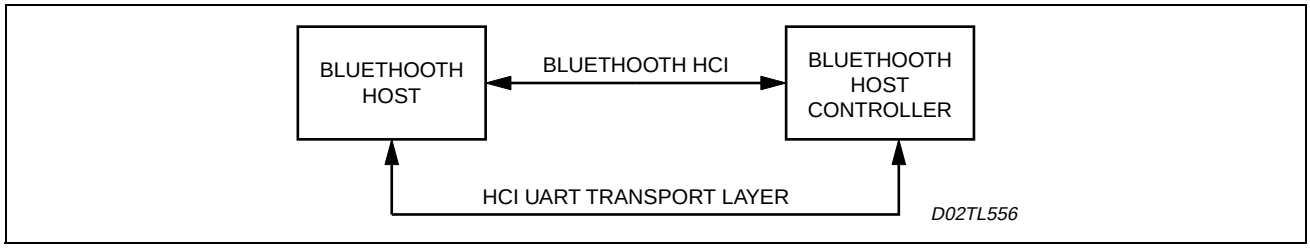
Flow control with RTS/CTS is used to prevent temporary UART buffer overrun. It should not be used for flow control of HCI, since HCI has its own flow control mechanisms for HCI commands, HCI events and HCI data.

If CTS is 1, then the Host/Host Controller is allowed to send.

If CTS is 0, then the Host/Host Controller is not allowed to send.

The flow-off response time defines the maximum time from setting RTS low until the byte flow actually stops. The signals should be connected in a null-modem fashion; i.e. the local TXD should be connected to the remote RXD and the local RTS should be connected to the remote CTS and vice versa.

Figure 12. UART Transport Layer



10 HCI USB TRANSPORT LAYER

The USB Transport Layer has been specified by the Bluetooth™ SIG, and allows HCI level communication between a host controller (STLC2411) and a host (e.g. PC), via a USB interface. The USB Transport Layer is completely implemented in SW. It accepts HCI messages from the HCI Layer, prepares it for transmission over a USB bus, and sends it to the USB Driver. It reassembles the HCI messages from USB data received from the USB Driver, and sends these messages to the HCI Layer. The Transport Layer does not interprete the contents (payload) of the HCI messages; it only examines the header.

11 CLASS1 POWER SUPPORT

The chip can control an external power amplifier (PA). Several signals are duplicated on GPIOs for this purpose in order to avoid digital/analogue noise loops in the radio.

A software controlled register enables the alternate functions of GPIO[15:6] to generate the signals for driving an external PA in a Bluetooth™ class1 power application.

Every bit enables a dedicated signal on a GPIO pin, as described in Table 14.

12 GPIOS

Table 14. GPIOs alternate functionalities

Involved GPIO	Description of alternate dedicated functionality
gpio0	No dedicated function
gpio1	WLAN 1
gpio2	WLAN 2
gpio3	WLAN 3
gpio4	WLAN 4
gpio5	(Used for USB reset pull.)
gpio6	Power Class 1 brxen
gpio7	Power Class 1 not_brxen
gpio8	Power Class 1 PA0 or PCM sync 1
gpio9	Power Class 1 PA1 or PCM sync 2
gpio10]	Power Class 1 PA2 or PCM sync 3
gpio11	Power Class 1 PA3
gpio12	Power Class 1 PA4
gpio13	Power Class 1 PA5
gpio14	Power Class 1 PA6
gpio15	Power Class 1 PA7

The signal brxen is the same as the brxen radio output pin. The signal not_brxen is the inverted signal, in order to save components on the application board.

PA7 to PA0 are the power amplifier control lines. They are managed, on a connection basis, by the baseband core. The Power Level programmed for a certain Bluetooth™ connection is managed by the firmware, as specified in the Bluetooth™ SIG spec.

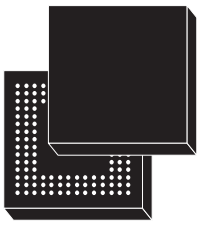
The WLAN signals, as described in section 7.12, can be enabled on GPIO pins.

The extra PCM sync signals, as described in section 8.7, can be flexibly configured on GPIO pins to connect multiple codecs.

Figure 13. TFBGA132 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.010		1.200	0.040		0.047
A1	0.150			0.006		
A2		0.820			0.032	
b	0.250	0.300	0.350	0.010	0.012	0.014
D	7.850	8.000	8.150	0.310	0.315	0.321
D1		6.500			0.256	
E	7.850	8.000	8.150	0.310	0.315	0.321
E1		6.500			0.256	
e	0.450	0.500	0.550	0.018	0.020	0.022
f	0.600	0.750	0.900	0.024	0.029	0.035
ddd			0.080			0.003

OUTLINE AND MECHANICAL DATA



Body: 8 x 8 x 1.20mm

TFBGA132
Fine Pitch Ball Grid Array

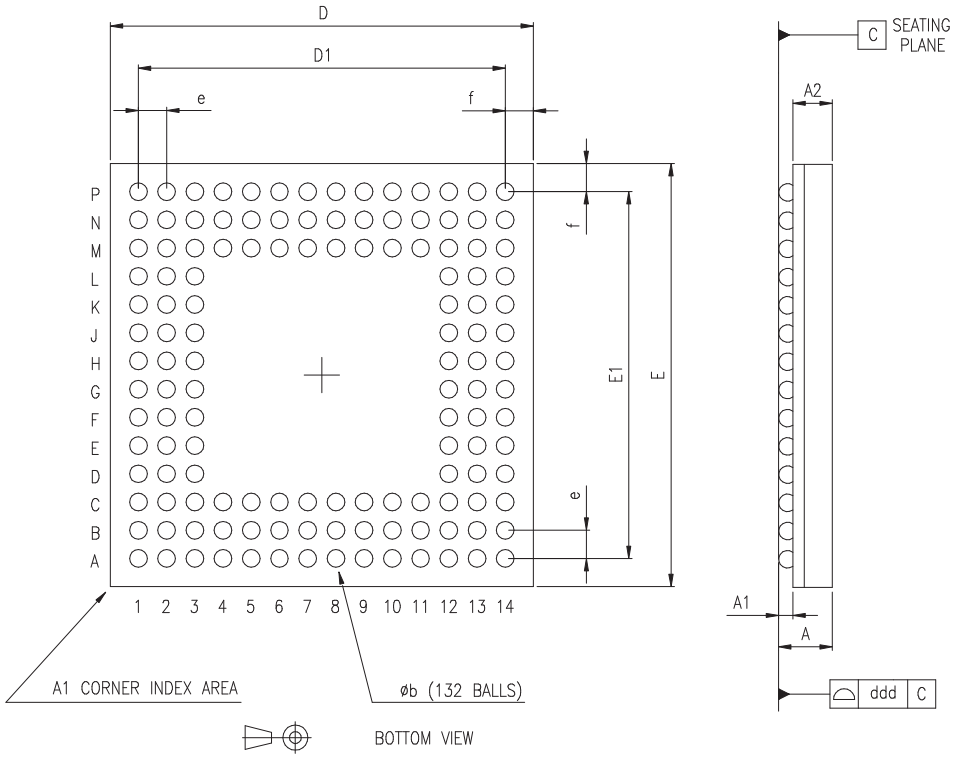


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Table 15. Revision History

Date	Revision	Description of Changes
June 2004	1	First Issue