

## Features

- ◆ **RC32300 32-bit Microprocessor**
  - Up to 150 MHz operation
  - Enhanced MIPS-II Instruction Set Architecture (ISA)
  - Cache prefetch instruction
  - Conditional move instruction
  - DSP instructions
  - Supports big or little endian operation
  - MMU with 32 page TLB
  - 8kB Instruction Cache, 2-way set associative
  - 2kB Data Cache, 2-way set associative
  - Cache locking per line
  - Programmable on a page basis to implement a write-through no write allocate, write-through write allocate, or write-back algorithms for cache management
  - Compatible with a wide variety of operating systems
- ◆ **Local Bus Interface**
  - Up to 75 MHz operation
  - 26-bit address bus
  - 32-bit data bus
  - Direct control of local memory and peripherals
  - Programmable system watch-dog timers
  - Big or little endian support
- ◆ **Interrupt Controller simplifies exception management**
- ◆ **Four general purpose 32-bit timer/counters**

- ◆ **Programmable I/O (PIO)**
  - Input/Output/Interrupt source
  - Individually programmable
- ◆ **SDRAM Controller (32-bit memory only)**
  - 4 banks, non-interleaved
  - Up to 512MB total SDRAM memory supported
  - Implements full, direct control of discrete, SODIMM, or DIMM memories
  - Supports 16Mb through 512Mb SDRAM device depths
  - Automatic refresh generation
- ◆ **Serial Peripheral Interface (SPI) master mode interface**
- ◆ **UART Interface**
  - Two 16550 compatible UARTs
  - Baud rate support up to 1.5 Mb/s
  - Modem control signals available on one channel
- ◆ **Memory & Peripheral Controller**
  - 6 banks, up to 64MB per bank
  - Supports 8-, 16-, and 32-bit interfaces
  - Supports Flash ROM, SRAM, dual-port memory, and peripheral devices
  - Supports external wait-state generation
  - 8-bit boot PROM support
  - Flexible I/O timing protocols

## Block Diagram

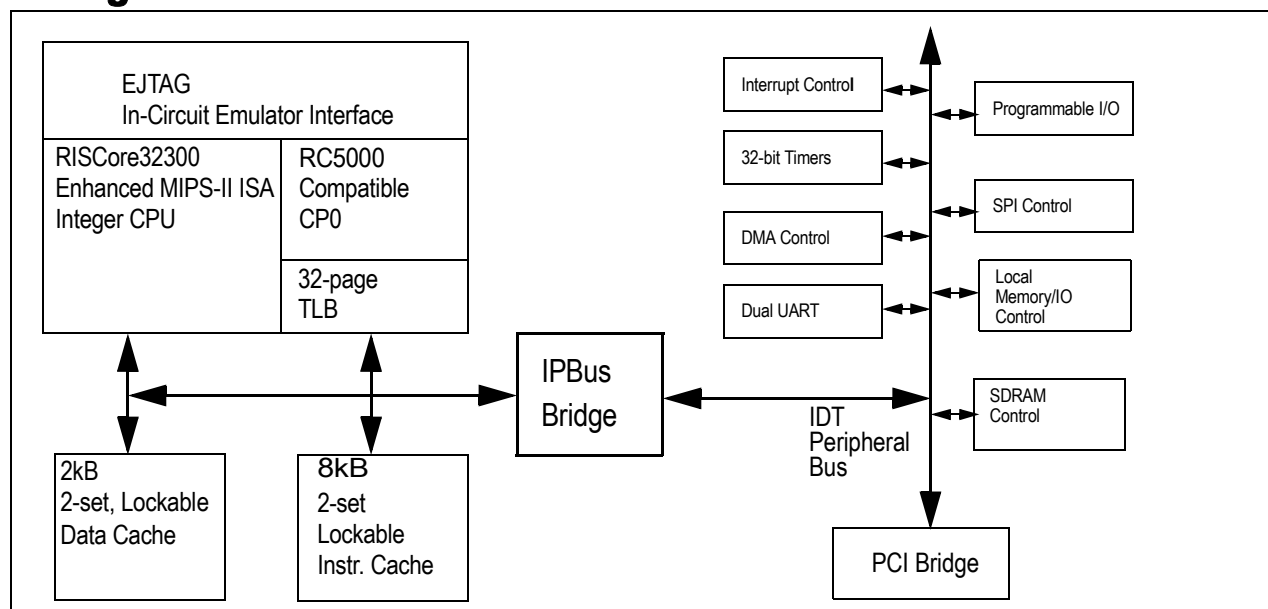


Figure 1 RC32334 Block Diagram

**Note:** This data sheet does not apply to revision Z silicon. Contact your IDT sales representative for information on revision Z.

- ◆ **4 DMA Channels**
  - 4 general purpose DMA, each with endianness swappers and byte lane data alignment
  - Supports scatter/gather, chaining via linked lists of records
  - Supports memory-to-memory, memory-to-I/O, memory-to-PCI, PCI-to-PCI, and I/O-to-I/O transfers
  - Supports unaligned transfers
  - Supports burst transfers
  - Programmable DMA bus transactions burst size (up to 16 bytes)
- ◆ **PCI Bus Interface**
  - 32-bit PCI, up to 66 MHz
  - Revision 2.2 compatible
  - Target or master
  - Host or satellite
  - Three slot PCI arbiter
  - Serial EEPROM support, for loading configuration registers
- ◆ **Off-the-shelf development tools**
- ◆ **JTAG Interface (IEEE Std. 1149.1 compatible)**
- ◆ **256-ball BGA (1.0mm spacing)**
- ◆ **3.3V operation with 5V tolerant I/O**
- ◆ **EJTAG in-circuit emulator interface**

## Device Overview

The IDT RC32334 device is an integrated processor based on the RC32300 CPU core. This product incorporates a high-performance, low-cost 32-bit CPU core with functionality common to a large number of embedded applications. The RC32334 integrates these functions to enable the use of low-cost PC commodity market memory and I/O devices, allowing the aggressive price/performance characteristics of the CPU to be realized quickly into low-cost systems.

## CPU Execution Core

The RC32334 integrates the RISCORE32300, the same CPU core found in the award-winning RC32364 microprocessor.

The RISCORE32300 implements the Enhanced MIPS-II ISA. Thus, it is upwardly compatible with applications written for a wide variety of MIPS architecture processors, and it is kernel compatible with the modern operating systems that support IDT's 64-bit RISCController product family.

The RISCORE32300 was explicitly defined and designed for integrated processor products such as the RC32334. Key attributes of the execution core found within this product include:

- ◆ High-speed, 5-stage scalar pipeline executes to 150MHz. This high performance enables the RC32334 to perform a variety of performance intensive tasks, such as routing, DSP algorithms, etc.
- ◆ 32-bit architecture with enhancements of key capabilities. Thus, the RC32334 can execute existing 32-bit programs, while enabling designers to take advantage of recent advances in CPU architecture.
- ◆ Count leading-zeroes/ones. These instructions are common to a wide variety of tasks, including modem emulation, voice over IP compression and decompression, etc.
- ◆ Cache PREFetch instruction support, including a specialized form intended to help memory coherency. System programmers can allocate and stage the use of memory bandwidth to achieve maximum performance.
- ◆ 8kB of 2-way set associative instruction cache

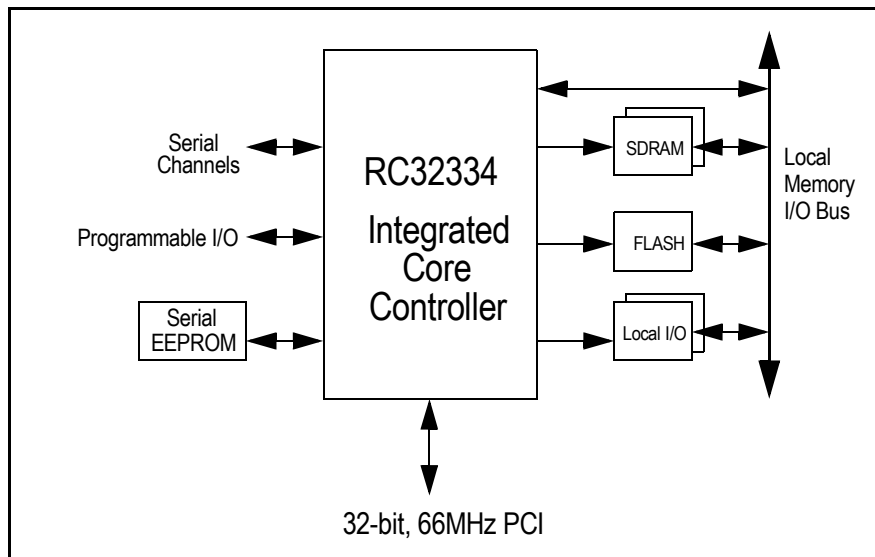


Figure 2 RC32334 Based System Diagram

- ◆ 2KB of 2-way set associative data cache, capable of write-back and write-through operation.
- ◆ Cache locking per line to speed real-time systems and critical system functions
- ◆ On-chip TLB to enable multi-tasking in modern operating systems
- ◆ EJTAG interface to enable sophisticated low-cost in-circuit emulation.

## Synchronous-DRAM Interface

The RC32334 integrates a SDRAM controller which provides direct control of system SyncDRAM running at speeds to 75MHz.

Key capabilities of the SDRAM controller include:

- ◆ Direct control of 4 banks of SDRAM (up to 2 64-bit wide DIMMs)
- ◆ On-chip page comparators optimize access latency.
- ◆ Speeds to 75MHz
- ◆ Programmable address map.
- ◆ Supports 16, 64, 128, 256, or 512Mb SDRAM devices
- ◆ Automatic refresh generation driven by on-chip timer
- ◆ Support for discrete devices, SODIMM, or DIMM modules.

Thus, systems can take advantage of the full range of commodity memory that is available, enabling system optimization for cost, real-estate, or other attributes.

## Local Memory and I/O Controller

The local memory and I/O controller implements direct control of external memory devices, including the boot ROM as well as other memory areas, and also implements direct control of external peripherals.

The local memory controller is highly flexible, allowing a wide range of devices to be directly controlled by the RC32334 processor. For example, a system can be built using an 8-bit boot ROM, 16-bit FLASH cards (possibly on PCMCIA), a 32-bit SRAM or dual-port memory, and a variety of low-cost peripherals.

Key capabilities include:

- ◆ Direct control of EPROM, FLASH, RAM, and dual-port memories
- ◆ 6 chip-select outputs, supporting up to 64MB per memory space
- ◆ Supports mixture of 8-, 16-, and 32-bit wide memory regions
- ◆ Flexible timing protocols allow direct control of a wide variety of devices
- ◆ Programmable address map for 2 chip selects
- ◆ Automatic wait state generation.

## PCI Bus Bridge

In order to leverage the wide availability of low-cost peripherals for the PC market as well as to simplify the design of add-in functions, the RC32334 integrates a full 32-bit PCI bus bridge. Key attributes of this bridge include:

- ◆ 66 MHz operation
- ◆ PCI revision 2.2 compliant
- ◆ Programmable address mappings between CPU/Local memory and PCI memory and I/O
- ◆ On-chip PCI arbiter
- ◆ Extensive buffering allows PCI to operate concurrently with local memory transfers
- ◆ Selectable byte-ordering swapper
- ◆ 5V tolerant I/O.

## On-Chip DMA Controller

To minimize CPU exception handling and maximize the efficiency of system bandwidth, the RC32334 integrates a very sophisticated 4-channel DMA controller on chip.

The RC32334 DMA controller is capable of:

- ◆ Chaining and scatter/gather support through the use of a flexible, linked list of DMA transaction descriptors
- ◆ Capable of memory<->memory, memory<->I/O, and PCI<->memory DMA
- ◆ Unaligned transfer support
- ◆ Byte, halfword, word, quadword DMA support.

## On-Chip Peripherals

The RC32334 also integrates peripherals that are common to a wide variety of embedded systems.

- ◆ Dual channel 16550 compatible UARTs, with modem control interface on one channel.
- ◆ SPI master mode interface for direct interface to EEPROM, A/D, etc.
- ◆ Interrupt Controller to speed interrupt decode and management
- ◆ Four 32-bit on-chip Timer/Counters
- ◆ Programmable I/O module

## Debug Support

To facilitate rapid time to market, the RC32334 provides extensive support for system debug.

First and foremost, this product integrates an EJTAG in-circuit emulation module, allowing a low-cost emulator to interoperate with programs executing on the controller. By using an augmented JTAG interface, the RC32334 is able to reuse the same low-cost emulators developed around the RC32364 CPU.

Secondly, the RC32334 implements additional reporting signals intended to simplify the task of system debugging when using a logic analyzer. This product allows the logic analyzer to differentiate transactions initiated by DMA from those initiated by the CPU and further allows CPU transactions to be sorted into instruction fetches vs. data fetches.

Finally, the RC32334 implements a full boundary scan capability, allowing board manufacturing diagnostics and debug.

## Packaging

The RC32334 is packaged using a 256-lead PBGA package, with 1.0mm ball spacing.

## Thermal Considerations

The RC32334 consumes less than 2.1 W peak power. The device is guaranteed in an ambient temperature range of 0° to +70° C for commercial temperature devices; -40° to +85° for industrial temperature devices.

## Revision History

**May 16, 2000:** Initial version.

**June 8, 2000:** In CPU Core Specific Signals section of Table 1, changed `cpu_dr_r_n` pin from Input to Output. Updated document from Advance to Preliminary Information.

**June 15, 2000:** In Table 1, switched assertion and de-assertion for `debug_cpu_dma_n` signal. In the AC Timing Characteristics table, added SPI section and adjusted parameters in the Reset section.

**July 12, 2000:** Removed "Preliminary Information" statement. Added information regarding external pull-ups and pull-downs to the Pin Description Table. Made minor revisions in other parts of the data sheet.

**August 3, 2000:** Added Pin Layout diagram showing power and ground pins. Revised Power Curves section to reflect support of only 2x, 3x, and 4x.

**August 30, 2000:** Added Standby mode and values to Power Consumption table. Extended Power Curve figure to 75 MHz.

**September 25, 2000:** Changed MIPS32 ISA to Enhanced MIPS-II. In Local System Interface section of Table 6, changed Thld2 values for `mem_data[31:0]` from 1.8 to 1.5 ns and changed Tdoh3 values for `mem_addr[25:2]`, etc. from 1.8 to 1.5 ns.

**December 12, 2000:** Changed Max values for `cpu_masterclock` period in Table 5 and added footnote. In Table 1, added 2nd alternate function for `spi_mosi`, `spi_miso`, `spi_sck`. In Table 10, removed the "1" from Alt column for `cpu_masterclk` and added "2" in Alt column for pins G3, G4, H2. In RC32334 Alternate Signal Functions table: added pin T2; added pin names in Alt #2 column for pins G3, G4, H2; added PIO[11] to Alt #2 column for pin R3.

**January 4, 2001:** In Table 6 under Interrupt Handling, moved the values for Tsu9 from the Max to the Min columns.

**March 13, 2001:** Changed upper ambient temperature for industrial and commercial uses from +70° C to +85° C.

**June 7, 2001:** In the Clock Parameters table, added footnote 3 to `output_clk` category and added NA to Min and Max columns. In Figure 3 (Reset Specification), enhanced signal line for `cpu_masterclk`. In Local System Interface section of AC Timing Characteristics table, changed values in Min column for last category of signals (Tdoh3) from 1.5 to 2.5 for all speeds. In SDRAM Controller section of same table, changed values in Min column for last category of signals (9 signals) from 1 to 2.5 for all speeds.

**September 14, 2001:** In the Reset category of Table 6: switched `mem_addr[19:17]` from Tsu22 and Thld22 to Tsu10 and Thld10; switched `mem_addr[22:20]` from Tsu10 and Thld10 to Tsu22 and Thld22; moved `eitag_pcst[2:0]` from Reset to Debug Interface category under Tsu20 and Thld20.

**November 1, 2001:** Added Input Voltage Undershoot parameter and 2 footnotes to Table 10.

**March 20, 2002:** In Local System Interface section of AC Timing Characteristics table, changed values in Min column for last category of signals (Tdoh3) from 2.5 to 1.5 for all speeds. In Table 8, PCI Drive Output Pads, the Conditions for parameters  $V_{OL}$ ,  $V_{OH}$ ,  $V_{IL}$ , and  $V_{IH}$  were changed to read Per PCI 2.2.

**May 2, 2002:** Changed upper ambient temperature for commercial uses back from +85° C to +70° C (changed erroneously from 70 to 85 on March 13, 2001). Added Reset State Status column to Table 1. Revised description of `jtag_trst_n` in Table 1 and changed this pin to a pull-down instead of a pull-up.

**July 3, 2002:** This data sheet now describes revision Y silicon and is no longer applicable to revision Z.

**July 12, 2002:** In Table 6: PCI section, changed Thld Min values from 1 to zero; DMA section, changed Thld9 Min values from 2 to 1; in PIO section, changed Thld9 Min values from 2 to 1; in Timer section, changed Thld10 Min values from 2 to 1. Revision Y data sheet changed from Preliminary to Final.

**September 18, 2002:** Added `cpu_coldreset_n` rise time to Table 5, Clock Parameters. Added `mem_addr[16]` and `sdram_addr[16]` to Tables 1 and 12. Changed Logic Diagram to include `sdram_addr[16]`.

**December 18, 2002:** In the Reset section of Table 6, AC Timing Characteristics, setup and hold time categories for `cpu_coldreset_n` have been deleted.

**July 30, 2003:** In Table 8, added 3 new categories (Input Pads, PCI Input Pads, and All Pads) and added footnotes 2 and 3.

**March 24, 2004:** In Table 1, changed description in Satellite Mode for `pci_rst_n`. Specified "cold" reset on pages 11 and 12. Changed the maximum value for Vcc to 4.0 in Table 10, Absolute Maximum Ratings, and changed footnote 1 to that table. Added Power Ramp-up section on page 21.

**August 31, 2004:** Added "Green" orderable parts on page 30.

## Pin Description Table

The following table lists the pins provided on the RC32334. Note that those pin names followed by "\_n" are active-low signals. All external pull-ups and pull-downs require 10 kΩ resistor.

| Name                          | Type                       | Reset State Status   | Drive Strength Capability  | Description   |            |                            |             |             |             |              |             |             |             |             |        |             |             |             |             |        |                        |             |                       |                       |       |                        |             |             |                   |
|-------------------------------|----------------------------|----------------------|----------------------------|---|------------|----------------------------|-------------|-------------|-------------|--------------|-------------|-------------|-------------|-------------|--------|-------------|-------------|-------------|-------------|--------|------------------------|-------------|-----------------------|-----------------------|-------|------------------------|-------------|-------------|-------------------|
| <b>Local System Interface</b> |                            |                      |                            |   |            |                            |             |             |             |              |             |             |             |             |        |             |             |             |             |        |                        |             |                       |                       |       |                        |             |             |                   |
| mem_data[31:0]                | I/O                        | Z                    | High                       | <b>Local System Data Bus</b><br>Primary data bus for memory. I/O and SDRAM.   |            |                            |             |             |             |              |             |             |             |             |        |             |             |             |             |        |                        |             |                       |                       |       |                        |             |             |                   |
| mem_addr[25:2]                | I/O                        | [25:10] Z<br>[9:2] L | [25:17] Low<br>[16:2] High | <b>Memory Address Bus</b><br>These signals provide the Memory or DRAM address, during a Memory or DRAM bus transaction. During each word data, the address increments either in linear or sub-block ordering, depending on the transaction type. The table below indicates how the memory write enable signals are used to address discreet memory port width types. <table border="1" data-bbox="625 709 1490 982"> <thead> <tr> <th>Port Width</th> <th>Pin Signals<br/>mem_we_n[3]</th> <th>mem_we_n[2]</th> <th>mem_we_n[1]</th> <th>mem_we_n[0]</th> </tr> </thead> <tbody> <tr> <td>DMA (32-bit)</td> <td>mem_we_n[3]</td> <td>mem_we_n[2]</td> <td>mem_we_n[1]</td> <td>mem_we_n[0]</td> </tr> <tr> <td>32-bit</td> <td>mem_we_n[3]</td> <td>mem_we_n[2]</td> <td>mem_we_n[1]</td> <td>mem_we_n[0]</td> </tr> <tr> <td>16-bit</td> <td>Byte High Write Enable</td> <td>mem_addr[1]</td> <td>Not Used (Driven Low)</td> <td>Byte Low Write Enable</td> </tr> <tr> <td>8-bit</td> <td>Not Used (Driven High)</td> <td>mem_addr[1]</td> <td>mem_addr[0]</td> <td>Byte Write Enable</td> </tr> </tbody> </table><br>mem_addr[22] Alternate function: reset_boot_mode[1].<br>mem_addr[21] Alternate function: reset_boot_mode[0].<br>mem_addr[20] Alternate function: reset_pci_host_mode.<br>mem_addr[19] Alternate function: modebit [9].<br>mem_addr[18] Alternate function: modebit [8].<br>mem_addr[17] Alternate function: modebit [7].<br>mem_addr[16] Alternate function: sdram_addr[16].<br>mem_addr[15] Alternate function: sdram_addr[15].<br>mem_addr[14] Alternate function: sdram_addr[14].<br>mem_addr[13] Alternate function: sdram_addr[13].<br>mem_addr[11] Alternate function: sdram_addr[11].<br>mem_addr[10] Alternate function: sdram_addr[10].<br>mem_addr[9] Alternate function: sdram_addr[9].<br>mem_addr[8] Alternate function: sdram_addr[8].<br>mem_addr[7] Alternate function: sdram_addr[7].<br>mem_addr[6] Alternate function: sdram_addr[6].<br>mem_addr[5] Alternate function: sdram_addr[5].<br>mem_addr[4] Alternate function: sdram_addr[4].<br>mem_addr[3] Alternate function: sdram_addr[3].<br>mem_addr[2] Alternate function: sdram_addr[2]. | Port Width | Pin Signals<br>mem_we_n[3] | mem_we_n[2] | mem_we_n[1] | mem_we_n[0] | DMA (32-bit) | mem_we_n[3] | mem_we_n[2] | mem_we_n[1] | mem_we_n[0] | 32-bit | mem_we_n[3] | mem_we_n[2] | mem_we_n[1] | mem_we_n[0] | 16-bit | Byte High Write Enable | mem_addr[1] | Not Used (Driven Low) | Byte Low Write Enable | 8-bit | Not Used (Driven High) | mem_addr[1] | mem_addr[0] | Byte Write Enable |
| Port Width                    | Pin Signals<br>mem_we_n[3] | mem_we_n[2]          | mem_we_n[1]                | mem_we_n[0]   |            |                            |             |             |             |              |             |             |             |             |        |             |             |             |             |        |                        |             |                       |                       |       |                        |             |             |                   |
| DMA (32-bit)                  | mem_we_n[3]                | mem_we_n[2]          | mem_we_n[1]                | mem_we_n[0]   |            |                            |             |             |             |              |             |             |             |             |        |             |             |             |             |        |                        |             |                       |                       |       |                        |             |             |                   |
| 32-bit                        | mem_we_n[3]                | mem_we_n[2]          | mem_we_n[1]                | mem_we_n[0]   |            |                            |             |             |             |              |             |             |             |             |        |             |             |             |             |        |                        |             |                       |                       |       |                        |             |             |                   |
| 16-bit                        | Byte High Write Enable     | mem_addr[1]          | Not Used (Driven Low)      | Byte Low Write Enable   |            |                            |             |             |             |              |             |             |             |             |        |             |             |             |             |        |                        |             |                       |                       |       |                        |             |             |                   |
| 8-bit                         | Not Used (Driven High)     | mem_addr[1]          | mem_addr[0]                | Byte Write Enable   |            |                            |             |             |             |              |             |             |             |             |        |             |             |             |             |        |                        |             |                       |                       |       |                        |             |             |                   |
| mem_cs_n[5:0]                 | Output                     | H                    | Low with internal pull-up  | <b>Memory Chip Select Negated</b><br>Recommend external pull-up.<br>Signals that a Memory Bank is actively selected.  |            |                            |             |             |             |              |             |             |             |             |        |             |             |             |             |        |                        |             |                       |                       |       |                        |             |             |                   |
| mem_oe_n                      | Output                     | H                    | High                       | <b>Memory Output Enable Negated</b><br>Recommend external pull-up.<br>Signals that a Memory Bank can output its data lines onto the cpu_ad bus.   |            |                            |             |             |             |              |             |             |             |             |        |             |             |             |             |        |                        |             |                       |                       |       |                        |             |             |                   |

Table 1 Pin Description (Part 1 of 7)

| Name           | Type   | Reset State Status | Drive Strength Capability | Description  |
|----------------|--------|--------------------|---------------------------|--|
| mem_we_n[3:0]  | Output | H                  | High                      | <b>Memory Write Enable Negated Bus</b><br>Signals which bytes are to be written during a memory transaction. Bits act as Byte Enable and mem_addr[1:0] signals for 8-bit or 16-bit wide addressing.  |
| mem_wait_n     | Input  |                    | —                         | <b>Memory Wait Negated</b><br>Requires external pull-up.<br>SRAM/IOI/IOM modes: Allows external wait-states to be injected during last cycle before data is sampled.<br>DPM (dual-port) mode: Allows dual-port busy signal to restart memory transaction.<br>Alternate function: sdram_wait_n. |
| mem_245_oe_n   | Output | H                  | Low                       | <b>Memory FCT245 Output Enable Negated</b><br>Controls output enable to optional FCT245 transceiver bank by asserting during both reads and writes to a memory or I/O bank.  |
| mem_245_dt_r_n | Output | Z                  | High                      | <b>Memory FCT245 Direction Xmit/Rcv Negated</b><br>Recommend external pull-up.<br>Alternate function: cpu_dt_r_n. See CPU Core Specific Signals below.   |
| output_clk     | Output | cpu_masterclk      | High                      | <b>Output Clock</b><br>Optional clock output.  |

**PCI Interface**

|                |                       |   |     |   |
|----------------|-----------------------|---|-----|---|
| pci_ad[31:0]   | I/O                   | Z | PCI | <b>PCI Multiplexed Address/Data Bus</b><br>Address driven by Bus Master during initial frame_n assertion, and then the Data is driven by the Bus Master during writes; or the Data is driven by the Bus Slave during reads. |
| pci_cbe_n[3:0] | I/O                   | Z | PCI | <b>PCI Multiplexed Command/Byte Enable Bus</b><br>Command (not negated) Bus driven by the Bus Master during the initial frame_n assertion. Byte Enable Negated Bus driven by the Bus Master during the data phase(s).       |
| pci_par        | I/O                   | Z | PCI | <b>PCI Parity</b><br>Even parity of the pci_ad[31:0] bus. Driven by Bus Master during Address and Write Data phases. Driven by the Bus Slave during the Read Data phase.  |
| pci_frame_n    | I/O                   | Z | PCI | <b>PCI Frame Negated</b><br>Driven by the Bus Master. Assertion indicates the beginning of a bus transaction. De-assertion indicates the last datum.  |
| pci_trdy_n     | I/O                   | Z | PCI | <b>PCI Target Ready Negated</b><br>Driven by the Bus Slave to indicate the current datum can complete.  |
| pci_irdy_n     | I/O                   | Z | PCI | <b>PCI Initiator Ready Negated</b><br>Driven by the Bus Master to indicate that the current datum can complete.   |
| pci_stop_n     | I/O                   | Z | PCI | <b>PCI Stop Negated</b><br>Driven by the Bus Slave to terminate the current bus transaction.  |
| pci_idsel_n    | Input                 |   | —   | <b>PCI Initialization Device Select</b><br>Uses pci_req_n[2] pin. See the PCI subsection.   |
| pci_perr_n     | I/O                   | Z | PCI | <b>PCI Parity Error Negated</b><br>Driven by the receiving Bus Agent 2 clocks after the data is received, if a parity error occurs.   |
| pci_serr_n     | I/O<br>Open-collector | Z | PCI | <b>System Error</b><br>External pull-up resistor is required.<br>Driven by any agent to indicate an address parity error, data parity during a Special Cycle command, or any other system error.                            |
| pci_clk        | Input                 |   | —   | <b>PCI Clock</b><br>Clock for PCI Bus transactions. Uses the rising edge for all timing references.   |

Table 1 Pin Description (Part 2 of 7)

| Name                             | Type                         | Reset State Status                          | Drive Strength Capability | Description   |
|----------------------------------|------------------------------|---|---------------------------|---|
| pci_rst_n                        | Input                        | L   | —                         | <b>PCI Reset Negated</b><br>Host mode: Resets all PCI related logic.<br>Satellite mode: Resets all PCI related logic and also warm resets the 32334.  |
| pci_devsel_n                     | I/O                          | Z   | PCI                       | <b>PCI Device Select Negated</b><br>Driven by the target to indicate that the target has decoded the present address as a target address.   |
| pci_req_n[2]                     | Input                        | Z   | —                         | <b>PCI Bus Request #2 Negated</b><br>Requires external pull-up.<br>Host mode: pci_req_n[2] is an input indicating a request from an external device.<br>Satellite mode: used as pci_idsel pin which selects this device during a configuration read or write.<br>Alternate function: pci_idsel (satellite).   |
| pci_req_n[1]                     | Input                        | Z   | —                         | <b>PCI Bus Request #1 Negated</b><br>Requires external pull-up.<br>Host mode: pci_req_n[1] is an input indicating a request from an external device.<br>Alternate function: Unused (satellite).   |
| pci_req_n[0]                     | I/O                          | Z   | High                      | <b>PCI Bus Request #0 Negated</b><br>Requires external pull-up for burst mode.<br>Host mode: pci_req_n[0] is an input indicating a request from an external device.<br>Satellite mode: pci_req_n[0] is an output indicating a request from this device.   |
| pci_gnt_n[2]                     | Output                       | Z <sup>1</sup>                              | High                      | <b>PCI Bus Grant #2 Negated</b><br>Recommend external pull-up.<br>Host mode: pci_gnt_n[2] is an output indicating a grant to an external device.<br>Satellite mode: pci_gnt_n[2] is used as the pci_inta_n output pin.<br>Alternate function: pci_inta_n (satellite).   |
| pci_gnt_n[1] /<br>pci_eeeprom_cs | I/O                          | X for 1 pci<br>clock then<br>H <sup>2</sup> | High                      | <b>PCI Bus Grant #1 Negated</b><br>Recommend external pull-up.<br>Host mode: pci_gnt_n[1] is an output indicating a grant to an external device.<br>Satellite mode: Used as pci_eprom_cs output pin for Serial Chip Select for loading PCI Configuration Registers in the RC32334 Reset Initialization Vector PCI boot mode. Defaults to the output direction at reset time.<br>1st Alternate function: pci_eeeprom_cs (satellite).<br>2nd Alternate function: PIO[11]. |
| pci_gnt_n[0]                     | I/O                          | Z   | High                      | <b>PCI Bus Grant #0 Negated</b><br>Host mode: pci_gnt_n[0] is an output indicating a grant to an external device. Recommend external pull-up.<br>Satellite mode: pci_gnt_n[0] is an input indicating a grant to this device. Require external pull-up.  |
| pci_inta_n                       | Output<br>Open-<br>collector | Z   | PCI                       | <b>PCI Interrupt #A Negated</b><br>Uses pci_gnt_n[2]. See the PCI subsection.   |
| pci_lock_n                       | Input                        |   | —                         | <b>PCI Lock Negated</b><br>Driven by the Bus Master to indicate that an exclusive operation is occurring.   |

<sup>1</sup> Z in host mode; L in satellite non-boot mode; Z in satellite boot mode.  
<sup>2</sup> H in host mode; L in satellite non-boot and boot modes. X = unknown.

**SDRAM Control Interface**

|                |        |   |      |  |
|----------------|--------|---|------|--|
| sdr_am_addr_12 | Output | L | High | <b>SDRAM Address Bit 12 and Precharge All</b><br>SDRAM mode: Provides SDRAM address bit 12 (10 on the SDRAM chip) during row address and "pre-charge all" signal during refresh, read and write command. |
| sdr_am_ras_n   | Output | H | High | <b>SDRAM RAS Negated</b><br>SDRAM mode: Provides SDRAM RAS control signal to all SDRAM banks.  |

Table 1 Pin Description (Part 3 of 7)

| Name                | Type   | Reset State Status | Drive Strength Capability | Description  |
|---------------------|--------|--------------------|---------------------------|--|
| sdras_cas_n         | Output | H                  | High                      | <b>SDRAM CAS Negated</b><br>SDRAM mode: Provides SDRAM CAS control signal to all SDRAM banks.  |
| sdras_we_n          | Output | H                  | High                      | <b>SDRAM WE Negated</b><br>SDRAM mode: Provides SDRAM WE control signal to all SDRAM banks.  |
| sdras_cke           | Output | H                  | High                      | <b>SDRAM Clock Enable</b><br>SDRAM mode: Provides clock enable to all SDRAM banks.   |
| sdras_cs_n[3:0]     | Output | H                  | High                      | <b>SDRAM Chip Select Negated Bus</b><br>Recommend external pull-up.<br>SDRAM mode: Provides chip select to each SDRAM bank.<br>SODIMM mode: Provides upper select byte enables [7:4].                          |
| sdras_s_n[1:0]      | Output | H                  | High                      | <b>SDRAM SODIMM Select Negated Bus</b><br>SDRAM mode: Not used.<br>SDRAM SODIMM mode: Upper and lower chip selects.  |
| sdras_bemask_n[3:0] | Output | H                  | High                      | <b>SDRAM Byte Enable Mask Negated Bus (DQM)</b><br>SDRAM mode: Provides byte enables for each byte lane of all DRAM banks.<br>SODIMM mode: Provides lower select byte enables [3:0].                           |
| sdras_245_oe_n      | Output | H                  | Low                       | <b>SDRAM FCT245 Output Enable Negated</b><br>Recommend external pull-up.<br>SDRAM mode: Controls output enable to optional FCT245 transceiver bank by asserting during both reads and writes to any DRAM bank. |
| sdras_245_dt_r_n    | Output | Z                  | High                      | <b>SDRAM FCT245 Direction Transmit/Receive</b><br>Recommend external pull-up.<br>Uses cpu_dt_r_n. See CPU Core Specific Signals below.   |

**On-Chip Peripherals**

|                                       |     |                  |     |   |
|---------------------------------------|-----|------------------|-----|---|
| dma_ready_n[1:0] /<br>dma_done_n[1:0] | I/O | Z                | Low | <b>DMA Ready Negated Bus</b><br>Requires external pull-up.<br>Ready mode: Input pin for each general purpose DMA channel that can initiate the next datum in the current DMA descriptor frame.<br>Done mode: Input pin for each general purpose DMA channel that can terminate the current DMA descriptor frame.<br>dma_ready_n[0] 1st Alternate function PIO[1]; 2nd Alternate function: dma_done_n[0].<br>dma_ready_n[1] 1st Alternate function PIO[0]; 2nd Alternate function: dma_done_n[1].  |
| pio[15:0]                             | I/O | See related pins | Low | <b>Programmable Input/Output</b><br>General purpose pins that can each be configured as a general purpose input or general purpose output. These pins are multiplexed with other pin functions:<br>uart_cts_n[0], uart_dsr_n[0], uart_dtr_n[0], uart_rts_n[0], pci_gnt_n[1], spi_mosi, spi_miso, spi_sck, spi_ss_n, uart_rx[0], uart_tx[0], uart_rx[1], uart_tx[1], timer_tc_n[0], dma_ready_n[0], dma_ready_n[1].<br>Note that pci_gnt_n[1], spi_mosi, spi_sck, and spi_ss_n default to outputs at reset time. The others default to inputs. |
| timer_tc_n[0] /<br>timer_gate_n[0]    | I/O | Z                | Low | <b>Timer Terminal Count Overflow Negated</b><br>Terminal count mode (timer_tc_n): Output indicating that the timer has reached its count compare value and has overflowed back to 0.<br>Gate mode (timer_gate_n): input indicating that the timer may count one tick on the next clock edge.<br>1st Alternate function: PIO[2].<br>2nd Alternate function: timer_gate_n[0].   |
| uart_rx[1:0]                          | I/O | Z                | Low | <b>UART Receive Data Bus</b><br>UART mode: Each UART channel receives data on their respective input pin.<br>uart_rx[0] Alternate function: PIO[6].<br>uart_rx[1] Alternate function: PIO[4].   |

Table 1 Pin Description (Part 4 of 7)



| Name   | Type | Reset State Status | Drive Strength Capability | Description  |
|--|------|--------------------|---------------------------|--|
| uart_tx[1:0]   | I/O  | Z                  | Low                       | <b>UART Transmit Data Bus</b><br>UART mode: Each UART channel sends data on their respective output pin. Note that these pins default to inputs at reset time and must be programmed via the PIO interface before being used as UART outputs.<br>uart_tx[0] Alternate function: PIO[5].<br>uart_tx[1] Alternate function: PIO[3].  |
| uart_cts_n[0]<br>uart_dsr_n[0]<br>uart_dtr_n[0]<br>uart_rts_n[0] | I/O  | Z                  | Low                       | <b>UART Transmit Data Bus</b><br>UART mode: Data bus modem control signal pins for UART channel 0.<br>uart_cts_n[0] Alternate function: PIO[15].<br>uart_dsr_n[0] Alternate function: PIO[14].<br>uart_dtr_n[0] Alternate function: PIO[13].<br>uart_rts_n[0] Alternate function: PIO[12].   |
| spi_mosi   | I/O  | L                  | Low                       | <b>SPI Data Output</b><br>Serial mode: Output pin from RC32334 as an Input to a Serial Chip for the Serial data input stream.<br>In PCI satellite mode, acts as an Output pin from RC32334 that connects as an Input to a Serial Chip for the Serial data input stream for loading PCI Configuration Registers in the RC32334 Reset Initialization Vector PCI boot mode.<br>1st Alternate function: PIO[10]. Defaults to the output direction at reset time.<br>2nd Alternate function: pci_eeeprom_mdo. |
| spi_miso   | I/O  | Z                  | Low                       | <b>SPI Data Input</b><br>Serial mode: Input pin to RC32334 from the Output of a Serial Chip for the Serial data output stream.<br>In PCI satellite mode, acts as an Input pin from RC32334 that connects as an output to a Serial Chip for the Serial data output stream for loading PCI Configuration Registers in the RC32334 Reset Initialization Vector PCI boot mode.<br>Defaults to input direction at reset time.<br>1st Alternate function: PIO[7].<br>2nd Alternate function: pci_eeeprom_mdi.  |
| spi_sck  | I/O  | L                  | Low                       | <b>SPI Clock</b><br>Serial mode: Output pin for Serial Clock.<br>In PCI satellite mode, acts as an Output pin for Serial Clock for loading PCI Configuration Registers in the RC323334 Reset Initialization Vector PCI boot mode.<br>1st Alternate function: PIO[9]. Defaults to the output direction at reset time.<br>2nd Alternate function: pci_eeeprom_sk.  |
| spi_ss_n   | I/O  | H                  | Low                       | <b>SPI Chip Select</b><br>Output pin selecting the serial protocol device as opposed to the PCI satellite mode EEPROM device.<br>Alternate function: PIO[8]. Defaults to the output direction at reset time.   |

**CPU Core Specific Signals**

|                       |       |   |   |  |
|-----------------------|-------|---|---|--|
| cpu_nmi_n             | Input |   | — | <b>CPU Non-Maskable Interrupt</b><br>Requires external pull-up.<br>This interrupt input is active low to the CPU.  |
| cpu_masterclk         | Input |   | — | <b>CPU Master System Clock</b><br>Provides the basic system clock.   |
| cpu_int_n[5:4], [2:0] | Input |   | — | <b>CPU Interrupt</b><br>Requires external pull-up.<br>These interrupt inputs are active low to the CPU.  |
| cpu_coldreset_n       | Input | L | — | <b>CPU Cold Reset</b><br>This active-low signal is asserted to the RC32334 after $V_{CC}$ becomes valid on the initial power-up. The Reset initialization vectors for the RC32334 are latched by cold reset. |

Table 1 Pin Description (Part 5 of 7)

| Name       | Type   | Reset State Status | Drive Strength Capability | Description  |
|------------|--------|--------------------|---------------------------|--|
| cpu_dt_r_n | Output | Z                  | —                         | <b>CPU Direction Transmit/Receive</b><br>This active-low signal controls the DT/R pin of an optional FCT245 transceiver bank. It is asserted during read operations.<br>1st Alternate function: mem_245_dt_r_n.<br>2nd Alternate function: sdram_245_dt_r_n. |

**JTAG Interface Signals**

|                           |        |   |                                  |  |
|---------------------------|--------|---|----------------------------------|--|
| jtag_tck                  | Input  |   | —                                | <b>JTAG Test Clock</b><br>Requires external pull-down.<br>An input test clock used to shift into or out of the Boundary-Scan register cells. jtag_tck is independent of the system and the processor clock with nominal 50% duty cycle.  |
| jtag_tdi,<br>ejtag_dint_n | Input  |   | —                                | <b>JTAG Test Data In</b><br>Requires an external pull-up on the board.<br>On the rising edge of jtag_tck, serial input data are shifted into either the Instruction or Data register, depending on the TAP controller state. During Real Mode, this input is used as an interrupt line to stop the debug unit from Real Time mode and return the debug unit back to Run Time Mode (standard JTAG). This pin is also used as the ejtag_dint_n signal in the EJTAG mode. |
| jtag_tdo,<br>ejtag_tpc    | Output | Z | High                             | <b>JTAG Test Data Out</b><br>The jtag_tdo is serial data shifted out from instruction or data register on the falling edge of jtag_tck. When no data is shifted out, the jtag_tdo is tri-stated. During Real Time Mode, this signal provides a non-sequential program counter at the processor clock or at a division of processor clock. This pin is also used as the ejtag_tpc signal in the EJTAG mode.   |
| jtag_tms                  | Input  |   | —                                | <b>JTAG Test Mode Select</b><br>Requires external pull-up.<br>The logic signal received at the jtag_tms input is decoded by the TAP controller to control test operation. jtag_tms is sampled on the rising edge of the jtag_tck.  |
| jtag_trst_n               | Input  | L | —                                | <b>JTAG Test Reset</b><br>When neither JTAG nor EJTAG are being used, jtag_trst_n must be driven low (pulled down) or the jtag_tms/ejtag_tms signals must be pulled up and jtag_clk actively clocked.  |
| ejtag_dclk                | Output | Z | —                                | <b>EJTAG Test Clock</b><br>Processor Clock. During Real Time Mode, this signal is used to capture address and data from the ejtag_tpc signal at the processor clock speed or any division of the internal pipeline.  |
| ejtag_pcstf[2:0]          | I/O    | Z | Low                              | <b>EJTAG PC Trace Status Information</b><br>111 (STL) Pipe line Stall<br>110 (JMP) Branch/Jump forms with PC output<br>101 (BRT) Branch/Jump forms with no PC output<br>100 (EXP) Exception generated with an exception vector code output<br>011 (SEQ) Sequential performance<br>010 (TST) Trace is outputted at pipeline stall time<br>001 (TSQ) Trace trigger output at performance time<br>000 (DBM) Run Debug Mode<br>Alternate function: modebit[2:0].           |
| ejtag_debugboot           | Input  |   | —<br>Requires external pull-down | <b>EJTAG DebugBoot</b><br>The ejtag_debugboot input is used during reset and forces the CPU core to take a debug exception at the end of the reset sequence instead of a reset exception. This enables the CPU to boot from the ICE probe without having the external memory working. This input signal is level sensitive and is not latched internally. This signal will also set the JtagBrk bit in the JTAG_Control_Register[12].                                  |
| ejtag_tms                 | Input  |   | —<br>Requires external pull-up   | <b>EJTAG Test Mode Select</b><br>An external pull-up on the board is required.<br>The ejtag_tms is sampled on the rising edge of jtag_tck.   |

Table 1 Pin Description (Part 6 of 7)

| Name                 | Type | Reset State Status | Drive Strength Capability | Description  |
|----------------------|------|--------------------|---------------------------|--|
| <b>Debug Signals</b> |      |                    |                           |  |
| debug_cpu_dma_n      | I/O  | Z                  | Low                       | <b>Debug CPU versus DMA Negated</b><br>De-assertion high during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction was generated from the CPU.<br>Assertion low during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction was generated from DMA.<br>Alternate function: modebit[6].                     |
| debug_cpu_ack_n      | I/O  | Z                  | Low                       | <b>Debug CPU Acknowledge Negated</b><br>Indicates either a data acknowledge to the CPU or DMA.<br>Alternate function: modebit[4].  |
| debug_cpu_ads_n      | I/O  | Z                  | Low                       | <b>Debug CPU Address/Data Strobe Negated</b><br>Assertion indicates that either a CPU or a DMA transaction is beginning and that the mem_data[31:4] bus has the current block address.<br>Alternate function: modebit[5].  |
| debug_cpu_i_d_n      | I/O  | Z                  | Low                       | <b>Debug CPU Instruction versus Data Negated</b><br>Assertion during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction is a CPU or DMA data transaction.<br>De-assertion during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction is a CPU instruction transaction.<br>Alternate function: modebit[3]. |

Table 1 Pin Description (Part 7 of 7)

## Mode Bit Settings to Configure Controller on Reset

The following table lists the mode bit settings to configure the controller on cold reset.

| Pin             | Mode Bit    | Description  | Value | Mode Setting             |
|-----------------|-------------|--|-------|--------------------------|
| ejtag_pcst[2:0] | 2:0 MSB (2) | Clock Multiplier<br><b>MasterClock</b> is multiplied internally to generate PClock | 0     | Multiply by 2            |
|                 |             |  | 1     | Multiply by 3            |
|                 |             |  | 2     | Multiply by 4            |
|                 |             |  | 3     | Reserved                 |
|                 |             |  | 4     | Reserved                 |
|                 |             |  | 5     | Reserved                 |
|                 |             |  | 6     | Reserved                 |
|                 |             |  | 7     | Reserved                 |
| debug_cpu_i_d_n | 3           | EndBit   | 0     | Little-endian ordering   |
|                 |             |  | 1     | Big-endian ordering      |
| debug_cpu_ack_n | 4           | Reserved   | 0     |                          |
| debug_cpu_ads_n | 5           | Reserved   | 0     |                          |
| debug_cpu_dma_n | 6           | TmrIntEn<br>Enables/Disables the timer interrupt on Int*[5]                        | 0     | Enables timer interrupt  |
|                 |             |  | 1     | Disables timer interrupt |
| mem_addr[17]    | 7           | Reserved for future use  | 1     |                          |

Table 2 Boot-Mode Configuration Settings (Part 1 of 2)

| Pin             | Mode Bit    | Description   | Value | Mode Setting |
|-----------------|-------------|---|-------|--------------|
| mem_addr[19:18] | 9:8 MSB (9) | Boot-Prom Width specifies the memory port width of the memory space which contains the boot prom. | 00    | 8 bits       |
|                 |             |   | 01    | 16 bits      |
|                 |             |   | 10    | 32 bits      |
|                 |             |   | 11    | Reserved     |

Table 2 Boot-Mode Configuration Settings (Part 2 of 2)

### reset\_boot\_mode Settings

By using the non-boot mode cold reset initialization mode the user can change the internal register addresses from base 1800\_0000 to base 1900\_0000, as required. The RC32334 cold reset-boot mode initialization setting values and mode descriptions are listed below.

| Pin             | Reset Boot Mode | Description   | Value | Mode Settings      |
|-----------------|-----------------|---|-------|--------------------|
| mem_addr[22:21] | 1:0 MSB (1)     | Tri-state memory bus and EEPROM bus during cold reset_n assertion   | 11    | Tri-state_bus_mode |
|                 |                 | Reserved  | 10    |                    |
|                 |                 | <b>PCI-boot mode</b> (pci_host_mode must be in satellite mode)<br>RC32334 will reset either from a cold reset or from a PCI reset. Boot code is provided via PCI. | 01    | PCI_boot_mode      |
|                 |                 | <b>Standard-boot mode</b><br>Boot from the RC32334's memory controller (typical system).  | 00    | standard_boot_mode |

Table 3 RC32334 reset\_boot\_mode Initialization Settings

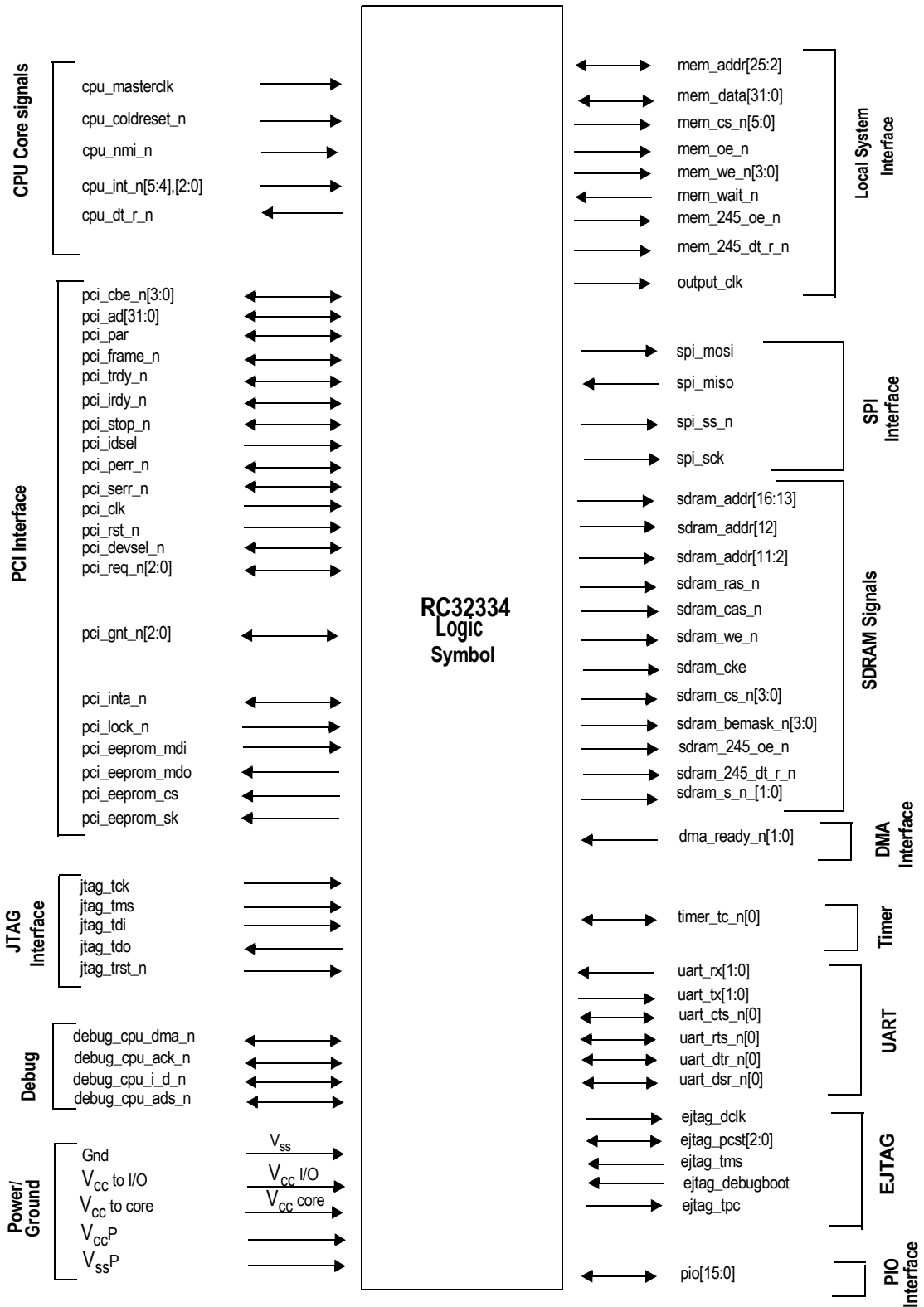
### pci\_host\_mode Settings

During cold reset initialization, the RC32334's PCI interface can be set to the Satellite or Host mode settings. When set to the Host mode, the CPU must configure the RC32334's PCI configuration registers, including the read-only registers. If the RC32334's PCI is in the PCI-boot mode Satellite mode, read-only configuration registers are loaded by the serial EEPROM.

| Pin          | Reset Boot Mode | Description                          | Value | Mode Settings |
|--------------|-----------------|--------------------------------------|-------|---------------|
| mem_addr[20] | PCI host mode   | PCI is in satellite mode             | 1     | PCI_satellite |
|              |                 | PCI is in host mode (typical system) | 0     | PCI_host      |

Table 4 RC32334 pci\_host\_mode Initialization Settings

# Logic Diagram — RC32334



## Clock Parameters — RC32334

(Ta = 0°C to +70°C Commercial, Ta = -40°C to +85°C Industrial, V<sub>cc</sub> I/O = +3.3V±5%, V<sub>cc</sub> Core = +3.3V±5%)

| Parameter                                     | Symbol  | Test Conditions   | RC32334<br>100MHz |       | RC32334<br>133MHz |       | RC32334<br>150MHz |       | Units |
|---|---|-------------------|-------------------|-------|-------------------|-------|-------------------|-------|-------|
|   |   |                   | Min               | Max   | Min               | Max   | Min               | Max   |       |
| cpu_masterclock HIGH                          | t <sub>MCHIGH</sub>   | Transition ≤ 2ns  | 8                 | —     | 6.75              | —     | 6                 | —     | ns    |
| cpu_masterclock LOW                           | t <sub>MCLOW</sub>  | Transition ≤ 2ns  | 8                 | —     | 6.75              | —     | 6                 | —     | ns    |
| cpu_masterclock period <sup>1</sup>           | t <sub>MCP</sub>  | —                 | 20                | 66.6  | 15                | 66.6  | 13.33             | 66.6  | ns    |
| cpu_masterclock Rise & Fall Time <sup>2</sup> | t <sub>MCRise</sub> , t <sub>MCFall</sub>   | —                 | —                 | 3     | —                 | 3     | —                 | 3     | ns    |
| cpu_masterclock Jitter                        | t <sub>JITTER</sub>   | —                 | —                 | ± 250 | —                 | ± 250 | —                 | ± 200 | ps    |
| pci_clk Rise & Fall Time                      | t <sub>PCRise</sub> , t <sub>PCFall</sub>   | PCI 2.2           | —                 | 1.6   | —                 | 1.6   | —                 | 1.6   | ns    |
| pci_clk Period <sup>1</sup>                   | t <sub>PCP</sub>  | —                 | 15                | —     | 15                | —     | 15                | —     | ns    |
| jtag_tck Rise & Fall Time                     | t <sub>JCRise</sub> , t <sub>JCFall</sub>   | —                 | —                 | 5     | —                 | 5     | —                 | 5     | ns    |
| ejtag_dck period                              | t <sub>DCK</sub> , t <sub>t1</sub>  | —                 | 10                | —     | 10                | —     | 10                | —     | ns    |
| jtag_tck clock period                         | t <sub>TCK</sub> , t <sub>t3</sub>  | —                 | 100               | —     | 100               | —     | 100               | —     | ns    |
| ejtag_dck High, Low Time                      | t <sub>DCK High</sub> , t <sub>t9</sub><br>t <sub>DCK Low</sub> , t <sub>t10</sub>  | —                 | 4                 | —     | 4                 | —     | 4                 | —     | ns    |
| ejtag_dck Rise, Fall Time                     | t <sub>DCK Rise</sub> , t <sub>t9</sub><br>t <sub>DCK Fall</sub> , t <sub>t10</sub> | —                 | —                 | 1     | —                 | 1     | —                 | 1     | ns    |
| output_clk <sup>3</sup>                       | Tdo21   | —                 | N/A               | N/A   | N/A               | N/A   | N/A               | N/A   | —     |
| cpu_coldreset_n<br>Asserted during power-up   | —   | power-on sequence | 120               | —     | 120               | —     | 120               | —     | ms    |
| cpu_coldreset_n Rise Time                     | t <sub>CRRise</sub>   | —                 | —                 | 5     | —                 | 5     | —                 | 5     | ns    |

Table 5 Clock Parameters - RC32334

<sup>1</sup> cpu\_masterclock frequency should never be below pci\_clk frequency if PCI interface is used.

<sup>2</sup> Rise and fall times are measured between 10% and 90%

<sup>3</sup> Output\_clk should not be used in a system. Only the cpu\_masterclock or its derivative must be used to drive all the subsystems with designs based on the RC32334 device. Refer to the RC3233x Device Errata for more information.

## Reset Specification

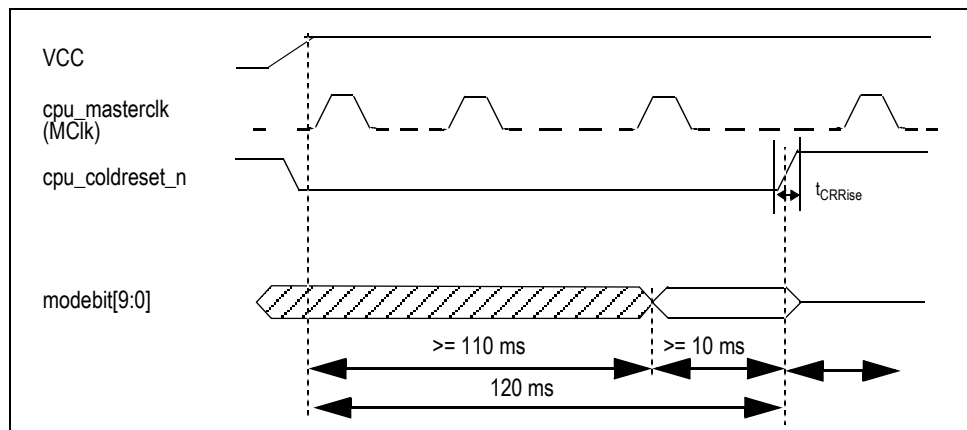


Figure 3 Mode Configuration Interface Cold Reset Sequence

**Power Ramp-up**

There is no special requirement for how fast Vcc and VccP ramp up to 3.3V. However, all timing references are based on Vcc and VccP stabilized at 3.3V -5%.

**AC Timing Characteristics — RC32334**

(Ta = 0°C to +70°C Commercial, Ta = -40°C to +85°C Industrial, V<sub>cc</sub> I/O = +3.3V±5%, V<sub>cc</sub> Core = +3.3V±5%)

| Signal | Symbol | Reference Edge | RC32334 <sup>1</sup><br>100MHz |     | RC32334 <sup>1</sup><br>133MHz |     | RC32334 <sup>1</sup><br>150MHz |     | Unit | User Manual Timing Diagram Reference |
|--------|--------|----------------|--------------------------------|-----|--------------------------------|-----|--------------------------------|-----|------|--------------------------------------|
|        |        |                | Min                            | Max | Min                            | Max | Min                            | Max |      |                                      |

**Local System Interface**

|   |       |                      |     |                 |     |                 |     |                  |    |                                       |
|---|-------|----------------------|-----|-----------------|-----|-----------------|-----|------------------|----|---------------------------------------|
| mem_data[31:0] (data phase)   | Tsu2  | cpu_masterclk rising | 6   | —               | 5   | —               | 4.8 | —                | ns | Chapter 9, Figures 9.2 and 9.3        |
| mem_data[31:0] (data phase)   | Thld2 | cpu_masterclk rising | 1.5 | —               | 1.5 | —               | 1.5 | —                | ns |                                       |
| cpu_dt_r_n  | Tdo3  | cpu_masterclk rising | —   | 15              | —   | 12              | —   | 10               | ns |                                       |
| mem_data[31:0]  | Tdo4  | cpu_masterclk rising | —   | 12              | —   | 10              | —   | 9.3              | ns |                                       |
| mem_data[31:0] output hold time   | Tdoh1 | cpu_masterclk rising | 1   | —               | 1   | —               | 1   | —                | ns |                                       |
| mem_data[31:0] (tristate disable time)  | Tdz   | cpu_masterclk rising | —   | 12 <sup>2</sup> | —   | 10 <sup>2</sup> | —   | 9.3 <sup>2</sup> | ns |                                       |
| mem_data[31:0] (tristate to data time)  | Tzd   | cpu_masterclk rising | —   | 12 <sup>2</sup> | —   | 10 <sup>2</sup> | —   | 9.3 <sup>2</sup> | ns |                                       |
| mem_wait_n  | Tsu6  | cpu_masterclk rising | 9   | —               | 7   | —               | 6   | —                | ns | Chapter 10, Figures 10.6 through 10.8 |
| mem_wait_n  | Thld8 | cpu_masterclk rising | 1   | —               | 1   | —               | 1   | —                | ns |                                       |
| mem_addr[25:2]  | Tdo5  | cpu_masterclk rising | —   | 12              | —   | 9               | —   | 8                | ns |                                       |
| mem_cs_n[5:0]   | Tdo6  | cpu_masterclk rising | —   | 12              | —   | 9               | —   | 8                | ns |                                       |
| mem_oe_n, mem_245_oe_n  | Tdo7  | cpu_masterclk rising | —   | 12              | —   | 9               | —   | 8                | ns |                                       |
| mem_we_n[3:0]   | Tdo7a | cpu_masterclk rising | —   | 15              | —   | 12              | —   | 10               | ns |                                       |
| mem_245_dt_r_n  | Tdo8  | cpu_masterclk rising | —   | 15              | —   | 12              | —   | 10               | ns |                                       |
| mem_addr[25:2]<br>mem_cs_n[5:0]<br>mem_oe_n, mem_we_n[3:0], mem_245_dt_r_n,<br>mem_245_oe_n | Tdoh3 | cpu_masterclk rising | 1.5 | —               | 1.5 | —               | 1.5 | —                | ns |                                       |

**PCI**

|  |      |  |    |   |    |   |    |   |    |             |
|--|------|--|----|---|----|---|----|---|----|-------------|
| pci_ad[31:0], pci_cbe_n[3:0], pci_par, pci_frame_n,<br>pci_trdy_n, pci_irdy_n, pci_stop_n, pci_perr_n,<br>pci_serr_n, pci_devsel_n, pci_lock_n <sup>3</sup>            | Tsu  | pci_clk rising                           | 3  | — | 3  | — | 3  | — | ns | Per PCI 2.2 |
| pci_idsel, pci_req_n[2], pci_req_n[1], pci_req_n[0],<br>pci_gnt_n[0], pci_inta_n   | Tsu  | pci_clk rising                           | 5  | — | 5  | — | 5  | — | ns |             |
| pci_gnt_n[0]   | Tsu  | pci_clk rising                           | 5  | — | 5  | — | 5  | — | ns |             |
| pci_ad[31:0], pci_cbe_n[3:0], pci_par, pci_frame_n,<br>pci_trdy_n, pci_irdy_n, pci_stop_n, pci_perr_n,<br>pci_serr_n, pci_rst_n, pci_devsel_n, pci_lock_n <sup>3</sup> | Thld | pci_clk rising                           | 0  | — | 0  | — | 0  | — | ns |             |
| pci_idsel, pci_req_n[2], pci_req_n[1], pci_req_n[0],<br>pci_gnt_n[0], pci_inta_n   | Thld | pci_clk rising                           | 0  | — | 0  | — | 0  | — | ns |             |
| pci_eeprom_mdi   | Tsu  | pci_clk rising,<br>pci_eeprom_sk falling | 15 | — | 12 | — | 10 | — | ns |             |

Table 6 AC Timing Characteristics - RC32334 (Part 1 of 4)

| Signal   | Symbol | Reference Edge                            | RC32334 <sup>1</sup><br>100MHz |     | RC32334 <sup>1</sup><br>133MHz |     | RC32334 <sup>1</sup><br>150MHz |     | Unit | User Manual Timing Diagram Reference |
|--|--------|---|--------------------------------|-----|--------------------------------|-----|--------------------------------|-----|------|--------------------------------------|
|  |        |   | Min                            | Max | Min                            | Max | Min                            | Max |      |                                      |
| pci_eeeprom_mdi  | Thld   | pci_clk rising,<br>pci_eeeprom_sk falling | 15                             | —   | 12                             | —   | 10                             | —   | ns   |                                      |
| pci_eeeprom_mdo, pci_eeeprom_cs  | Tdo    | pci_clk rising,<br>pci_eeeprom_sk falling | —                              | 15  | —                              | 12  | —                              | 10  | ns   |                                      |
| pci_eeeprom_sk   | Tdo    | pci_clk rising                            | —                              | 15  | —                              | 12  | —                              | 10  | ns   |                                      |
| pci_ad[31:0], pci_cbe_n[3:0], pci_par, pci_frame_n,<br>pci_trdy_n, pci_irdy_n, pci_stop_n, pci_perr_n,<br>pci_serr_n, pci_devsel_n | Tdo    | pci_clk rising                            | 2                              | 6   | 2                              | 6   | 2                              | 6   | ns   | Per PCI 2.2                          |
| pci_req_n[0], pci_gnt_[2], pci_gnt_n[1],<br>pci_gnt_n[0], pci_inta_n   | Tdo    | pci_clk rising                            | 2                              | 6   | 2                              | 6   | 2                              | 6   | ns   |                                      |

**SDRAM Controller**

|  |       |                      |     |    |     |    |     |    |    |   |
|--|-------|----------------------|-----|----|-----|----|-----|----|----|---|
| sdram_245_dt_r_n   | Tdo8  | cpu_masterclk rising | —   | 15 | —   | 12 | —   | 10 | ns | Chapter 11,<br>Figures 11.4<br>and 11.5 |
| sdram_ras_n, sdram_cas_n, sdram_we_n,<br>sdram_cs_n[3:0], sdram_s_n[1:0],<br>sdram_bemask_n[3:0], sdram_cke                                  | Tdo9  | cpu_masterclk rising | —   | 12 | —   | 9  | —   | 8  | ns |   |
| sdram_addr_12  | Tdo10 | cpu_masterclk rising | —   | 12 | —   | 9  | —   | 8  | ns |   |
| sdram_245_oe_n   | Tdo11 | cpu_masterclk rising | —   | 12 | —   | 9  | —   | 8  | ns |   |
| sdram_245_dt_r_n   | Tdoh4 | cpu_masterclk rising | 1   | —  | 1   | —  | 1   | —  | ns |   |
| sdram_ras_n, sdram_cas_n, sdram_we_n,<br>sdram_cs_n[3:0], sdram_s_n[1:0],<br>sdram_bemask_n[3:0] sdram_cke,<br>sdram_addr_12, sdram_245_oe_n | Tdoh4 | cpu_masterclk rising | 2.5 | —  | 2.5 | —  | 2.5 | —  | ns |   |

**DMA**

|                                   |       |                      |   |   |   |   |   |   |    |                            |
|-----------------------------------|-------|----------------------|---|---|---|---|---|---|----|----------------------------|
| dma_ready_n[1:0], dma_done_n[1:0] | Tsu7  | cpu_masterclk rising | 9 | — | 7 | — | 6 | — | ns | Chapter 13,<br>Figure 13.4 |
| dma_ready_n[1:0], dma_done_n[1:0] | Thld9 | cpu_masterclk rising | 1 | — | 1 | — | 1 | — | ns |                            |

**Interrupt Handling**

|   |        |                      |   |   |   |   |   |   |    |                             |
|---|--------|----------------------|---|---|---|---|---|---|----|-----------------------------|
| cpu_int_n[5:4], cpu_int_n[2:0], cpu_nmi_n | Tsu9   | cpu_masterclk rising | 9 | — | 9 | — | 6 | — | ns | Chapter 14,<br>Figure 14.12 |
| cpu_int_n[5:4], cpu_int_n[2:0], cpu_nmi_n | Thld13 | cpu_masterclk rising | 1 | — | 1 | — | 1 | — | ns |                             |

**PIO**

|                      |       |                      |   |    |   |    |   |    |    |  |
|----------------------|-------|----------------------|---|----|---|----|---|----|----|--|
| PIO[15:0]            | Tsu7  | cpu_masterclk rising | 9 | —  | 7 | —  | 6 | —  | ns | Chapter 15,<br>Figures 15.9<br>and 15.10 |
| PIO[15:0]            | Thld9 | cpu_masterclk rising | 1 | —  | 1 | —  | 1 | —  | ns |  |
| PIO[15:10], PIO[8:0] | Tdo16 | cpu_masterclk rising | — | 15 | — | 12 | — | 10 | ns |  |
| PIO[9]               | Tdo19 | cpu_masterclk rising | — | 15 | — | 12 | — | 10 | ns |  |
| PIO[15:10], PIO[8:0] | Tdoh7 | cpu_masterclk rising | 1 | —  | 1 | —  | 1 | —  | ns |  |
| PIO[9]               | Tdoh7 | cpu_masterclk rising | 1 | —  | 1 | —  | 1 | —  | ns |  |

**Timer**

|                                |        |                      |   |    |   |    |   |    |    |   |
|--------------------------------|--------|----------------------|---|----|---|----|---|----|----|---|
| timer_tc_n[0], timer_gate_n[0] | Tsu8   | cpu_masterclk rising | 9 | —  | 7 | —  | 6 | —  | ns | Chapter 16,<br>Figures 16.6<br>and 16.7 |
| timer_tc_n[0], timer_gate_n[0] | Thld10 | cpu_masterclk rising | 1 | —  | 1 | —  | 1 | —  | ns |   |
| timer_tc_n[0], timer_gate_n[0] | Tdo15  | cpu_masterclk rising | — | 15 | — | 12 | — | 10 | ns |   |
| timer_tc_n[0], timer_gate_n[0] | Tdoh6  | cpu_masterclk rising | 1 | —  | 1 | —  | 1 | —  | ns |   |

Table 6 AC Timing Characteristics - RC32334 (Part 2 of 4)



| Signal  | Symbol         | Reference Edge         | RC32334 <sup>1</sup><br>100MHz |     | RC32334 <sup>1</sup><br>133MHz |     | RC32334 <sup>1</sup><br>150MHz |     | Unit | User Manual Timing Diagram Reference                       |
|---|----------------|------------------------|--------------------------------|-----|--------------------------------|-----|--------------------------------|-----|------|--|
|   |                |                        | Min                            | Max | Min                            | Max | Min                            | Max |      |  |
| <b>UARTs</b>  |                |                        |                                |     |                                |     |                                |     |      |  |
| uart_rx[1:0], uart_tx[1:0], uart_cts_n[0],<br>uart_dsr_n[0], uart_dtr_n[0], uart_rts_n[0] | Tsu7           | cpu_masterclk rising   | 15                             | —   | 12                             | —   | 10                             | —   | ns   | Chapter 17,<br>Figure 17.16                                |
| uart_rx[1:0], uart_tx[1:0], uart_cts_n[0],<br>uart_dsr_n[0], uart_dtr_n[0], uart_rts_n[0] | Thld9          | cpu_masterclk rising   | 15                             | —   | 12                             | —   | 10                             | —   | ns   |  |
| uart_rx[1:0], uart_tx[1:0], uart_cts_n[0],<br>uart_dsr_n[0], uart_dtr_n[0], uart_rts_n[0] | Tdo16          | cpu_masterclk rising   | —                              | 15  | —                              | 12  | —                              | 10  | ns   |  |
| uart_rx[1:0], uart_tx[1:0], uart_cts_n[0],<br>uart_dsr_n[0], uart_dtr_n[0], uart_rts_n[0] | Tdoh8          | cpu_masterclk rising   | 1                              | —   | 1                              | —   | 1                              | —   | ns   |  |
| <b>SPI Interface</b>  |                |                        |                                |     |                                |     |                                |     |      |  |
| spi_clk, spi_mosi, spi_miso   | Tsu7           | cpu_masterclk rising   | 15                             | —   | 12                             | —   | 10                             | —   | ns   | Chapter 18,<br>Figures 18.8<br>and 18.9                    |
| spi_clk, spi_mosi, spi_miso   | Thld9          | cpu_masterclk rising   | 15                             | —   | 12                             | —   | 10                             | —   | ns   |  |
| spi_clk, spi_mosi, spi_miso   | Tdo16          | cpu_masterclk rising   | —                              | 15  | —                              | 12  | —                              | 10  | ns   |  |
| spi_clk, spi_mosi, spi_miso   | Tdoh8          | cpu_masterclk rising   | 1                              | —   | 1                              | —   | 1                              | —   | ns   |  |
| <b>Reset</b>  |                |                        |                                |     |                                |     |                                |     |      |  |
| mem_addr[19:17]   | Tsu10          | cpu_coldreset_n rising | 10                             | —   | 10                             | —   | 10                             | —   | ms   | Chapter 19<br>Figures 19.8<br>and 19.9                     |
| mem_addr[19:17]   | Thld10         | cpu_coldreset_n rising | 1                              | —   | 1                              | —   | 1                              | —   | ns   |  |
| mem_addr[22:20],  | Tsu22          | cpu_masterclk rising   | 9                              | —   | 7                              | —   | 6                              | —   | ns   |  |
| mem_addr[22:20]   | Thld22         | cpu_masterclk rising   | 1                              | —   | 1                              | —   | 1                              | —   | ns   |  |
| <b>Debug Interface</b>  |                |                        |                                |     |                                |     |                                |     |      |  |
| debug_cpu_dma_n, debug_cpu_ack_n,<br>debug_cpu_ads_n, debug_cpu_i_d_n,<br>ejtag_pcst[2:0] | Tsu20          | cpu_coldreset_n rising | 10                             | —   | 10                             | —   | 10                             | —   | ms   | Chapter 19,<br>Figure 19.9 and<br>Chapter 9,<br>Figure 9.2 |
| debug_cpu_dma_n, debug_cpu_ack_n,<br>debug_cpu_ads_n, debug_cpu_i_d_n,<br>ejtag_pcst[2:0] | Thld20         | cpu_coldreset_n rising | 1                              | —   | 1                              | —   | 1                              | —   | ns   |  |
| debug_cpu_dma_n, debug_cpu_ack_n,<br>debug_cpu_ads_n, debug_cpu_i_d_n                     | Tdo20          | cpu_masterclk rising   | —                              | 15  | —                              | 12  | —                              | 10  | ns   |  |
| debug_cpu_dma_n, debug_cpu_ack_n,<br>debug_cpu_ads_n, debug_cpu_i_d_n                     | Tdoh20         | cpu_masterclk rising   | 1                              | —   | 1                              | —   | 1                              | —   | ns   |  |
| <b>JTAG Interface</b>   |                |                        |                                |     |                                |     |                                |     |      |  |
| jtag_tms, jtag_tdi, jtag_trst_n   | t <sub>5</sub> | jtag_tck rising        | 10                             | —   | 10                             | —   | 10                             | —   | ns   | See Figure 4<br>below.                                     |
| jtag_tms, jtag_tdi, jtag_trst_n   | t <sub>6</sub> | jtag_tck rising        | 10                             | —   | 10                             | —   | 10                             | —   | ns   |  |
| jtag_tdo  | t <sub>4</sub> | jtag_tck falling       | —                              | 10  | —                              | 10  | —                              | 10  | ns   |  |

Table 6 AC Timing Characteristics - RC32334 (Part 3 of 4)

| Signal                       | Symbol                                 | Reference Edge    | RC32334 <sup>1</sup><br>100MHz |     | RC32334 <sup>1</sup><br>133MHz |     | RC32334 <sup>1</sup><br>150MHz |     | Unit | User Manual Timing Diagram Reference |
|------------------------------|--|-------------------|--------------------------------|-----|--------------------------------|-----|--------------------------------|-----|------|--------------------------------------|
|                              |  |                   | Min                            | Max | Min                            | Max | Min                            | Max |      |                                      |
| <b>EJTAG Interface</b>       |  |                   |                                |     |                                |     |                                |     |      |                                      |
| ejtag_tms, ejtag_debugboot   | t <sub>5</sub>                         | jtag_tclk rising  | 4                              | —   | 4                              | —   | 4                              | —   | ns   | See Figure 4 below.                  |
| ejtag_tms, ejtag_debugboot   | t <sub>6</sub>                         | jtag_clk rising   | 2                              | —   | 2                              | —   | 2                              | —   | ns   |                                      |
| jtag_tdo Output Delay Time   | t <sub>TDODO</sub> , t <sub>4</sub>    | jtag_tck falling  | —                              | 6   | —                              | 6   | —                              | 6   | ns   |                                      |
| jtag_tdi Input Setup Time    | t <sub>TDIS</sub> , t <sub>5</sub>     | jtag_tck rising   | 4                              | —   | 4                              | —   | 4                              | —   | ns   |                                      |
| jtag_tdi Input Hold Time     | t <sub>TDIH</sub> , t <sub>6</sub>     | jtag_tck rising   | 2                              | —   | 2                              | —   | 2                              | —   | ns   |                                      |
| jtag_trst_n Low Time         | t <sub>TRSTLow</sub> , t <sub>12</sub> | —                 | 100                            | —   | 100                            | —   | 100                            | —   | ns   |                                      |
| jtag_trst_n Removal Time     | t <sub>TRSTR</sub> , t <sub>13</sub>   | jtag_tck rising   | 3                              | —   | 3                              | —   | 3                              | —   | ns   |                                      |
| ejtag_tpc Output Delay Time  | t <sub>TPCDO</sub> , t <sub>8</sub>    | ejtag_dclk rising | -1                             | 3   | -1                             | 3   | -1                             | 3   | ns   |                                      |
| ejtag_pcst Output Delay Time | t <sub>PCSTDO</sub> , t <sub>7</sub>   | ejtag_dclk rising | -1                             | 3   | -1                             | 3   | -1                             | 3   | ns   |                                      |

Table 6 AC Timing Characteristics - RC32334 (Part 4 of 4)

<sup>1</sup>. At all pipeline frequencies.

<sup>2</sup>. Guaranteed by design.

<sup>3</sup>. pci\_rst\_n is tested per PCI 2.2 as an asynchronous signal.

### Standard EJTAG Timing — RC32334

Figure 4 represents the timing diagram for the EJTAG interface signals.

The standard JTAG connector is a 10-pin connector providing 5 signals and 5 ground pins. For Standard EJTAG, a 24-pin connector has been chosen providing 12 signals and 12 ground pins. This guarantees elimination of noise problems by incorporating signal-ground type arrangement. Refer to the RC32334 User Reference Manual for connector pinout and mechanical specifications.

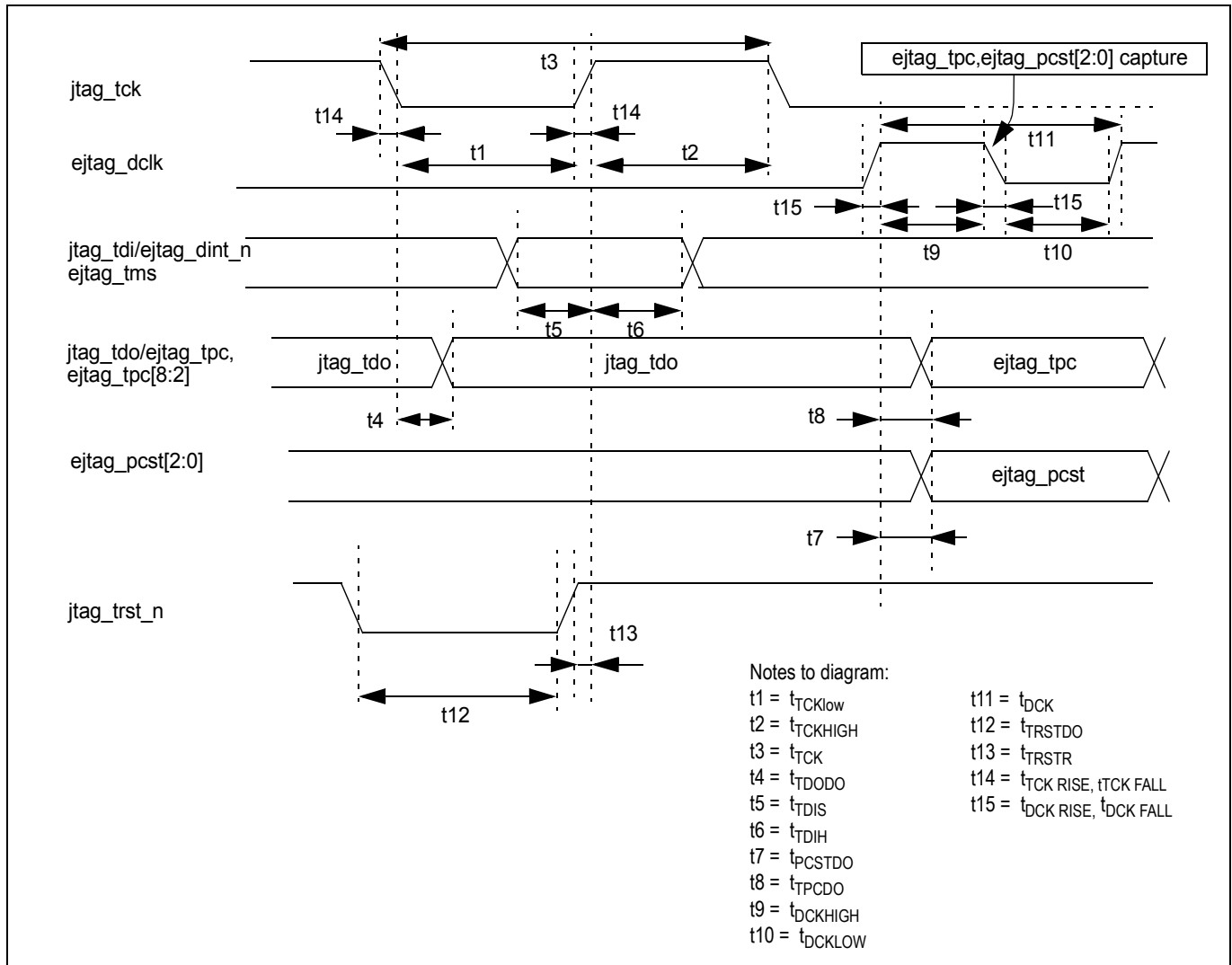
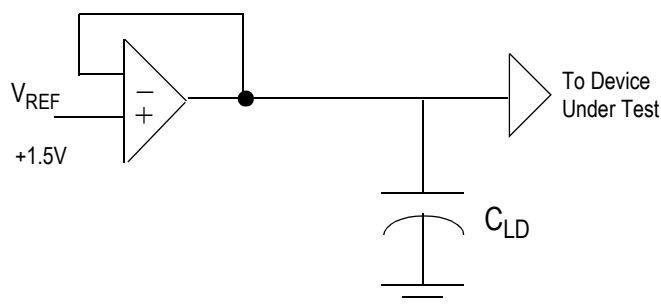


Figure 4 Standard EJTAG Timing

## Output Loading for AC Testing



| Signal                 | C <sub>ld</sub> |
|------------------------|-----------------|
| All High Drive Signals | 50 pF           |
| All Low Drive Signals  | 25 pF           |

Figure 5 Output Loading for AC Testing

Note: PCI pins have been correlated to PCI 2.2.

## Recommended Operation Temperature and Supply Voltage

| Grade      | Temperature              | Gnd | V <sub>cc</sub> IO | V <sub>cc</sub> Core | V <sub>cc</sub> P |
|------------|--------------------------|-----|--------------------|----------------------|-------------------|
| Commercial | 0°C to +70°C (Ambient)   | 0V  | 3.3V±5%            | 3.3V±5%              | 3.3V±5%           |
| Industrial | -40°C to +85°C (Ambient) | 0V  | 3.3V±5%            | 3.3V±5%              | 3.3V±5%           |

Table 7 Temperature and Voltage

## DC Electrical Characteristics — RC32334

Commercial Temperature Range—RC32334

(T<sub>a</sub> = 0°C to +70°C Commercial, T<sub>a</sub> = -40°C to +85°C Industrial, V<sub>cc</sub> I/O = +3.3V±5%, V<sub>cc</sub> Core = +3.3V±5%)

|                        | Parameter       | RC32334 <sup>1</sup>   |         | Pin Numbers  | Conditions                |
|------------------------|-----------------|------------------------|---------|--|---------------------------|
|                        |                 | Minimum                | Maximum |  |                           |
| Input Pads             | V <sub>IL</sub> | —                      | 0.8V    | B14, E13, F4, K1, L2, M1, M3, M4, M14, N1-N3, P14, R2, R16   | —                         |
|                        | V <sub>IH</sub> | 2.0V                   | —       |  | —                         |
| LOW Drive Output Pads  | V <sub>OL</sub> | —                      | 0.4V    | A1, A12, A15, A16, B1, B2, B12, B15, C1-C3, C12, C13, C14, D12, D13, E1-E4, F1, F2, G1-G4, H1, H2, J1, J2, K2-K4, L1, L3, L4, P3, P14, R2, R15, R16, T16   | I <sub>OUT</sub>   = 6mA  |
|                        | V <sub>OH</sub> | V <sub>cc</sub> - 0.4V | —       |  | I <sub>OUT</sub>   = 8mA  |
|                        | V <sub>IL</sub> | —                      | 0.8V    |  | —                         |
|                        | V <sub>IH</sub> | 2.0V                   | —       |  | —                         |
| HIGH Drive Output Pads | V <sub>OL</sub> | —                      | 0.4V    | A2-A4, A6-A11, A13, A14, B3, B4, B6-B11, B13, B16, C4, C6-C8, C10, C11, C15, C16, D1-D4, D6, D7, D10, D11, D14-D16, E14, E15, F3, F13-F16, G13-G16, H15, H16, J13, J14, K5, K13, K14, K16, L13-L16, M2, M13, M16, P2, P4, R1, R3, R4 | I <sub>OUT</sub>   = 7mA  |
|                        | V <sub>OH</sub> | V <sub>cc</sub> - 0.4V | —       |  | I <sub>OUT</sub>   = 16mA |
|                        | V <sub>IL</sub> | —                      | 0.8V    |  | —                         |
|                        | V <sub>IH</sub> | 2.0V                   | —       |  | —                         |
| PCI Drive Input Pads   | V <sub>IL</sub> | —                      | —       | P1, R1, R10, T2, T3  | Per PCI 2.2               |
|                        | V <sub>IH</sub> | —                      | —       |  |                           |

Table 8 DC Electrical Characteristics - RC32334 (Part 1 of 2)

|                       | Parameter    | RC32334 <sup>1</sup> |            | Pin Numbers   | Conditions           |
|-----------------------|--------------|----------------------|------------|---|----------------------|
|                       |              | Minimum              | Maximum    |   |                      |
| PCI Drive Output Pads | $V_{OL}$     | —                    | —          | M15, N4-N7, N10-N16, P5-P13, P15, P16, R5-R9, R11-R14, T4-T15 | Per PCI 2.2          |
|                       | $V_{OH}$     | —                    | —          |   |                      |
|                       | $V_{IL}$     | —                    | —          |   |                      |
|                       | $V_{IH}$     | —                    | —          |   |                      |
| All Pads              | $C_{IN}$     | —                    | 10pF       | All input pads except T3 and R3                               | —                    |
|                       | $C_{IN}^2$   | 5pF                  | 12pF       | T3  | Per PCI 2.2          |
|                       | $C_{IN}^3$   | —                    | 8pF        | R3  | Per PCI 2.2          |
|                       | $C_{OUT}$    | —                    | 10pF       | All output pads   | —                    |
|                       | $I/O_{LEAK}$ | —                    | 10 $\mu$ A | All non-internal pull-up pins                                 | Input/Output Leakage |
|                       | $I/O_{LEAK}$ | —                    | 50 $\mu$ A | All internal pull-up pins                                     | Input/Output Leakage |

Table 8 DC Electrical Characteristics - RC32334 (Part 2 of 2)

<sup>1</sup>: At all pipeline frequencies.

<sup>2</sup>: Applies only to pad T3.

<sup>3</sup>: Applies only to pad R3.

### Capacitive Load Deration — RC32334

Refer to the IDT document [79RC32334 IBIS Model](#) located on the company's web site.

### Power Consumption — RC32334

**Note:** This table is based on a 2:1 pipeline-to-bus clock ratio.

| Parameter         |                           | 100MHz RC32334 |      | 133MHz RC32334 |      | 150MHz RC32334 |      | Unit | Conditions  |
|-------------------|---------------------------|----------------|------|----------------|------|----------------|------|------|---|
|                   |                           | Typical        | Max. | Typical        | Max. | Typical        | Max. |      |   |
| $I_{CC}$          | Normal mode               | 360            | 480  | 480            | 630  | 550            | 700  | mA   | $C_L$ = (See Figure 5, Output Loading for AC Testing)<br>$T_a = 25^\circ\text{C}$<br>$V_{CC}$ core = 3.46V (for max. values)<br>$V_{CC}$ I/O = 3.46V (for max. values)<br>$V_{CC}$ core = 3.3V (for typical values)<br>$V_{CC}$ I/O = 3.3V (for typical values) |
|                   | Standby mode <sup>1</sup> | 250            | 370  | 330            | 480  | 390            | 540  | mA   |   |
| Power Dissipation | Normal mode               | 1.2            | 1.7  | 1.5            | 2.2  | 1.7            | 2.4  | W    |   |
|                   | Standby mode <sup>1</sup> | .87            | 1.3  | 1.1            | 1.7  | 1.3            | 1.9  | W    |   |

Table 9 Power Consumption

<sup>1</sup>: RISCORE 32300 CPU core enters Standby mode by executing WAIT instructions. On-chip logic outside the CPU core continues to function.

### Power Ramp-up

There is no special requirement for how fast  $V_{CC}$  I/O ramps up to 3.3V. However, all timing references are based on a stable  $V_{CC}$  I/O.

## Power Curves

The following two graphs contain the simulated power curves that show power consumption at various bus frequencies.

**Note:** Only pipeline frequencies that are integer multiples (2x, 3x, 4x) of bus frequencies are supported.

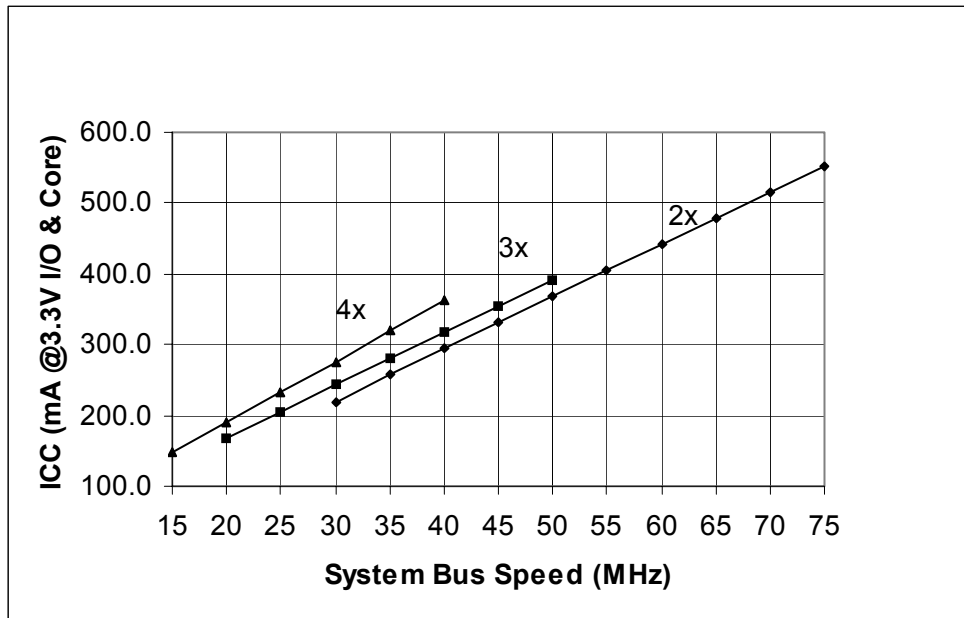


Figure 6 Typical Power Usage - RC32334

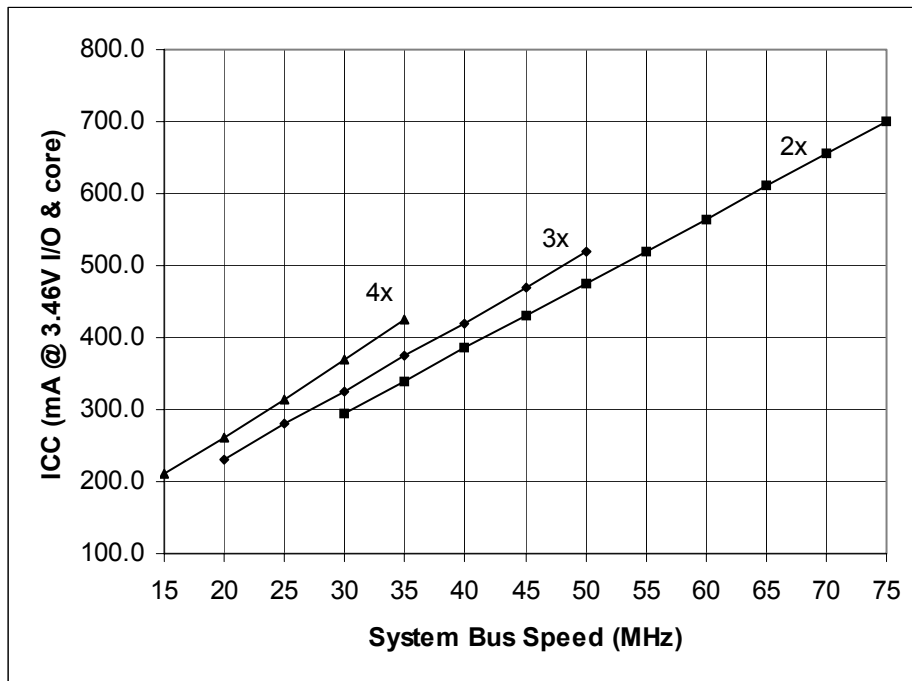


Figure 7 Maximum Power Usage - RC32334

## Absolute Maximum Ratings

| Symbol            | Parameter                               | Min <sup>1</sup> | Max <sup>1</sup> | Unit      |
|-------------------|---|------------------|------------------|-----------|
| V <sub>CC</sub>   | Supply Voltage                          | -0.3             | 4.0              | V         |
| V <sub>i</sub>    | Input Voltage                           | -0.3             | 5.5              | V         |
| V <sub>imin</sub> | Input Voltage - undershoot <sup>2</sup> | -0.6             | —                | V         |
| T <sub>stg</sub>  | Storage Temperature                     | -40              | 125              | degrees C |

**Table 10 Absolute Maximum Ratings**

<sup>1</sup> Functional and tested operating conditions are given in Table 7. Absolute maximum ratings are stress ratings only, and functional operation is not guaranteed beyond recommended operating voltages and temperatures. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

<sup>2</sup> All PCI pads are fully compatible with PCI Specification version 2.2.

## Package Pin-out — 256-PBGA Pinout for RC32334

The following table lists the pin numbers and signal names for the RC32334. Signal names ending with an “\_n” are active when low.

| Pin | Function          | Alt | Pin | Function             | Alt | Pin | Function             | Alt | Pin | Function             | Alt |
|-----|-------------------|-----|-----|----------------------|-----|-----|----------------------|-----|-----|----------------------|-----|
| A1  | uart_cts_n[0]     | 1   | E1  | mem_cs_n[4]          |     | J1  | debug_cpu_dma_n      | 1   | N1  | cpu_int_n[1]         |     |
| A2  | sdram_245_oe_n    |     | E2  | mem_cs_n[5]          |     | J2  | debug_cpu_ack_n      | 1   | N2  | cpu_int_n[0]         |     |
| A3  | sdram_cas_n       |     | E3  | mem_cs_n[3]          |     | J3  | V <sub>CC</sub> IO   |     | N3  | jtag_tdi             |     |
| A4  | sdram_bemask_n[1] |     | E4  | mem_cs_n[2]          |     | J4  | V <sub>SS</sub>      |     | N4  | pci_ad[30]           |     |
| A5  | sdram_ras_n       |     | E5  | V <sub>CC</sub> IO   |     | J5  | V <sub>CC</sub> IO   |     | N5  | pci_ad[26]           |     |
| A6  | mem_addr[3]       | 1   | E6  | V <sub>CC</sub> IO   |     | J6  | V <sub>SS</sub>      |     | N6  | pci_ad[23]           |     |
| A7  | mem_addr[7]       | 1   | E7  | V <sub>CC</sub> IO   |     | J7  | V <sub>SS</sub>      |     | N7  | pci_ad[19]           |     |
| A8  | mem_addr[11]      | 1   | E8  | V <sub>CC</sub> IO   |     | J8  | V <sub>SS</sub>      |     | N8  | V <sub>CC</sub> core |     |
| A9  | sdram_cke         |     | E9  | V <sub>CC</sub> IO   |     | J9  | V <sub>SS</sub>      |     | N9  | V <sub>SS</sub>      |     |
| A10 | sdram_bemask_n[2] |     | E10 | V <sub>CC</sub> IO   |     | J10 | V <sub>SS</sub>      |     | N10 | pci_trdy_n           |     |
| A11 | mem_addr[15]      | 1   | E11 | V <sub>CC</sub> IO   |     | J11 | V <sub>SS</sub>      |     | N11 | pci_perr_n           |     |
| A12 | mem_addr[19]      | 1   | E12 | V <sub>CC</sub> IO   |     | J12 | V <sub>CC</sub> IO   |     | N12 | pci_ad[15]           |     |
| A13 | mem_data[10]      |     | E13 | cpu_masterclk        |     | J13 | mem_data[26]         |     | N13 | pci_ad[1]            |     |
| A14 | mem_data[20]      |     | E14 | mem_data[15]         |     | J14 | mem_data[5]          |     | N14 | pci_ad[3]            |     |
| A15 | mem_addr[23]      |     | E15 | mem_data[16]         |     | J15 | V <sub>CC</sub> core |     | N15 | pci_ad[4]            |     |
| A16 | timer_tc_n[0]     | 2   | E16 | V <sub>CC</sub> core |     | J16 | V <sub>SS</sub>      |     | N16 | pci_ad[2]            |     |
| B1  | uart_rts_n[0]     | 1   | F1  | mem_cs_n[0]          |     | K1  | ejtag_debugboot      |     | P1  | pci_rst_n            |     |
| B2  | uart_dsr_n[0]     | 1   | F2  | mem_cs_n[1]          |     | K2  | ejtag_dclk           |     | P2  | pci_gnt_n[2]         | 1   |
| B3  | sdram_we_n        |     | F3  | mem_oe_n             |     | K3  | debug_cpu_i_d_n      | 1   | P3  | dma_ready_n[1]       | 2   |
| B4  | sdram_bemask_n[0] |     | F4  | mem_wait_n           | 1   | K4  | debug_cpu_ads_n      | 1   | P4  | pci_req_n[0]         |     |
| B5  | sdram_cs_n[1]     |     | F5  | V <sub>CC</sub> IO   |     | K5  | V <sub>CC</sub> IO   |     | P5  | pci_ad[27]           |     |
| B6  | mem_addr[2]       | 1   | F6  | V <sub>SS</sub>      |     | K6  | V <sub>SS</sub>      |     | P6  | pci_cbe_n[3]         |     |
| B7  | mem_addr[6]       | 1   | F7  | V <sub>SS</sub>      |     | K7  | V <sub>SS</sub>      |     | P7  | pci_ad[20]           |     |
| B8  | mem_addr[10]      | 1   | F8  | V <sub>SS</sub>      |     | K8  | V <sub>SS</sub>      |     | P8  | pci_ad[16]           |     |

**Table 11 RC32334 256-pin PBGA Package Pin-Out (Part 1 of 3)**

| Pin | Function             | Alt | Pin | Function             | Alt | Pin | Function           | Alt | Pin | Function        | Alt |
|-----|----------------------|-----|-----|----------------------|-----|-----|--------------------|-----|-----|-----------------|-----|
| B9  | sdram_addr[12]       |     | F9  | V <sub>SS</sub>      |     | K9  | V <sub>SS</sub>    |     | P9  | pci_cbe_n[2]    |     |
| B10 | sdram_bemask_n[3]    |     | F10 | V <sub>SS</sub>      |     | K10 | V <sub>SS</sub>    |     | P10 | pci_devsel_n    |     |
| B11 | mem_addr[16]         | 1   | F11 | V <sub>SS</sub>      |     | K11 | V <sub>SS</sub>    |     | P11 | pci_serr_n      |     |
| B12 | mem_addr[20]         | 1   | F12 | V <sub>CC</sub> IO   |     | K12 | V <sub>CC</sub> IO |     | P12 | pci_ad[14]      |     |
| B13 | mem_data[11]         |     | F13 | mem_data[1]          |     | K13 | cpu_dt_r_n         | 2   | P13 | pci_ad[11]      |     |
| B14 | cpu_coldreset_n      |     | F14 | mem_data[30]         |     | K14 | mem_data[6]        |     | P14 | cpu_int_n[5]    |     |
| B15 | mem_addr[25]         |     | F15 | mem_data[31]         |     | K15 | mem_data[24]       |     | P15 | pci_ad[6]       |     |
| B16 | mem_data[12]         |     | F16 | mem_data[0]          |     | K16 | mem_data[25]       |     | P16 | pci_ad[5]       |     |
| C1  | uart_rx[0]           | 1   | G1  | dma_ready_n[0]       | 2   | L1  | ejtag_pcst[0]      |     | R1  | pci_req_n[2]    | 1   |
| C2  | uart_tx[0]           | 1   | G2  | mem_245_oe_n         |     | L2  | jtag_trst_n        |     | R2  | cpu_int_n[2]    |     |
| C3  | uart_dtr_n[0]        | 1   | G3  | spi_mosi             | 2   | L3  | ejtag_pcst[1]      | 1   | R3  | pci_gnt_n[1]    | 2   |
| C4  | sdram_cs_n[0]        |     | G4  | spi_miso             | 2   | L4  | ejtag_pcst[2]      | 1   | R4  | pci_gnt_n[0]    |     |
| C5  | sdram_s_n[0]         |     | G5  | V <sub>CC</sub> IO   |     | L5  | V <sub>CC</sub> IO |     | R5  | pci_ad[29]      |     |
| C6  | mem_addr[4]          | 1   | G6  | V <sub>SS</sub>      |     | L6  | V <sub>SS</sub>    |     | R6  | pci_ad[25]      |     |
| C7  | mem_addr[9]          | 1   | G7  | V <sub>SS</sub>      |     | L7  | V <sub>SS</sub>    |     | R7  | pci_ad[22]      |     |
| C8  | output_clk           |     | G8  | V <sub>SS</sub>      |     | L8  | V <sub>SS</sub>    |     | R8  | pci_ad[18]      |     |
| C9  | mem_addr[12]         |     | G9  | V <sub>SS</sub>      |     | L9  | V <sub>SS</sub>    |     | R9  | pci_irdy_n      |     |
| C10 | sdram_cs_n[3]        |     | G10 | V <sub>SS</sub>      |     | L10 | V <sub>SS</sub>    |     | R10 | pci_lock_n      |     |
| C11 | mem_addr[14]         | 1   | G11 | V <sub>SS</sub>      |     | L11 | V <sub>SS</sub>    |     | R11 | pci_cbe_n[1]    |     |
| C12 | mem_addr[18]         | 1   | G12 | V <sub>CC</sub> IO   |     | L12 | V <sub>CC</sub> IO |     | R12 | pci_ad[12]      |     |
| C13 | mem_addr[22]         | 1   | G13 | mem_data[3]          |     | L13 | mem_data[7]        |     | R13 | pci_ad[10]      |     |
| C14 | mem_addr[24]         |     | G14 | mem_data[28]         |     | L14 | mem_data[8]        |     | R14 | pci_cbe_n[0]    |     |
| C15 | mem_data[19]         |     | G15 | mem_data[29]         |     | L15 | mem_data[22]       |     | R15 | uart_tx[1]      | 1   |
| C16 | mem_data[13]         |     | G16 | mem_data[2]          |     | L16 | mem_data[23]       |     | R16 | cpu_int_n[4]    |     |
| D1  | mem_we_n[1]          |     | H1  | spi_ss_n             | 1   | M1  | jtag_tms           |     | T1  | V <sub>SS</sub> |     |
| D2  | mem_we_n[3]          |     | H2  | spi_sck              | 2   | M2  | jtag_tdo           |     | T2  | pci_req_n[1]    | 1   |
| D3  | mem_we_n[2]          |     | H3  | V <sub>CC</sub> IO   |     | M3  | ejtag_tms          |     | T3  | pci_clk         |     |
| D4  | mem_we_n[0]          |     | H4  | V <sub>CC</sub> core |     | M4  | jtag_tck           |     | T4  | pci_ad[31]      |     |
| D5  | sdram_s_n[1]         |     | H5  | V <sub>CC</sub> IO   |     | M5  | V <sub>CC</sub> IO |     | T5  | pci_ad[28]      |     |
| D6  | mem_addr[5]          | 1   | H6  | V <sub>SS</sub>      |     | M6  | V <sub>CC</sub> IO |     | T6  | pci_ad[24]      |     |
| D7  | mem_addr[8]          | 1   | H7  | V <sub>SS</sub>      |     | M7  | V <sub>CC</sub> IO |     | T7  | pci_ad[21]      |     |
| D8  | V <sub>SS</sub>      |     | H8  | V <sub>SS</sub>      |     | M8  | V <sub>CC</sub> IO |     | T8  | pci_ad[17]      |     |
| D9  | V <sub>CC</sub> core |     | H9  | V <sub>SS</sub>      |     | M9  | V <sub>CC</sub> IO |     | T9  | pci_frame_n     |     |
| D10 | sdram_cs_n[2]        |     | H10 | V <sub>SS</sub>      |     | M10 | V <sub>CC</sub> IO |     | T10 | pci_stop_n      |     |
| D11 | mem_addr[13]         | 1   | H11 | V <sub>SS</sub>      |     | M11 | V <sub>CC</sub> IO |     | T11 | pci_par         |     |
| D12 | mem_addr[17]         | 1   | H12 | V <sub>CC</sub> IO   |     | M12 | V <sub>CC</sub> IO |     | T12 | pci_ad[13]      |     |
| D13 | mem_addr[21]         | 1   | H13 | V <sub>SS</sub> P    |     | M13 | mem_data[9]        |     | T13 | pci_ad[9]       |     |

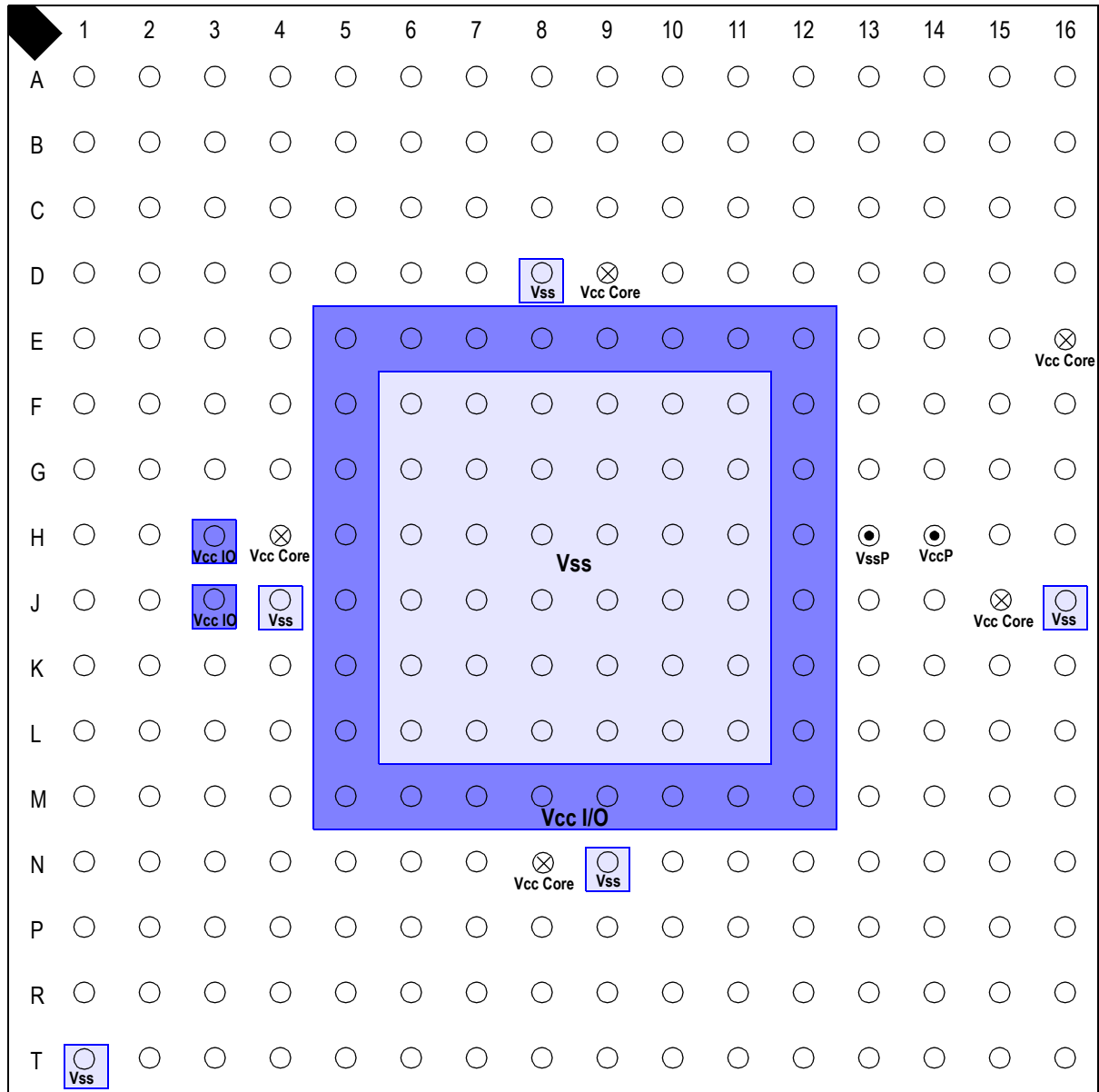
Table 11 RC32334 256-pin PBGA Package Pin-Out (Part 2 of 3)



| Pin | Function     | Alt | Pin | Function          | Alt | Pin | Function     | Alt | Pin | Function   | Alt |
|-----|--------------|-----|-----|-------------------|-----|-----|--------------|-----|-----|------------|-----|
| D14 | mem_data[17] |     | H14 | V <sub>cc</sub> P |     | M14 | cpu_nmi_n    |     | T14 | pci_ad[8]  |     |
| D15 | mem_data[14] |     | H15 | mem_data[27]      |     | M15 | pci_ad[0]    |     | T15 | pci_ad[7]  |     |
| D16 | mem_data[18] |     | H16 | mem_data[4]       |     | M16 | mem_data[21] |     | T16 | uart_rx[1] | 1   |

Table 11 RC32334 256-pin PBGA Package Pin-Out (Part 3 of 3)

# Pin Layout







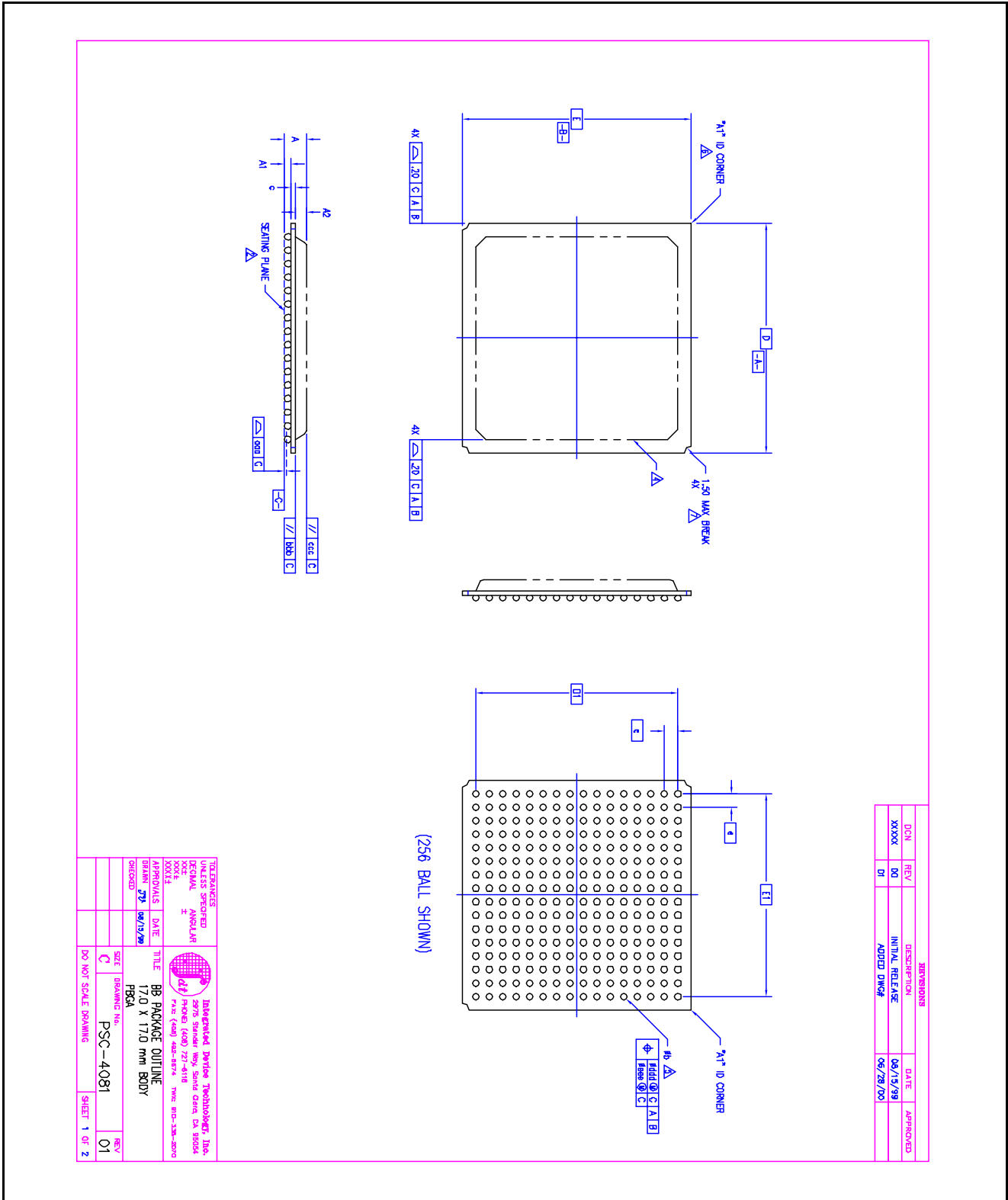
-  The lighter shaded area shows the ground pins (Vss)
-  The darker shaded area shows the supply voltage pins (Vcc I/O)
-  Vcc Core
-  VccP, VssP

Figure 8 RC32334 Chip — Top View

**RC32334 Alternate Signal Functions**

| Pin | Alt #1              | Alt #2          | Pin | Alt #1             | Alt #2          | Pin | Alt #1                     | Alt #2           |
|-----|---------------------|-----------------|-----|--------------------|-----------------|-----|----------------------------|------------------|
| A1  | PIO[15]             |                 | C3  | PIO[13]            | C3              | H2  | PIO[9]                     | pci_eeeprom_sk   |
| A6  | sdram_addr[3]       |                 | C6  | sdram_addr[4]      |                 | J1  | modebit[6]                 |                  |
| A7  | sdram_addr[7]       |                 | C7  | sdram_addr[9]      |                 | J2  | modebit[4]                 |                  |
| A8  | sdram_addr[11]      |                 | C11 | sdram_addr[14]     |                 | K3  | modebit[3]                 |                  |
| A11 | sdram_addr[15]      |                 | C12 | modebit[8]         |                 | K4  | modebit[5]                 |                  |
| A12 | modebit[9]          |                 | C13 | reset_boot_mode[1] |                 | K13 | mem_245_dt_r_n             | sdram_245_dt_r_n |
| A16 | PIO[2]              | timer_gate_n[0] | D6  | sdram_addr[5]      |                 | L1  | modebit[0]                 |                  |
| B1  | PIO[12]             |                 | D7  | sdram_addr[8]      |                 | L3  | modebit[1]                 |                  |
| B2  | PIO[14]             |                 | D11 | sdram_addr[13]     |                 | L4  | modebit[2]                 |                  |
| B6  | sdram_addr[2]       |                 | D12 | modebit[7]         |                 | P2  | pci_inta_n (satellite)     |                  |
| B7  | sdram_addr[6]       |                 | D13 | reset_boot_mode[0] |                 | P3  | PIO[0]                     | dma_done_n[1]    |
| B8  | sdram_addr[10]      |                 | F4  | sdram_wait_n       |                 | R1  | pci_idsel (satellite)      |                  |
| B11 | sdram_addr[16]      |                 | G1  | PIO[1]             | dma_done_n[0]   | R3  | pci_eeeprom_cs (satellite) | PIO[11]          |
| B12 | reset_pci_host_mode |                 | G3  | PIO[10]            | pci_eeeprom_mdo | R15 | PIO[3]                     |                  |
| C1  | PIO[6]              |                 | G4  | PIO[7]             | pci_eeeprom_mdi | T2  | Unused (satellite)         |                  |
| C2  | PIO[5]              |                 | H1  | PIO[8]             |                 | T16 | PIO[4]                     |                  |

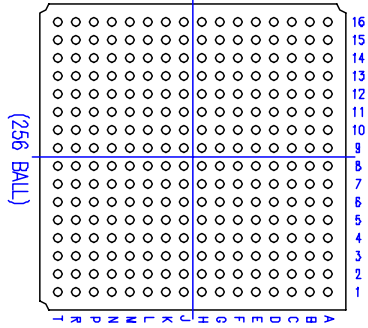
# RC32334 Package Drawing — 256-pin PBGA



| REVISIONS |     | DATE     | APPROVED |
|-----------|-----|----------|----------|
| 001       | REV | 06/15/98 |          |
| 002       | DO  | 06/28/00 |          |
| 003       | DI  |          |          |

|                                |         |   |                     |
|--------------------------------|---------|---|---------------------|
| TOLERANCES<br>UNLESS SPECIFIED |         | <b>Integrated Device Technology, Inc.</b><br>2975 Strider Way, Santa Clara, CA 95054<br>Phone (408) 737-4118 Fax (408) 486-8719 |                     |
| DECIMAL                        | ANGULAR | TITLE <b>BB PACKAGE OUTLINE</b><br>17.0 X 17.0 mm BODY<br>PBGA  |                     |
| 0.001                          | ±       | DATE  | 06/15/98            |
| 0.001                          | ±       | APPROVALS   |                     |
| 0.001                          | ±       | DRN   | 72V                 |
| 0.001                          | ±       | ORGRD   |                     |
| 0.001                          | ±       | SIZE  | 17.0 X 17.0 mm BODY |
| 0.001                          | ±       | DRAWING NO.   | PSC-4081            |
| 0.001                          | ±       | REV   | 01                  |
| 0.001                          | ±       | DO NOT SCALE DRAWING  | SHEET 1 OF 2        |

RC32334 Package Drawing — Page Two



| SYMBOL | DIMEN. B8256-1        |      |      | NOM. | MAX. | NOM. |
|--------|-----------------------|------|------|------|------|------|
|        | JEDEC VARIATION AAF-1 |      |      |      |      |      |
| A      | —                     | 2.15 | 3.50 |      |      |      |
| A1     | .30                   | .40  | .50  |      |      |      |
| A2     | —                     | —    | 2.50 |      |      |      |
| D      | 17.00 BSC             |      |      |      |      |      |
| D1     | 15.00 BSC             |      |      |      |      |      |
| E      | 17.00 BSC             |      |      |      |      |      |
| E1     | 15.00 BSC             |      |      |      |      |      |
| MD     | 16                    |      |      |      |      | 3    |
| ME     | 16                    |      |      |      |      | 3    |
| N      | 256                   |      |      |      |      | 3    |
| e      | 1.00 BSC              |      |      |      |      |      |
| b      | .40                   | .50  | .60  |      |      | 5    |
| c      | .10                   | —    | 2.50 |      |      |      |
| ddd    | —                     | —    | .20  |      |      |      |
| ddd    | —                     | —    | .25  |      |      |      |
| ccc    | —                     | —    | .35  |      |      |      |
| ddd    | —                     | —    | .30  |      |      |      |
| eee    | —                     | —    | .10  |      |      |      |

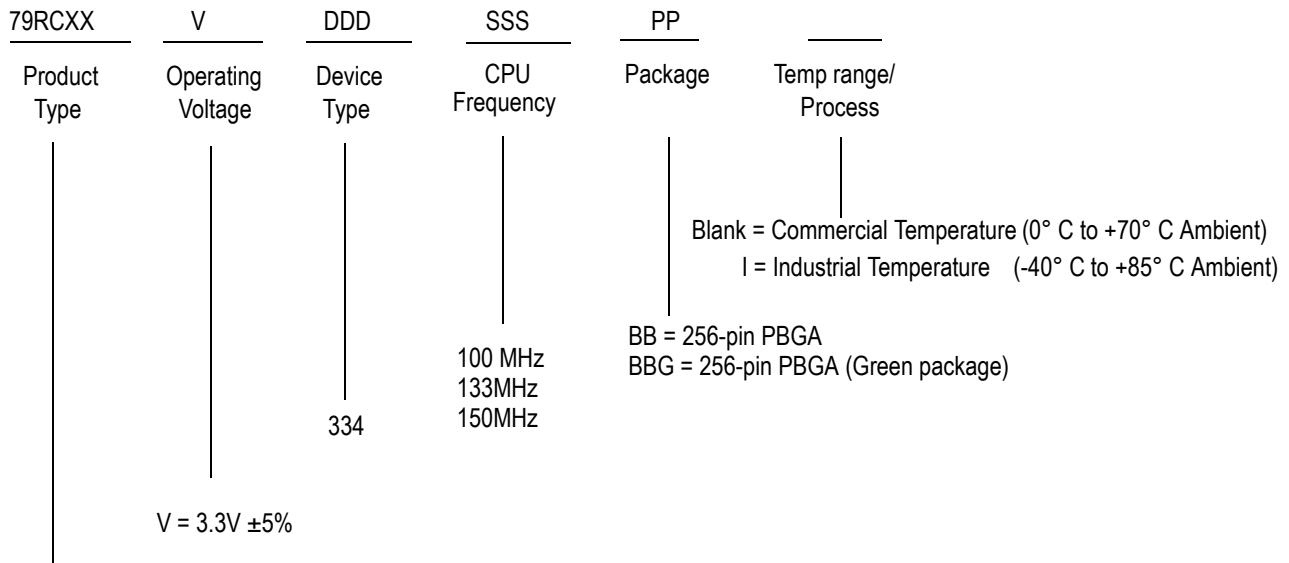
| REVISIONS |     |                 |          |
|-----------|-----|-----------------|----------|
| DCN       | REV | DESCRIPTION     | DATE     |
| XXXX      | D0  | INITIAL RELEASE | 06/15/99 |
|           | D1  | ADDED DIMEN     | 06/28/00 |

NOTES:

- 1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994
- 2 SEATING PLANE AND PRIMARY DATUM  $\text{---C---}$  ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS
- 3  $M_D^*$  IS THE BALL MATRIX SIZE IN THE "D" DIRECTION  
 $M_E^*$  IS THE BALL MATRIX SIZE IN THE "E" DIRECTION  
 $N^*$  IS THE NUMBER OF SOLDER BALLS
- 4 PACKAGE MAY EXTEND TO EDGE PERIPHERY AND MAY CONSIST OF MOLDED COMPOUND, EPOXY, METAL, CERAMIC OR OTHER MATERIAL
- 5 DIMENSION  $b^*$  IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM  $\text{---C---}$
- 6  $A_1^*$  ID CORNER MUST BE IDENTIFIED. IDENTIFICATION MAY BE BY MEANS OF CHAMFER, METALLIZED OR INK MARK, INDENTATION OR OTHER FEATURE OF THE PACKAGE BODY. MARK MUST BE VISIBLE FROM TOP SURFACE
- 7 ACTUAL SHAPE OF THIS FEATURE IS OPTIONAL
- 8 ALL DIMENSIONS ARE IN MILLIMETERS
- 9 THIS DRAWING CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-151, VARIATION AAF-1.  
 EXCEPTIONS:  
 A1 MIN = .40  
 b MIN = .50

|   |  |  |                  |
|---|--|--|------------------|
| <b>TOLERANCES</b><br>UNLESS SPECIFIED<br>DIMEN. MILLIMETER<br>HOLE .25<br>FINISH .25<br>APPROVALS DATE<br>DRAWN 299 06/13/98<br>CHECKED |  | IDT<br>2975 Stoner Way, Santa Clara, CA 95054<br>Phone (408) 271-6118 Fax (408) 488-8874 TWC: 810-338-0900 |                  |
| TITLE<br><b>B8 PACKAGE OUTLINE</b><br>17.0 X 17.0 mm B80Y<br>PSCA   |  | DRAWING NO.<br><b>PSC-4081</b>   | REV<br><b>01</b> |
| SIZE C<br>DO NOT SCALE DRAWING  |  | SHEET 2 OF 2   | REV 01           |

## Ordering Information



79RC32 = 32-bit family product

## Valid Combinations

|  |                  |
|--|------------------|
| 79RC32V334 - 100BB, 133BB, 150BB       | Commercial       |
| 79RC32V334 - 100BBG, 133BBG, 150BBG    | Commercial Green |
| 79RC32V334 - 100BBI, 133BBI, 150BBI    | Industrial       |
| 79RC32V334 - 100BBGI, 133BBGI, 150BBGI | Industrial Green |



**CORPORATE HEADQUARTERS**  
6024 Silver Creek Valley Road  
San Jose, CA 95138

**for SALES:**  
800-345-7015 or 408-284-8200  
fax: 408-284-2775  
www.idt.com

**for Tech Support:**  
email: [rischelp@idt.com](mailto:rischelp@idt.com)  
phone: 408-284-8208