FAIRCHILD SEMICONDUCTOR®

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FMPA2151
2.4–2.5GHz and 4.9–5.9GHz Dual Band Linear Power Amplifier Module

Features

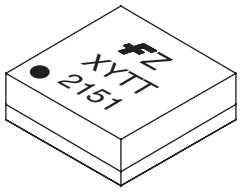
- Dual band operation in a single package design
- Integrated bias bypass
- >33dB modulated gain 2.4 to 2.5GHz band
- >33dB modulated gain 4.9 to 5.9GHz band
- 3.0% EVM at 19dBm modulated power out (2.4GHz)
- 3.5% EVM at 19dBm modulated power out (5.5GHz)
- 3.3V positive supply operation
- Separate integrated power detectors with 20dB dynamic range
- 16 pin 4 x 4 x 1.4mm leadless package
- Internally matched to 50Ω and DC blocked RF input/output
- Optimized for use in 802.11a/b/g applications

General Description

The FMPA2151 is a dual frequency band power amplifier module designed for high performance WLAN applications in the 2.4 to 2.5GHz and the 4.90 to 5.9GHz frequency bands. The 16 pin 4 x 4 x 1.4 mm package with internal matching on both input and output to 50Ω minimizes next level PCB space and allows for simplified integration. Only two external bias bypass capacitors are required. The two on-chip detectors provide power sensing capability. The PA's low power consumption and excellent linearity are achieved using our InGaP Heterojunction Bipolar Transistor (HBT) technology.

Complimentary pin out available with part number FMPA2153 for MIMO applications.

Device (4 x 4 x 1.4mm)



Electrical Characteristics[1] 802.11g (2.4-2.5 GHz) OFDM Modulation

(with 176 µs burst time, 100 µs idle time) 54 Mbps Data Rate, 16.7 MHz Bandwidth

Parameter	Min.	Typ.	Max.	Units
Frequency	2.4		2.5	GHz
Collector Supply Voltage	3.0	3.3	3.6	V
Mirror Supply Voltage (PA ON 2.4)	2.6	3.0	3.6	V
Mirror Supply Current (PA ON 2.4)		0.1		mA
Gain		31		dB
Average Packet Current @ +19dBm Pout		140		mA
EVM @ +19dBm Pout[2]		3.0		%
Detector Output @ +19dBm Pout		600		mV
Detector Output @ +7dBm Pout		280		mV
POUT Spectral Mask Compliance[3]		+20		dBm

Notes:

1. V_{CC} = 3.3V, PA ON 2.4 = 3.3V, T_A = 25°C, PA is constantly biased, 50Ω system.
2. Percentage includes system noise floor of EVM = 0.8%.
3. Measured at PIN at which Spectral Mask Compliance is satisfied. Two-sample windowing length applied.

Electrical Characteristics[1] 802.11a OFDM Modulation

(with 176 µs burst time, 100 µs idle time) 54 Mbps Data Rate, 16.7 MHz Bandwidth

Parameter	Min.	Typ.	Max.	Units
Frequency	4.9		5.9	GHz
Collector Supply Voltage	3.0	3.3	3.6	V
Mirror Supply Voltage (PA ON 5.5)	2.6	3.0	3.6	V
Mirror Supply Current (PA ON 5.5)		0.1		mA
Gain		33		dB
Average Packet Current @ +19dBm Pout		240		mA
EVM @ +19dBm Pout[2] (4.9 to 5.9GHz)		3.5		%
Detector Output @ +19dBm Pout		600		mV
Detector Output @ +7dBm Pout		375		mV
POUT Spectral Mask Compliance[3]		+20		dBm

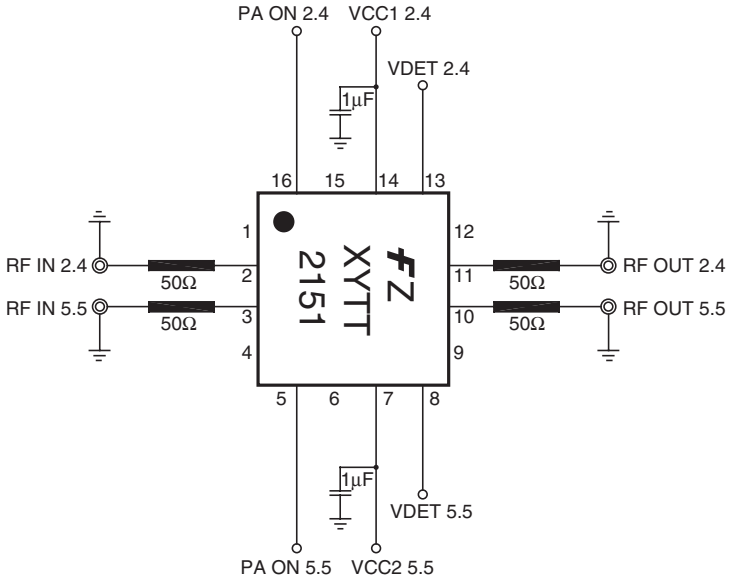
Absolute Maximum Ratings[4]

Symbol	Parameter	Ratings	Units
V_{CC}	Positive Supply Voltage	6	V
I_{CC}	Supply Current	500	mA
PA ON	Positive Bias Voltage	4	V
Pin	RF Input Power	0	dBm
Tcase	Case Operating Temperature	-40 to +85	°C
Tstg	Storage Temperature	-55 to +150	°C

Notes:

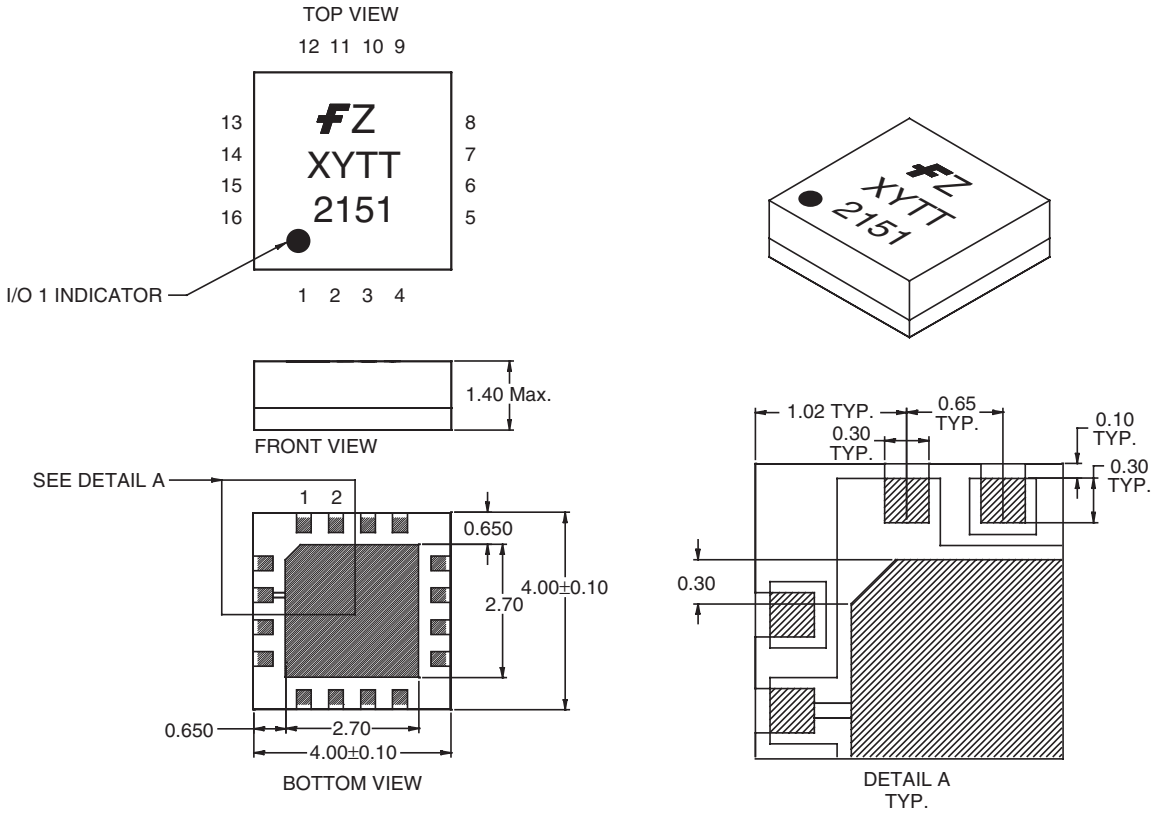
1. V_{CC} = 3.3V, PA ON 5.5 = 3.3V, T_A = 25°C, PA is constantly biased, 50Ω system.
2. Percentage includes system noise floor of EVM = 0.8%.
3. Measured at PIN at which Spectral Mask Compliance is satisfied. Two-sample windowing length applied.
4. No permanent damage with one parameter set at extreme limit. Other parameters set to typical values.

Schematic



Pin	Description
1	GND
2	RF IN 2.4
3	RF IN 5.5
4	GND
5	PA ON 5.5
6	GND
7	VCC2 5.5
8	VDET 5.5
9	GND
10	RF OUT 5.5
11	RF OUT 2.4
12	GND
13	VDET 2.4
14	VCC1 2.4
15	GND
16	PA ON 2.4
17	CENTER GND

Package Outline



Applications Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

Precautions to Avoid Permanent Device Damage:

- Cleanliness: Observe proper handling procedures to ensure clean devices and PCBs. Devices should remain in their original packaging until component placement to ensure no contamination or damage to RF, DC and ground contact areas.
- Device Cleaning: Standard board cleaning techniques should not present device problems provided that the boards are properly dried to remove solvents or water residues.
- Static Sensitivity: Follow ESD precautions to protect against ESD damage:
  - A properly grounded static-dissipative surface on which to place devices.
  - Static-dissipative floor or mat.
  - A properly grounded conductive wrist strap for each person to wear while handling devices.
- General Handling: Handle the package on the top with a vacuum collet or along the edges with a sharp pair of bent tweezers. Avoiding damaging the RF, DC, and ground contacts on the package bottom. Do not apply excessive pressure to the top of the lid.
- Device Storage: Devices are supplied in heat-sealed, moisture-barrier bags. In this condition, devices are protected and require no special storage conditions. Once the sealed bag has been opened, devices should be stored in a dry nitrogen environment.

Device Usage:
Fairchild recommends the following procedures prior to assembly.

- Assemble the devices within 7 days of removal from the dry pack.
- During the 7-day period, the devices must be stored in an environment of less than 60% relative humidity and a maximum temperature of 30°C
- If the 7-day period or the environmental conditions have been exceeded, then the dry-bake procedure, at 125°C for 24 hours minimum, must be performed.

Solder Materials & Temperature Profile:
Reflow soldering is the preferred method of SMT attachment. Hand soldering is not recommended.

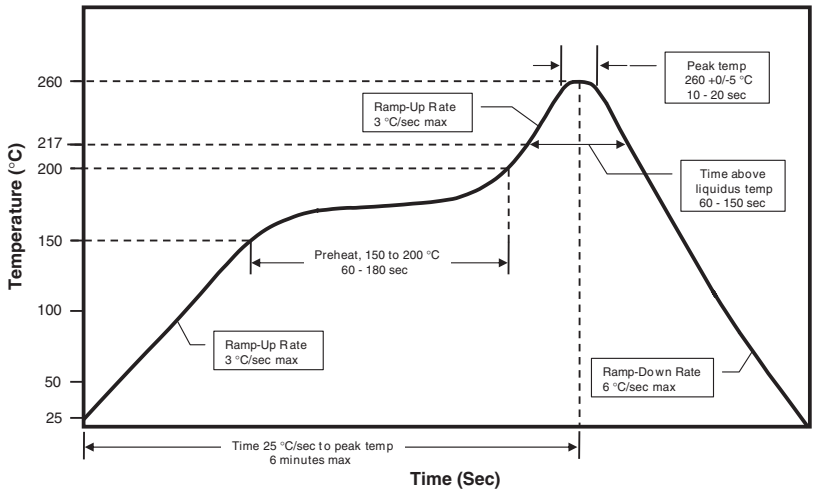
Reflow Profile

- Ramp-up: During this stage the solvents are evaporated from the solder paste. Care should be taken to prevent rapid oxidation (or paste slump) and solder bursts caused by violent solvent out-gassing. A maximum heating rate is 3°C/sec.
- Pre-heat/soak: The soak temperature stage serves two purposes; the flux is activated and the board and devices achieve a uniform temperature. The recommended soak condition is: 60-180 seconds at 150-200°C.
- Reflow Zone: If the temperature is too high, then devices may be damaged by mechanical stress due to thermal mismatch or there may be problems due to excessive solder oxidation. Excessive time at temperature can enhance the formation of inter-metallic compounds at the lead/board interface and may lead to early mechanical failure of the joint. Reflow must occur prior to the flux being completely driven off. The duration of peak reflow temperature should not exceed 20 seconds. Soldering temperatures should be in the range 255–260°C, with a maximum limit of 260°C.
- Cooling Zone: Steep thermal gradients may give rise to excessive thermal shock. However, rapid cooling promotes a finer grain structure and a more crack-resistant solder joint. The illustration below indicates the recommended soldering profile.

Solder Joint Characteristics:
Proper operation of this device depends on a reliable void-free attachment of the heat sink to the PWB. The solder joint should be 95% void-free and be a consistent thickness.

Rework Considerations:
Rework of a device attached to a board is limited to reflow of the solder with a heat gun. The device should be subjected to no more than 15°C above the solder melting temperature for no more than 5 seconds. No more than 2 rework operations should be performed.

Recommended Solder Reflow Profile



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FASTr™	MicroPak™	QT Optoelectronics™	TinyPWM™	
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Definition of Terms

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