WS2512-TR1G

4 x 4 Power Amplifier Module
for UMTS2100 (1920-1980 MHz)

Data Sheet

Description

The WS2512-TR1G, a Wide-band Code Division Multiple Access (WCDMA) Power Amplifier (PA), is a fully matched 10-pin surface mount module developed for WCDMA handset applications. This power amplifier module operates in the 1920-1980 MHz bandwidth. The WS2512-TR1G meets the stringent WCDMA linearity requirements for output power of up to 28 dBm.

A low current (Vcont) pin is provided for high efficiency improvement of the low output power range.

The WS2512-TR1G features CoolPAM circuit technology offering state-of-the-art reliability, temperature stability and ruggedness. The WS2512-TR1G is self contained, incorporating 50 Ω input and output matching networks.

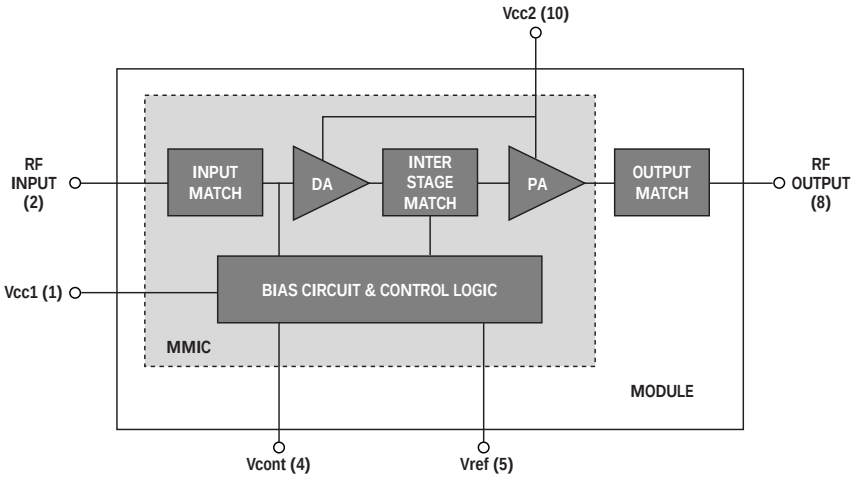
Features

- Excellent linearity
- Low quiescent current
- High efficiency
- 10-pin surface mounting package
  4 mm x 4 mm x 1.1 mm (typ.)
- Internal 50 Ω matching networks for both RF input and output
- RoHS compliant

Applications

- WCDMA handset (HSDPA)

Functional Block Diagram



Order Information

Part Number	No. of Devices	Container
WS2512-TR1G	1,000	7" Tape and Reel

Table 1. Absolute Maximum Ratings[1]

Parameter	Symbol	Min.	Nominal	Max.	Unit
RF Input Power	Pin	–	–	10.0	dBm
DC Supply Voltage	Vcc	0	3.4	5.0	V
DC Reference Voltage	Vref	0	2.85	3.3	V
Mode Control Voltage	Vcont	0	2.85	3.3	V
Storage Temperature	Tstg	-55	–	+125	°C

Table 2. Recommended Operating Condition

Parameter	Symbol	Min.	Nominal	Max.	Unit
DC Supply Voltage					
- High/Mid Power Mode	Vcc	3.2	3.4	4.2	V
- Low Power Mode		–	1.5		
DC Reference Voltage	Vref	2.75	2.85	2.95	V
Mode Control Voltage					
– High Power Mode	Vcont	–	0	–	V
– Mid/Low Power Mode	Vcont	–	2.85	–	V
Operating Frequency	Fo	1920		1980	MHz
Ambient Temperature	Ta	-20	+25	+90	°C

Table 3. Power Range Truth Table

Power Mode	Symbol	Vref	Vcont[2]	Vcc	Range
High Power Mode	PR3	2.85	Low	3.4	~28 dBm
Mid Power Mode	PR2	2.85	High	3.4	~16 dBm
Low Power Mode	PR1	2.85	High	1.5	~7 dBm
Shut Down Mode	–	0	–	3.4	–

Notes:
1. No damage assuming only one parameter is set at limit at a time with all other parameters set at or below nominal value.
2. High (1.5 – 3.0 V), Low (0.0 V – 0.5 V).

Table 4. Electrical Characteristics for WCDMA Mode (Vcc = 3.4 V, Vref = 2.85 V, T = 25°C, Zin/Zout = 50 Ω)[1]

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Frequency Range	F		1920	–	1980	MHz
Gain	Gain_hi	High Power Mode, Pout = 28 dBm	23.5	26.5		dB
	Gain_mid	Mid Power Mode, Pout = 16 dBm	14.5	17.5		dB
	Gain_low	Low Power Mode, Pout = 7 dBm, Vcc = 1.5 V	9.5	12.5		dB
Power Added Efficiency	PAE_hi	High Power Mode, Pout = 28 dBm	36	40		%
	PAE_mid	Mid Power Mode, Pout = 16 dBm	16.2	21.5		%
	PAE_low	Low Power Mode, Pout = 7 dBm, Vcc = 1.5 V	9.6	14.3		%
Total Supply Current	Icc_hi	High Power Mode, Pout = 28 dBm		465	510	mA
	Icc_mid	Mid Power Mode, Pout = 16 dBm		54	71	mA
	Icc_low	Low Power Mode, Pout = 7 dBm, Vcc = 1.5 V		22	33	mA
Quiescent Current	Iq_hi	High Power Mode	45	65	90	mA
	Iq_mid	Mid Power Mode	7	13	22	mA
	Iq_low	Low Power Mode, Vcc = 1.5 V	5	11	18	mA
Reference Current	Iref_hi	High Power Mode		3.5	1	mA
	Iref_mid	Mid Power Mode		4	7	mA
	Iref_low	Low Power Mode, Vcc = 1.5 V		4	8	mA
Control Current[2]	Icont_mid	Mid Power Mode		0.18	1	mA
	Icont_low	Low Power Mode, Vcc = 1.5 V		0.18	1	mA
Total Current in Power-Down Mode	Ipd	Iref = 0 V		0.2	5	µA
Adjacent Channel Leakage Ratio[3]						
5 MHz offset	ACLR1_hi	High Power Mode, Pout = 28 dBm		-42	-37	dBc
10 MHz offset	ACLR2_hi			-54	-47	dBc
5 MHz offset	ACLR1_mid	Mid Power Mode, Pout = 16 dBm		-46	-37	dBc
10 MHz offset	ACLR2_mid			-56	-47	dBc
5 MHz offset	ACLR1_low	Low Power Mode, Pout = 7 dBm,		-40	-37	dBc
10 MHz offset	ACLR2_low	Vcc = 1.5 V		-56	-47	dBc
Harmonic Suppression						
Second	2f0	High Power Mode, Pout = 28 dBm		-42	-30	dBc
Third	3f0			-60	-45	dBc
Input VSWR	VSWR			2:1	2.5:1	
Stability (Spurious Output)	S	VSWR 6:1, All Phase			-50	dBc
Noise Power in Rx Band	RxBN	High Power Mode, Pout = 28 dBm		-139	-136	dBm/Hz
Phase Discontinuity	Phmid_hi	Mid↔Hi at Pout = 16 dBm		7	25	Degree
	Phlow_mid	Low↔Mid at Pout = 7 dBm		15	25	Degree
Ruggedness	Ru	Pout <28 dBm, Pin <10 dBm, All phase		10:1	VSWR	
		High Power Mode				
Switching Time High[4]	DC	TswhighDC	–	20	–	µs
	RF	TswhighRF		1	–	µs

Table 4. Electrical Characteristics for WCDMA Mode (Vcc = 3.4 V, Vref = 2.85 V, T = 25°C, Zin/Zout = 50 Ω)[1] (cont'd.)

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Switching Time Low [4]	DC	TswlowDC	–	20	–	µs
	RF	TswlowRF		1	–	µs
Turn On Time[5]	DC	TonDC	–	20	–	µs
	RF	TonRF		1	–	µs
Turn Off Time[6]	DC	ToffDC	–	20	–	µs
	RF	ToffRF		1	–	µs

Notes:
1. Electrical characteristics are specified under WCDMA modulated (3 GPP Uplink DPCCH + 1DPDCH) signal unless specified otherwise.
2. Control current when series 6.2 kΩ is used.
3. ACP is expressed as a ratio of total adjacent power to signal power, both with 3.84 MHz bandwidth at specified offsets.
4. TswhighDC, TswlowDC is time required to reach stable quiescent bias (10%) after Vcont is switched low and high, respectively.
   TswhighRF, TswlowRF is time required to reach final output power (± 1 dB) after Vcont is switched low and high, respectively.
5. TonDC is time required to reach stable quiescent bias (10%) after Vref is switched high.
   ToffDC is time required for the current to be less than 10% of the Iq after Vref is switched low.
6. TonRF is time required to reach final output power (±1 dB) after Vref is switched high.
   ToffRF is time required to output power to drop 30 dB after Vref is switched low.

Table 5. Electrical Characteristics for HSDPA Mode (Vcc = 3.4 V, Vref = 2.85 V, T = 25°C, Zin/Zout = 50 Ω)[1]

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Frequency Range	F		1920	–	1980	MHz
Gain	Gain_hih	High Power Mode, Pout = 27.5 dBm	23.5	26.5		dB
	Gain_midh	Mid Power Mode, Pout = 16.0 dBm	14.5	17.5		dB
	Gain_lowh	Low Power Mode, Pout = 7.0 dBm, Vcc = 1.5 V	9.5	12..5		dB
Power Added Efficiency	PAE_hih	High Power Mode, Pout = 27.5 dBm	34	38.8		%
	PAE_midh	Mid Power Mode, Pout = 16.0 dBm	16.4	21.7		%
	PAE_lowh	Low Power Mode, Pout = 7.0 dBm, Vcc = 1.5 V	9.6	14.3		%
Total Supply Current	Icc_hih	High Power Mode, Pout = 27.5 dBm		425	485	mA
	Icc_midh	Mid Power Mode, Pout = 16.0 dBm		53	70	mA
	Icc_lowh	Low Power Mode, Pout = 7.0 dBm, Vcc = 1.5 V		22	33	mA
Adjacent Channel Leakage Ratio[2]						
5 MHz offset	ACLR1_hih	High Power Mode, Pout = 27.5 dBm		-40	-37	dBc
10 MHz offset	ACLR2_hih			-55	-47	
5 MHz offset	ACLR1_midh	Mid Power Mode, Pout = 16 dBm		-44	-37	dBc
10 MHz offset	ACLR2_midh			-56	-47	dBc
5 MHz offset	ACLR1_lowh	Low Power Mode, Pout = 7 dBm,		-40	-37	dBc
10 MHz offset	ACLR2_lowh	Vcc = 1.5 V		-56	-47	dBc

Notes:
1. Electrical characteristics are specified under HSDPA modulated Up-Link signal (DPCCH/DPDCH = 12/15, HS-DPCCH/DPDCH = 15/15).
2. ACP is expressed as a ratio of total adjacent power to signal power, both with 3.84 MHz bandwidth at specified offsets.

Characteristics Data (WCDMA, Control Scheme: 3-Mode Control, Vcc = 3.4/1.5 V, Vref = 2.85 V, T=25℃, Zin/Zout = 50 Ω)

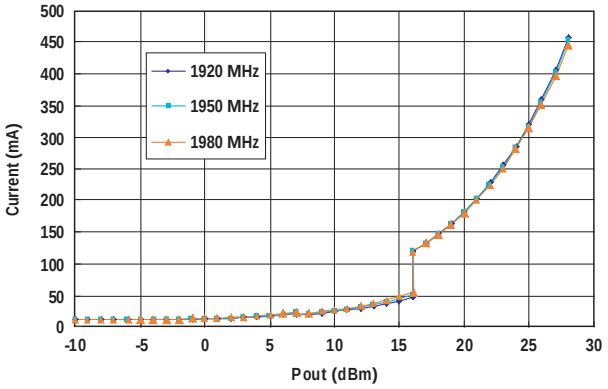


Figure 1. Total current vs. output power

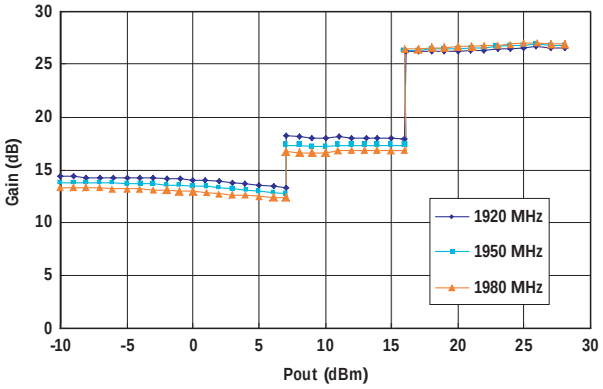


Figure 2. Gain vs. output power

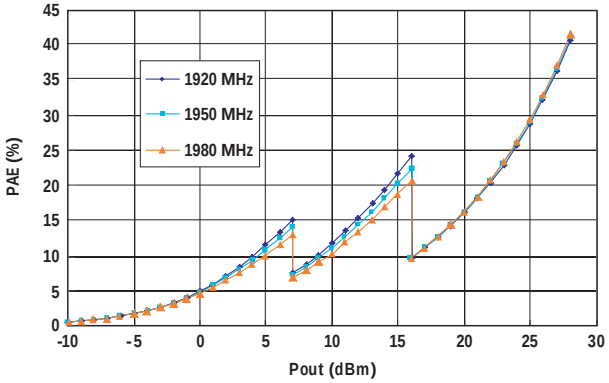


Figure 3. Power added efficiency vs. output power

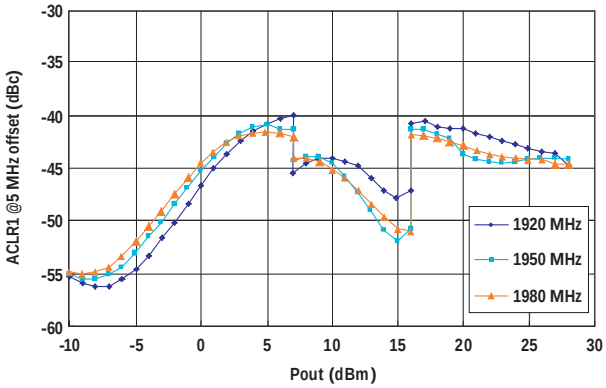


Figure 4. Adjacent channel leakage ratio 1 vs. output power

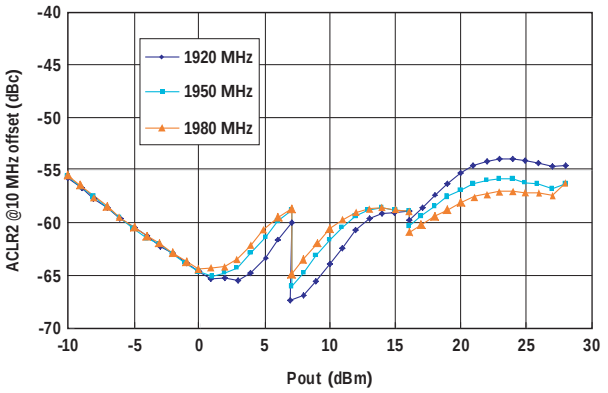


Figure 5. Adjacent channel leakage ratio 2 vs. output power

Characteristics Data (WCDMA, Control Scheme: 2-Mode Control, Vcc = 3.4 V, Vref = 2.85 V, T=25℃, Zin/Zout = 50 Ω)

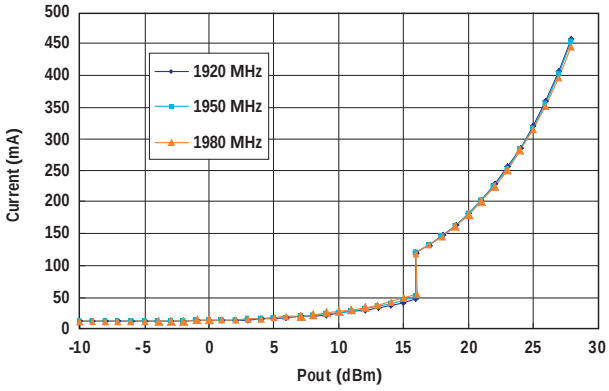


Figure 6. Total current vs. output power

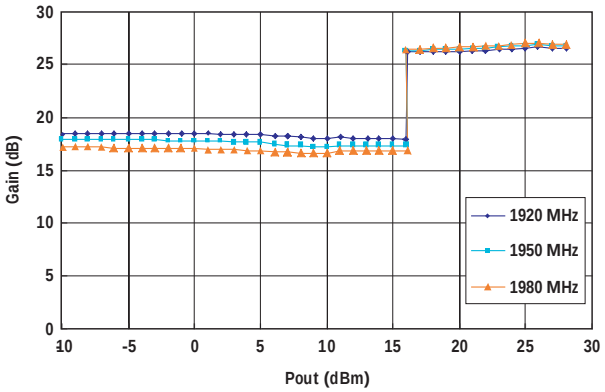


Figure 7. Gain vs. output power

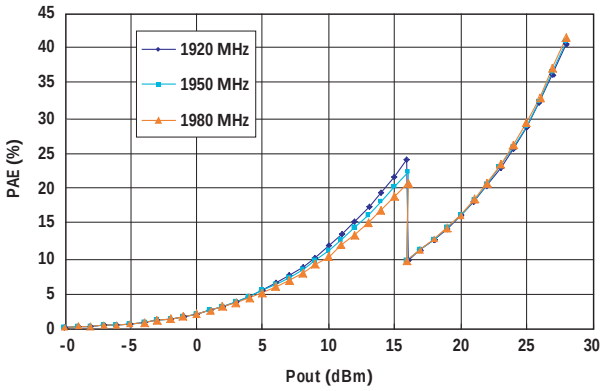


Figure 8. Power added efficiency vs. output power

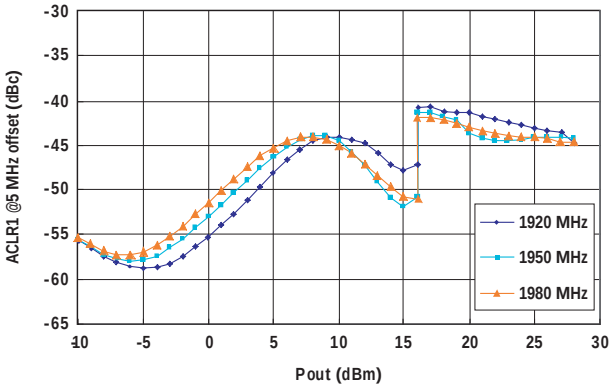


Figure 9. Adjacent channel leakage ratio 1 vs. output power

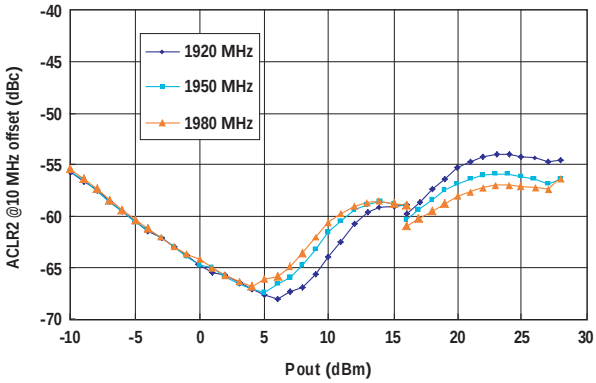


Figure 10. Adjacent channel leakage ratio 2 vs. output power

Characteristics Data (HSDPA, Control Scheme: 3-Mode Control, Vcc = 3.4/1.5 V, Vref = 2.85 V, T=25℃, Zin/Zout = 50 Ω)

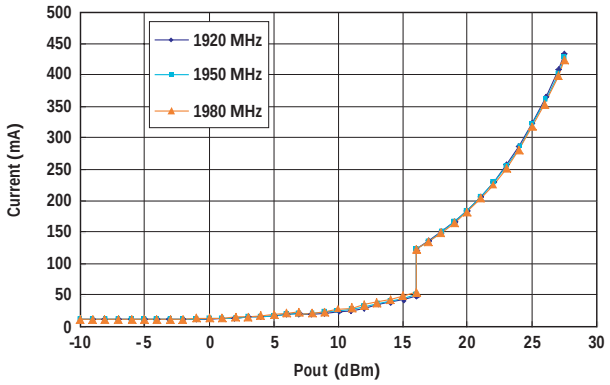


Figure 11. Total current vs. output power

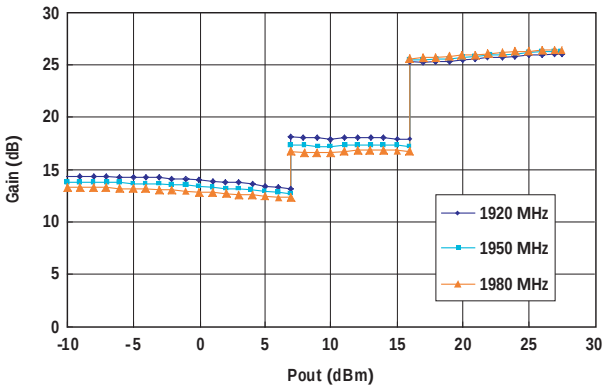


Figure12. Gain vs. output power

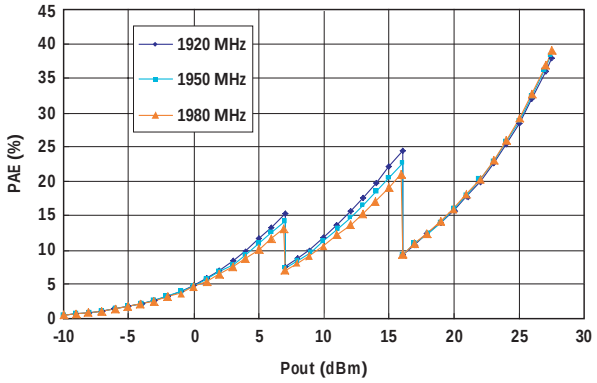


Figure 13. Power added efficiency vs. output power

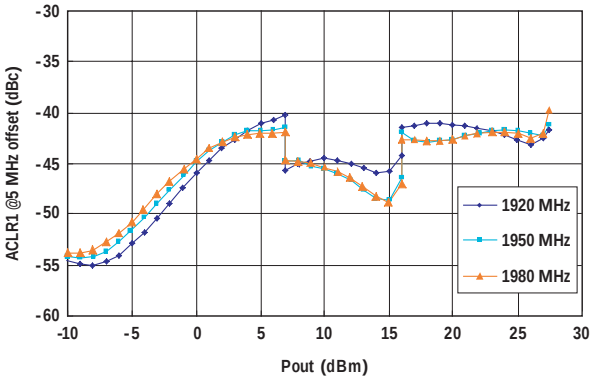


Figure 14. Adjacent channel leakage ratio 1 vs. output power

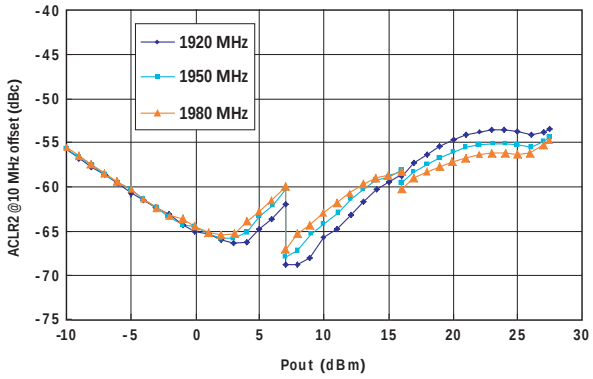


Figure 15. Adjacent channel leakage ratio 2 vs. output power

Evaluation Board Descrpition

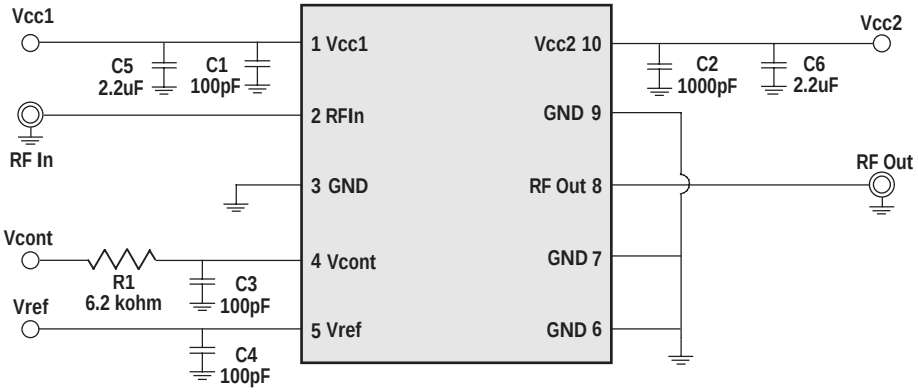


Figure 16. Evaluation board schematic

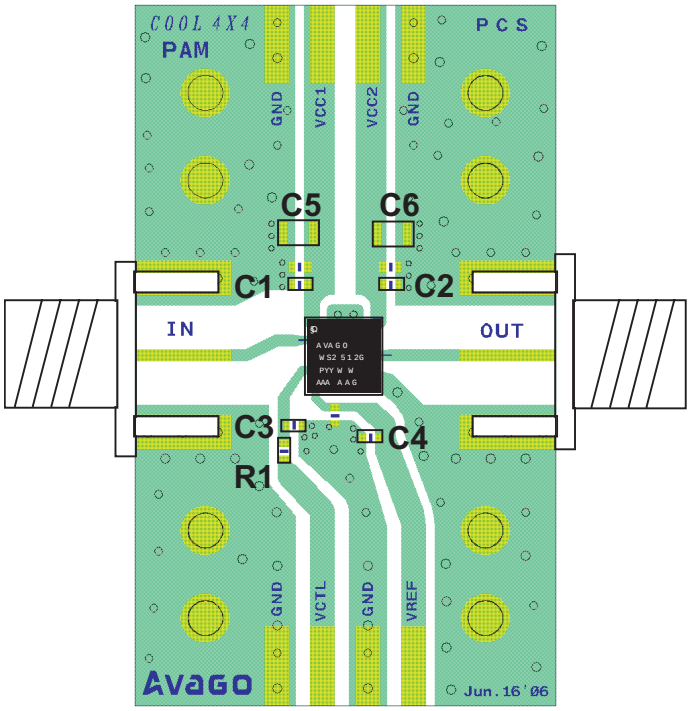
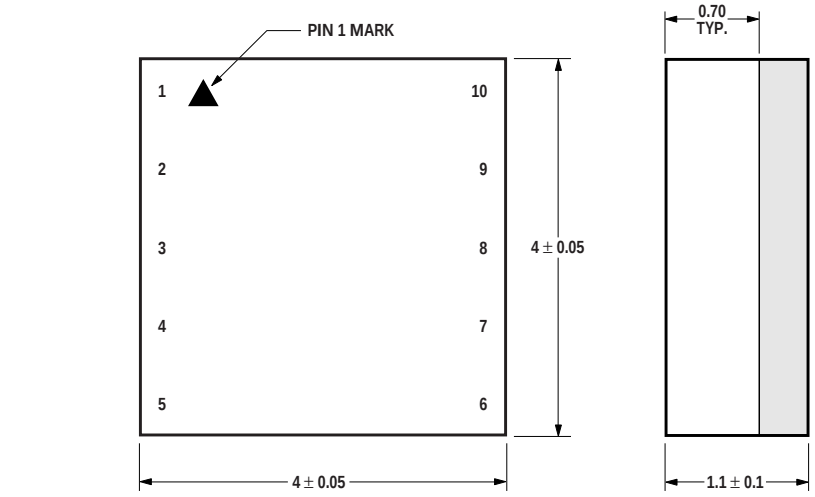
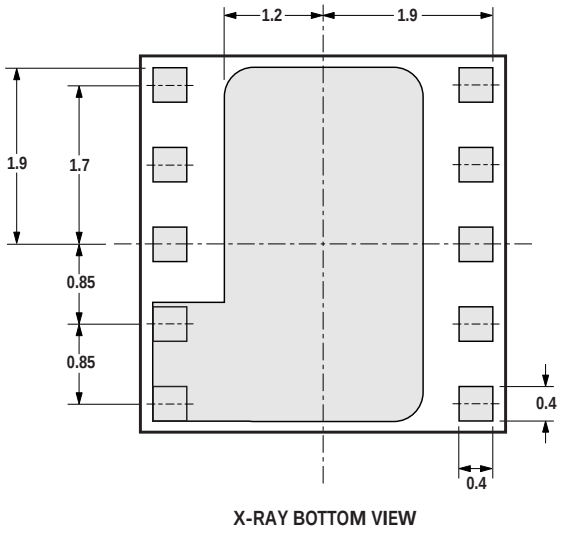


Figure 17. Evaluation board assembly diagram

Package Dimensions and Pin Descriptions





PIN DESCRIPTIONS

PIN #	NAME	DESCRIPTION
1	Vcc1	Supply Voltage
2	RF In	RF Input
3	GND	Ground
4	Vcont	Control Voltage
5	Vref	Reference Voltage
6	GND	Ground
7	GND	Ground
8	RF Out	RF Output
9	GND	Ground
10	Vcc2	Supply Voltage

Figure 18. Package dimensional drawing and pin descriptions (all dimensions are in millimeters)

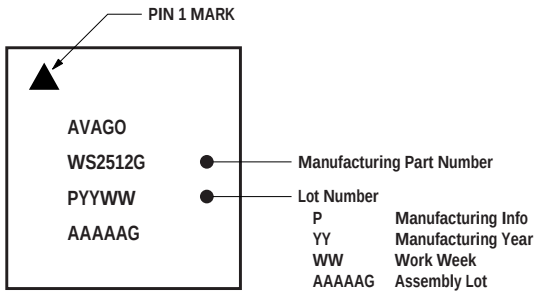
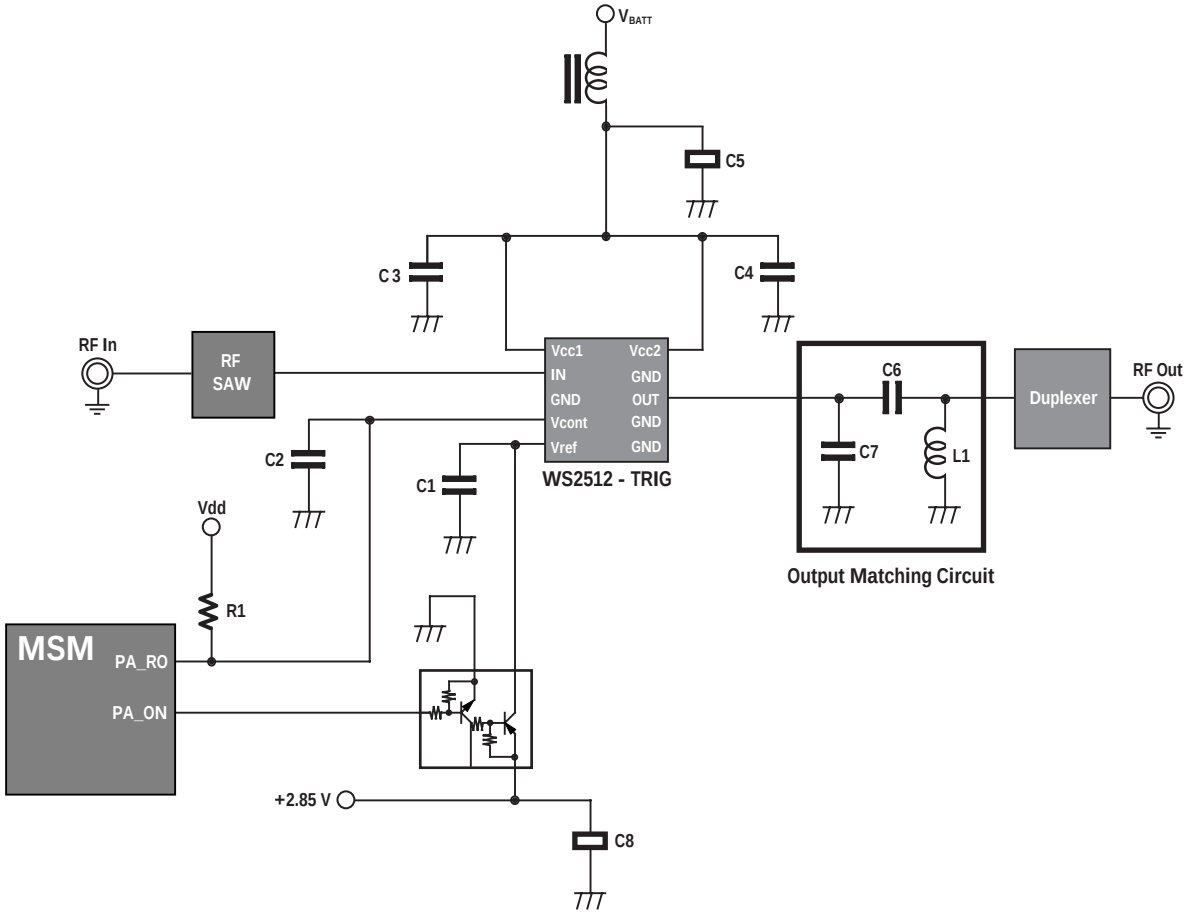


Figure 19. Marking specifications

Peripheral Circuit in Handset



NOTES:

- Recommended voltage for Vref is 2.85 V.
- Place C1 near to Vref pin.
- Place C3 and C4 close to pin 1 (Vcc1) and pin 10 (Vcc2). These capacitors can affect the RF performance.
- Use 50 Ω transmission line between PAM and Duplexer and make it as short as possible to reduce conduction loss.
- π-type circuit topology is good to use for matching circuit between PA and Duplexer.
- Pull-up resistor (R1) should be used to limit current drain. 6.2 kΩ is recommended for WS2512-TR1G.

Figure 20. Peripheral circuit

Calibration

Calibration procedure is shown in Figure 21. Cool PAM requires two calibration tables for high mode and low mode respectively. This is due to gain difference in each mode.

For continuous output power at the points of mode change, the input power should be adjusted according to gain step during the mode change .

Offset Value
(Difference between Rising Point and Falling Point)

Offset value, which is the difference between the rising point (output power where PA mode changes from low mode to high mode) and falling point (output power where PA mode changes from high mode to low mode), should be set to prevent system oscillation. 3 to 5 dB is recommended for Hysteresis.

Average Current & Talk Time

Probability Distribution Function implies that what is important for longer talk time is the efficiency of low or medium power range rather than the efficiency at full power. WS2512-TR1G idle current is 13 mA and operating current at 16 dBm is 54 mA at nominal condition. Average current calculated with CDMA PDF is 26 mA in urban area and 43 mA in suburban area for 2-mode control. Average current can be reduced with 3-mode control, which results in 22 mA in urban area and 38 mA in suburban area. This PA with low current consumption prolongs talk time by no less than 30 minutes compared to other PAs.

$$\text{Average currrent} = \int(\text{PDF} \times \text{Current})dp$$

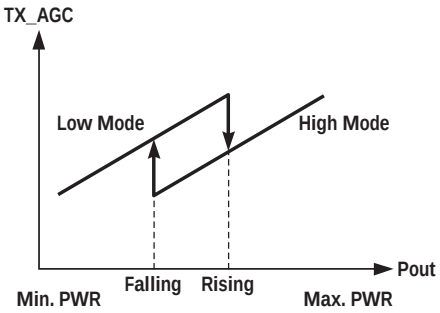


Figure 21. Calibration procedure

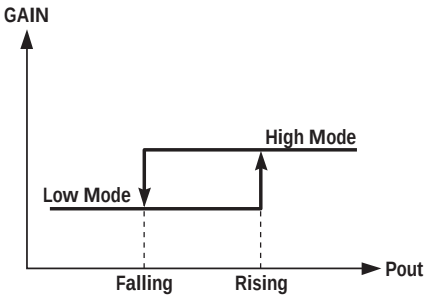


Figure 22. Setting of offset between rising and falling power

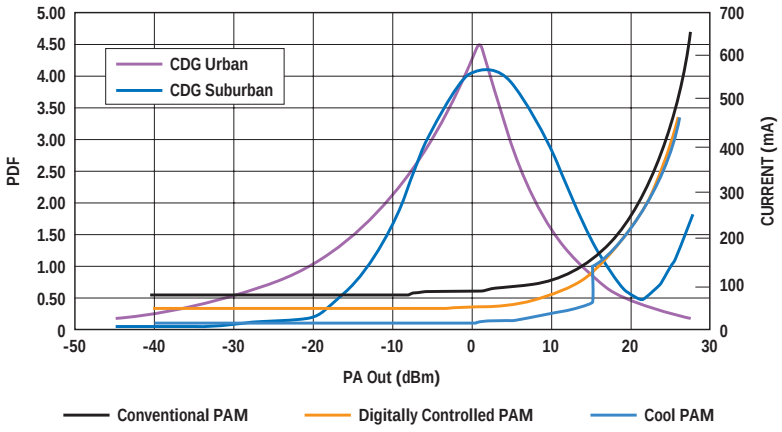


Figure 23. CDMA power distribution function

Power Saving by Using DC-DC Converter

The PA (power amplifier) consumes battery power more than any other parts on mobile board. Therefore, reducing PA power consumption is important for longer talk time. Power savings in the PA allow subscribers to enjoy other utilities longer, and handsets can use smaller, lower cost batteries and achieve the same talk time. CoolPAM technology produces extended talk time by itself using stage-bypass technology. Coupling this technology with a DC-DC converter can result in further power saving.

WS2512 was developed to be compatible with a DC-DC converter serving as the DC power supply, which can improve system efficiency when lower supply voltage is adequate. Typical nominal battery voltage is 3.4 V, and it is usually connected to the PA directly.

System power can be saved at low output power levels when voltage applied to PA is lowered. There are mainly two kinds of voltage control schemes — step voltage control and continuous voltage control.

1. Step voltage control

In this control scheme, voltage is kept constant over some power range. Table 3 shows truth table of one example and Figure 24 shows voltages of Vcc and Vcont. In this application, Vcc is kept 1.5 V up to 7 dBm, then it changes to 3.4 V when output is higher than 7 dBm. Vcont changes at 16 dBm.

2. Continuous voltage change

Additional power savings can be seen if the supply voltage is varied rather than stepped. RF performance degrades as voltage decreases, so care must be taken to keep the supply voltage at a level that is high enough to ensure RF performance requirements are satisfied. Figure 25 shows the relationship between supply voltage Vcc and output power Pout that results in optimal system efficiency. In this graph, Vcc is nonlinear with respect to output power. The SC251 DC-DC converter from Semtech Corporation produces this Vcc vs. Pout transfer function when its control voltage is varied linearly with respect to Pout. This device eliminates the need to calibrate this relationship or develop software that adjusts the voltage based on look-up tables. In handset applications, the analog control voltage pin is connected directly to the TX_AGC signal so that the supply voltage tracks the appropriate gain setting of the transmitter chain. Figure 26 shows the efficiency improvement of WS2512 when used with the SC251.

The step voltage control scheme reduces average power consumption of the PA by about 15%, and the continuous voltage control scheme improves system efficiency by about 25%.

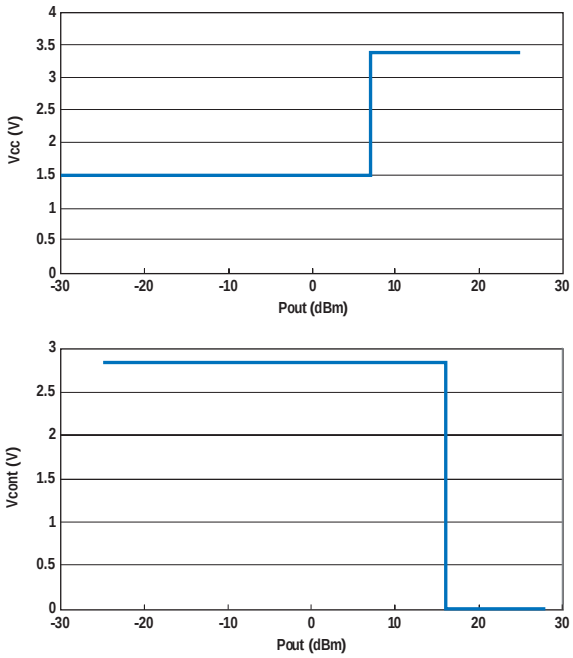


Figure 24. Vcc and Vcont for step voltage control

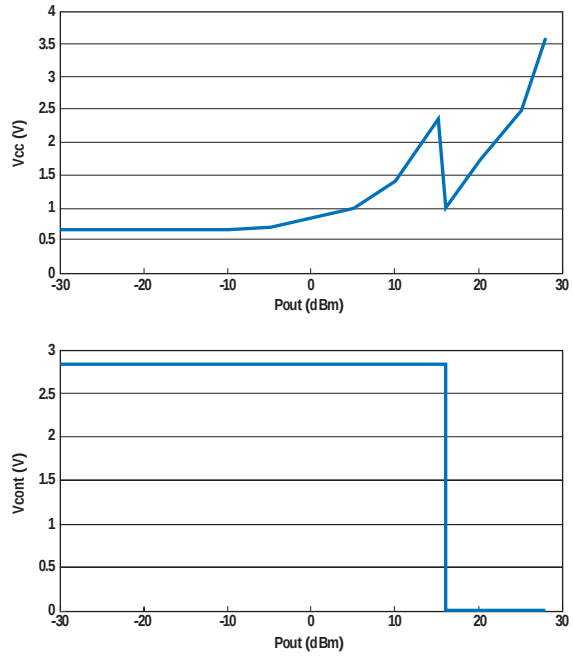


Figure 25. Vcc and Vcont for continuous voltage control

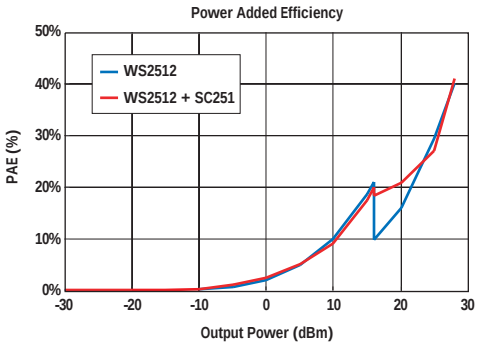


Figure 26. Power added efficiency with SC251

Power Control Scheme

2-Mode Control Scheme

This control scheme doesn't require DC-DC converter. Vcont changes PA into Low Power Mode or High Power Mode, which results in 2-mode control without DC-DC converter. WS2512-TR1G is designed to change the mode at 16 dBm output power.

3-Mode Control Scheme (Step Voltage Control)

This control scheme requires DC-DC converter. When DC-DC converter is used, Vcc voltage as well as Vcont can be changed, which results in 3-mode control scheme — Low/Mid/High power mode. Vcc changes at 7 dBm output and Vcont changes at 16 dBm output. Voltages for Vcc are 1.5 V for low power mode and 3.4 V (battery voltage) for mid and high power mode.

PAE graphs for 2-mode control and 3-mode control are shown in Figure 27 and Figure 28.

HSDPA

WS2512-TR1G meets stringent HSDPA linearity requirement up to 27dBm. WS2512-TR1G can operate up to 28 dBm with Rel.99, which has a lower PAR than HSDPA.

Table 6. Control Scheme: 2-Mode Control

Power Mode	Vref	Vcont	Vcc	Power Range
High Power Mode	2.85	Low	3.4	~ 28 dBm
Low Power Mode	2.85	High	3.4	~ 16 dBm
Shut Down Mode	0.0	–	3.4	–

Table 7. Control Scheme: 3-Mode Control (DC-DC Converter Compatible)

Power Mode	Vref	Vcont	Vcc	Power Range
High Power Mode	2.85	Low	3.4	~ 28 dBm
Mid Power Mode	2.85	High	3.4	~ 16 dBm
Low Power Mode	2.85	High	1.5	~ 7 dBm
Shut Down Mode	0.0	–	3.4	–

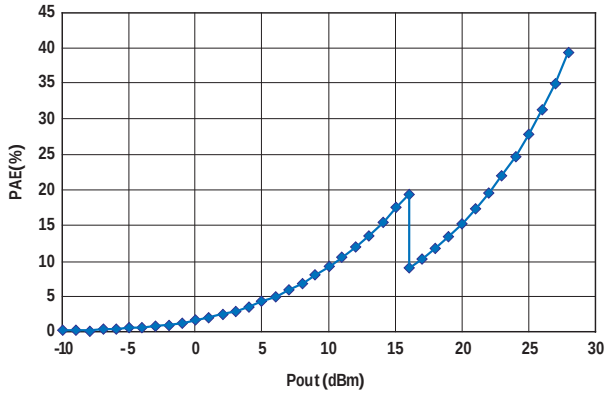


Figure 27. PAE (2-mode control)

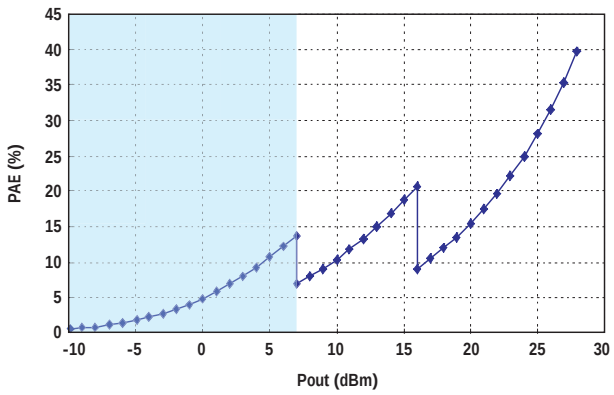


Figure 28. PAE (3-mode control)

PCB Design Guidelines

The recommended WS2512-TR1G PCB land pattern is shown in Figure 29 and Figure 30. The substrate is coated with solder mask between the I/O and conductive paddle to protect the gold pads from short circuit that is caused by solder bleeding/bridging.

Stencil Design Guidelines

A properly designed solder screen or stencil is required to ensure optimum amount of solder paste is deposited onto the PCB pads.

The recommended stencil layout is shown in Figure 31. Reducing the stencil opening can potentially generate more voids. On the other hand, stencil openings larger than 100% will lead to excessive solder paste smear or bridging across the I/O pads or conductive paddle to adjacent I/O pads. Considering the fact that solder paste thickness will directly affect the quality of the solder joint, a good choice is to use laser cut stencil composed of 0.100 mm (4 mils) or 0.127 mm (5 mils) thick stainless steel which is capable of producing the required fine stencil outline.

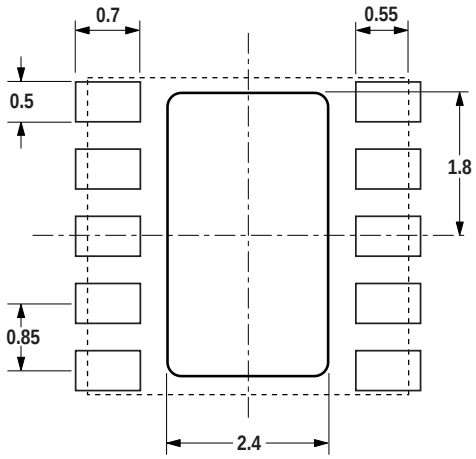


Figure 30. Solder mask opening

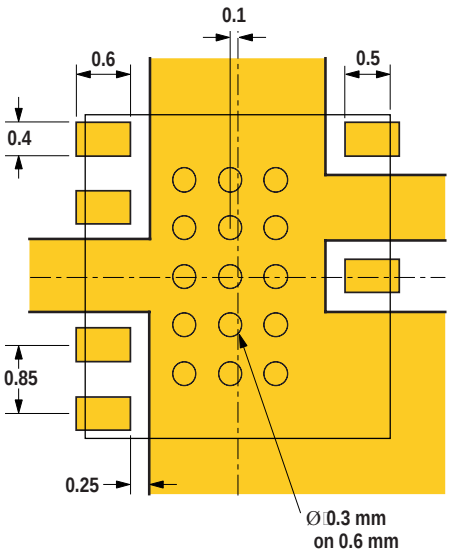


Figure 29. Metallization

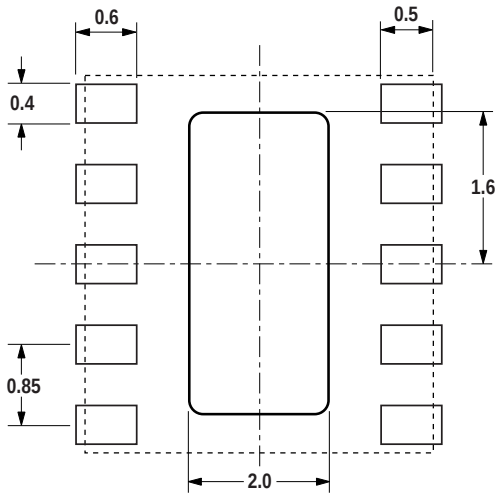
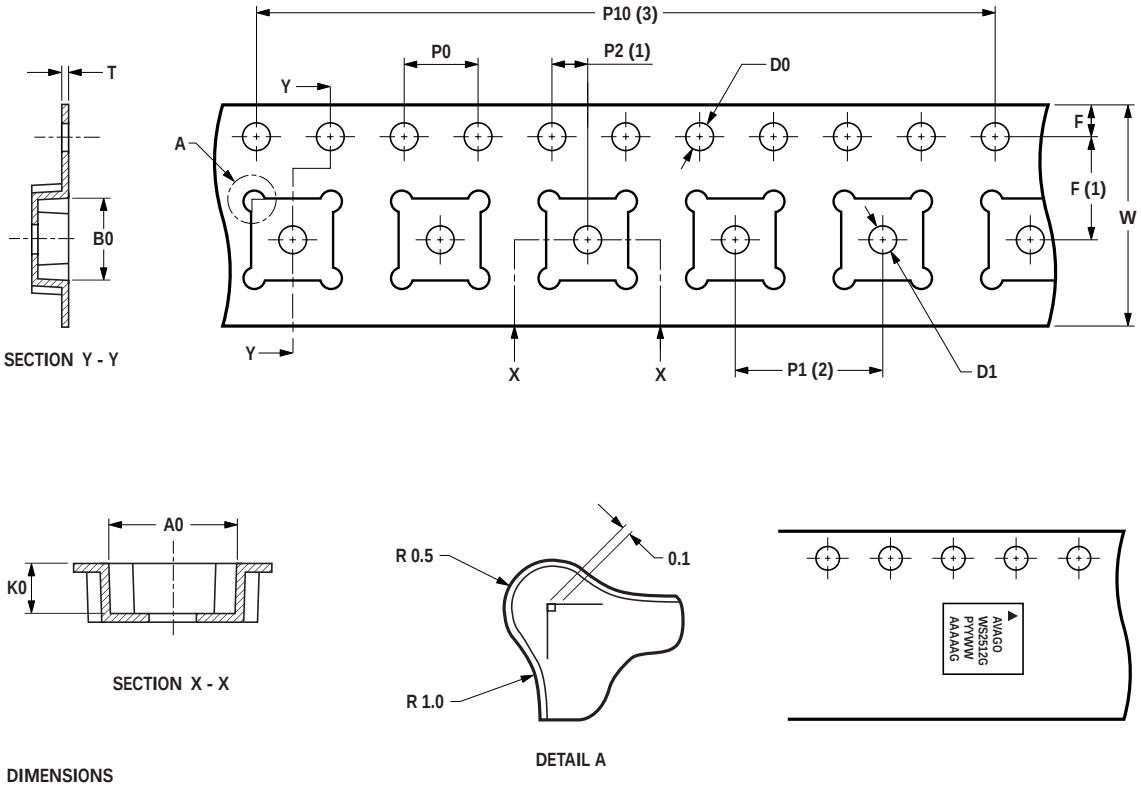


Figure 31. Solder paste stencil aperture

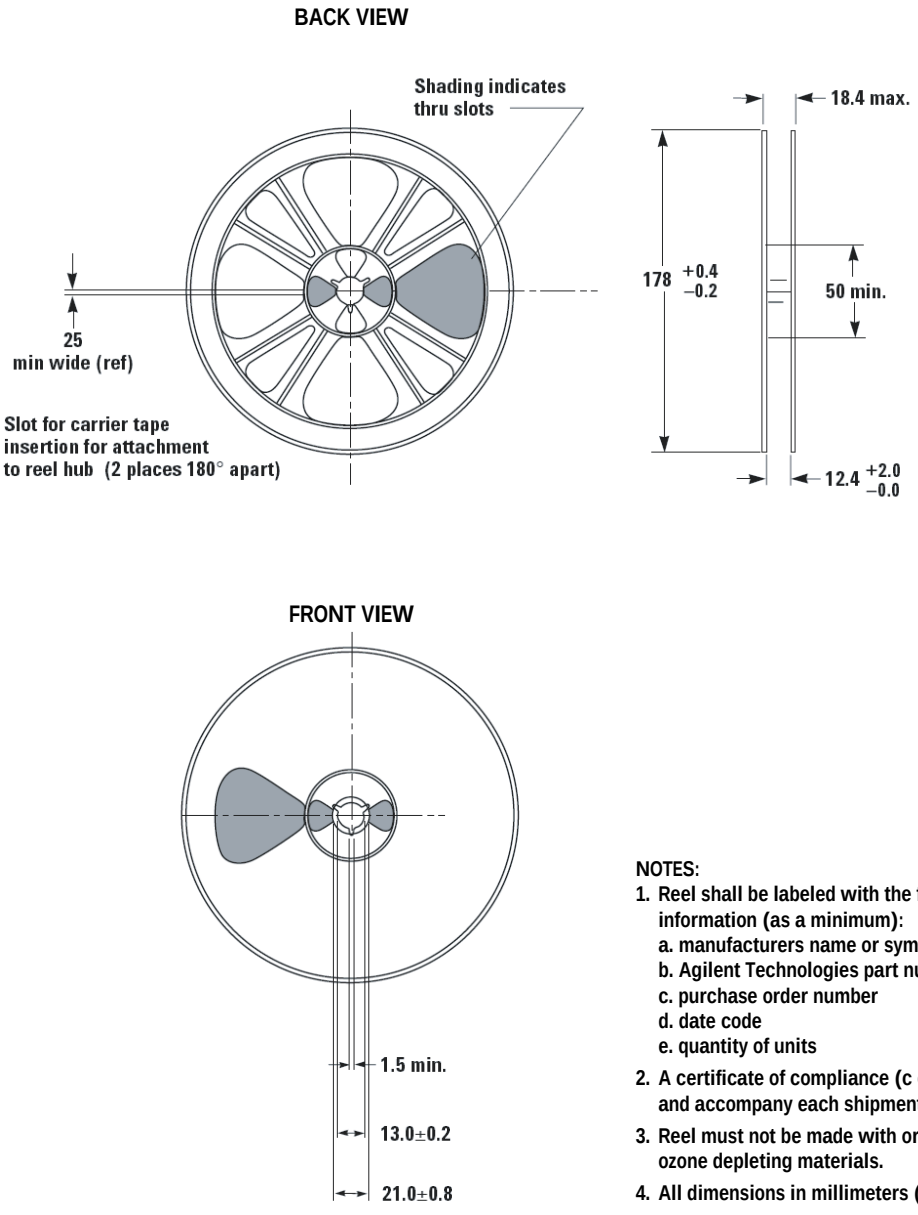
Tape and Reel Information



DIMENSIONS	
NOTATION	MILLIMETERS
A0	4.40 ± 0.10
B0	4.40 ± 0.10
K0	1.70 ± 0.10
D0	1.55 ± 0.05
D1	1.60 ± 0.10
P0	4.00 ± 0.10
P1	8.00 ± 0.10
P2	2.00 ± 0.05
P10	40.00 ± 0.20
E	1.75 ± 0.10
F	5.50 ± 0.05
W	12.00 ± 0.30
T	0.30 ± 0.05

Figure 32. Tape and reel format – 4 mm x 4 mm

Reel Drawing



NOTES:

1. Reel shall be labeled with the following information (as a minimum):
   a. manufacturers name or symbol
   b. Agilent Technologies part number
   c. purchase order number
   d. date code
   e. quantity of units
2. A certificate of compliance (c of c) shall be issued and accompany each shipment of product.
3. Reel must not be made with or contain ozone depleting materials.
4. All dimensions in millimeters (mm).

Figure 33. Plastic reel format (all dimensions are in millimeters)

Handling and Storage

ESD (Electrostatic Discharge)

Electrostatic discharge occurs naturally in the environment. With the increase in voltage potential, the outlet of neutralization or discharge will be sought. If the acquired discharge route is through a semiconductor device, destructive damage will result.

ESD countermeasure methods should be developed and used to control potential ESD damage during handling in a factory environment at each manufacturing site.

MSL (Moisture Sensitivity Level)

Plastic encapsulated surface mount package is sensitive to damage induced by absorbed moisture and temperature.

Avago Technologies follows JEDEC Standard J-STD 020B. Each component and package type is classified for moisture sensitivity by soaking a known dry package at various temperatures and relative humidity, and times. After soak, the components are subjected to three consecutive simulated reflows.

The out of bag exposure time maximum limits are determined by the classification test describe below which corresponds to a MSL classification level 6 to 1 according to the JEDEC standard IPC/JEDEC J-STD-020B and J-STD-033.

WS2512-TR1G is MSL3. Thus, according to the J-STD-033 p. 11 the maximum Manufacturers Exposure Time (MET) for this part is 168 hours. After this time period, the part would need to be removed from the reel, detaped and then rebaked. MSL classification reflow temperature for the WS2512-TR1G is targeted at 260°C +0/-5°C. Figure 34 and Table 10 show typical SMT profile for maximum temperature of 260 +0/-5°C.

Table 8. ESD Classification

Pin No.	HBM		MM		CDM	
	Rating	Class	Rating	Class	Rating	Class
All Pins	±1000 V	Class IC (JESD22-A114C)	±200 V	Class B (JESD22-A115-A)	±200 V	Class II (JESD22-C101C)

Note :
1. Module products should be considered extremely ESD sensitive.

Table 9. Moisture Classification Level and Floor Life

MSL Level	Floor Life (out of bag) at factory ambient =<30°C/60% RH or as stated
1	Unlimited at =<30°C/85% RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.

Note :
1. The MSL Level is marked on the MSL Label on each shipping bag.

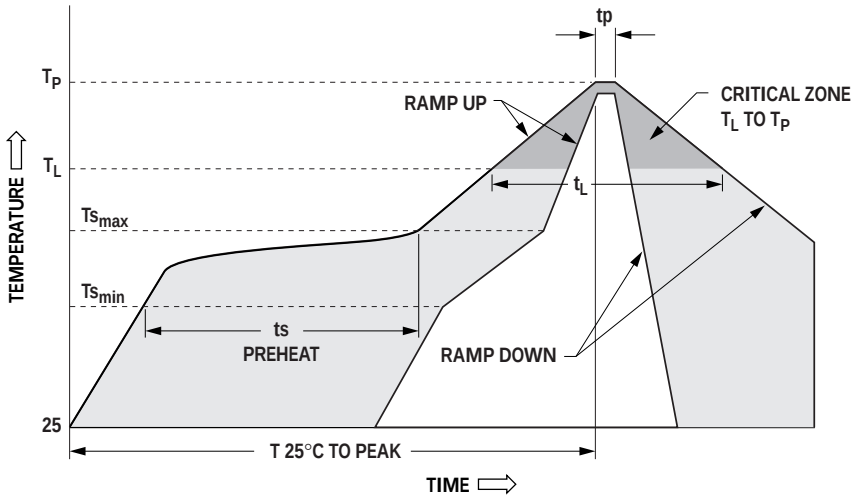


Figure 34. Typical SMT reflow profile for maximum temperature = 260 + 0/-5°C

Table 10. Typical SMT Reflow Profile for Maximum Temperature = 260 +0/-5°C

Profile Feature	Sn-Pb Solder	Pb-Free Solder
Average Ramp-Up Rate (TL to TP)	3°C/sec max	3°C/sec max
Preheat		
- Temperature Min (Tsmin)	100°C	150°C
- Temperature Max (Tsmax)	150°C	200°C
- Time (Min to Max) (ts)	60-120 sec	60-180 sec
Tsmax to TL		
- Ramp-Up Rate		3°C/sec max
Time Maintained Above:		
- Temperature (TL)	183°C	217°C
- Time (TL)	60-150 sec	60-150 sec
Peak Temperature (Tp)	240 +0/-5°C	260 +0/-5°C
Time Within 5°C of Actual Peak Temperature (tp)	10-30 sec	20-40 sec
Ramp-Down Rate	6°C/sec max	6°C/sec max
Time 25°C to Peak Temperature	6 min max.	8 min max.

Storage Condition

Packages described in this document must be stored in sealed moisture barrier, antistatic bags. Shelf life in a sealed moisture barrier bag is 12 months at <40°C and 90% relative humidity (RH) J-STD-033 p. 7.

Out-of-Bag Time Duration

After unpacking the device must be soldered to the PCB within 168 hours as listed in the J-STD-020B p. 11 with factory conditions <30°C and 60% RH.

Baking

It is not necessary to rebake the part if both conditions (storage conditions and out-of bag conditions) have been satisfied. Baking must be done if at least one of the conditions above have not been satisfied. The baking conditions are 125°C for 12 hours J-STD-033 p. 8.

CAUTION

Tape and reel materials typically cannot be baked at the temperature described above. If out-of-bag exposure time is exceeded, parts must be baked for a longer time at low temperatures, or the parts must be dereeled, detaped, rebaked and then put back on tape and reel. (See moisture sensitive warning label on each shipping bag for information of baking).

Board Rework

Component Removal, Rework and Remount

If a component is to be removed from the board, it is recommended that localized heating be used and the maximum body temperatures of any surface mount component on the board not exceed 200°C. This method will minimize moisture related component damage. If any component temperature exceeds 200°C, the board must be baked dry per 4-2 prior to rework and/or component removal. Component temperatures shall be measured at the top center of the package body. Any SMD packages that have not exceeded their floor life can be exposed to a maximum body temperature as high as their specified maximum reflow temperature.

Removal for Failure Analysis

Not following the above requirements may cause moisture/reflow damage that could hinder or completely prevent the determination of the original failure mechanism.

Baking of Populated Boards

Some SMD packages and board materials are not able to withstand long duration bakes at 125°C. Examples of this are some FR-4 materials, which cannot withstand a 24 hr bake at 125°C. Batteries and electrolytic capacitors are also temperature sensitive. With component and board temperature restrictions in mind, choose a bake temperature from Table 4-1 in J-STD 033; then determine the appropriate bake duration based on the component to be removed. For additional considerations see IPC-7711 and IPC-7721.

Derating Due to Factory Environmental Conditions

Factory floor life exposures for SMD packages removed from the dry bags will be a function of the ambient environmental conditions. A safe, yet conservative, handling approach is to expose the SMD packages only up to the maximum time limits for each moisture sensitivity level as shown in Table 9. This approach, however, does not work if the factory humidity or temperature is greater than the testing conditions of 30°C/60% RH. A solution for addressing this problem is to derate the exposure times based on the knowledge of moisture diffusion in the component package materials ref. JESD22-A120). Recommended equivalent total floor life exposures can be estimated for a range of humidities and temperatures based on the nominal plastic thickness for each device.

Table 11 lists equivalent derated floor lives for humidities ranging from 20-90% RH for three temperature, 20°C, 25°C, and 30°C.

This table is applicable to SMDs molded with novolac, biphenyl or multifunctional epoxy mold compounds. The following assumptions were used in calculating Table 11:

1. Activation Energy for Diffusion = 0.35eV (smallest known value).
2. For ≤60% RH, use Diffusivity = 0.121 exp (-0.35 eV/kT) mm2/s (this used smallest known Diffusivity @ 30°C).
3. For >60% RH, use Diffusivity = 1.320 exp (-0.35 eV/kT) mm2/s (this used largest known Diffusivity @ 30°C).

Table 11. Recommended Equivalent Total Floor Life (Days) @ 20°C, 25°C & 30°C for ICs with Novolac, Biphenyl and Multifunctional Epoxies (reflow at same temperature at which the component was classified)

		Maximum Percent Relative Humidity										
Package Type and Body Thickness	**Moisture Sensitivity Level**	**5%**	**10%**	**20%**	**30%**	**40%**	**50%**	**60%**	**70%**	**80%**	**90%**	
Body Thickness ≥3.1 mm Including PQFPs >84 Pin, PLCCs (square) All MQFPs or All BGAs ≥1 mm	Level 2a	∞	∞	∞	60	41	33	28	10	7	6	30°C
		∞	∞	∞	78	53	42	36	14	10	8	25°C
		∞	∞	∞	103	69	57	47	19	13	10	20°C
	Level 3	∞	∞	10	9	8	7	7	5	4	4	30°C
		∞	∞	13	11	10	9	9	7	6	5	25°C
		∞	∞	17	14	13	12	12	10	8	7	20°C
	Level 4	∞	5	4	4	4	3	3	3	2	2	30°C
		∞	6	5	5	5	5	4	3	3	3	25°C
		∞	8	7	7	7	7	6	5	4	4	20°C
	Level 5	∞	4	3	3	2	2	2	2	1	1	30°C
		∞	5	5	4	4	3	3	2	2	2	25°C
		∞	7	7	6	5	5	4	3	2	3	20°C
	Level 5a	∞	2	1	1	1	1	1	1	1	1	30°C
		∞	3	2	2	2	2	2	1	1	1	25°C
		∞	5	4	3	3	3	2	2	2	2	20°C
Body 2.1 mm ≤ Thickness <3.1 mm Including PLCCs (Rectangular) 18-32 Pin SOICs (Wide Body) SOICs ≥20 Pins, PQFPs ≥80 Pins	Level 2a	∞	∞	∞	∞	86	39	28	4	3	2	30°C
		∞	∞	∞	∞	148	51	37	6	4	3	25°C
		∞	∞	∞	∞	∞	69	49	8	5	4	20°C
	Level 3	∞	∞	19	12	9	8	7	3	2	2	30°C
		∞	∞	25	15	12	10	9	5	3	3	25°C
		∞	∞	32	19	15	13	12	7	5	4	20°C
	Level 4	∞	7	5	4	4	3	3	2	2	1	30°C
		∞	9	7	5	5	4	4	3	2	2	25°C
		∞	11	9	7	6	6	5	4	3	3	20°C
	Level 5	∞	4	3	3	2	2	2	1	1	1	30°C
		∞	5	4	3	3	3	3	2	1	1	25°C
		∞	5	5	5	4	4	4	3	3	2	20°C
	Level 5a	∞	2	1	1	1	1	1	1	0.5	0.5	30°C
		∞	2	2	2	2	2	2	1	1	1	25°C
		∞	3	2	2	2	2	2	2	2	1	20°C
Body Thickness .1 mm Including SOICs <18 Pin All TQFPs, TSOPs or All BGAs <1 mm Body Thickness	Level 2a	∞	∞	∞	∞	∞	∞	28	1	1	1	30°C
		∞	∞	∞	∞	∞	∞	∞	2	1	1	25°C
		∞	∞	∞	∞	∞	∞	∞	2	2	1	20°C
	Level 3	∞	∞	∞	∞	∞	11	7	1	1	1	30°C
		∞	∞	∞	∞	∞	14	10	2	1	1	25°C
		∞	∞	∞	∞	∞	20	13	2	2	1	20°C
	Level 4	∞	∞	∞	9	5	4	3	1	1	1	30°C
		∞	∞	∞	12	7	5	4	2	1	1	25°C
		∞	∞	∞	17	9	7	6	2	2	1	20°C
	Level 5	∞	∞	13	5	3	2	2	1	1	1	30°C
		∞	∞	18	6	4	3	3	2	1	1	25°C
		∞	∞	36	8	6	5	4	2	2	1	20°C
	Level 5a	∞	10	3	2	1	1	1	1	1	0.5	30°C
		∞	13	5	3	2	2	2	1	1	1	25°C
		∞	18	6	4	3	2	2	2	2	1	20°C

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