700 MHz to 1000 MHz 2-Stage 1W RF Driver Amplifier

Preliminary Technical Data

ADL5605

FEATURES

- Operation from 700 MHz to 1000 MHz
- Gain of 23 dB at 943 MHz
- OIP3 of 44.3 dBm at 943 MHz
- P1dB of 31.1 dBm at 943 MHz
- Noise figure of 4.8 dB at 943 MHz
- Power supply 5 V
- Power supply current 312 mA typical
- Internal active biasing
- Power down function
- Compact 4mm x 4mm 16-lead LFCSP
- ESD rating of ±1 kV (Class 1C)
- Pin-Compatible with the ADL5606, 1800 – 2700 MHz

FUNCTIONAL BLOCK DIAGRAM

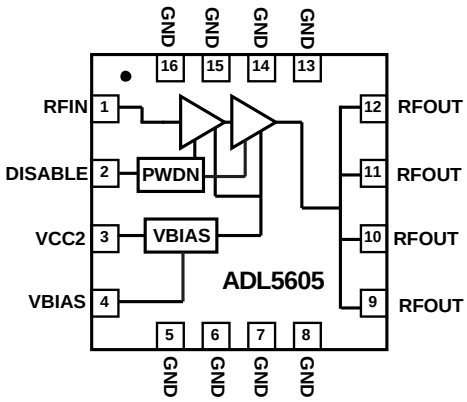

Figure 1

GENERAL DESCRIPTION

The ADL5605 is a broadband 2-stage 1 W RF driver amplifier that operates over a frequency range of 700 MHz to 1000 MHz. The device can be used in a wide variety of wired and wireless applications including ISM, MC-GSM, CDMA, and LTE.

The ADL5605 operates on a 5 V supply voltage and a supply current of 312 mA. The driver also incorporates a fast turn on/off function for applications requiring a power saving mode, or for applications that intermittently transmit data.

The ADL5605 is fabricated on a GaAs HBT process. The device is packaged in a compact 4mm x 4mm 16-lead LFCSP that uses an exposed paddle for excellent thermal impedance. It operates from −40°C to +85°C, and a fully populated evaluation board is available.

Rev. PrA

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SPECIFICATIONS

VCC = 5 V and T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		700		1000	MHz
FREQUENCY = 748 ± 20 MHz					
Gain		20.5	22	23.5	dB
vs. Frequency	±20 MHz		±0.25		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.5		dB
vs. Supply	4.75 V to 5.25 V		±0.1		dB
Output 1 dB Compression Point			30		dBm
vs. Frequency	±20 MHz		±0.25		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.5		dB
vs. Supply	4.75 V to 5.25 V		±0.1		dB
ACP	Pout =19dBm, 1 Carrier WCDMA 64 DPCH		-55		dBc
Output Third-Order Intercept	Δf = 1 MHz, P_{OUT} = 14dBm per tone	44	47		dBm
vs. Frequency	±20 MHz		±0.25		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.5		dB
vs. Supply	4.75 V to 5.25 V		±0.1		dB
Noise Figure			4.8	7	dB
Input Return Loss	±20 MHz		-15		dB
Output Return Loss	±20 MHz		-10		dB
FREQUENCY = 881 ±13 MHz					
Gain		19.5	21	22.5	dB
vs. Frequency	±13 MHz		±0.5		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.5		dB
vs. Supply	4.75 V to 5.25 V		±0.1		dB
Output 1 dB Compression Point			30		dBm
vs. Frequency	±13 MHz		±0.3		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.5		dB
vs. Supply	4.75 V to 5.25 V		±0.1		dB
ACP	Pout =19dBm, 1 Carrier WCDMA 64 DPCH		-55		dBc
Output Third-Order Intercept	Δf = 1 MHz, P_{OUT} = 14dBm per tone	44	47		dBm
vs. Frequency	±13 MHz		±0.3		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.5		dB
vs. Supply	4.75 V to 5.25 V		±0.1		dB
Noise Figure			4.8	7	dB
Input Return Loss	±13 MHz		-15		dB
Output Return Loss	±13 MHz		-10		dB

Parameter	Conditions	Min	Typ	Max	Unit
FREQUENCY = 943 MHz ±18 MHz					
Gain		22	23	24	dB
vs. Frequency	±18 MHz		±0.25		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.5		dB
vs. Supply	4.75 V to 5.25 V		±0.1		dB
Output 1 dB Compression Point			31		dBm
vs. Frequency	±18 MHz		±0.25		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.5		dB
vs. Supply	4.75 V to 5.25 V		±0.1		dB
ACP	Pout =19dBm, 1 Carrier WCDMA 64 DPCH		-55		dBc
Output Third-Order Intercept	Δf = 1 MHz, POUT = 14dBm per tone		44		dBm
vs. Frequency	±18 MHz		±0.25		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.5		dB
vs. Supply	4.75 V to 5.25 V		±0.1		dB
Noise Figure			4.8		dB
Input Return Loss	±18 MHz		-15		dB
Output Return Loss	±18 MHz		-10		dB
POWER-DOWN INTERFACE	Pin DISABLE				
Logic Level to Enable	VPWDN decreasing	0.5	TBD	4.5	V
Logic Level to Disable	VPWDN increasing	0.5	TBD	4.5	V
Input Current	VPWDN Enabled		0.5	2	mA
	VPDWN Disabled		0.5	2	mA
Enable Time	10-90%		TBD		µs
Disable Time	10-90%		TBD		µs
POWER INTERFACE	Pin RFOUT				
Supply Voltage		4.75	5	5.25	V
Supply Current			312	TBD	mA
vs. Temperature	−40°C ≤ T_A ≤ +85°C		TBD		mA

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

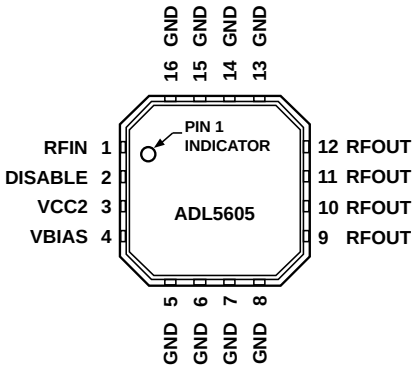

Figure 2 Pin Configuration

Table 2. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RFIN	RF Input. Requires a dc blocking capacitor.
5, 6, 7, 8, 13,14, 15, 16	GND	Solder to a low impedance electrical and thermal ground plane.
2	DISABLE	Connect disable pin to 5V to disable the part, draws around 5mA under the disabled state
3	VCC2	Under normal operation, this pin is connected to the power supply and draws around 312 mA of current. This pin when grounded along with the VBIAS pin disables the device and draws around 10uA of current
4	VBIAS	Applying 5 V to this pin enables the bias circuit. Grounding this pin disables the device and draws around 10uA of current
9, 10, 11, 12	RFOUT	RF Output, DC bias is provided to this pin through an inductor that is connected to the 5 V power supply. The RF path requires a dc blocking capacitor.
	EP	The exposed paddle is connected internally to ground. Solder to a low impedance electrical and thermal ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

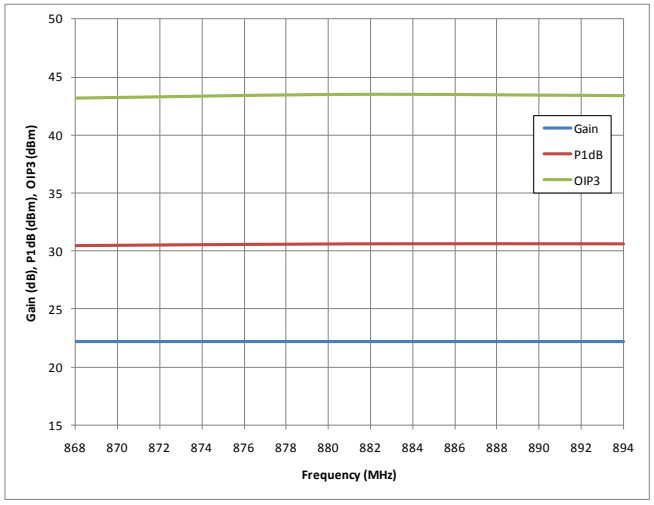

Figure 3 Gain, P1dB, OIP3 at P_{OUT}=14 dBm/Tone vs. Frequency

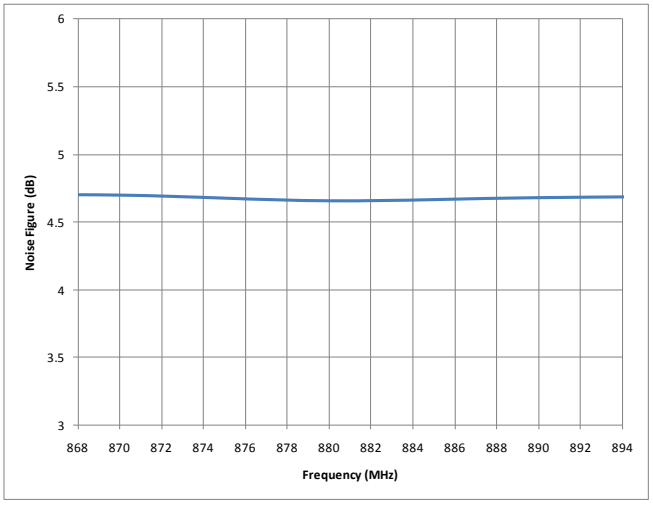

Figure 6 Noise Figure vs. Frequency

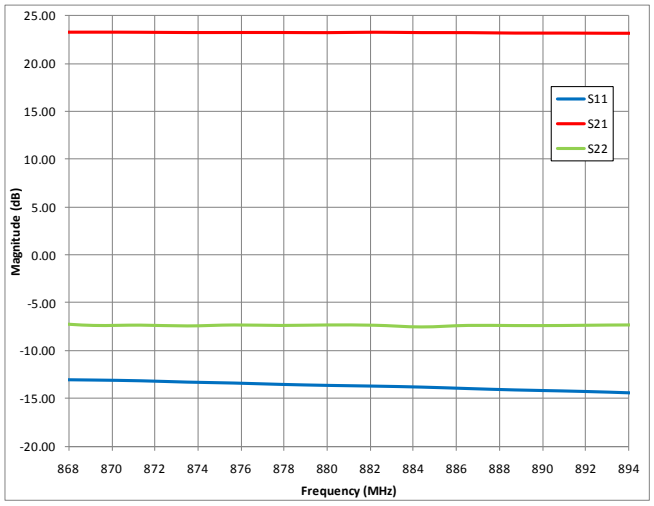

Figure 4 Input Return Loss (S11), Output Return Loss (S22), and Gain (S21) vs. Frequency

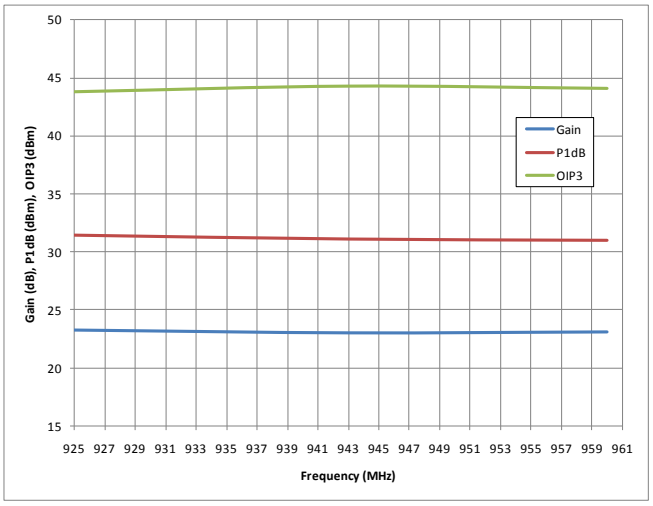

Figure 7 Gain, P1dB, OIP3 at P_{OUT}=14 dBm/Tone vs. Frequency

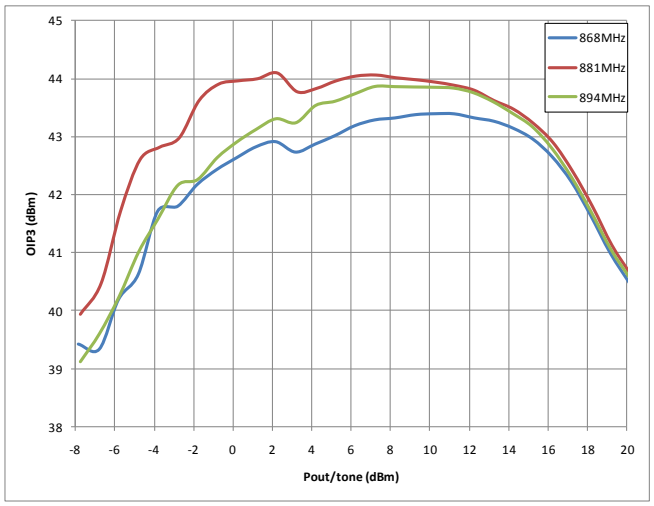

Figure 5 OIP3 vs. P_{OUT} and Frequency

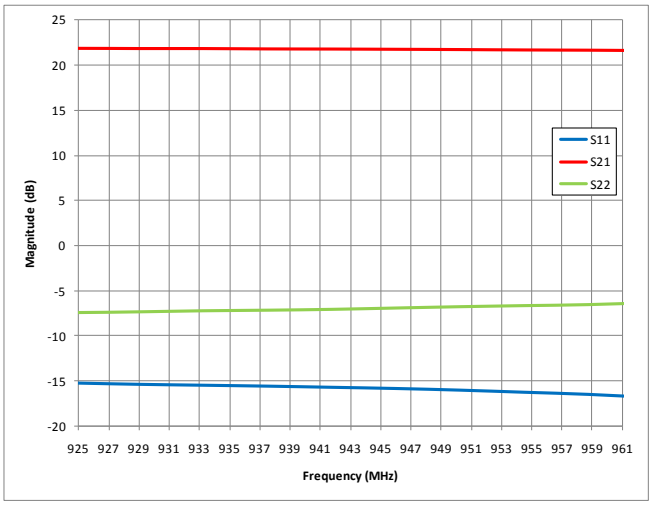

Figure 8 Input Return Loss (S11), Output Return Loss (S22), and Gain (S21) vs. Frequency

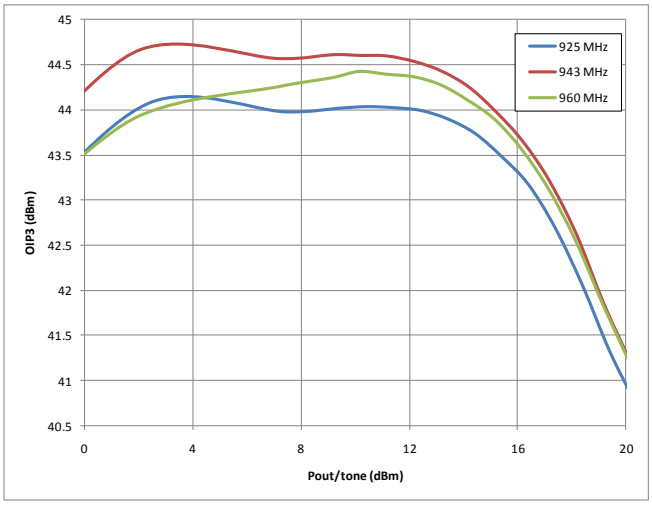

Figure 9 OIP3 vs. P_{OUT} and Frequency

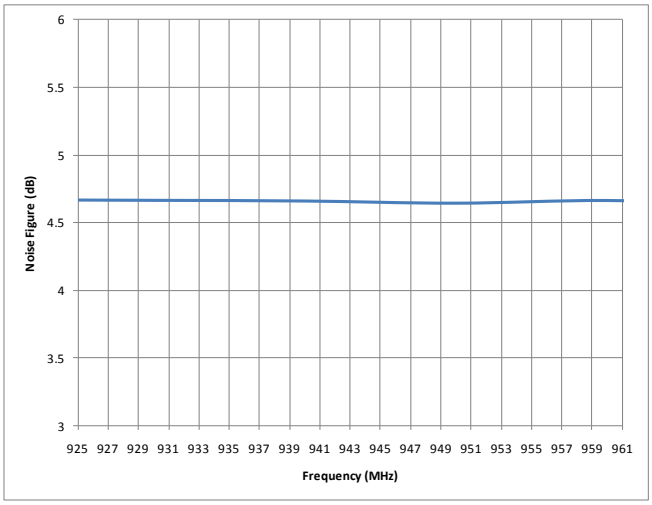

Figure 10 Noise Figure vs. Frequency

OUTLINE DIMENSIONS

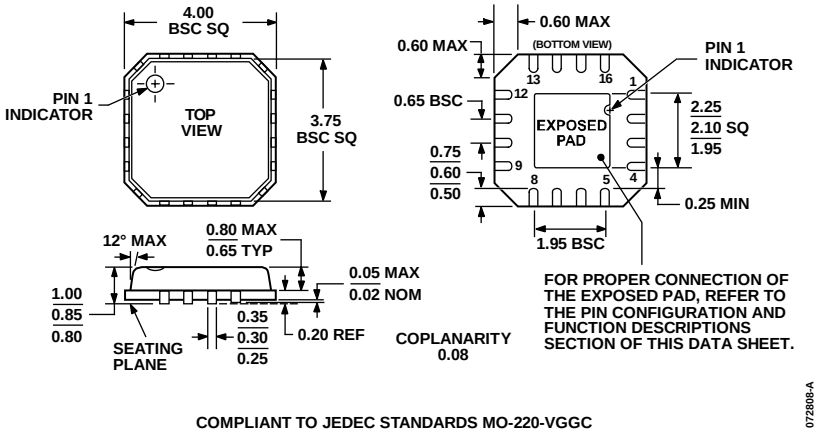

Figure 11. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-16-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADL5605ACPZ-R7	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-4
ADL5605-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

PR09353-0-6/11(PrA)