NEC

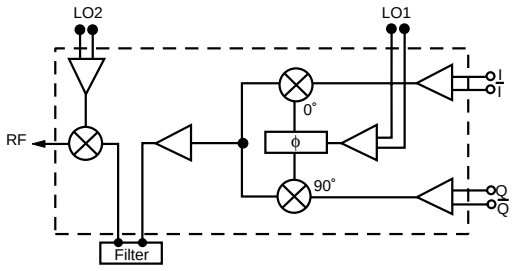
SILICON MMIC UPCONVERTER AND QUADRATURE MODULATOR

UPC8104GR

FEATURES

- **WIDE SUPPLY VOLTAGE RANGE:** 2.7 ~ 5.5 V
- **BROADBAND OPERATION:** RF_{OUT} = 0.8 - 2.4 GHz MOD_{OUT} = 100 - 400 MHz, I/Q = DC to 10 MHz
- **INTERNAL 90° PHASE SHIFTER**
- **PORTS FOR EXTERNAL IF FILTER**
- **LOW POWER CONSUMPTION:** 28 mA AT 3 VOLT TYPICAL
- **SMALL SSOP 20 PACKAGE**
- **TAPE AND REEL PACKAGING AVAILABLE**

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

The UPC8104GR Silicon MMIC Frequency Upconverter with I/Q Modulator is manufactured using the NESAT III MMIC process. The NESAT III process produces transistors with f_T approaching 20 GHz. The device was designed for use in 800 MHz to 2.4 GHz Digital Mobile Communications circuits such as 900 MHz Digital Cordless Phones, WLAN and PCN/PCS Handset Transmitters.

NEC's stringent quality assurance and test procedures ensure the highest reliability and performance.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 3.0 V, V_{PS} ≥1.8 V)

	PART NUMBER / PACKAGE OUTLINE			UPC8104GR S20 (SSOP 20)		
	SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
Total	I_{CC}	Total Circuit Current (no signal) V_{PS} ≥ 1.8 V V_{PS} ≤ 1.0 V	mA µA	18	28 0.1	37 10
Total	P_{RF}	Total Output Power[1,2]	dBm	-18.5	-13.5	-8.5
Total	LOL	Upconverter LO Carrier Leakage[1]	dBc		-40	-30
Total	ImR	Image Rejection[1] (Side Band Leakage)	dBc		-40	-30
Up Converter	I_{CC}	Circuit Current - Upconverter (no signal) V_{PS} ≥ 1.8 V V_{PS} ≤ 1.0 V	mA µA		12	 5
Up Converter	CG	Conversion Gain[1] f_{RF} = 900 MHz, f_{IF} = 240 MHz, f_{LO} = 1140 MHz f_{RF} = 1900 MHz, f_{IF} = 240 MHz, f_{LO} = 1660 MHz f_{RF} = 2450 MHz, f_{IF} = 240 MHz, f_{LO} = 2210 MHz	dB dB dB		10 4.5 4	
Up Converter	$P_{RF\ (SAT)}$	Maximum Output Power - Upconverter f_{RF} = 900 MHz, f_{IF} = 240 MHz f_{RF} = 1900 MHz, f_{IF} = 240 MHz	dBm dBm		-2 -6	
Up Converter	OIP_3	Output 3rd Order Intercept Point f_{RFOUT} = 1.9 GHz f_{IF} = 240.0 MHz/240.2 MHz	dBm		0	
Modulator	I_{CC}	Circuit Current - Modulator (no signal) V_{PS} ≥ 1.8 V V_{PS} ≤ 1.0 V	mA µA	10	16	21 5
Modulator	P_{MOD}	Output Power - Modulator[2]	dBm		-17.5	
Modulator	LO_{LEAK}	Local Oscillator Leakage[2]	dBc		-40	-30
Modulator	ImR	Image Rejection[2]	dBc		-40	-30
Modulator	$IM_{3\ I/Q}$	I/Q 3rd Order Intermodulation Distortion[2]	dBc		-50	
Modulator	RL_{IN}	I/Q LO Input Return Loss	dB		20	
Modulator	$Z_{I/Q}$	Input Impedance I and Q Ports[2]	kΩ		20	
Modulator	$I_{I/Q}$	I/Q Bias Current	µA		5	
Modulator	T_{PS}(RISE)	Power Save Rise Time V_{PS} ≤ 1.0 V to V_{PS} ≥ 1.8V	µS		2.0	5.0
Modulator	T_{PS} (FALL)	Power Save Fall Time V_{PS} ≥1.8 V to V_{PS} ≤1.0 V	µS		2.0	5.0

Notes:
1. P_{IFIN} = -20 dBm 2. $V_{I/Q}$ = 1.5 V (DC) +0.5 Vp-p (AC)

ABSOLUTE MAXIMUM RATINGS[1] (T_A = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{CC}	Supply Voltage	V	6.0
V_{PS}	Enable Voltage for Power Save	V	6.0
P_D	Power Dissipation[2]	mW	530
T_{OP}	Operating Temperature	°C	-40 to +85
T_{STG}	Storage Temperature	°C	-65 to +150

Notes:
1. Operation in excess of any one of these parameters may result in permanent damage.
2. Mounted on a 50x50x1.6 mm epoxy glass PWB (T_A = 85°C).

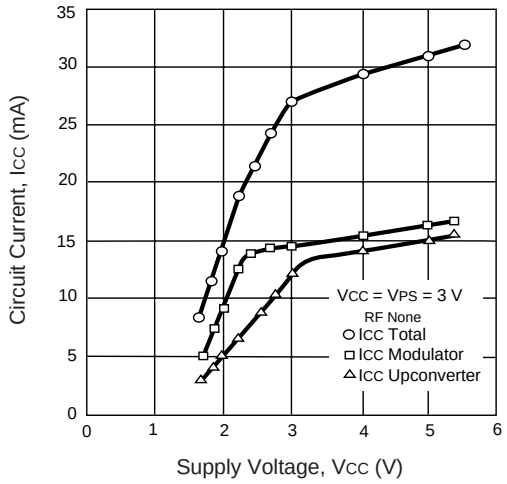
RECOMMENDED OPERATING CONDITIONS

SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
V_{CC}	Supply Voltage	V	2.7	3.0	5.5
T_{OP}	Operating Temperature	°C	-40	+25	+85
f_{RF}	Up Converter RF Frequency	GHz	0.9		2.4
f_{IF}	IF Frequency[1]	MHz	100		400
f_{LO2}	Up Converter LO Frequency	GHz	0.9		2.2
$f_{I/Q}$	I/Q Input Frequency[2]	MHz	DC		10

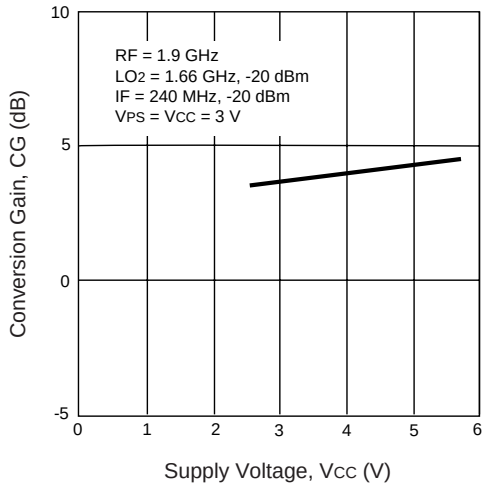
Notes:
1. IF frequency range includes Up-Converter IF input, Modulator IF Output and Modulator LO Input Frequency (LO1).
2. $V_{I/QIN}$ = 600 mVp-p maximum.

TYPICAL PERFORMANCE CURVES (T_A = 25°C, V_{CC} = V_{PS} = 3 V, I/Q DC Offset = $\overline{I}/\overline{Q}$ DC Offset = 1.5 V, I/Q Input Signal = 500 mVp-p (Single Ended), P_{LO1IN} = -10 dBm, P_{LO2IN} = -10 dBm unless otherwise specified)

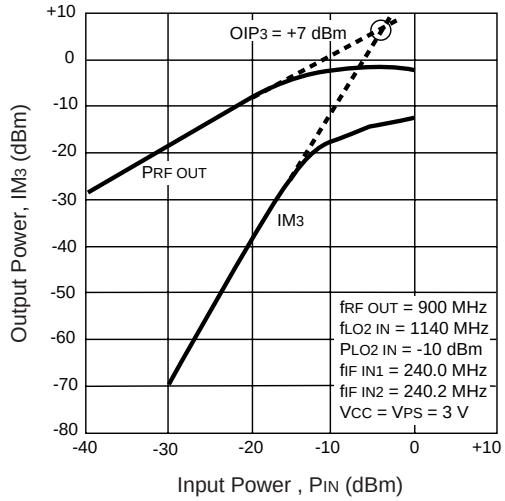
CURRENT vs. VOLTAGE



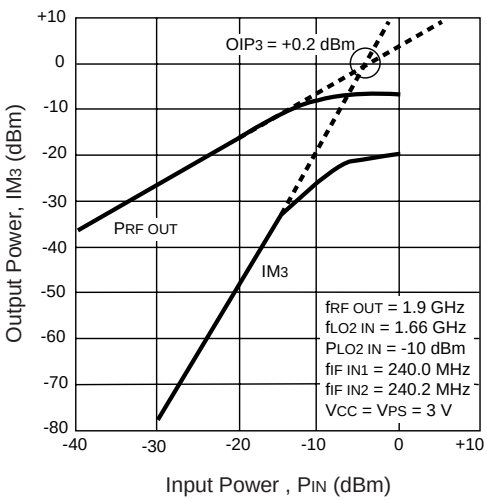
UPCONVERTER CONVERSION GAIN vs. VOLTAGE



UPCONVERTER INPUT POWER vs. OUTPUT POWER

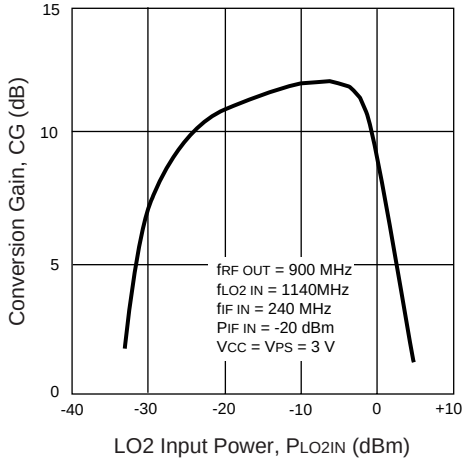


UPCONVERTER INPUT POWER vs. OUTPUT POWER

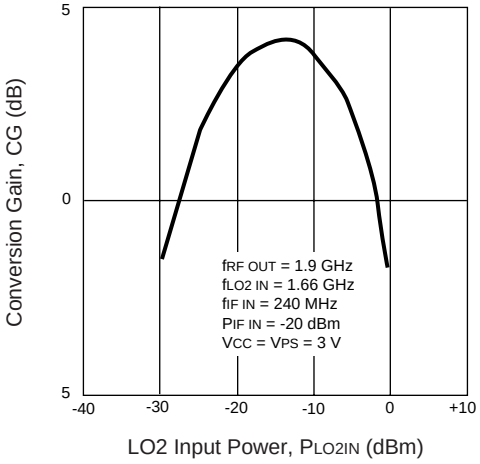


TYPICAL PERFORMANCE CURVES (T_A = 25°C)

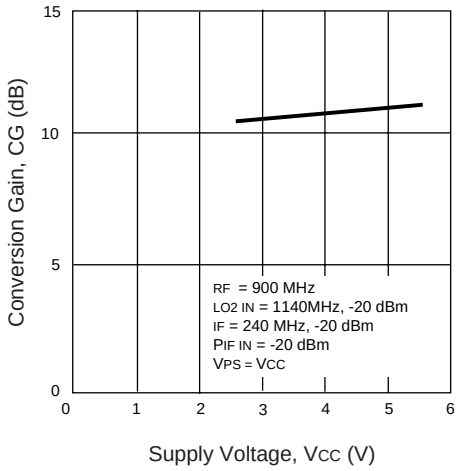
UPCONVERTER
CONVERSION GAIN vs. LO POWER



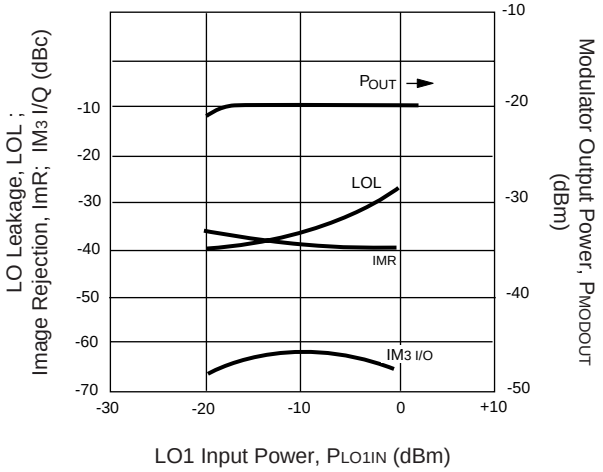
UPCONVERTER
CONVERSION GAIN vs. LO POWER



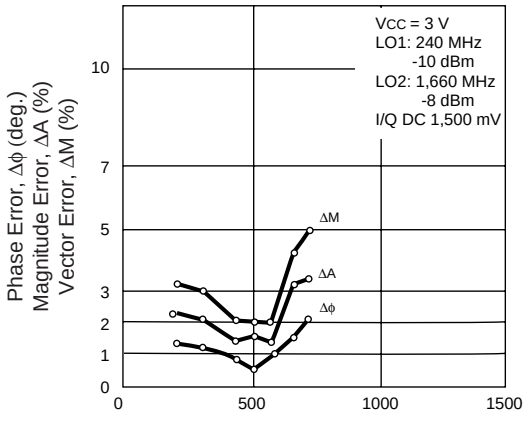
UPCONVERTER
CONVERSION GAIN vs. VOLTAGE



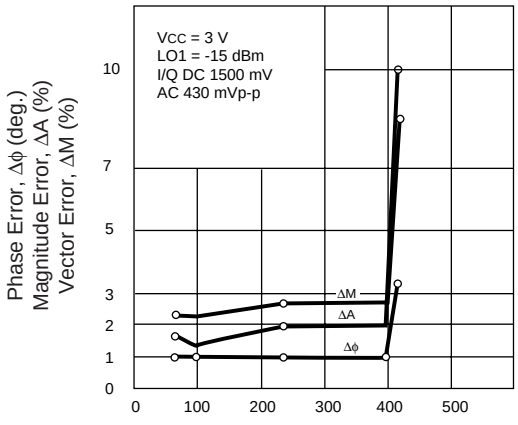
MODULATOR
OUTPUT POWER, LO LEAKAGE , IMAGE REJECTION
AND I/Q 3rd ORDER INTERMODULATION DISTORTION
vs. LO1 INPUT POWER



VECTOR ERROR, MAGNITUDE ERROR,
PHASE ERROR vs. I/Q INPUT SIGNAL

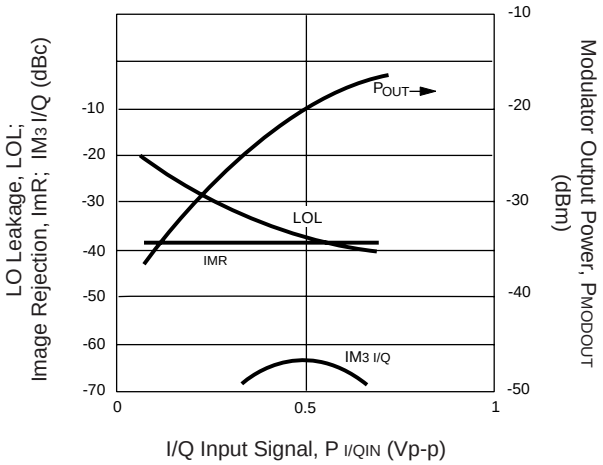


VECTOR ERROR, MAGNITUDE ERROR,
PHASE ERROR vs. LO1 INPUT FREQUENCY

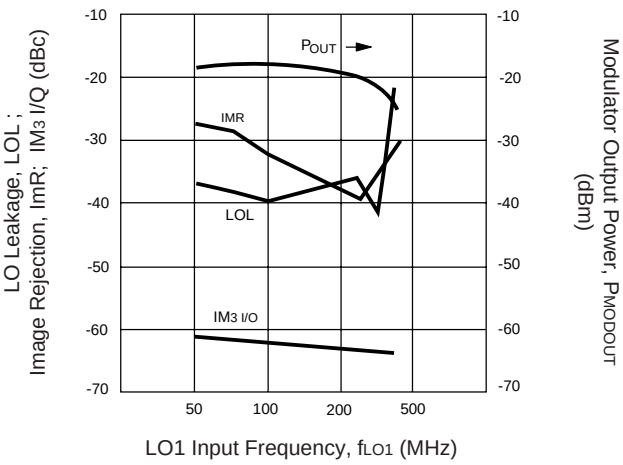


TYPICAL PERFORMANCE CURVES (T_A = 25°C)

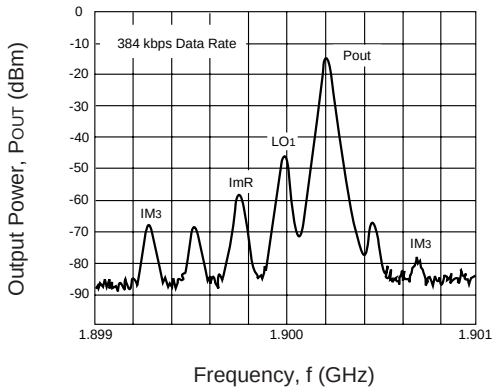
MODULATOR OUTPUT POWER, LO LEAKAGE , IMAGE REJECTION AND I/Q 3rd ORDER INTERMODULATION DISTORTION vs. I/Q INPUT SIGNAL



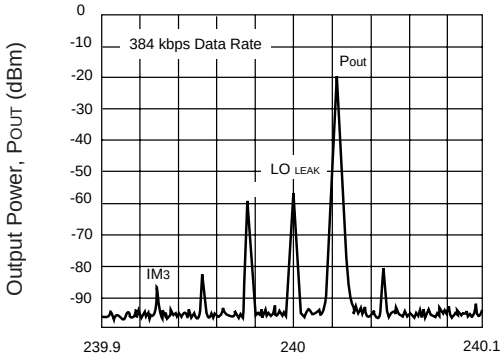
MODULATOR OUTPUT POWER, LO LEAKAGE, IMAGE REJECTION AND I/Q 3rd ORDER INTERMODULATION DISTORTION vs. LO1 INPUT FREQUENCY



MODULATOR AND UPCONVERTER TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM



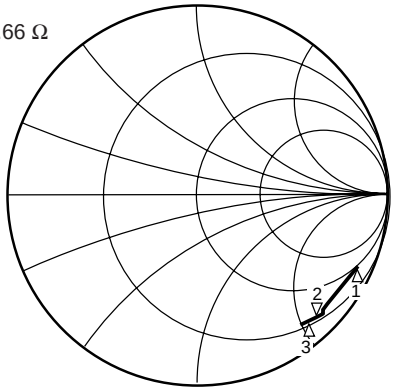
MODULATOR TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM



TYPICAL PERFORMANCE CURVES (T_A = 25°C)

$LO2_{IN}$ INPUT IMPEDANCE

Impedance at
Marker 2:
20.184 - j113.66 Ω

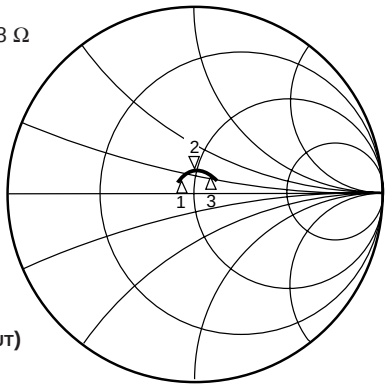


$LO2_{IN}$
Marker
1. 900 MHz
2. 1.66 GHz
3. 1.8 GHz

Start 800 MHz
Stop 1900 MHz

MOD_{OUT} OUTPUT IMPEDANCE

Impedance at
Marker 2:
49.224 - j13.58 Ω

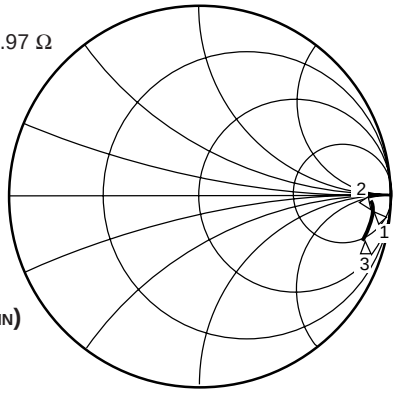


MOD_{OUT} (IF_{OUT})
Marker
1. 100 MHz
2. 240 MHz
3. 400 4Hz

Start 50 MHz
Stop 500 MHz

Upconverter Input Impedance

Impedance at
Marker 2:
262.19 - j394.97 Ω

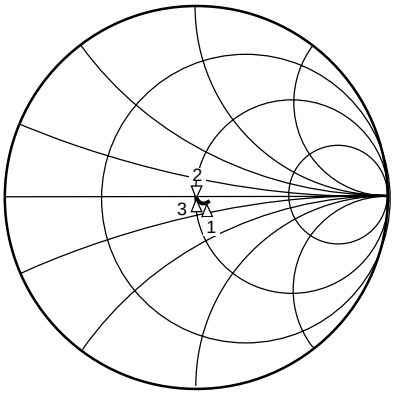


$UPCON_{IN}$ (IF_{IN})
Marker
1. 100 MHz
2. 240 MHz
3. 400 MHz

Start 50 MHz
Stop 500 MHz

LO_{IN} Input Impedance

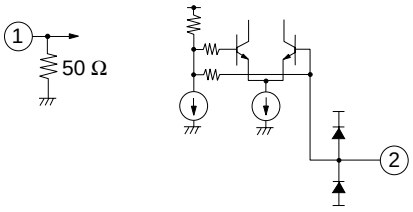
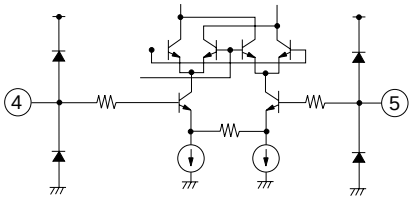
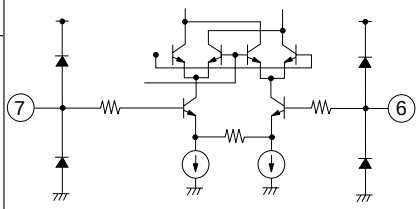
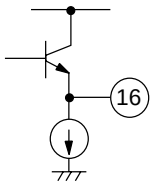
Impedance at
Marker 2:
51.727 - j2 Ω



$LO1_{IN}$
Marker
1. 100 MHz
2. 240 MHz
3. 400 MHz

Start 50 MHz
Stop 500 MHz

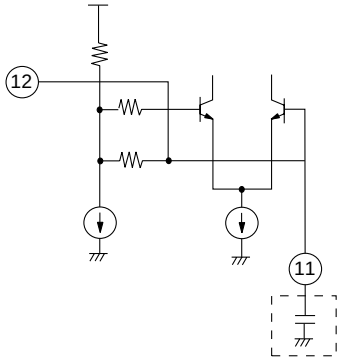
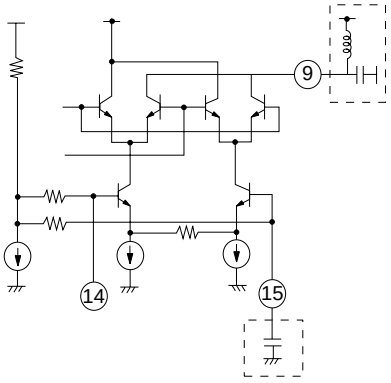
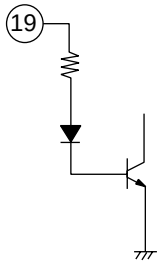
PIN FUNCTIONS

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Supply Voltage</th><th>Pin Voltage</th><th>Description</th><th>Equivalent Circuit</th></tr>
<tr><td>1</td><td>LO_{1IN}
(Modulator)</td><td>—</td><td>0</td><td>LO1 input for the phase shifter. This input impedance is internally matched to 50 Ω.</td><td rowspan="2">  </td></tr>
<tr><td>2</td><td>$\overline{LO1_{IN}}$
(Bypass)</td><td>—</td><td></td><td>Bypass of the LO1 input.This pin is grounded through an internal capacitor. For a single-ended design this pin should be left open.</td></tr>
<tr><td>3</td><td>GND
(Modulator)</td><td></td><td></td><td>Connect to ground with minimum inductance. Track length should be kept as short as possible.</td><td></td></tr>
<tr><td>4</td><td>I</td><td>$V_{CC/2}$*2</td><td>—</td><td>Input for I signal. This input impedance is larger than 20 kΩ. The relationship between the amplitude and the DC bias of the input signal are as follows: *1
<table><tr><th>$V_{CC/2}$ (V)</th><th>Amp. (mVp-p)</th></tr><tr><td>≥1.35</td><td>400</td></tr><tr><td>≥1.5</td><td>600</td></tr><tr><td>≥1.75</td><td>1000</td></tr></table></td><td rowspan="2">  </td></tr>
<tr><td>5</td><td>$\overline{I}$</td><td>$V_{CC/2}$*2</td><td>—</td><td>Input for I signal. This input impedance is larger than 20 kΩ. $V_{CC/2}$ biased DC signal should be input.</td></tr>
<tr><td>6</td><td>$\overline{Q}$</td><td>$V_{CC/2}$*2</td><td>—</td><td>Input for Q signal. This input impedance is larger than 20 kΩ. $V_{CC/2}$ biased DC signal should be input.</td><td rowspan="2">  </td></tr>
<tr><td>7</td><td>Q</td><td>$V_{CC/2}$*2</td><td>—</td><td>Input for Q signal. This input impedance is larger than 20 kΩ. The relationship between the amplitude and the DC bias of the input signal are as follows: *1
<table><tr><th>$V_{CC/2}$ (V)</th><th>Amp. (mVp-p)</th></tr><tr><td>≥1.35</td><td>400</td></tr><tr><td>≥1.5</td><td>600</td></tr><tr><td>≥1.75</td><td>1000</td></tr></table></td></tr>
<tr><td>16</td><td>MOD_{OUT}</td><td>—</td><td></td><td>Output from the modulator. This is emitter follower output. Connect around 15 Ω in series to match to 50 Ω.</td><td>  </td></tr>
</table>

*1: In case I/Q input signals are single ended. I/Q signal inputs can be used either single-ended or differentially with proper terminations.

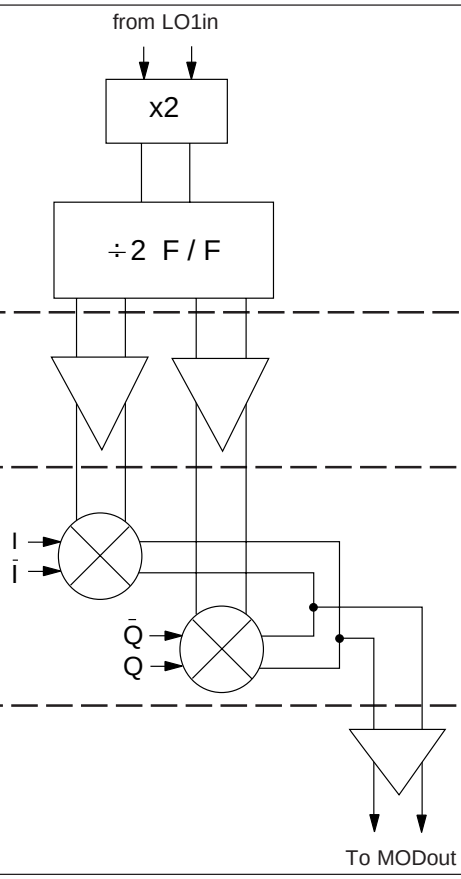
*2: $V_{CC}/2$ DC bias must be supplied to I, $\overline{I}$, Q, $\overline{Q}$.

PIN FUNCTIONS

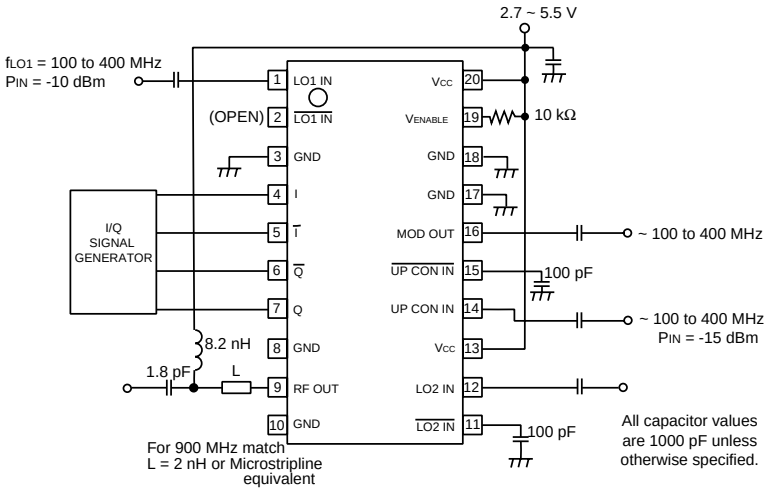
Pin No.	Symbol	Supply Voltage	Pin Voltage	Description	Equivalent Circuit
8 10	GND (Upconverter))	0	-	Connect to ground with minimum inductance. Track length should be kept as short as possible.	
11	$\overline{LO_{2IN}}$ (Bypass)	—	2.0	Bypass of the LO2 input. Requires grounding through an external capacitor.	
12	LO_{2IN} (Upconverter)	-—	0	LO2 input for the Upconverter. This pin is a high impedance input.	
13	V_{CC} (Upconverter)	2.7~5.5	—	Supply voltage pin for the Upconverter.	
9	RF_{OUT}	V_{CC}	—	RF output from the Upconverter. This pin is an open collector output.	
14	Upconverter in	—	2.0	IF input for the Upconverter. This pin is a high impedance input.	
15	$\overline{\text{Upconverter in}}$ (Bypass)	—	2.0	Bypass of the IF input. Requires grounding through an external capacitor.	
17 18	GND	0	—	Connect to ground with minimum inductance. Track length should be kept as short as possible.	
19	V_{PS} (Power Save)	V_{PS}	—	Power save control pin can control the On/Sleep state with bias as follows: V_{PS} (V) / STATE: 1.8~5.5 / ON; 0~1.0 / SLEEP	
20	V_{CC} (Modulator)	2.7~5.5	—	Supply voltage pin for the modulator. An internal regulator helps keep the device stable against temperature or V_{CC} variation.	

MODULATOR INTERNAL FUNCTIONS

Block	Function/Operation	Block Diagram
90° Phase Shifter	Input signal from LO1 is sent to a T-type flip-flop through a frequency doubler. The output signal from the T-type F/F is changed to the same frequency as LO1 with a quadrature phase shift of 0°, 90°, 180°, or 270°. These circuits provide self phase correction for proper quadrature signals.	
Buffer Amplifier	Buffer amplifiers for each phase signal are sent to each mixer.	
Mixer	Each signal from the buffer amps is quadrature modulated with two double-balanced mixers. High accurate phase and amplitude inputs are realized to provide excellent image rejection.	
Adder	Output signal from each mixer is added and sent through a final amplifier stage to pin 16 for further off-chip filtering if necessary.	



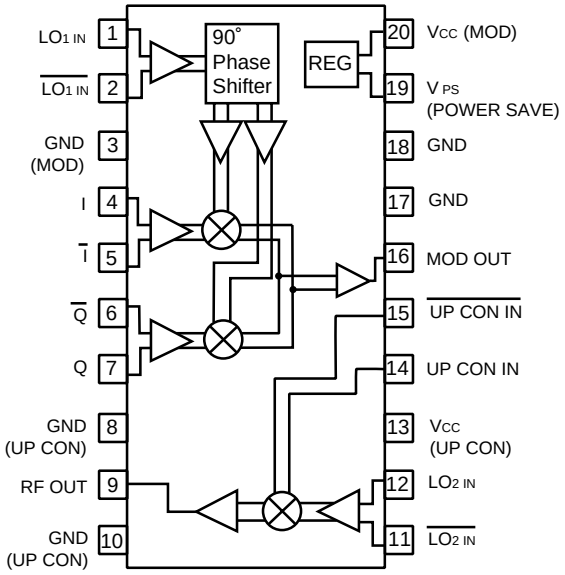
TEST CIRCUIT



Desired Matching Network Impedance, Based On Load Pull Measurements

Frequency	Γ_{Load} (Mag)	Γ_{Load} (Ang)
900 MHz	0.614	67.7°
1900 MHz	0.606	169°
2450 MHz	0.318	-127°

INTERNAL BLOCK DIAGRAM

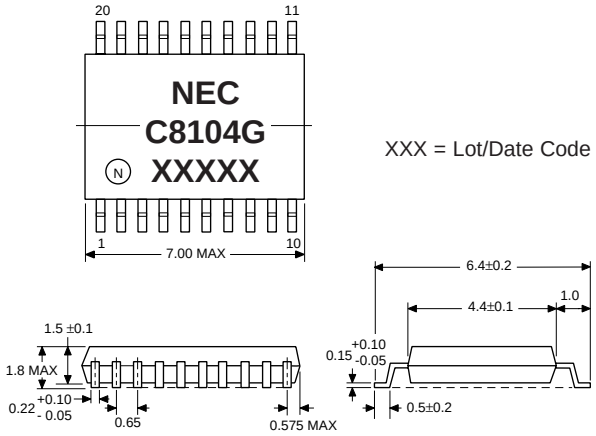


ORDERING INFORMATION

PART NUMBER	QUANTITY
UPC8104GR-E1	2500/Reel

OUTLINE DIMENSIONS (Units in mm)

PACKAGE OUTLINE SSOP 20



LEAD CONNECTIONS

1. LO1IN (Modulator)
2. LO1IN (Bypass)
3. GND (Modulator)
4. I Input
5. Ī Input
6. Q̄ Input
7. Q Input
8. GND (Up Converter)
9. RF OUT
10. GND (Up Converter)
11. LO2IN (Bypass)
12. LO2IN (Upconverter)
13. VCC (Up Converter)
14. Up Converter Input
15. Up Converter Input (Bypass)
16. MOD Out
17. GND
18. GND
19. VPS (Power Save)
20. VCC (Modulator)

All dimensions are typical unless specified otherwise.