ST-NXP Wireless

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- **Company name - Philips Semiconductors** is replaced with **ST-NXP Wireless**.

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- **Web site** - http://www.semiconductors.philips.com is replaced with http://www.stnwireless.com

- **Contact information** - the list of sales offices previously obtained by sending an email to sales.addresses@www.semiconductors.philips.com, is now found at http://www.stnwireless.com under Contacts.

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ST-NXP Wireless

TEA5777

Low-power AM/FM stereo radio for handheld applications

Rev. 01 — 11 April 2006 Product data sheet

1. General description

The TEA5777 is a BiCMOS single-chip (32-pin or 48-pin package), electronically tuned AM/FM stereo radio circuit, with fully integrated IF selectivity and demodulation including local synthesized oscillator, and is intended to be used in electronically tuned radio sets.

In FM mode the radio is completely alignment free and in AM mode only a minimum of antenna input alignment is required. The radio requires a minimum number of small and low cost external components.

The IC communicates with a microcontroller via the I^2C-bus or the 3-wire bus.

2. Features

2.1 General

- High integration level of the AM and FM receiver means a very limited number of external components are required
- On-board PLL synthesizer tuning function which includes VCOs, dividers, phase detectors and charge pump
- FM mixer conversion for US and Europe, OIRT and Japanese band to IF
- Crystal reference frequency oscillator operating at 4 MHz
- External reference input frequency of 13 MHz (bus selectable)
- Autonomous search function
- IF counter with 1-bit output via the bus
- Silent readout of mono or stereo information and IF in-window indication
- Level detector with 4-bit level information output via the bus
- I^2C-bus or 3-wire bus
- Standby mode switched via the bus
- 2 software programmable I/O ports with multiple functions
- Supply voltage range: 2.7 V to 7 V (typical 3 V)
- Low current consumption: 9.8 mA in AM mode and 13.9 mA in FM mode

2.2 AM

- Fully integrated AM RF tuning function (no external varicap required)
- High-impedance MOSFET input
- Fully integrated AM IF filters
- Fully integrated AM VCO
- Integrated image rejection mixer structure
- LW and MW reception possibility

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2.3 FM

- High input sensitivity
- Fully integrated FM IF selectivity
- Fully integrated FM demodulator (no external discriminator)
- Integrated image rejection mixer structure
- RF LC oscillator operating with low cost fixed inductors (referenced to ground)
- FM I/Q mixer for conversion of the US, Europe, Japanese and OIRT band to IF
- Fully integrated, adjustment free, stereo decoder
- Signal dependent mono or stereo blend (with on and off function)
- FM stereo readout via the bus and silent readout mode
- RDS MPX output available
- Stereo decoder can be switched off via the bus
- Integrated anti-birdy filter

3. Applications

- Portable AM/FM stereo radio
- Mini and midi receiver sets
- PC radio applications
- GSM handsets

4. Quick reference data

Table 1. Quick reference data

V_{CCA} = V_{CCD} = 3 V; T_{amb} = 25 °C; all AC values are given in RMS.
See Figure 9 for details on the dummy inputs V_{i1}, V_{i2} and V_{i3}.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General						
V_{CCA}	analog supply voltage		2.7	3.0	7.0	V
V_{CCD}	digital supply voltage		2.7	3.0	5.0	V
I_{CCA}	analog supply current	FM mode	10	13.9	17	mA
		AM mode	8	9.8	11	mA
		Standby mode via bus control	-	0.03	0.15	mA
I_{CCD}	digital supply current	FM mode	0.5	0.8	1.5	mA
		AM mode	0.5	0.8	1.5	mA
		Standby mode via bus control	-	0.13	0.25	mA
T_{amb}	ambient temperature		–10	-	+65	°C
Tuning						
V_O	output voltage	tuning voltage range on pin CPOUT	0.2	-	V_{CCA} – 0.3	V

Table 1. Quick reference data *...continued*

V_{CCA} = V_{CCD} = 3 V; T_{amb} = 25 °C; all AC values are given in RMS.
See Figure 9 for details on the dummy inputs V_{i1}, V_{i2} and V_{i3}.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{RF}	RF frequency	FM	[1]				
		f_{step} = 10 kHz; f_{IF} = 150 kHz		10.24	-	81.91	MHz
		f_{step} = 33.333 kHz; f_{IF} = 133.333 kHz		34.13	-	273.03	MHz
		f_{step} = 50 kHz; f_{IF} = 150 kHz		51.2	-	409.55	MHz
		AM; f_{step} = 1 kHz; f_{IF} = 21 kHz	[1]				
		LW		128	-	511.75	kHz
		MW		512	-	2047	kHz
FM performance[2]							
V_i	input voltage	V_i = V_{i2} = RF sensitivity at dummy input	[3]	-	2.7	3.5	µV
$V_{o(AF)}$	AF output voltage	measured on pins VAFL and VAFR	[4]				
		f_{IF} = 133.333 kHz		70	95	120	mV
		f_{IF} = 150 kHz		55	75	95	mV
S/N	signal-to-noise ratio	measured on pin MPXOUT		-	60	-	dB
THD	total harmonic distortion	measured on pin MPXOUT	[6]	-	0.55	1.5	%
AM performance[7]							
V_i	input voltage	V_i = V_{i1} = RF sensitivity at dummy input	[8]	-	155	-	µV
E	electric field strength	RF sensitivity with ferroceptor	[9]	-	2.9	-	mV/m
$V_{o(AF)}$	AF output voltage	measured on pins VAFL and VAFR	[10]	72	90	108	mV
S/N	signal-to-noise ratio		[11]	40	48	-	dB
THD	total harmonic distortion		[12]	-	1	2.5	%
MPX stereo decoder performance							
α_{cs}	channel separation		[13]	26	40	-	dB

[1] Programmable frequency range of the synthesizer referred to the antenna input.

[2] f_{RF} = 100 MHz; $\Delta f_{FM(max)}$ = 22.5 kHz; f_{mod} = 1 kHz; τ_{deemp} = 50 µs.

[3] The sensitivity at the dummy input is equivalent to EMF in a 75 Ω system.
Conditions: (S+N)/N = 26 dB; L = R; $B_{aud(-3dB)}$ = 300 Hz to 15 kHz, A-weighted; f_{IF} = 133.333 kHz.

[4] V_{i2} = 1 mV; $\Delta f_{FM(max)}$ = 22.5 kHz.

[5] V_{i2} = 1 mV; L = R; $B_{aud(-3dB)}$ = 300 Hz to 15 kHz, A-weighted; f_{IF} = 133.333 kHz.

[6] V_{i2} = 1 mV; Δf = 75 kHz; with external τ_{deemp} = 50 µs; $B_{aud(-3dB)}$ limited to 15 kHz.

[7] f_{RF} = 918 kHz; m = 0.3; f_{mod} = 1 kHz; τ_{deemp} = 75 µs

[8] Conditions: (S+N)/N = 26 dB; m = 0.3; A-weighting filter.

[9] With ferroceptor C8E-A0424 TOKO Inc; (S+N)/N = 26 dB; A-weighting filter.

[10] V_{i1} = 5 mV.

[11] V_{i1} = 5 mV; A-weighting filter.

[12] V_{i1} = 5 mV; m = 0.8; bit AGCRF = 0 (slow AGC RF); bit AGCIF = 0 (slow AGC IF); $B_{aud(-3dB)}$ limited to 15 kHz.

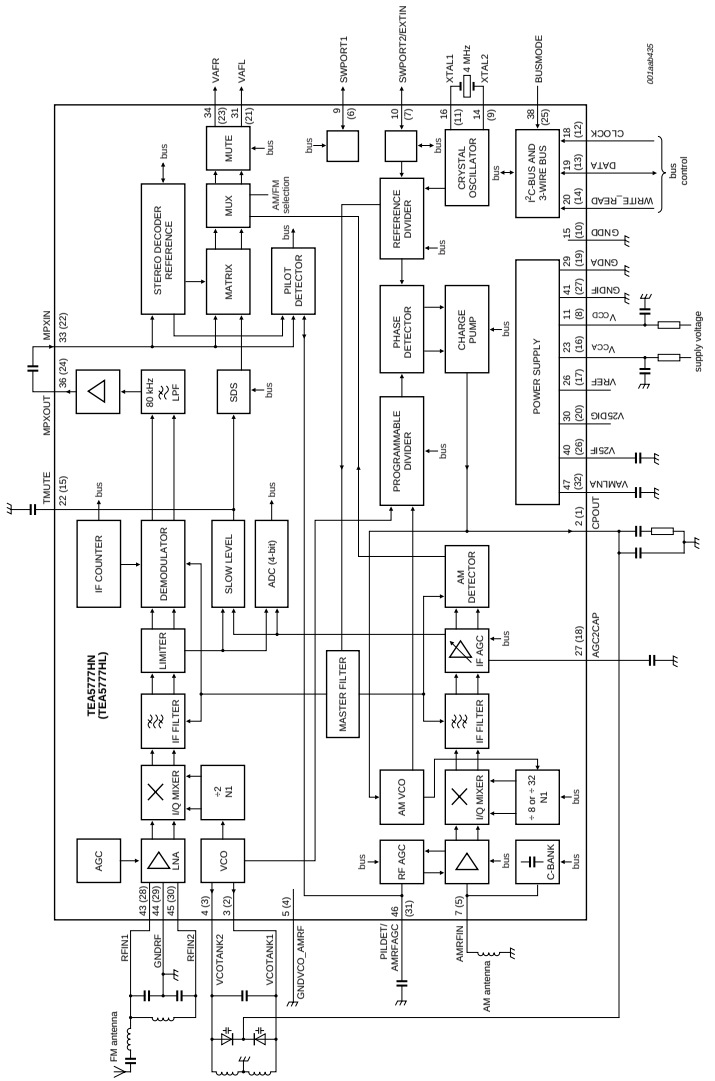
[13] V_{i3} = 300 mV; f_{mod} = 1 kHz; V_{pilot} = 30 mV; R = 1 and L = 0 or R = 0 and L = 1; V_{TMUTE} = 1 V; f_{IF} = 133.333 kHz; $B_{aud(-3dB)}$ limited to 15 kHz.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TEA5777HN	HVQFN48	plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 × 7 × 0.85 mm	SOT619-1
TEA5777HL	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1

6. Block diagram



Pin numbers in parenthesis apply to TEA5777HL.

Fig 1. Block diagram

7. Pinning information

7.1 Pinning

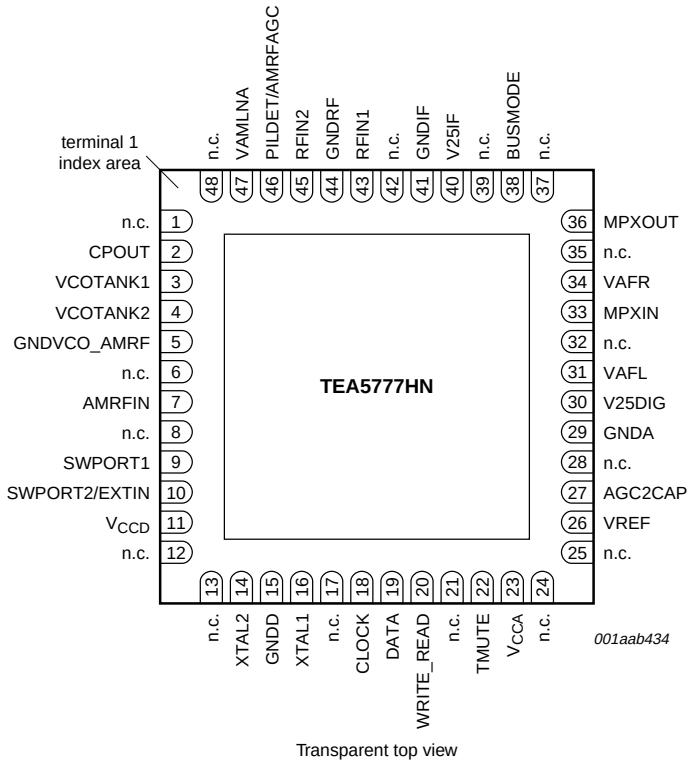


Fig 2. Pin configuration HVQFN48

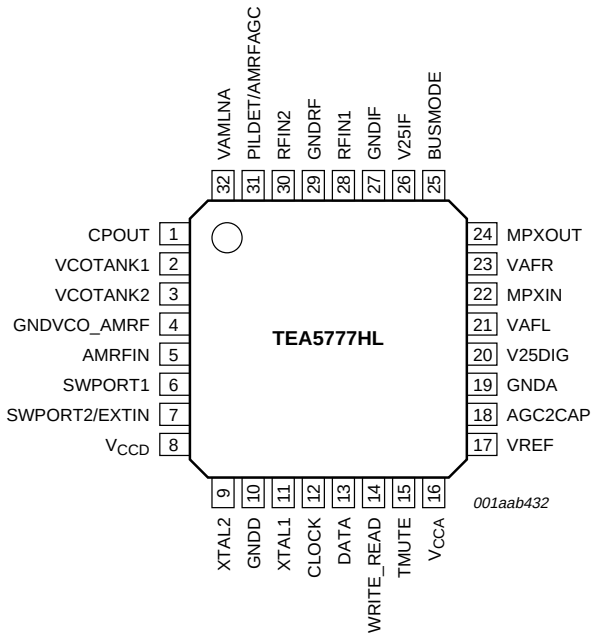


Fig 3. Pin configuration LQFP32

7.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	HVQFN48	LQFP32	
n.c.	1	-	not connected
CPOUT	2	1	tuning current output
VCOTANK1	3	2	parallel tuned FM oscillator to ground output 1
VCOTANK2	4	3	parallel tuned FM oscillator to ground output 2
GNDVCO_AMRF	5	4	FM VCO and AM RF input ground
n.c.	6	-	not connected
AMRFIN	7	5	AM RF input (FET input)
n.c.	8	-	not connected
SWPORT1	9	6	programmable output and input port 1
SWPORT2/EXTIN	10	7	programmable output and input port 2 or external reference frequency input
V_{CCD}	11	8	digital supply voltage
n.c.	12	-	not connected
n.c.	13	-	not connected
XTAL2	14	9	crystal input 2
GNDD	15	10	digital ground
XTAL1	16	11	crystal input 1
n.c.	17	-	not connected

Table 3. Pin description *...continued*

Symbol	Pin		Description
	HVQFN48	LQFP32	
CLOCK	18	12	I^2C-bus and 3-wire bus clock input
DATA	19	13	I^2C-bus and 3-wire bus data input and output
WRITE_READ	20	14	3-wire bus write and read input
n.c.	21	-	not connected
TMUTE	22	15	field strength indicator capacitor connection
V_{CCA}	23	16	analog supply voltage
n.c.	24	-	not connected
n.c.	25	-	not connected
VREF	26	17	1.25 V stabilized reference voltage output
AGC2CAP	27	18	AM IF AGC capacitor connection
n.c.	28	-	not connected
GNDA	29	19	analog ground
V25DIG	30	20	internal stabilized supply voltage (digital part) output
VAFL	31	21	left channel output
n.c.	32	-	not connected
MPXIN	33	22	stereo decoder input
VAFR	34	23	right channel output
n.c.	35	-	not connected
MPXOUT	36	24	FM MPX output
n.c.	37	-	not connected
BUSMODE	38	25	bus mode selection input
n.c.	39	-	not connected
V25IF	40	26	internal stabilized supply voltage (IF, demodulator and integrated birdy filter) output
GNDIF	41	27	ground of IF, demodulator and integrated birdy filter
n.c.	42	-	not connected
RFIN1	43	28	FM RF antenna input 1
GNDRF	44	29	FM RF ground
RFIN2	45	30	FM RF antenna input 2
PILDET/AMRFAGC	46	31	stereo decoder pilot detector filter input or AM RF AGC capacitor connection
VAMLNA	47	32	internal stabilized supply voltage (AM front end) output
n.c.	48	-	not connected

8. Functional description

The TEA5777 is an integrated AM/FM stereo radio circuit with very high integration level including digital tuning and control functions.

The IC communicates with a microcontroller via the I^2C-bus or the 3-wire bus interface and provides the following functions:

- AM single conversion receiver with integrated image rejection for f_{IF} = 21 kHz
- FM single conversion receiver with integrated image rejection for f_{IF} = 133.333 kHz or 150 kHz (software selectable)
- FM stereo decoder with signal dependent stereo effect

The AM circuit incorporates:

- Integrated antenna tuning function
- Integrated I/Q IF channel
- On-chip image reject mixer structure
- A fully integrated AM VCO with $f_{VCO} = 8 \times (f_{RF} + f_{IF})$
- Software selectable high-side or low-side oscillator injection
- A fully integrated AM detector

The FM circuit incorporates:

- Integrated I/Q IF channel
- On-chip image reject mixer structure
- External RF VCO running at $f_{VCO} = 2 \times (f_{RF} \pm f_{IF})$
- Software selectable high-side or low-side oscillator injection
- A fully integrated demodulator
- Japan band possibility

The stereo decoder incorporates:

- A 1.52 MHz VCO, that needs no external adjustment, which can lock to the 19 kHz stereo pilot tone by means of a PLL system; the sub-carrier frequencies of 19 kHz, 38 kHz and others are regenerated from the VCO output
- Integrated 50 µs or 75 µs (switchable) de-emphasis
- Signal Dependent Stereo (SDS) function can be switched off via the bus interface
- Stereo decoder can be switched off in order to save power

Tuning function:

- The tuning synthesizer is on-chip with the radio and utilizes a PLL system for tuning and an IF counter has been added for search-stop detection
- Tuning to a wanted input signal can be achieved by preset tuning or search tuning. For the latter the IC has a built-in auto search function which reduces the load of the microcontroller

Bus communication:

- Bus communication takes place via the I^2C-bus or the 3-wire bus protocol. Selection of the bus mode is done by hardware programming via pin BUSMODE
- 4-bit ADC level information, 1-bit IF counter and mono or stereo indication (in FM mode) can be read via the bus. Alternatively, the mono or stereo and the IF in-window indication can be obtained via silent readout via the bus lines CLOCK and DATA

8.1 AM radio part

8.1.1 AM RF amplifier

The AM input pin AMRFIN has a (selectable) high-impedance input. The input is intended to be connected to the top of a tuned circuit. The input impedance is determined by the LNA gain (bit LNA) and the value of the LNA feedback resistor (bit RFB).

For large RF input signals, the RF AGC reduces the input signal level to the AM front end in order to prevent overloading. The required AM RF AGC time constant is created by means of an internal current source and the capacitor connected to pin PILDET/AMRFAGC. During search operation the response time of this RF AGC circuit can be speeded up via the bus control by bit AGCRF.

8.1.2 Tuning AM antenna circuit

The tuning capacitor for the AM antenna circuit has been integrated by means of a capacitor bank (C-bank) and the tuning frequency can be programmed in discrete steps via the bus. No external varactor diode is required. In order to match the capacitor bank to the external AM antenna coil, a provision has been made to electronically align the IC to the AM antenna. For this bit CALLIGN has to be set to logic 1 and the corresponding bits C[6:0] have to be programmed. After this alignment bit CALLIGN should be set to logic 0 again to freeze the alignment capacitor value and to enable the control over the main capacitor bank again.

For more details on the alignment, see Section 13.1 and the application note.

For LW mode an external capacitor needs to be added in parallel to the LW coil.

8.1.3 AM I/Q mixer

AM quadrature mixers, in an orthogonal architecture, convert AM RF signals to the internal f_{IF} = 21 kHz. The mixer architecture provides inherent image rejection.

8.1.4 AM VCO

The fully integrated VCO provides the local oscillator signals for the AM quadrature mixers. No external components are required.

The internal VCO frequency ranges from 4 MHz to 14 MHz and the proper divider ratio is chosen by selecting the MW or LW band via the bus control bit MWLW.

Programming of the VCO is done:

- For MW: $f_{VCO} = 8 \times (f_{RF} \pm f_{IF})$
- For LW: $f_{VCO} = 32 \times (f_{RF} \pm f_{IF})$

High-side injection or low-side injection of the VCO can be chosen:

- High-side injection: local oscillator frequency at mixer input is higher than RF input signal frequency.
- Low-side injection: local oscillator frequency at mixer input is lower than RF input signal frequency.

8.1.5 AM IF filter

The AM circuit incorporates an I and Q orthogonal channel path with fully integrated polyphase IF filter. All AM IF filtering is done inside the IC, therefore no external filter components are required. The center frequency of the filter is 21 kHz and the −3 dB bandwidth amounts to 8 kHz.

8.1.6 AM IF amplification and AM detection

The IF AGC controls the IF amplification and a fully integrated AM detector converts the AM IF signal into audio. In AM mode the capacitor connected to pin AGC2CAP is used for IF AGC filtering. The value of this capacitor is a compromise between AGC speed and THD. In order to achieve an acceptable THD in normal mode and an acceptable AGC response during e.g. a search action, the time constant can be switched to a value 15 times lower by means of bit AGCIF. In autonomous search mode (bit SEARCH = 1) the time constant is switched automatically to the lowest value.

8.2 FM radio part

8.2.1 Low noise RF amplifier

The FM circuit incorporates a wideband input. The LNA input impedance together with the LC RF input circuit defines a low Q, FM band-pass filter. The input filter is also used for impedance matching between the source impedance and the 300 Ω LNA input impedance between pins RFIN1 and RFIN2. An RF AGC circuit prevents the mixer and IF filter from overdrive conditions.

8.2.2 FM I/Q mixer

FM quadrature mixers, in an orthogonal I/Q architecture, convert FM RF signals to the internal f_{IF} = 133.333 kHz or 150 kHz. The mixer architecture provides inherent image rejection. Whether f_{IF} = 133.333 kHz or 150 kHz is chosen depends on bits FREF[1:0].

For choosing the best signal conditions with respect to the influence of the image signals, high-side or low-side injection can be selected:

- High-side injection: local oscillator frequency at mixer input is higher than RF input signal frequency.
- Low-side injection: local oscillator frequency at mixer input is lower than RF input signal frequency.

8.2.3 FM VCO

The symmetrical LC, varactor tuned VCO provides the oscillator signals for the FM quadrature mixers (pins VCOTANK1 and VCOTANK2). The VCO operates at double the RF frequency $f_{VCO} = 2 \times (f_{RF} \pm f_{IF})$ and has an internal AGC control circuit in order to guarantee good start-up behavior and carrier-to-noise ratio (C/N) even with low Q coils (Q > 40). High-side injection ($+f_{IF}$) or low-side injection ($-f_{IF}$) of the VCO can be chosen via the bus control.

8.2.4 FM IF filter

The FM signal path incorporates an I and Q orthogonal FM channel with fully integrated polyphase IF filter. All FM IF filtering is done inside the IC, therefore no external filter components are required. The center frequency of the filter matches the chosen IF (f_{IF} = 133.333 kHz or 150 kHz) and has a −3 dB bandwidth of approximately 110 kHz.

8.2.5 FM demodulator

The FM demodulator is fully integrated and needs no external components. In order to remove undesired IF and or RF input related components, a 80 kHz low-pass filter has been integrated.

8.3 Stereo decoder

8.3.1 MPX decoder

The PLL stereo decoder is alignment free and incorporates a fully integrated PLL loop filter. The stereo decoder can be switched to forced mono via bus control bit FOMO.

8.3.2 Signal strength depending mono/stereo blend

When decreasing the RF input level, the MPX decoder blends from stereo to mono to limit the output noise. The control signal is obtained from the low-pass filtered level information at pin TMUTE. This blend function, called SDS, can also be switched off via bus control bit SDSOFF and a RF level related sudden change from stereo to mono transition will result.

8.3.3 Pilot detector

A pilot detector, with external filter capacitor at pin PILDET/AMRFAGC, is used to detect the presence of a stereo signal. Mono or stereo reception can be read via the bus control, but can also be passed to pin DATA in the Dbus mode (see Section 9). For this option, bit DBUS has to be programmed. In this case, no bus action is required (silent readout) to read the status of the pilot detector and the information is continuously available.

8.3.4 De-emphasis

In FM mode, the de-emphasis is switchable between 50 µs and 75 µs (bit DEEM). In AM mode, bit DEEM selects a low-pass filter with the time constant 50 µs or 75 µs in order to limit the noise bandwidth.

8.4 Tuning function

The tuning concept of the TEA5777 is based on a PLL and programming of the required frequency takes place via the bus control.

8.4.1 Reference frequency generation

The internally required reference frequency can be obtained from the integrated crystal oscillator or from an externally applied reference signal of 13 MHz. Selection of the reference signal (internal or external) takes place via the bus control.

The reference frequency signals are used for:

- Reference frequency divider for the PLL synthesizer
- Center frequency adjustment of the IF filters
- Free running frequency adjustment of the stereo decoder VCO
- Clocking the stereo decoder state machine
- Timing of the IF counter
- Sampling the RF level for the level ADC

8.4.2 Crystal oscillator

The symmetrical crystal oscillator can operate with a 4 MHz clock crystal. An amplitude control function is implemented in order to minimize the higher harmonic component signal levels.

8.4.3 IF counter

An IF counter has been added for search-stop detection (optional, i.e. can be enabled or disabled via bit IFCE). The IF counter result is a 1-bit output and in-window yes or no and available via bus control. In order to minimize the interference, the IF counter can be disabled via the bus control bit IFCE. In both AM and FM modes, two IF window settings can be chosen by bit IFW.

When Dbus mode is activated and bit IFCE = 1, the IF counter result is available at pin DATA (see Table 8). In this mode, the IF counter ready flag (bit IFCRDY) is put on pin DATA. Disabling bit IFCE, while Dbus mode is active, puts the mono or stereo indication information on pin DATA. In this case no bus actions are required to read the status of the IF counter (silent readout).

Remark: For updating the IF counter information a short pulse on pin WRITE_READ should be generated.

8.4.4 Automatic search operation

The IC can be programmed to an autonomous search mode operation. In this mode, the IC will search for a new station without the need of communication to the microcontroller. To enable this mode, bit SEARCH has to be set. Under control of bit UPDWN, search stop level bits SLEV[1:0] and search step control bits STEP[1:0], various search modes can be selected (see Section 9).

Before this mode can be activated, first the upper and lower band limits have to be programmed. Bit PROGBLIM = 1 and bit UPDWN = 1 programs the upper band limit, while bit PROGBLIM = 1 and bit UPDWN = 0 programs the lower band limit. Bit SFOUND signals whether a new station is found. Bit BLIM signals whether a band limit is reached.

In AM mode, bit AMDELAY selects either a 40 ms or 80 ms delay time. The best value to be selected depends on the realized AM IF AGC response (see Section 8.1.6).

8.5 RF level information (RSSI)

For processing Receiver Signal Strength Information (RSSI) in both AM and FM modes, the internal level voltage is analog-to-digital converted with a 4-bit ADC. The level information can be read by bits LEV[3:0] in the read register. In autonomous search mode, bits LEV[3:0] still indicate some momentary level information, however the data is dependent upon the readout timing and can be considered to have no relevance to the user. The ADC full-scale goes from 0.25 V to 0.95 V. In AM mode, the level information covers the ADC full-scale. In FM mode, the level information does not fully cover the ADC full-scale.

8.6 Software programmable ports

Two software programmable ports can be addressed via the bus control. These ports can be independently switched to multiple functions, knowing:

- Outputs: SWPORT1 and SWPORT2 can act as output ports which are capable of sourcing and sinking approximately 9 mA.
- Inputs: SWPORT1 and SWPORT2 can act as input ports of which the status can be read out via bus control.

Remark: Port SWPORT2 can be switched as input for the 13 MHz reference signal. In that case, no other functions can be programmed for this port.

9. Control functions via I²C-bus and 3-wire bus

9.1 Bus interface

Via the bus interface a couple of main blocks are controlled:

- Tuning system
- Autonomous search
- AM capacitor bank (C-bank control)
- IF counter
- 4-bit level ADC
- Stereo decoder
- Mute and de-emphasis
- SWPORT1 and SWPORT2 outputs (I/O port control)

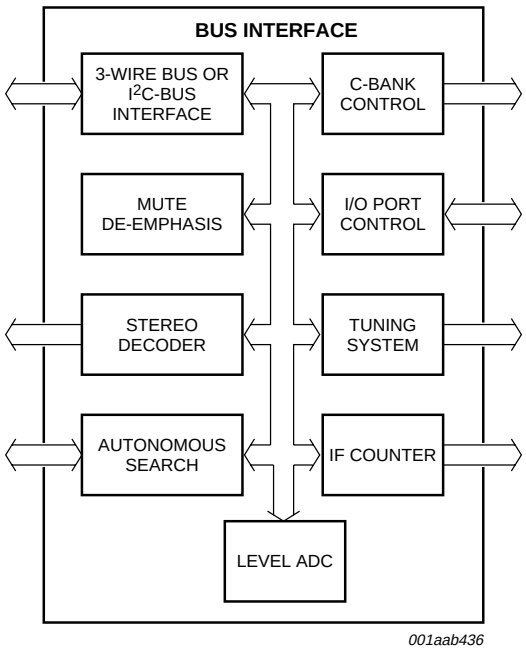


Fig 4. Bus interface

9.2 Bus protocol

The TEA5777 bus interface is a combination of an I²C-bus and a 3-wire-bus. The bus mode is determined by the bus mode input pin BUSMODE which will be connected to ground or to V_{CCD}:

- Pin BUSMODE = HIGH enables the 3-wire mode
- Pin BUSMODE = LOW enables I²C-bus mode

9.3 I²C-bus mode

The I²C-bus interface is based on *'The I²C-bus specification'* version 2.1 January 2000.

In the I²C-bus mode, only pins CLOCK and DATA are used for data transfer. The level on pin WRITE_READ is don't care.

Data transfer to the bus interface is byte oriented and no sub-addressing is used.

The data transfer consists of a START condition, device address byte plus R/W

Data is written at the rising edge and data is clocked out at the falling edge. The I²C-bus can operate at a maximum clock frequency of 400 kHz.

The I²C-bus device address of the TEA5777 is: 110 0000 (7 bits).

Table 4. I²C-bus data transfer

Condition	Byte	Description
START		start by master
	Address byte	device address + R/W bit
ACK		acknowledge by slave
	Byte 1	data byte 1
ACK		acknowledge by slave
	Byte 2	data byte 2
ACK		acknowledge by slave
	Byte n	data byte n
ACK		acknowledge by slave
STOP		stop by master

9.3.1 Write mode

The bus interface has a total of 6 write registers. Before data can be written to these registers, the I²C-bus device address byte has to be written to the IC

After the bus interface (slave) recognizes a start of transmission, the address byte is written to the bus. If the address is equal to the internal address of the bus interface, an acknowledge is given to the master and data can be written to the write registers.

If the bus address does not match, no acknowledge is given and the internal bus interface clock is disabled until a next start is detected.

Table 5. I²C-bus write mode

Condition	Byte	Description
START		start by master
	Address byte	1100 0000 (bit R/W = 0)
ACK		acknowledge by slave
	Byte 1	data byte 1
ACK		acknowledge by slave
	Byte 2	data byte 2
ACK		acknowledge by slave
	:	:
	Byte 6	data byte 6
ACK		acknowledge by slave
STOP		stop by master

9.3.2 Read mode

The bus interface has a total of 3 read bytes. If a start of transmission is detected and the I²C-bus device address matches with the internal address, an acknowledge is given and the data is clocked out. If not, the internal clock is disabled and the data output will be logic 1s (FFh).

Table 6. I²C-bus read mode

Condition	Byte	Description
START		start by master
	Address byte	1100 0001 (bit R/W = 1)
ACK		acknowledge by slave
	Byte 1	data byte 1
ACK		acknowledge by slave
	Byte 2	data byte 2
ACK		acknowledge by slave
	Byte 3	data byte 3
STOP		stop by master

9.3.3 Dbus function in I²C-bus mode (silent readout)

The Dbus function becomes active when bit DBUS = 1 and when the maximum available bytes are written in the write mode or when the maximum available bytes are read in the read mode. At every start of an I²C-bus data transfer, the Dbus mode is deactivated.

When the Dbus mode is active in I²C-bus mode, pin WRITE_READ becomes an open-collector output (pull-up resistor required). Depending on the setting of bit IFCE and bit SEARCH, the following data will be available at pin WRITE_READ:

- Mono or stereo indication flag
- IFC counter flag
- SFOUND flag or BLIM reached flag

In Table 7 the data at pin WRITE_READ is depicted as a function of bits DBUS, SEARCH and IFCE.

Table 7. Definition pin WRITE_READ functionality in I²C-bus Dbus mode

Bit			Pin WRITE_READ	
DBUS	SEARCH	IFCE	Output signal	Status[1]
0	X	X	3-state	not applicable
1	0	0	mono or stereo flag	H = stereo, L = mono
	0	1	IFCRDY flag	H = IF counter ready
	1	X	SFOUND or BLIM flag	H = station found or band limit reached

[1] H = HIGH-level output voltage
L = LOW-level output voltage

9.4 3-wire bus mode

For the 3-wire bus mode pin BUSMODE = HIGH, i.e. connected to V_{CCA}. The pins CLOCK, DATA and WRITE_READ are used to communicate with the external hardware (microcontroller or PC). The bus operates at a maximum clock of 1 MHz.

The selected mode (read or write mode) is determined by the rising or falling edge of signal WRITE_READ.

9.4.1 Write mode

At the rising edge of signal WRITE_READ the bus interface is set to the write mode. At every rising edge of the clock input (CLOCK) the data is clocked in. Signal DATA has to be stable before it can be clocked in.

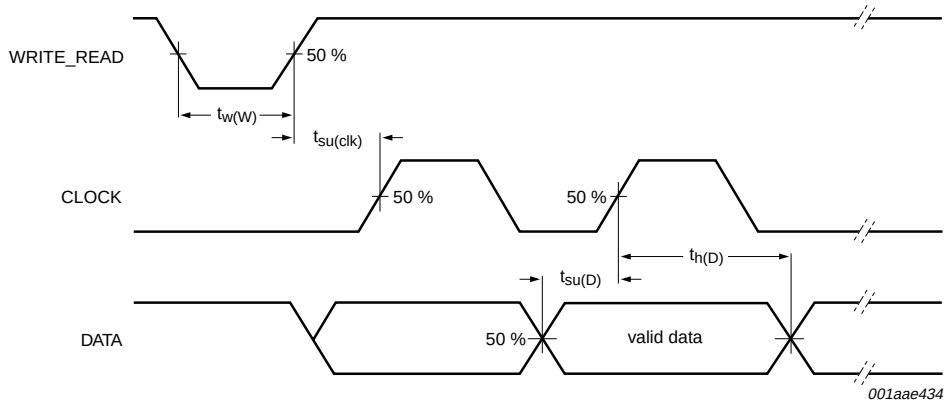


Fig 5. 3-wire bus write data

9.4.2 Read mode

At the falling edge of signal WRITE_READ the bus interface is set to the read mode. Data is clocked out on every falling edge of the input clock. In the read mode, pin DATA becomes an open-collector output and an external pull-up resistor is required.

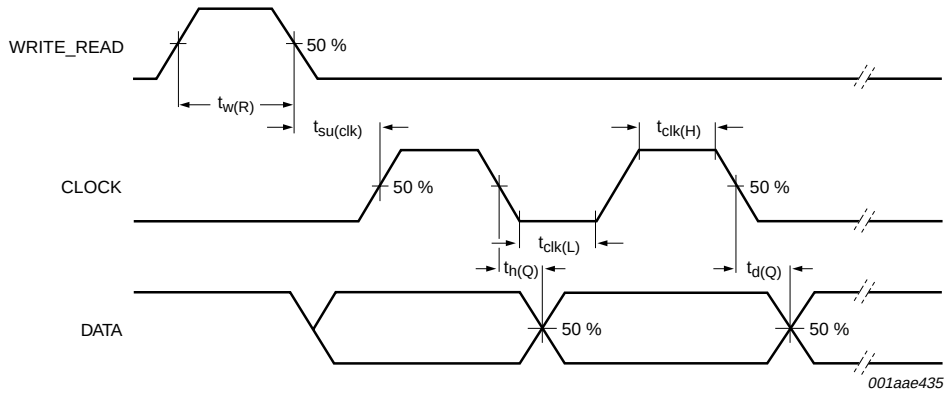


Fig 6. 3-wire bus read data

9.4.3 Dbus function in 3-wire mode (silent readout)

Bus pins CLOCK and DATA are bidirectional and act as inputs when bit DBUS = 0, but are open-collector outputs when bit DBUS = 1. External pull-up resistors are required in this case.

In Dbus mode, pins CLOCK and DATA are used for output data and pin WRITE_READ is used as an input.

With a rising edge (write mode) or falling edge (read mode) of signal WRITE_READ the Dbus mode is deactivated and a transmission is started.

The Dbus mode is activated with bit DBUS = 1 and after transfer of all 6 data bytes in the write mode or all 3 data bytes in the read mode.

Data on pins CLOCK and DATA in the Dbus mode is given in Table 8.

Table 8. CLOCK and DATA lines in Dbus-mode

Bit			Pin CLOCK		Pin DATA	
DBUS	**SEARCH**	**IFCE**	**Signal**	**Status[1]**	**Signal**	**Status[1]**
0	X	X	input	-	input	-
1	0	0	IFC flag	H = IF in-window	mono/stereo flag	H = stereo, L = mono
		1	IFC flag	H = IF in-window	IFCRDY flag	H = IF counter ready
1	1	X	SFOUND flag	H = station found	BLIM flag	H = band limit reached

[1] H = HIGH-level output voltage
L = LOW-level output voltage

9.5 Data transfer in I²C-bus and 3-wire mode

In the write mode, the data transfer between the TEA5777 (slave) and the microcontroller (master) is byte oriented.

In the read mode, the data transfer from slave to master is bit oriented.

Remark: For writing to the PLL, it is necessary to write both the first and second data byte. Only after completing the data transfer of data byte 2 is the PLL word copied into the PLL register.

9.5.1 Register definition in write mode

Table 9. Survey of bit names in FM write mode

*Bits marked with * are common for FM and AM mode.*

Bits	7	6	5	4	3	2	1	0
Byte 1	MUTE*	AM/FM*	STB*	PLL12	PLL11	PLL10	PLL9	PLL8
Byte 2	PLL7	PLL6	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0
Byte 3	FREF1	FREF0	IFCE*	IFW*	HILO*	DBUS*	-	INTEXT*
Byte 4	P1*	P0*	PEN1*	PEN0*	-	CHP0*	DEEM*	-
Byte 5	FOMO	SDSOFF	DOFF	-	-	-	-	-
Byte 6	SEARCH*	PROGBLIM*	UPDWN*	SLEV1*	SLEV0*	STEP1	STEP0*	-

9.5.1.1 FM write mode

Table 10. FM write mode - data byte 1

*Bits marked with * are common for FM and AM mode.*

Bit	Symbol	Description
7 (MSB)	MUTE*	audio mute: 0 = audio not muted; 1 = audio muted
6	AM/FM*	AM/FM selection: 0 = FM; 1 = AM
5	STBY*	operating mode: 0 = operating; 1 = standby
4	PLL12	setting of synthesizer programmable counter
3	PLL11	
2	PLL10	
1	PLL9	
0 (LSB)	PLL8	

Table 11. FM write mode - data byte 2

*Bits marked with * are common for FM and AM mode.*

Bit	Symbol	Description
7 (MSB)	PLL7	setting of synthesizer programmable counter
6	PLL6	
5	PLL5	
4	PLL4	
3	PLL3	
2	PLL2	
1	PLL1	
0 (LSB)	PLL0	

Table 12. FM write mode - data byte 3

*Bits marked with * are common for FM and AM mode.*

Bit	Symbol	Description
7 (MSB)	FREF1	IF and reference frequency control: see Table 13
6	FREF0	
5	IFCE*	IF counter: 0 = not enabled; 1 = enabled
4	IFW*	IF window: 0 = 10 kHz; 1 = 20 kHz
3	HILO*	VCO injection mode: 0 = low-side; 1 = high-side
2	DBUS*	Dbus mode selection: 0 = off; 1 = on
1	-	no function
0 (LSB)	INTEXT*	reference frequency source select: 0 = external; 1 = internal

Table 13. FM IF and reference frequency control

Bits FREF[1:0	$f_{ref(VCO)}$	$f_{ref(RF)}$	FM mode
	VCO step frequency (kHz)	reference frequency referred to RF input (kHz)	
00	100	50	f_{IF} = 150 kHz
01	20	10	f_{IF} = 150 kHz for East Europe
10	66.666	33.333	f_{IF} = 133.333 kHz
11	100	50	f_{IF} = 150 kHz

Table 14. FM write mode - data byte 4

*Bits marked with * are common for FM and AM mode.*

Bit	Symbol	Description
7 (MSB)	P1*	I/O port control: see Table 28 and Table 29
6	P0*	
5	PEN1*	
4	PEN0*	
3	-	no function
2	CHP0*	charge pump current: 0 = large; 1 = small
1	DEEM*	de-emphasis: 0 = 50 µs; 1 = 75 µs
0 (LSB)	-	no function

Table 15. FM write mode - data byte 5

*Bits marked with * are common for FM and AM mode.*

Bit	Symbol	Description
7 (MSB)	FOMO	stereo reception: 0 = allow; 1 = force mono
6	SDSOFF	stereo decoder blend function: 0 = on; 1 = off
5	DOFF	stereo decoder: 0 = on; 1 = standby
4	-	
3	-	
2	-	
1	-	
0 (LSB)	-	

Table 16. FM write mode - data byte 6

*Bits marked with * are common for FM and AM mode.*

Bit	Symbol	Description
7 (MSB)	SEARCH*	search mode: 0 = disabled; 1 = enabled
6	PROGBLIM*	copy word: 0 = no copy; 1 = copy PLL word to BLIM register
5	UPDWN*	if bit PROGBLIM = 0: 0 = down search; 1 = up search if bit PROGBLIM = 1: 0 = lower band-limit; 1 = upper band-limit
4	SLEV1*	search level settings: see Table 17
3	SLEV0*	
2	STEP1	search steps FM: see Table 18
1	STEP0*	
0 (LSB)	-	no function

Table 17. Search level settings

Bits SLEV[1:0]	RF level (FM)	ADC[3:0] level bits
00	5 µV	0010
01	10 µV	0100
10	30 µV	0110
11	60 µV	1001

Table 18. Search steps FM

Programmable steps		FM		
Bits STEP[1:0]	Step size	100 kHz reference	66 kHz reference	20 kHz reference
00	1	50	33.333	10
01	2	100	66.666	20
10	3	150	100	30
11	4	200	133.333	40

9.5.1.2 AM write mode

Table 19. Survey of bit names in AM write mode

*Bits marked with * are common for FM and AM mode.*

Bits	7	6	5	4	3	2	1	0
Byte 1	MUTE*	AM/FM*	STB*	PLL10	PLL9	PLL8	PLL7	PLL6
Byte 2	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0	AGCRF	AGCIF
Byte 3	MWLW	LNA	IFCE*	IFW*	HILO*	DBUS*	PEAK	INTEXT*
Byte 4	P1*	P0*	PEN1*	PEN0*	-	CHP0*	DEEM*	RFB
Byte 5	CALLIGN	C6	C5	C4	C3	C2	C1	C0
Byte 6	SEARCH*	PROGBLIM*	UPDWN*	SLEV1*	SLEV0*	AMDELAY	STEP0*	-

Table 20. AM write mode - data byte 1

*Bits marked with * are common for FM and AM mode.*

Bit	Symbol	Description
7 (MSB)	MUTE*	audio mute: 0 = audio not muted; 1 = audio muted
6	AM/FM*	AM/FM selection: 0 = FM; 1 = AM
5	STBY*	operating mode: 0 = operating; 1 = standby
4	PLL10	setting of synthesizer programmable counter
3	PLL9	
2	PLL8	
1	PLL7	
0 (LSB)	PLL6	

Table 21. AM write mode - data byte 2

*Bits marked with * are common for FM and AM mode.*

Bit	Symbol	Description
7 (MSB)	PLL5	setting of synthesizer programmable counter
6	PLL4	
5	PLL3	
4	PLL2	
3	PLL1	
2	PLL0	
1	AGCRF	RF AGC response: 0 = slow; 1 = fast
0 (LSB)	AGCIF	IF AGC response: 0 = slow; 1 = fast

Table 22. AM write mode - data byte 3

*Bits marked with * are common for FM and AM mode.*

Bit	Symbol	Description
7 (MSB)	MWLW	band select: 1 = MW; 0 = LW
6	LNA	LNA gain: 0 = 5 ×; 1 = 10 ×
5	IFCE*	IF counter: 0 = not enabled; 1 = enabled
4	IFW*	IF window: 0 = 2 kHz; 1 = 4 kHz
3	HILO*	VCO injection mode: 0 = low-side; 1 = high-side
2	DBUS*	Dbus mode selection: 0 = off; 1 = on
1	PEAK	RFAGC speed-up: 0 = off; 1 = fast attack, normal decay
0 (LSB)	INTEXT*	reference frequency source select: 0 = external; 1 = internal

Table 23. AM write mode - data byte 4

*Bits marked with * are common for FM and AM mode.*

Bit	Symbol	Description
7 (MSB)	P1*	I/O port control: see Table 28 and Table 29
6	P0*	
5	PEN1*	
4	PEN0*	
3	-	no function

Table 23. AM write mode - data byte 4 *...continued*

*Bits marked with * are common for FM and AM mode.*

Bit	Symbol	Description
2	CHP0*	charge pump current: 0 = large; 1 = small
1	DEEM*	de-emphasis: 0 = 50 μs; 1 = 75 μs
0 (LSB)	RFB	LNA feedback resistor: 0 = 1 MΩ; 1 = 2.2 MΩ

Table 24. AM write mode - data byte 5

*Bits marked with * are common for FM and AM mode.*

Bit	Symbol	Description
7 (MSB)	CALLIGN	selection bit: 0 = C[6:0] sets C-bank; 1 = C[6:0] sets C-align
6	C6	C[6:0] sets C-bank or C-align word depending upon bit CALLIGN:
5	C5	C-align: C[6:0] should be between 0 and 128 (decimal)
4	C4	C-bank: C[6:0] should be between 0 and 122 (decimal)
3	C3	
2	C2	
1	C1	
0 (LSB)	C0	

Table 25. AM write mode - data byte 6

*Bits marked with * are common for FM and AM mode.*

Bit	Symbol	Description
7 (MSB)	SEARCH*	search mode: 0 = disabled; 1 = enabled
6	PROGBLIM*	copy word: 0 = no copy; 1 = copy PLL word to BLIM register
5	UPDWN*	if bit PROGBLIM = 0: 0 = down search; 1 = up search if bit PROGBLIM = 1: 0 = lower band limit; 1 = upper band limit
4	SLEV1*	search level settings: see Table 26
3	SLEV0*	
2	AMDELAY	IF counter delay; 0 = 40 ms; 1 = 80 ms
1	STEP0*	search steps AM: see Table 27
0 (LSB)	-	no function

Table 26. Search level settings

Bits SLEV[1:0]	RF level (AM)[1]	ADC[3:0] level bits
00	0.9 mV/m	0010
01	1.2 mV/m	0100
10	1.9 mV/m	0110
11	3.8 mV/m	1001

[1] Measured with ferroceptor C8E-A0424 TOKO Inc.

Table 27. Search steps AM

Programmable steps			AM f_{ref} = 8 kHz			
Bit STEP0	Step size		PLL step		C-bank step	
	MW	LW	MW	LW	MW	LW
0	9	36	9 kHz	9 kHz	9 kHz mode	9 kHz mode
1	10	40	10 kHz	10 kHz	10 kHz mode	10 kHz mode

Table 28. I/O port control SWPORT1

Bit PEN0	Bit P0	PORT P0 (pin SWPORT1)
0	X[1]	input
1	0	output logic 0
	1	output logic 1

[1] X = don't care.

Table 29. I/O port control SWPORT2

Bit INTEXT	Bit PEN1	Bit P1	PORT P1 (SWPORT2)
1	0	X [1]	input (internal reference)
1	1	0	output logic 0 (internal reference)
		1	output logic 1 (internal reference)
0	X[1]	1	reference input (13 MHz)

[1] X = don't care.

9.5.2 Register definition in read mode

Table 30. Survey of bit names in FM read mode

*Bits marked with * are common for FM and AM mode.*

Bits	7	6	5	4	3	2	1	0
Byte 1	IFCRDY*	IFCE*	MOST	LEV3*	LEV2*	LEV1*	LEV0*	SFOUND*
Byte 2	BLIM*	P1*	P0*	PLL12	PLL11	PLL10	PLL9	PLL8
Byte 3	PLL7	PLL6	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0

9.5.2.1 FM read mode

Table 31. FM read mode - data byte 1

*Bits marked with * are common for FM and AM mode.*

Bit	Symbol	Description
7 (MSB)	IFCRDY*	IF counter ready
6	IFCE*	IF counter enable
5	MOST	mono or stereo setting
4	LEV3*	search level setting
3	LEV2*	
2	LEV1*	
1	LEV0*	
0 (LSB)	SFOUND*	station found

Table 32. FM read mode - data byte 2

*Bits marked with * are common for FM and AM mode.*

Bit	Symbol	Description
7 (MSB)	BLIM*	band limit reached
6	P1*	port 1 setting
5	P0*	port 0 setting
4	PLL12	setting of synthesizer
3	PLL11	
2	PLL10	
1	PLL9	
0 (LSB)	PLL8	

Table 33. FM read mode - data byte 3

*Bits marked with * are common for FM and AM mode.*

Bit	Symbol	Description
7 (MSB)	PLL7	setting of synthesizer
6	PLL6	
5	PLL5	
4	PLL4	
3	PLL3	
2	PLL2	
1	PLL1	
0 (LSB)	PLL0	

9.5.2.2 AM read mode

Table 34. Survey of bit names in AM read mode

*Bits marked with * are common for FM and AM mode.*

Bits	7	6	5	4	3	2	1	0
Byte 1	IFCRDY*	IFCE*	-	LEV3*	LEV2*	LEV1*	LEV0*	SFOUND*
Byte 2	BLIM*	P1*	P0*	PLL10	PLL9	PLL8	PLL7	PLL6
Byte 3	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0	-	-

Table 35. AM read mode - data byte 1

*Bits marked with * are common for FM and AM mode.*

Bit	Symbol	Description
7 (MSB)	IFCRDY*	IF counter ready
6	IFCE*	IF counter enable
5	-	no function
4	LEV3*	search level setting
3	LEV2*	
2	LEV1*	
1	LEV0*	
0 (LSB)	SFOUND*	station found

Table 36. AM read mode - data byte 2

*Bits marked with * are common for FM and AM mode.*

Bit	Symbol	Description
7 (MSB)	BLIM*	band limit reached
6	P1*	port 1 setting
5	P0*	port 0 setting
4	PLL10	setting of synthesizer
3	PLL9	
2	PLL8	
1	PLL7	
0 (LSB)	PLL6	

Table 37. AM read mode - data byte 3

*Bits marked with * are common for FM and AM mode.*

Bit	Symbol	Description
7 (MSB)	PLL5	setting of synthesizer
6	PLL4	
5	PLL3	
4	PLL2	
3	PLL1	
2	PLL0	
1	-	no function
0 (LSB)	-	no function

10. Limiting values

Table 38. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CCA}	analog supply voltage			–0.3	+8	V
V_{CCD}	digital supply voltage			–0.3	+5	V
V_x	voltage on pin x					
	VCOTANK1 and VCOTANK2			–0.3	+8	V
T_{stg}	storage temperature			–55	+150	°C
T_{amb}	ambient temperature			–10	+65	°C
V_{esd}	electrostatic discharge voltage					
	on pins SWPORT1 and SWPORT2	MM	[1] -		±100	V
		HBM	[2] -		±1000	V
	on pin AMRFIN	MM	[1] -		±200	V
		HBM	[2] -		±1500	V
	on all other pins	MM	[1] -		±200	V
		HBM	[2] -		±2000	V

[1] Machine model: R = 10 Ω, L = 0.75 μH, C = 200 pF.

[2] Human body model: R = 1.5 kΩ, C = 100 pF.

11. Thermal characteristics

Table 39. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
	HVQFN48 package		29	K/W
	LQFP32 package		80	K/W

12. Characteristics

Table 40. Static characteristics

V_{CCA} = V_{CCD} = 3 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{CCA}	analog supply voltage			2.7	3.0	7.0	V
V_{CCD}	digital supply voltage			2.7	3.0	5.0	V
I_{CCA}	analog supply current	FM mode		10	13.9	17	mA
		AM mode		8	9.8	11	mA
		Standby mode via bus control		-	0.03	0.15	mA
I_{CCD}	digital supply current	FM mode		0.5	0.8	1.5	mA
		AM mode		0.5	0.8	1.5	mA
		Standby mode via bus control		-	0.13	0.25	mA
DC operating voltages							
V_O	output voltage	unloaded					
	on pin CPOUT	tuning voltage range		0.2	-	V_{CCA} – 0.3	V
	on pins XTAL1 and XTAL2			-	1.6	-	V
	on pin TMUTE	FM	[1]	0.2	-	0.8	V
		AM		0.1	-	1.2	V
	on pin VREF			-	1.25	-	V
	on pin AGC2CAP	FM		-	-	-	V
		AM		-	1.25	-	V
	on pin V25DIG			-	2.5	-	V
	on pins VAFL and VAFR	FM		0.675	0.750	0.825	V
		AM		0.55	0.65	0.75	V
	on pin MPXOUT	FM		1	1.25	1.5	V
		AM		-	0	-	V
	on pin V25IF			-	2.5	-	V
	on pin PILDET/AMRFAGC	FM		-	0.75	-	V
		AM		0	-	2.5	V
	on pin VAMLNA	FM		-	-	-	V
		AM		-	2.3	-	V
V_I	input voltage	unloaded					
	on pin MPXIN	FM		0.7	0.75	0.8	V
		AM		-	0	-	V
	on pins RFIN1 and RFIN2	FM		0	1.75	-	V
		AM		-	0	-	V

[1] These minimum and maximum values are typical values.

Table 41. Digital input and output characteristics

V_{CCA} = V_{CCD} = 3 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Software programmable ports: pins SWPORT1 and SWPORT2						
V_{OH}	HIGH-level output voltage	I_O = 0 A	-	2.4	-	V
V_{OL}	LOW-level output voltage	I_O = 1 mA				
		on pin SWPORT1	-	109.7	-	mV
		on pin SWPORT2	-	105.5	-	mV
$I_{o(source)}$	output source current	V_O = 0 V	–6	–9	–14	mA
$I_{o(sink)}$	output sink current	V_O = 3 V	6	9	14	mA
		V_O = 0.8 V; R_{pu} = 1 kΩ				
		on pin SWPORT1	-	7.85	-	mA
		on pin SWPORT2	-	8.04	-	mA
Digital inputs						
V_{IH}	HIGH-level input voltage		0.45V_{CCD}	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.2V_{CCD}	V
Digital outputs: pins CLOCK, DATA and WRITE_READ						
V_{OL}	LOW-level output voltage	I_{OL} = 500 µA; open-collector	-	-	450	mV
I_{OL}	LOW-level output current	open-collector	500	-	-	µA

Table 42. Bus timing characteristics

V_{CCA} = V_{CCD} = 3 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Timing I^2C-bus						
f_{SCL}	SCL clock frequency		-	-	400	kHz
t_{HIGH}	HIGH period of the SCL clock		1	-	-	µs
t_{LOW}	LOW period of the SCL clock		1	-	-	µs
Timing 3-wire bus; see Figure 7 and Figure 8						
$f_{i(clk)}$	clock input frequency		-	-	1	MHz
$t_{clk(H)}$	clock HIGH time		300	-	-	ns
$t_{clk(L)}$	clock LOW time		300	-	-	ns
Write mode						
$t_{w(W)}$	write enable pulse width		1	-	-	µs
$t_{su(clk)}$	clock setup time		300	-	-	ns
$t_{su(D)}$	data input set-up time	in write mode	100	-	-	ns
$t_{h(D)}$	data input hold time	in write mode	100	-	-	ns
Read mode						
$t_{w(R)}$	read enable pulse width		1	-	-	µs
$t_{su(clk)}$	clock setup time		300	-	-	ns
$t_{h(Q)}$	data output hold time	in read mode	10	-	-	ns
$t_{d(Q)}$	data output delay time	in read mode	-	-	100	ns

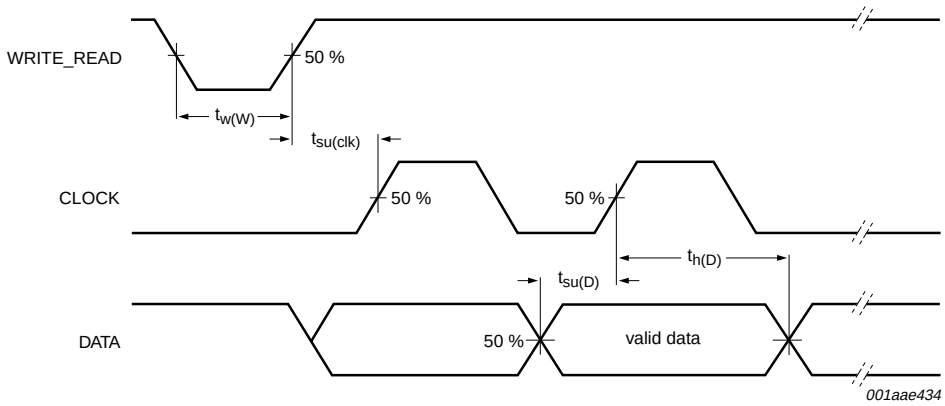


Fig 7. 3-wire bus write data

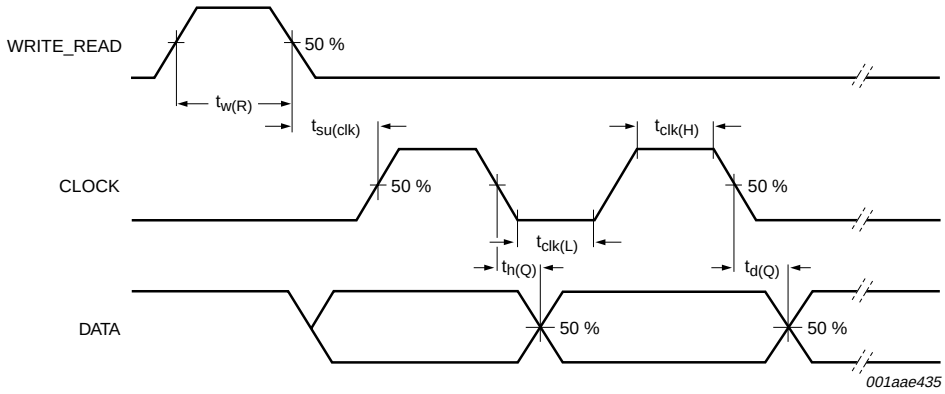


Fig 8. 3-wire bus read data

Table 43. Dynamic characteristics

V_{CCA} = V_{CCD} = 3 V; T_{amb} = 25 °C; all values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FM voltage controlled oscillator: pins VCOTANK1 and VCOTANK2						
f_{osc}	oscillator frequency	V_{CPOUT} = 0.2 V to (V_{CCA} – 0.3 V)	130	-	217	MHz
V_o	output voltage	measured between pins VCOTANK1 and VCOTANK2; f_{osc} = 200 MHz; Q = 40; L = 33 nH	-	500	-	mV
$I_{CCA(VCO)}$	VCO analog supply current		0.5	1	3	mA
Crystal oscillator: pins XTAL1 and XTAL2						
f_{xtal}	crystal frequency	internal reference source selected	-	4	-	MHz
Δf_{xtal}	crystal frequency accuracy	f_{xtal} = 4 MHz	-	20	50	ppm
$V_{o(xtal)(p-p)}$	peak-to-peak crystal oscillator output voltage	measured between pins XTAL1 and XTAL2	-	280	-	mV
$V_{O(bias)}$	bias output voltage		-	1.6	-	V
R_i	input resistance	measured between pins XTAL1 and XTAL2	150	-	-	Ω

Table 43. Dynamic characteristics *...continued*

V_{CCA} = V_{CCD} = 3 V; T_{amb} = 25 °C; all values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_i	input capacitance	measured between pins XTAL1 and XTAL2		-	16	-	pF
External reference frequency input: pin SWPORT2/EXTIN							
f_i	input frequency	FM		-	13	-	MHz
		AM		-	13	-	MHz
V_i	input voltage	external applied	[1]	150	-	1800	mV
V_I	input voltage	no external input signal applied		-	0.9	-	V
Z_i	input impedance	at indicated input frequency		-	100	-	kΩ
Synthesizer							
t_{srch}	search time	synthesizer search time for empty band					
		FM band from 87.5 MHz to 108 MHz; step = 100 kHz		-	2.3	-	s
		AM band from 522 kHz to 1620 kHz; AM delay = 40 ms		-	10	-	s
t_{acq}	acquisition time	synthesizer preset acquisition time between two band limits					
		FM		-	10	-	ms
		AM: MW		-	10	-	ms
		AM: LW		-	10	-	ms
f_{RF}	RF frequency	FM	[2]				
		f_{step} = 10 kHz; f_{IF} = 150 kHz		10.24	-	81.91	MHz
		f_{step} = 33.333 kHz; f_{IF} = 133.333 kHz		34.13	-	273.03	MHz
		f_{step} = 50 kHz; f_{IF} = 150 kHz		51.2	-	409.55	MHz
		AM; f_{step} = 1 kHz; f_{IF} = 21 kHz	[2]				
		LW		128	-	511.75	kHz
		MW		512	-	2047	kHz
Synthesizer programmable divider							
D/D_{prog}	programmable divider ratio	FM		1024		8191	
		AM		512		2047	
$D_{prog(step)}$	programmable divider step			-	1	-	
$N_{VCO(AM)}$	AM VCO divider	AM MW		-	8	-	
		AM LW		-	32	-	
Synthesizer reference divider							
$D/D_{ref(xtal)}$	crystal reference divider ratio	internal reference frequency; f_{xtal} = 4 MHz					
		FM					
		$f_{ref(RF)}$ = 10 kHz; f_{IF} = 150 kHz		-	200	-	
		$f_{ref(RF)}$ = 33.333 kHz; f_{IF} = 133.333 kHz		-	60	-	
		$f_{ref(RF)}$ = 50 kHz; f_{IF} = 150 kHz		-	40	-	
		AM					
		$f_{ref(RF)}$ = 1 kHz; f_{IF} = 21 kHz		-	500	-	

Table 43. Dynamic characteristics *...continued*

V_{CCA} = V_{CCD} = 3 V; T_{amb} = 25 °C; all values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$D/D_{ref(ext)}$	external reference divider ratio	external reference frequency; f_i = 13 MHz				
		FM				
		$f_{ref(RF)}$ = 10 kHz	-	650	-	
		$f_{ref(RF)}$ = 33.333 kHz	-	195	-	
		$f_{ref(RF)}$ = 50 kHz	-	130	-	
		AM				
		$f_{ref(RF)}$ = 1 kHz	-	1625	-	
Charge pump: pin CPOUT						
$I_{o(sink)}$	output sink current	high current range	300	350	410	µA
		low current range	200	250	300	µA
$I_{o(source)(M)}$	peak source output current	high current range	–200	–250	–300	µA
		low current range	–140	–170	–200	µA
IF counter						
N_{IFc}	IF counter length		-	13	-	bit
$N_{IFc(result)}$	IF counter result	in-window or out-window	-	1	-	bit
V_{sens}	sensitivity voltage	FM	-	5	-	µV
		AM	-	-	-	µV
$f_{IF(window)}$	IF window width frequency	FM				
		bit IFW = 0	–10		+10	kHz
		bit IFW = 1	–20		+20	kHz
		AM				
		bit IFW = 0	–2		+2	kHz
		bit IFW = 1	–4		+4	kHz
t_{IFc}	IF counter time	period measuring time				
		FM	-	20	-	ms
		AM	-	5	-	ms
$t_{d(IFc)}$	IF counter delay time	FM	-	5	-	ms
		AM				
		bit AMDELAY = 0	-	40	-	ms
		bit AMDELAY = 1	-	80	-	ms

[1] Works with digital input signal from 0 V to 1.4 V.

[2] Programmable frequency range of the synthesizer referred to the antenna input.

Table 44. FM performance

V_{CCA} = V_{CCD} = 3 V; T_{amb} = 25 °C; f_{RF} = 100 MHz; f_{mod} = 1 kHz; Δf = 22.5 kHz; τ_{deemp} = 50 µs; all AC values are given in RMS; see test circuit of Figure 9; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Inputs							
Input: pins RFIN1 and RFIN2							
R_i	input resistance	measured between pins RFIN1 and RFIN2		-	300	-	Ω
C_i	input capacitance			-	4	-	pF
FM dummy							
V_i	input voltage	$V_i = V_{i2}$ = sensitivity at dummy input; (S+N)/N = 26 dB; L = R; $B_{aud(-3dB)}$ = 300 Hz to 15 kHz A-weighted; f_{IF} = 133.333 kHz	[1]	-	2.7	3.5	µV
		large signal voltage handling capacity; THD < 10 %		-	1000	-	mV
FM channel							
$\Delta f_{AF(M)}$	peak AF frequency deviation	V_{i2} = 1 mV; f_{mod} = 1 kHz, L = R; f_{IF} = 133.333 kHz					
		THD < 1 %		75	102.7	-	kHz
		THD < 1.5 %		75	110.1	-	kHz
$IP3_{ib}$	in-band third-order intercept point	Δf_1 = 200 kHz; Δf_2 = 400 kHz; f_{RF} = 98 MHz	[2]	-	97	-	dBµV
$IP3_{ob}$	out-band third-order intercept point	Δf_1 = 5 MHz; Δf_2 = 10 MHz; f_{RF} = 88 MHz or 103 MHz	[2]	-	96	-	dBµV
S_{+300}	high-side 300 kHz selectivity			40	-	-	dB
S_{-300}	low-side 300 kHz selectivity			35	-	-	dB
α_{image}	image rejection	f_{RF} = 87.5 MHz to 108 MHz		25	41	-	dB
$B_{aud(-3dB)}$	–3 dB audio bandwidth	V_{i2} = 1 mV; $\Delta f_{FM(max)}$ = 22.5 kHz					
		low-end	[3]	-	-	50	Hz
		high-end		12 500	-	-	Hz
PSRR	power supply rejection ratio	ΔV_{CCA} = 147 mV (RMS); f_{ripple} = 1 kHz		-	42	-	dB
α_{AM}	AM suppression	100 µV < V_{i2} < 10 mV; m = 0.3; f_{mod} = 1 kHz		-	50	-	dB
I and Q channel IF filter							
f_{IF}	IF frequency	f_{step} = 33.333 kHz		-	133.333	-	kHz
		f_{step} = 10 kHz or 50 kHz		-	150	-	kHz
$\Delta f_{c(IF)}$	IF center frequency deviation	all combinations		-	-	5.5	kHz
B_{IF}	IF filter bandwidth	f_{IF} = 133.333 kHz		108	110	112	kHz
		f_{IF} = 150 kHz		123	125	127	kHz
Outputs							
MPX output: pin MPXOUT							
V_o	output voltage	V_{i2} = 1 mV					
		f_{IF} = 133.333 kHz		75	104	125	mV
		f_{IF} = 150 kHz		60	82	100	mV
$I_{o(AC)M}$	peak AC output current			-	100	-	µA

Table 44. FM performance *...continued*

V_{CCA} = V_{CCD} = 3 V; T_{amb} = 25 °C; f_{RF} = 100 MHz; f_{mod} = 1 kHz; Δf = 22.5 kHz; τ_{deemp} = 50 µs; all AC values are given in RMS; see test circuit of Figure 9; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_O	output voltage	properly tuned	1	1.25	1.5	V
THD	total harmonic distortion	V_{i2} = 1 mV; Δf = 75 kHz; with external τ_{deemp} = 50 µs; $B_{aud(-3dB)}$ limited to 15 kHz	-	0.55	1.5	%
S/N	signal-to-noise ratio	V_{i2} = 1 mV; L = R; $B_{aud(-3dB)}$ = 300 Hz to 15 kHz A-weighted; f_{IF} = 133.333 kHz	-	60	-	dB
Z_o	output impedance		300	420	550	Ω
C_L	load capacitance		-	-	40	pF
R_L	load resistance		33	-	-	kΩ
AF output: pins VAFL and VAFR						
$V_{o(AF)}$	AF output voltage	V_{i2} = 1 mV, $\Delta f_{FM(max)}$ = 22.5 kHz				
		f_{IF} = 133.333 kHz	70	95	120	mV
		f_{IF} = 150 kHz	55	75	95	mV
FM IF level detector						
Input FM dummy						
V_i	input voltage	V_i = V_{i2} = detector level voltage				
		start ADC	-	5	-	µV
		step size of ADC	-	4.7	-	dB
Level output: pin TMUTE						
V_O	output voltage	V_{i2} = 0 V	-	0.2	-	V
		V_{i2} = 5 mV	-	0.8	-	V
$V_{o(slope)}$	output voltage slope	10 mV < V_{i2} < 1 mV	-	214	-	mV/ 20dB
R_o	output resistance		200	250	350	kΩ

[1] The sensitivity at the dummy input is equivalent to EMF in a 75 Ω system.

[2] Related to LNA input.

[3] With a pre-emphasis of 50 µs.

Table 45. AM performance

V_{CCA} = V_{CCD} = 3 V; T_{amb} = 25 °C; f_{RF} = 918 kHz; f_{mod} = 1 kHz; m = 0.3; τ_{deemp} = 75 µs; V_{i1} measured at input of matching network; all AC values are given in RMS; see test circuit of Figure 9; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Inputs							
AM RF input: pin AMRFIN							
V_I	input voltage			-	0	-	V
I_I	input current	$V_{PILDET/AMRFAGC}$ = 0 V		-	0	-	µA
V_i	input voltage	RF sensitivity at dummy input; $V_i = V_{i1}$; (S+N)/N = 26 dB; A-weighting filter		-	155	-	µV
		large signal voltage handling capability; THD < 10 %		-	300	-	mV
E	electric field strength	RF sensitivity with ferroceptor; (S+N)/N = 26 dB; A-weighting filter	[1]	-	2.9	-	mV/m
AM channel							
Overall data							
$B_{aud(-3dB)}$	–3 dB audio bandwidth	V_{i1} = 5 mV					
		low-end		-	-	50	Hz
		high-end		1.5	2.1	-	kHz
S/N	signal-to-noise ratio	V_{i1} = 5 mV; A-weighting filter		40	48	-	dB
THD	total harmonic distortion	V_{i1} = 5 mV; m = 0.8; bit AGCRF = 0 (slow); bit AGCIF = 0 (slow); $B_{aud(-3dB)}$ limited to 15 kHz		-	1	2.5	%
PSRR	power supply rejection ratio	ΔV_{CCA} = 147 mV (RMS); f_{ripple} = 1 kHz		-	34	-	dB
S_{+9}	high-side 9 kHz selectivity	measured at dummy input V_{i1}		25	32	-	dB
S_{-9}	low-side 9 kHz selectivity	measured at dummy input V_{i1}		25	30	-	dB
S_{+27}	high-side 27 kHz selectivity	measured at dummy input V_{i1}		45	58	-	dB
S_{-27}	low-side 27 kHz selectivity	measured at dummy input V_{i1}		45	58	-	dB
S_{+100}	high-side 100 kHz selectivity	measured at dummy input V_{i1}		45	59	-	dB
S_{-100}	low-side 100 kHz selectivity	measured at dummy input V_{i1}		45	59	-	dB
α_{image}	image rejection	520 kHz ≤ f_{RF} ≤ 1720 kHz	[2]	40	-	-	dB
Capacitance bank							
C_i	input capacitance	bit CALLIGN = 0					
		minimum C[6:0] = 000 0000		-	20.5	-	pF
		maximum C[6:0] = 111 1010		390	453	544	pF
$N_{step(bank)}$	number of bank steps			-	122	-	
C_{align}	alignment capacitance	bit CALLIGN = 1					
		C[6:0] = 000 0000		-	0	-	pF
		C[6:0] = 111 1111		-	17	-	pF
$C_{align(step)}$	alignment capacitance step			-	0.134	-	pF
$N_{step(align)}$	number of alignment steps			-	128	-	

Table 45. AM performance *...continued*

V_{CCA} = V_{CCD} = 3 V; T_{amb} = 25 °C; f_{RF} = 918 kHz; f_{mod} = 1 kHz; m = 0.3; τ_{deemp} = 75 µs; V_{i1} measured at input of matching network; all AC values are given in RMS; see test circuit of Figure 9; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LNA						
G_{LNA}	LNA gain	bit LNA = 0 (5 ×)	-	14	-	dB
		bit LNA = 1 (10 ×)	-	20	-	dB
$\alpha_{AGC(RF)}$	RF AGC attenuation	$V_{PILDET/AMRFAGC}$ = 0 V	-	0	-	dB
		$V_{PILDET/AMRFAGC}$ = 2 V	-	25	-	dB
R_i	input resistance	bit LNA = 0 (5 ×)				
		RFB = 0 (low feed-back)	-	166	-	kΩ
		RFB = 1 (high feed-back)	-	366	-	kΩ
		bit LNA = 1 (10 ×)				
		RFB = 0 (low feed-back)	-	91	-	kΩ
		RFB = 1 (high feed-back)	-	200	-	kΩ
I and Q channel IF filter						
f_{IF}	IF frequency		-	21	-	kHz
Δf_{IF}	IF frequency deviation		-	-	0.2	kHz
B_{IF}	IF filter bandwidth		-	8	-	kHz
Outputs						
AF output: pins VAFL and VAFR						
$V_{o(AF)}$	AF output voltage	V_{i1} = 5 mV	72	90	108	mV
V_O	output voltage	properly tuned	0.55	0.65	0.75	V
Z_o	output impedance		300	500	800	Ω
AM IF level detector						
Input AM dummy						
V_i	input voltage	V_i = V_{i2} = detector level voltage; LNA = 1 and RFB = 0				
		start ADC	-	50	-	µV
		end ADC	-	2	-	mV
Level output: pin TMUTE						
V_O	output voltage	V_{i1} = 0 V	0.1	0.15	0.3	V
		V_{i1} = 10 mV	0.8	1	1.2	V
$V_{o(slope)}$	output voltage slope	100 µV< V_{i1} < 1 mV	-	375	-	mV/ 20dB
Z_o	output impedance		260	360	480	kΩ

[1] With ferroceptor C8E-A0424 TOKO Inc.

[2] Without antenna input contribution.

Table 46. Stereo decoder characteristics

V_{CCA} = V_{CCD} = 3 V; T_{amb} = 25 °C; τ_{deemp} = 50 µs; not forced to mono; all AC values are given in RMS; see test circuit of Figure 9; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Input: pin MPXIN							
V_I	input voltage			0.7	0.75	0.8	V
R_i	input resistance			300	400	500	kΩ
MPX stereo decoder channel							
Overall data							
G_v	voltage gain	f_{mod} = 1 kHz	[1]	–1.1	–0.82	–0.4	dB
α_{cs}	channel separation	V_{i3} = 300 mV; f_{mod} = 1 kHz; V_{pilot} = 30 mV; R = 1 and L = 0 or R = 0 and L = 1; V_{TMUTE} = 1 V; f_{IF} = 133.333 kHz; $B_{aud(-3dB)}$ limited to 15 kHz		26	40	-	dB
(S+N)/N	signal plus noise-to-noise ratio	measured at AF output; L = R; V_{i3} = 300 mV; f_{mod} = 1 kHz; V_{pilot} = 30 mV; A-weighted		-	68.5	-	dB
THD	total harmonic distortion	measured at AF output; L = R; V_{MPXOUT} = 300 mV; f_{mod} = 1 kHz; V_{pilot} = 30 mV; $B_{aud(-3dB)}$ limited to 15 kHz		-	0.05	0.5	%
α_{19}	19 kHz suppression	reference 300 mV = 0 dB		23	28	-	dB
α_{38}	38 kHz suppression	reference 300 mV = 0 dB		31	52	-	dB
Pilot detector							
V_{pilot}	pilot voltage	V_{TMUTE} = 1 V					
		switching to stereo		-	13	16	mV
		switching back to mono		3	6	-	mV
		mono hysteresis		6	7	8	mV
Integrated de-emphasis							
τ_{deemp}	de-emphasis time constant	bit DEEM = 0		-	50	-	µs
		bit DEEM = 1		-	75	-	µs
Hard mute							
α_{mute}	mute attenuation	measured on pins VAFL and VAFR; audio muted with bit MUTE = 1; A-weighted		60	70	-	dB
SDS curve (blend function)							
V_i	input voltage	SDS region voltage V_i = V_{i1}; V_{i3} = 300 mV; f_{mod} = 1 kHz; V_{pilot} = 30 mV; R = 1 and L = 0 or R = 0 and L = 1; bit SDSOFF = 0; bit DOFF = 0; bit FOMO = 0					
		start level		-	15	-	µV
		stop level		-	150	-	µV

Table 46. Stereo decoder characteristics *...continued*

V_{CCA} = V_{CCD} = 3 V; T_{amb} = 25 °C; τ_{deemp} = 50 µs; not forced to mono; all AC values are given in RMS; see test circuit of Figure 9; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AF output: pins VAFL and VAFR						
$V_{o(AF)}$	AF output voltage	measured with respect to input pin MPXIN; V_{i3} = 100 mV; L = R; f_{mod} = 1 kHz	83	91	99	mV
$I_{o(sink)M}$	peak sink output current	V_{i3} = 100 mV; L = R; f_{mod} = 1 kHz	-	60	-	µA
V_O	output voltage	measured with respect to input pin MPXIN; FM mode	0.675	0.75	0.825	V
R_o	output resistance		300	500	800	Ω

[1] This includes the attenuation due to the de-emphasis. At 1 kHz this is approximately 0.4 dB for 50 µs.

13. Application information

13.1 AM coil requirements and alignment

The AM receiver is a magnetic field receiver. It can be used with a ferroceptor or an antenna. In both cases, the antenna can be seen as an inductor that should be in resonance with the on-chip C-bank at the frequency of interest. The C-bank values are such that a nominal device and nominal antenna inductor value result in the correct tuning grid depending upon bit STEP0; see Table 16 and Table 27.This puts requirements on the nominal value and tuning range of the AM antenna. Due to spread an alignment is needed.

13.1.1 AM coil requirements

In order to align the antenna C-bank the antenna coil must meet the requirements of Table 47.

Table 47. AM coil requirements

Parameter	Value
Nominal value	203 µH
Tuning range needed for alignment (excluding own tolerance)	± 16 %
Optimal TC1[1]	–50 ppm/K

[1] Optimal means that the LC product (L of AM coil and C of C-bank) has zero TC1, since TC1(C-bank) = +50 ppm/K. Having TC1(L of AM coil) equal to –50 ppm/K is not a hard requirement. However, it is advisable to keep the TC1(LC product) < 350 ppm/K.

13.1.2 AM coil alignment

Alignment is setting the right C-align value and tuning the AM coil. This is done as follows:

1. Set C-align = 0
2. Measure the resonance frequency 1 (f_{rsn1}) with C-bank = 0
3. Measure the resonance frequency 2 (f_{rsn2}) with C-bank = 122
4. Set C-bank = 0:
   - Tune C-align until the resonance frequency 3 becomes f_{rsn3}
   - Tune AM coil until the resonance frequency 4 becomes f_{rsn4}

The f_{rsn3} and f_{rsn4} values can be calculated based upon f_{rsn1} and f_{rsn2}.

This procedure only has to be done once in order to fit the AM coil and device together. The C-align data has to be stored in the microcontroller and should be written every time the device is powered up.

For C-align the internal digital controlled capacitor is used in principle. It is also possible to use an external trim capacitor (0 pF to 17 pF) instead. This has the advantage that no alignment data has to be stored in the microcontroller at the cost of one trim capacitor.

14. Test information

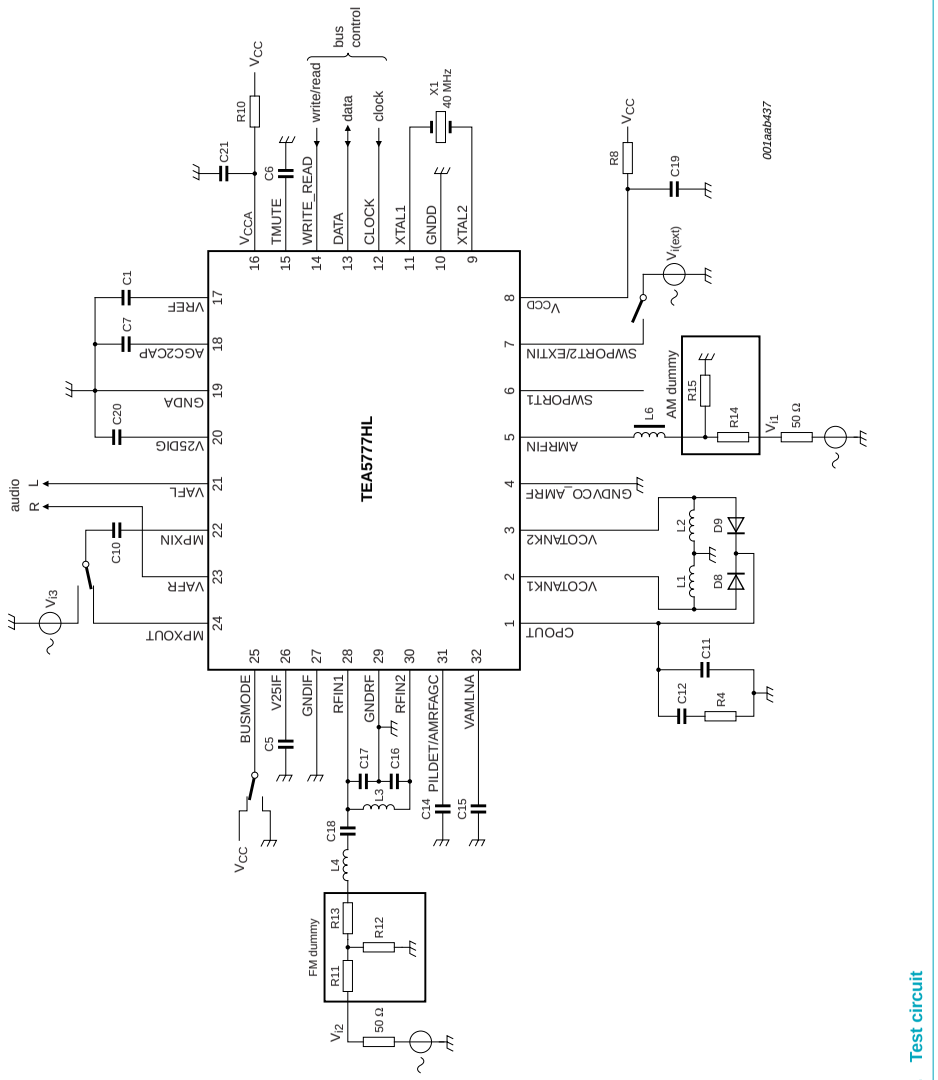


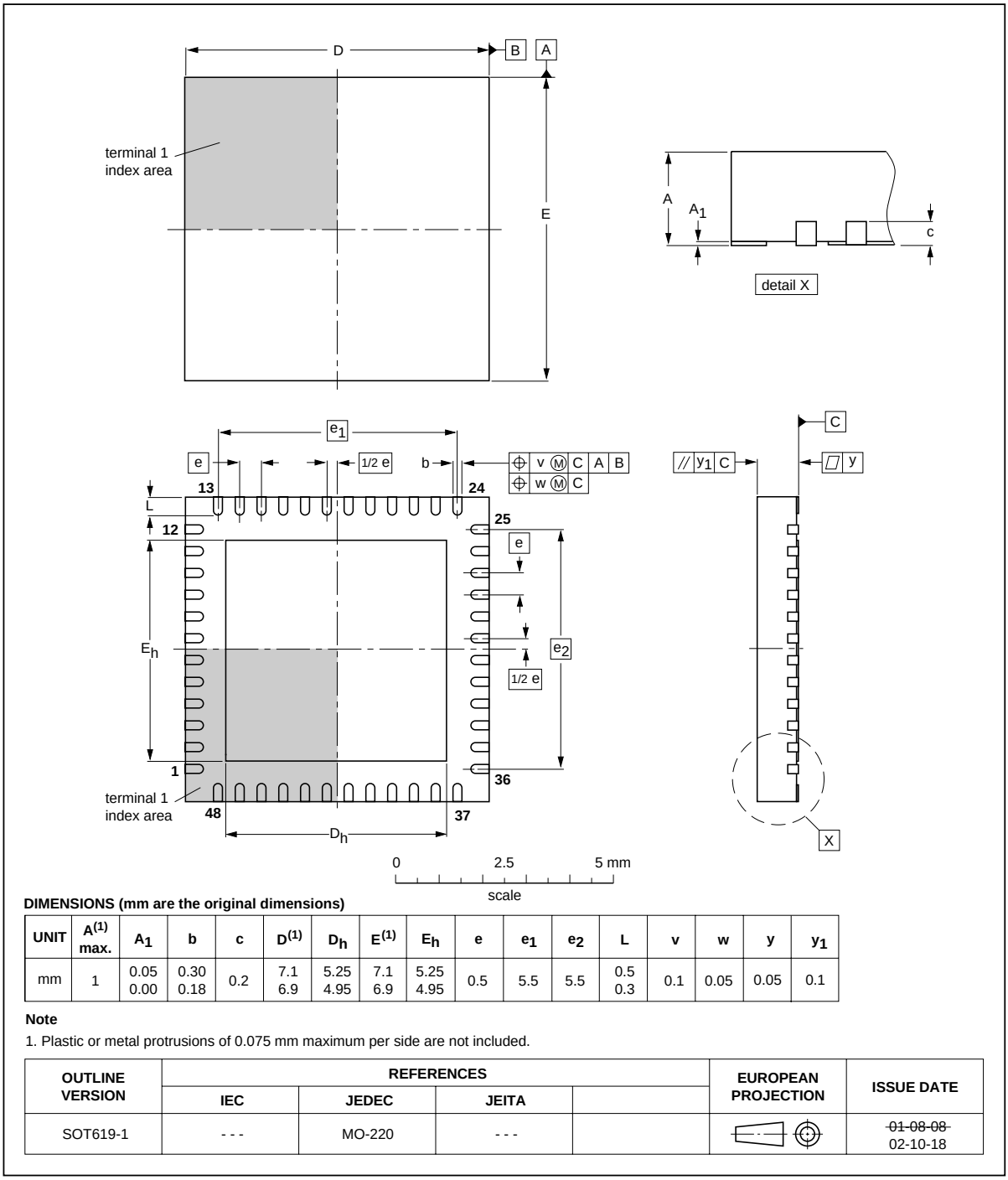
Fig 9. Test circuit

Table 48. Test circuit components

Part number	Specification			Remark
	Value	Tolerance	Type	
C1	100 nF	20 %	C0603	
C5	3.3 µF	20 %	6V3	B45196E1335M10*, EPCOS
C6	100 nF	20 %	C0603	
C7	2.2 µF	20 %	6V3	B45196E1225M10*, EPCOS
C10	220 nF	20 %	C0805	
C11	15 nF	20 %	C0603	
C12	220 nF	20 %	C0805	
C14	1 µF	20 %	C1206	low leakage (< 5 nA), X7R
C15	3.3 µF	20 %	6V3	B45196E1335M10*, EPCOS
C16	33 pF	5 %	C0603	NP0
C17	39 pF	5 %	C0603	NP0
C18	12 pF	5 %	C0603	NP0
C19	2.2 µF	20 %	6V3	B45196E1225M10*, EPCOS
C20	220 nF	20 %	C0603	NP0
C21	1 µF	20 %	16 V	B45196E3105M10*, EPCOS
D8	BB202			
D9	BB202			
L1	33 nH	5 %	Q = 40	TOKO, LLQ1608-A33N_J
L2	33 nH	5 %	Q = 40	TOKO, LLQ1608-A33N_J
L3	120 nH	5 %		TOKO, LLQ1608-AR120N_J
L4	220 nH	5 %		TOKO, LLQ1608-AR220N_J
L6	200 nH		Q > 120	tuning range larger than −16 % to +16 %; Sagami 940927266B (part of the AM dummy)
R4	2.2 kΩ	20 %	R0603	
R8	100 W	20 %	R0603	
R10	47 W	20 %	R0603	
R11	10 W	5 %	R0603	(part of the FM dummy, i.e. 50 Ω to 75 Ω)
R12	60 W	5 %	R0603	(part of the FM dummy, i.e. 50 Ω to 75 Ω)
R13	45 W	5 %	R0603	(part of the FM dummy, i.e. 50 Ω to 75 Ω)
R14	51 W	5 %	R0603	(part of the AM dummy)
R15	1 W	5 %	R0603	(part of the AM dummy)
X1	4 MHz		HC49	NDK

15. Package outline

HVQFN48: plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 x 7 x 0.85 mm **SOT619-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1
mm	1	0.05 0.00	0.30 0.18	0.2	7.1 6.9	5.25 4.95	7.1 6.9	5.25 4.95	0.5	5.5	5.5	0.5 0.3	0.1	0.05	0.05	0.1

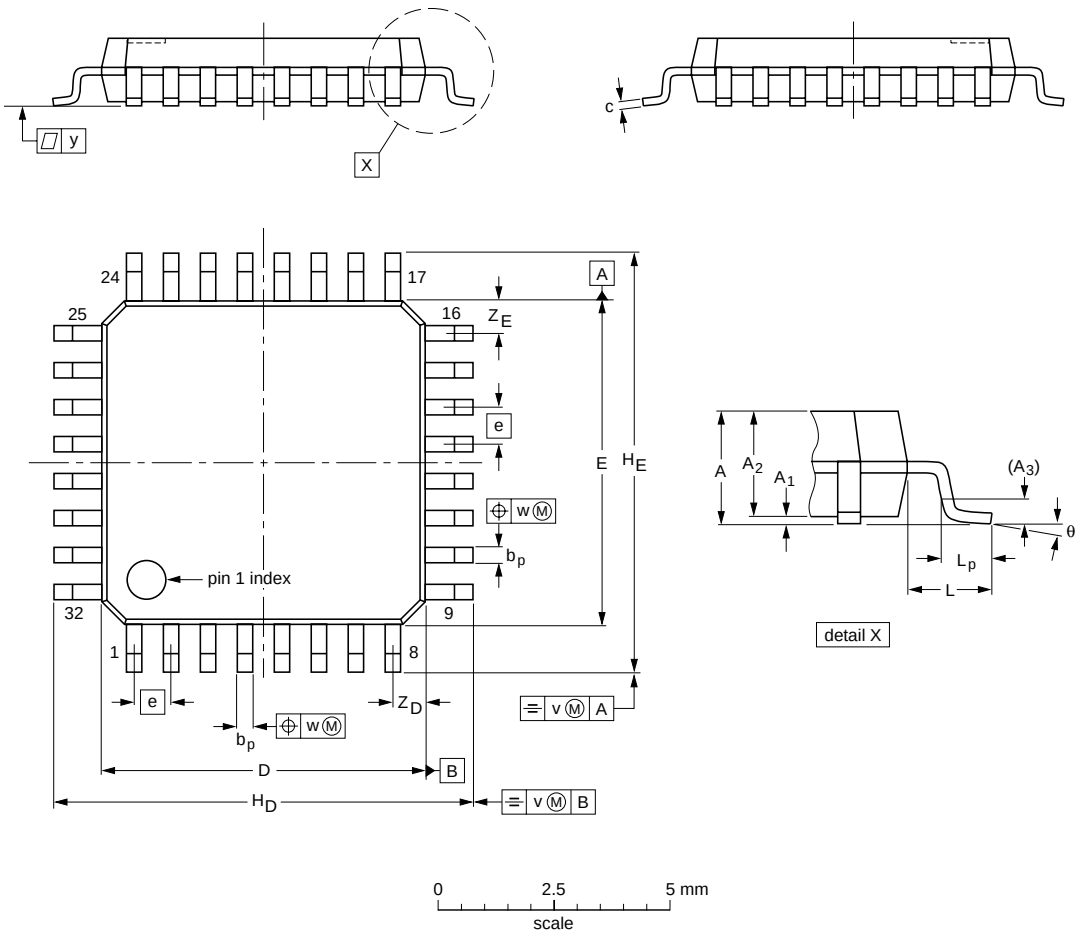
Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT619-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-18

Fig 10. Package outline SOT619-1 (HVQFN48)

LQFP32: plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm **SOT358-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.4 0.3	0.18 0.12	7.1 6.9	7.1 6.9	0.8	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.25	0.1	0.9 0.5	0.9 0.5	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT358 -1	136E03	MS-026				~~03-02-25~~ 05-11-09

Fig 11. Package outline SOT358-1 (LQFP32)

16. Abbreviations

Table 49. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
BiCMOS	Bi-polar Complementary Metal-Oxide Semiconductor
FET	Field-Effect Transistor
GSM	Global System for Mobile communication
HBM	Human Body Model
I/Q	In-phase/Quadrature-phase
LNA	Low Noise Amplifier
LW	Long Wave
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPX	Multiplex
MM	Machine Model
MW	Medium Wave
OIRT	Organisation Internationale de Radiodiffusion et de Télévision (International Radio and Television Organization)
PLL	Phase-Locked Loop
RDS	Radio Data System
RSSI	Receiver Signal Strength Information
SDS	Signal Dependent Stereo
VCO	Voltage Controlled Oscillator

17. Revision history

Table 50. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA5777_1	20060411	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

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20. Contents

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