CE5037

Digital Satellite Tuner with RF Bypass

Data Sheet

January 2007

Features

- Direct conversion tuner for quadrature down conversion from L-band to Zero IF
- Symbol rate 1-45 MS/s
- High sensitivity < -83 dBm at 27.5 MS/s Code rate 7/8
- Independent RF AGC and baseband gain control
- Fifth order baseband filters with bandwidth adjustable from 6 to 43 MHz
- Fully integrated alignment-free low phase noise local oscillator
- Selectable RF Bypass
- Low power consumption 0.5W at 3.3V.
- 28 pin 5x5 mm QFN Package

Applications

- DVB-S PayTV satellite receivers
- DSS satellite receivers
- DVB-S2 8PSK satellite receivers

Ordering Information

WGCE5037 882557	28 Pin QFN* Trays
WGCE5037 S L9FV 882558	28 Pin QFN* Tape & Reel

*Pb Free Matte Tin

-10°C to +85°C

Description

The CE5037 is a fully integrated direct conversion tuner for digital satellite receiver systems. It provides excellent immunity to composite undesired channels. The device also contains a RF Bypass for connecting to a second receiver module.

The CE5037 is simple to use, requiring no alignment or tuning algorithms and uses a minimum number of external components. The device is programmable via a I^2C compatible bus.

The CE5037 is qualified for DVB-S2 8PSK receiver applications

A complete reference design (CE9542) is available using CE6313 demodulator.

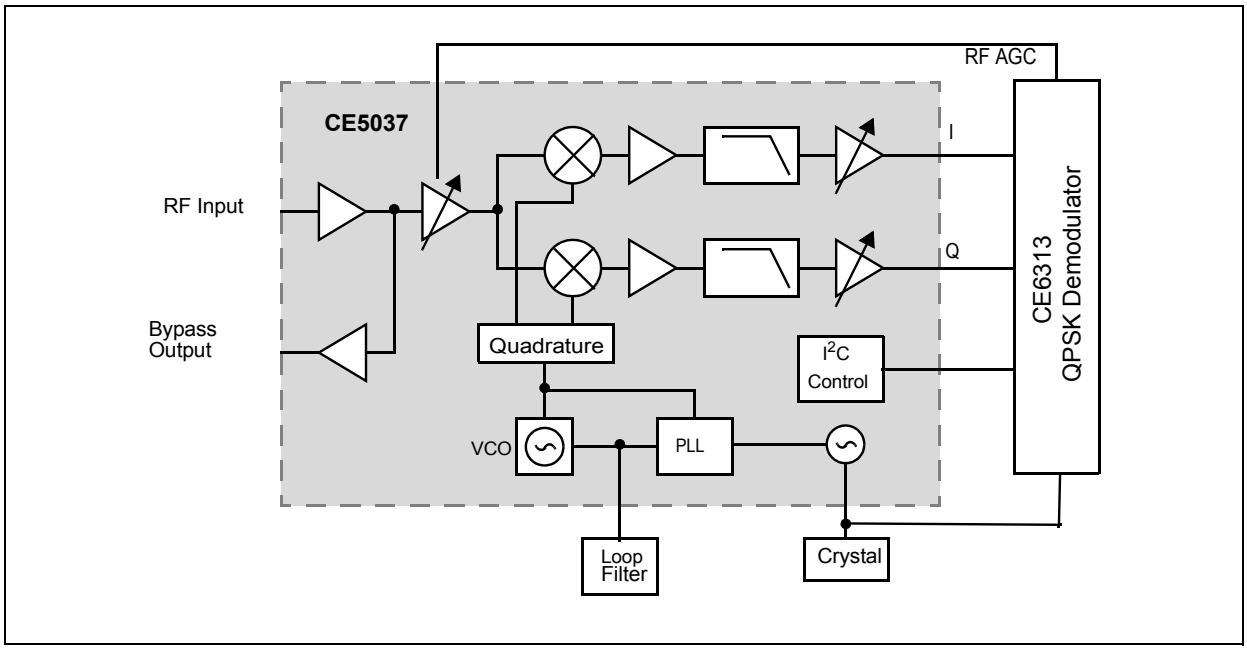

Figure 1 - Basic Block Diagram

Intel Corporation Order Number: D55745-002

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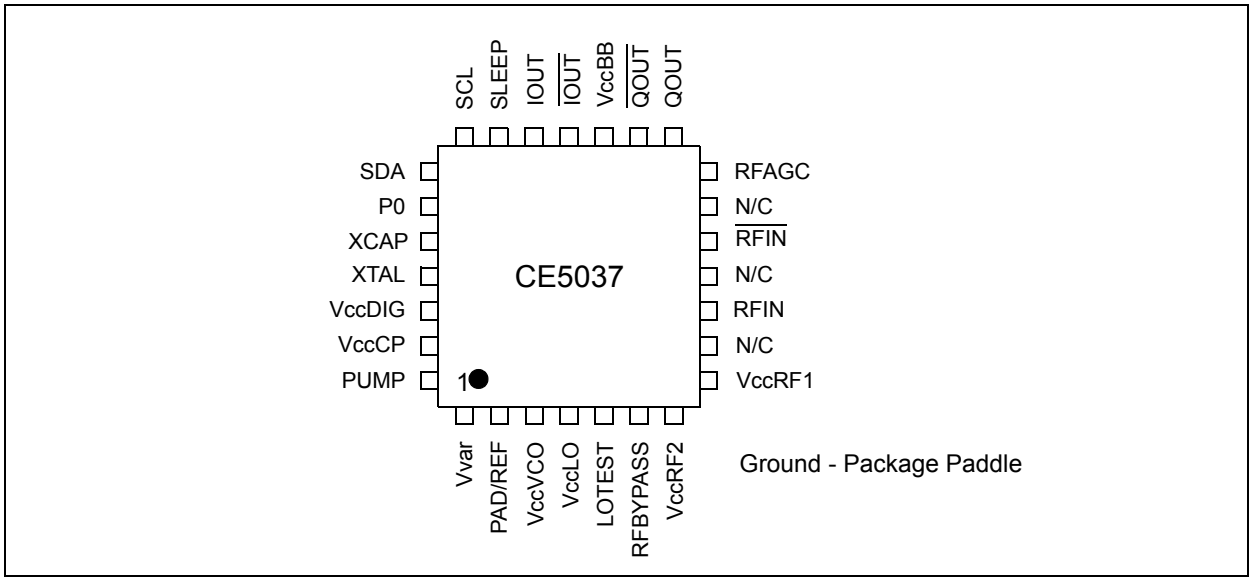


Figure 2 - Pin Diagram

Pin #	Name	Description	Pin #	Name	Description
1	Vvar	LO Tuning Voltage	15	QOUT	Q Channel baseband output
2	PAD/REF	Vvar Reference Ground / Continuity Test	16	$\overline{\text{QOUT}}$	Q Channel baseband output
3	VccVCO	VCO Supply	17	VccBB	Baseband Supply
4	VccLO	LO Supply	18	$\overline{\text{IOUT}}$	I Channel baseband output
5	LOTEST	LO Test pin - do not connect	19	IOUT	I Channel baseband output
6	RFBYPASS	RF Bypass output	20	SLEEP	Hardware power down input
7	VccRF2	RF Supply	21	SCL	I^2C Clock
8	VccRF1	RF Supply	22	SDA	I^2C Data
9	N/C	Not connected	23	P0	General purpose switching output
10	RFIN	RF Input	24	XCAP	Crystal oscillator feedback
11	N/C	Not connected	25	XTAL	Crystal oscillator crystal input
12	$\overline{\text{RFIN}}$	RF Complementary Input	26	VccDIG	Digital Supply
13	N/C	Not connected	27	VccCP	Varactor Tuning Supply
14	RFAGC	RF Gain control input	28	PUMP	PLL charge pump output

Table 1 - Pin Names

Note: Ground contact is via underside of package. Pin 2 is connected to ground internally.

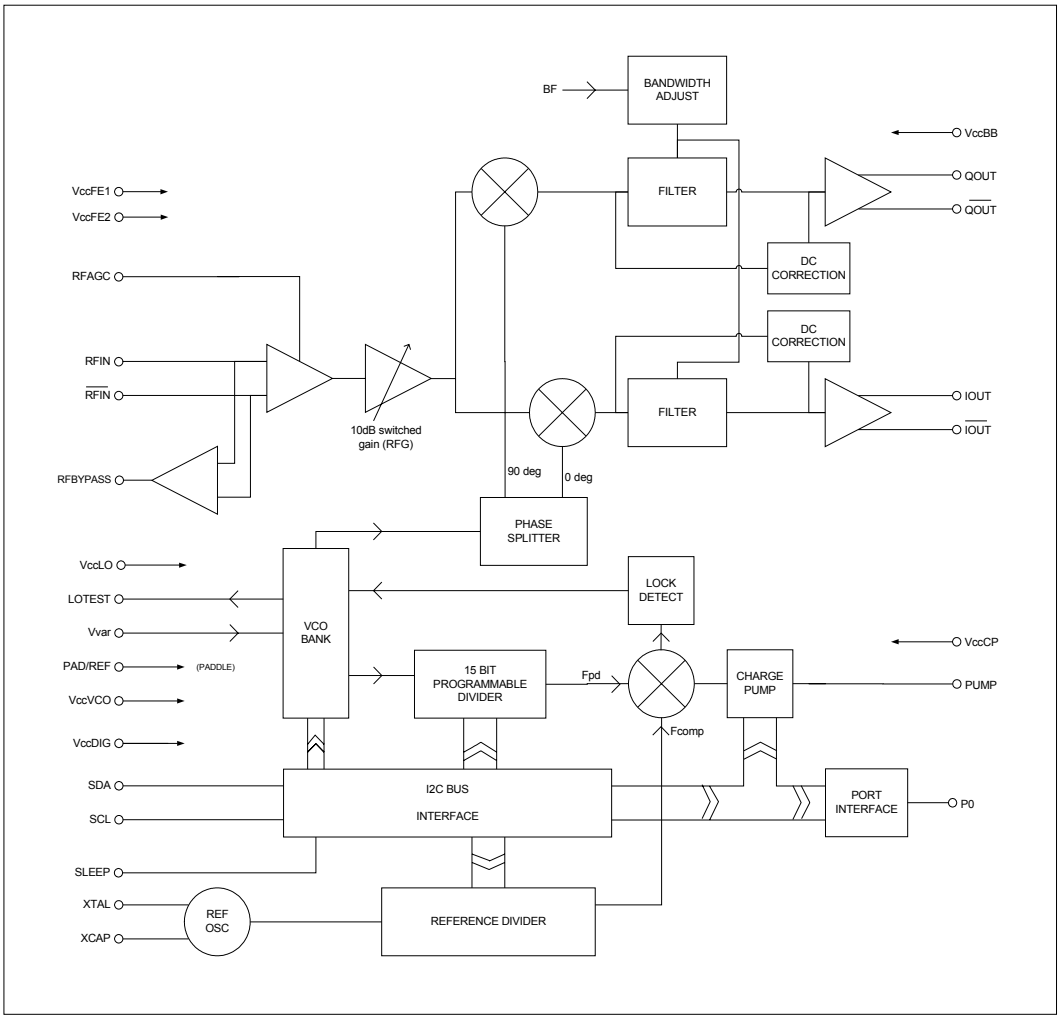


Figure 3 - Detailed Block Diagram

1.0 Circuit Description

1.1 Functional Description

The CE5037 is a single chip wide band direct conversion tuner with integral RF bypass optimised for digital satellite receiver systems. It provides excellent signal handling capability in the presence of high composite signal levels.

The device offers a highly integrated solution for a satellite tuner incorporating a low phase noise PLL frequency synthesizer, the quadrature down converter, a fully integrated local oscillator, and programmable baseband channel filters. A minimal number of additional peripheral components are required. The crystal reference source can be also used as the reference for the demodulator.

An I^2C compatible bus interface controls all of the tuner functionality.

The CE5037 contains both hardware and software power down modes.

1.2 Signal Path

1.2.1 RF Input

The tuner RF input signal at a frequency of 950 – 2150 MHz is fed to the CE5037 RF input pre-amplifier stage.

The signal handling is designed such that no tracking filter is required to offer immunity to input signal composite overload.

The RF input amplifier feeds an AGC stage, which provides RF gain control. There is additional gain adjustment in the baseband section. The total AGC gain range will guarantee an operating dynamic range of –92 to –10 dBm.

The RF AGC in the CE5037 is divided into two stages. The first stage is a continually variable gain control stage, and provides the main system AGC set under control of the analogue AGC signal generated by the demodulator section. The second stage is a programmable gain stage to reduce RF gain by 10 dB. This would normally be used when an external LNA is being used to improve system sensitivity.

The analogue RF AGC is optimised for S/N and S/I performance across the full dynamic range. Typical RF AGC characteristic and variation of IIP3, IIP2 and NF are shown in Section 8 - Typical Performance Curves.

The output of the AGC stage is coupled to the quadrature mixer where the RF signal is mixed with quadrature local oscillator signals generated by the on-board local oscillator.

1.2.2 Baseband

The outputs of the quadrature down converter are passed through the baseband filters followed by a programmable baseband gain stage.

The baseband paths are DC coupled. An integrated DC correction loop prevents saturation due to local oscillator self-mixing in the converter section. No external components are required for dc correction.

The baseband filters are 5^{th} order Chebychev and provide excellent matching in both amplitude and phase between the I and Q channels. The filters are fully programmable for 3 dB bandwidths from 6 MHz to 43 MHz. The recommended filter bandwidth is related to the required symbol rate by the following equation.

$$-3dBFilterBandwidth\ \ fc = \frac{SymbolRate \times 1.35}{2 \times 0.8}$$

This equation makes no allowance for LNB tuning offset at low symbol rates < 10 MS/s.

The baseband filter uses an automatic tuning algorithm to calibrate the filter bandwidth to the programmed requirement. This removes any variation due to operating conditions and process variations. The automatic tuning algorithm uses a frequency locked loop, which locks the filter bandwidth to a reference frequency derived from the crystal reference input frequency. Further details are provided in the programming section.

The filters are followed by a programmable gain stage. This provides twelve 1.5 dB gain steps. These can be used for optimising performance at different symbol rates and for adjusting the output level in applications not using CE6313.

The differential outputs of each channel stage are designed for low impedance drive capability and low intermodulation. The device can also be used in single-ended applications with unused outputs.

1.2.3 RF Bypass

The CE5037 provides a single ended bypass function, which can be used for driving a second receiver module. The electrical characteristics of the RF input are unchanged whether the RF bypass is enabled or disabled.

The RF Bypass powers up in the enabled state and can also operate with the remainder of the device in power down modes.

1.3 Local Oscillator Generation

1.3.1 On Chip VCO

The local oscillator on the CE5037 is fully integrated. It consists of three independently selectable oscillator stages with sub bands. The three oscillators and sub-bands are designed to provide optimum phase noise performance over the required tuning range of 950 to 2150 MHz, over operating conditions and process variations.

The local oscillators operate at a harmonic of the required local oscillator frequency and are divided down to the required LO frequency. The required divider ratio is automatically selected by the local oscillator control logic.

The oscillators are fully controlled by an on-chip automatic tuning algorithm. The user simply programs the required LO frequency. The control logic automatically selects the required VCO and sub band to give optimum performance. VCO settling time is minimized as different tuning algorithms are used, depending on the magnitude of the LO frequency change required. This choice of algorithm is also automatic and does not require user intervention.

The oscillator control logic tracks any changes in operating conditions and will retune the VCO if necessary, however hysteresis is built into this function to avoid unnecessary switching.

All oscillator components are included on the chip including the VCO varactor. An external loop filter is required as part of the PLL frequency synthesizer.

1.3.2 PLL Frequency Synthesizer

The fully integrated PLL frequency synthesizer section controls the LO frequency. The only external requirements are crystal reference and simple second order loop filter. The PLL can be operated up to comparison frequencies of 2 MHz enabling a wide loop bandwidth for maximizing the close in phase noise performance.

The local oscillator input signal is multiplexed from the active oscillator to an internal preamplifier, which provides gain and reverse isolation from the divider signals. The output of the preamplifier provides the input to a 15-bit fully programmable divider with MN+A architecture incorporating a dual modulus 16/17 prescaler.

The output of the programmable divider is fed to the phase comparator where it is compared in both phase and frequency domain with the comparison frequency. This frequency is derived either from the on-board crystal controlled oscillator or from an external reference source. In both cases the reference frequency is divided down to the comparison frequency by the reference divider, which is programmable into 1 of 15 ratios.

The output of the phase detector feeds a charge pump which combined with an external loop filter integrates the current pulses to control the varactor voltage. The charge pump current is automatically varied by the VCO control logic to compensate for VCO gain variations that are dependent on selected sub band. The varactor control voltage is externally coupled to the oscillator section through the input pin Vvar.

1.4 I²C Interface

All programming for the CE5037 is controlled by an I²C data bus and is compatible with 3V3 standard mode formats.

Data and Clock are fed in on the SDA and SCL lines respectively as defined by I²C bus format. The device can either accept data (write mode), or send data (read mode). The LSB of the address byte (R/W) sets the device into write mode if it is logic '0', and read mode if it is logic '1'. The I²C address is fixed at C0 (Write)/C1(Read) in hex format.

The CE5037 contains 16 control registers. These registers are read/write registers. These registers are addressed as sub-addresses on the I²C bus. Registers can be addressed as random access single write/read or random access sequential write and read as shown below.

Random Access Single Write

Stop	Start	Device Address	W	A	Register Address N	A	Register Data N	A	Stop

Random Access Sequential Write

Stop	Start	Device Address	W	A	Register Address N	A	Register Data N	A	Register Data N+1	...	Register Data N+M	A	Stop

Random Access Single Read

Stop	Start	Device Address	W	A	Register Address N	A	Start	Device Address	R	A	Register Data N	N	Stop

Random Access Sequential Read

Stop	Start	Device Address	W	A	Register Address N	A	Start	Device Address	R	A	Register Data N	A	...	Register Data N+M	N	Stop

W Write bit

A Acknowledge Bit

N Not Acknowledge

A SLEEP pin is provided. This powers down all sections of the chip including the crystal oscillator and I²C interface. The RF bypass function will be operational in this mode providing it has been previously enabled through the I²C interface.

2.0 Register Map and Programming

The register map is arranged as 16 byte-wide read/write registers grouped by functional block. The registers may be written to and read-back from either sequentially (for lowest overhead) or specifically (for maximum flexibility).

A significant number of bits are used for test and evaluation purposes only and are fixed at logic '0' or '1'. The correct programming for these test bits is shown in the table below. It is essential that these values are programmed for correct operation. When the contents of the registers are read back the value of some bits may have changed from their programmed value. This is due to the internal automatic control which can update registers. Any changes can be ignored.

Read only bits are marked with an asterisk (*). Any data written to these bits will be ignored.

Registers are set to default settings on applying power. These conditions are shown below and in the applicable tables.

Register	Block	Function							
0	PLL	PLF	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
1	PLL	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
2	PLL	0	0	C1	C0	R3	R2	R1	R0
3	PLL	X*	1	0	0	0	0	0	0
4	RF Front End	X*	1	1	0	1	1	LEN	RFG
5	Base Band	BF7	BF6	BF5	BF4	BF3	BF2	BF1	BF0
6	Base Band	0	LF	SF	BR4	BR3	BR2	BR1	BR0
7	Base Band	BLF*	BG3	BG2	BG1	BG0	0	0	0
8	Local Oscillator	FLF*	0	1	0	0	0	0	0
9	Local Oscillator	1	0	1	0	0	0	1	0
A	Local Oscillator	1	1	1	1	0	0	0	1
B	Local Oscillator	X*	X*	1	1	1	0	0	0
C	Local Oscillator	1	1	0	1	0	0	0	0
D	Local Oscillator	X*	X*	X*	1	0	0	0	0
E	Local Oscillator	X*	X*	1	1	0	0	0	0
F	General	PD	CLR	P0	0	X*	X*	X*	X*

Table 2 - Register Map

X* denotes a read only test bit

2.1 PLL Registers

There are four registers that control the PLL:

Bit Field	Name	Default	Type	Description
7	PLF	-	R	PLL Lock Flag
6:0	$2^{[14:8]}$	0	R/W	MSB bits of LO Divider register

Table 3 - Register 0

The PLF bit is the PLL lock detect circuit output. The PLF bit is set after 64 consecutive comparison cycles in lock. A chip-wide reset initializes the lock detect output to 0.

The $2^{[14:8]}$ bits are the MSB bits of the LO Divider divide value.

Bit Field	Name	Default	Type	Description
7:0	$2^{[7:0]}$	0	R/W	LSB bits of LO Divider register

Table 4 - Register 1

The $2^{[7:0]}$ bits are the LSB bits of the LO Divider divide value. The division ratio of the LO divider is fully programmable to integer values within the range of 240 to 32767.

Note that when the LO Divider divide value is to be changed, the new value is not actually presented to the LO Divider until all of the 15-bit control word $2^{[14:0]}$ has been programmed. Register 0 and 1 must be therefore be programmed (in any order) before the LO divider is updated even if the only data change is in one of the registers.

Bit Field	Name	Default	Type	Description
7:6	-	0	R/W	Test modes
5:4	C[1:0]	0	R/W	Charge pump current
3:0	R[3:0]	0	R/W	Reference divider ratio

Table 5 - Register 2

The C[1:0] bits set the programmed charge pump current

C[1]	C[0]	Typ	Units
0	0	400	uA
0	1	550	uA
1	0	750	uA
1	1	1000	uA

Table 6 - Charge Pump Currents

The charge pump current is automatically increased to the next setting dependent on the VCO sub band that has been selected by the VCO tuning algorithm. This is to compensate for changes in VCO gain and so provide consistent PLL performance across all sub bands. Programming the highest charge pump value will not allow the value to be incremented, therefore this value should not be programmed.

The value read back for the charge pump current is the actual value in use for the selected sub band.

The R[3:0] bits select the Reference Divider divide ratio. The ratio selected is not a simple binary power-of-two value but through a lookup table, see Table 7- PLL Reference Divider Ratios.

R3	R2	R1	R0	Division Ratio
0	0	0	0	2
0	0	0	1	4
0	0	1	0	8
0	0	1	1	16
0	1	0	0	32
0	1	0	1	64
0	1	1	0	128
0	1	1	1	256
1	0	0	0	3
1	0	0	1	5
1	0	1	0	10
1	0	1	1	20
1	1	0	0	40
1	1	0	1	80
1	1	1	0	160
1	1	1	1	320

Table 7 - PLL Reference Divider Ratios

Bit Field	Name	Default	Type	Description
7:0	-	0X40	R/W	Test Modes

Table 8 - Register 3

This register controls test modes within the PLL. This should be programmed with the default settings.

2.2 RF Control Register

A single register controls RF programmability.

Bit Field	Name	Default	Type	Description
7	-	-	R	Test Modes
6:2	-	11011	R/W	Test Modes
1	LEN	1	R/W	Bypass Enable
0	RFG	0	R/W	RF Gain Adjust

Table 9 - Register 4

The LEN bit enables the RFBYPASS output. With this bit set, the RF Bypass is active even if ‘software’ or ‘hardware’ power down has been selected.

The RFG bit controls the gain of the second section of RF gain control. With this bit set, the RF gain is reduced by 10dB. This setting would normally used when an external LNA is being used.

2.3 Base Band Registers

There are three registers that control the Base Band:

Bit Field	Name	Default	Type	Description
7:0	BF[7:0]	0X3C	R/W	Base Band Filter Cut-Off Frequency

Table 10 - Register 5

The bits BF[7:0] control the bandwidth of the baseband filter. An automatic adjustment routine synchronizes the filter bandwidth to a reference frequency derived from the crystal.

Bit Field	Name	Default	Type	Description
7	-	0	R/W	Test Mode
6	LF	0	R/W	Baseband Filter Adjust Disable
5	SF	0	R/W	Baseband Filter Adjust Disable
4:0	BR[4:0]	1000	R/W	Base Band Reference Division Ratio

Table 11 - Register 6

The LF and SF bits disable the baseband filter adjustment. It is recommended that these bits are set after programming the filter bandwidth to prevent interactions within the circuit. These bits must be reset to enable the baseband filter bandwidth to be reprogrammed.

The BR[4:0] bits set the crystal reference divide ratio. This effectively determines the resolution setting of the baseband filters. The baseband filter settings (BF[7:0]) can be calculated from the following equation.

$$BF[7:0] = \frac{(\text{Filter bandwidth}(MHz) * 5.088 * BR[4:0])}{\text{Crystal Frequency}(MHz)} - 1$$

See Section 3 Applications Information, for a typical programming example.

BR[4:0] = 0 is invalid

Bit Field	Name	Default	Type	Description
7	BLF	-	R	Base Band Lock Flag
6:3	BG[3:0]	0111	R/W	Base Band Gain Select
2:0	-	000	R/W	Test Modes

Table 12 - Register 7

The BLF bit indicates that the baseband adjustment has completed and locked.

The control bits BG[3:0] define the gain of the Base Band post-filter amplifier. The following table shows the gain - note this is relative gain. The 1.5 dB gain steps enable the baseband output level to be adjusted and optimise gain distribution for different symbol rates.

BG[3]	BG[2]	BG[1]	BG[0]	Gain (dB)
0	0	0	0	0
0	0	0	1	1.5
0	0	1	0	3.0
0	0	1	1	4.5
0	1	0	0	6.0
0	1	0	1	7.5
0	1	1	0	9.0
0	1	1	1	10.5
1	0	0	0	12.0
1	0	0	1	13.5
1	0	1	0	15.0
1	0	1	1	16.5

Table 13 - BG[3:0] Control of Base Band Post Filter Gain

2.4 Local Oscillator Registers

There are seven registers that control the Local Oscillator: These are used primarily for test and evaluation by Intel Corporation. Although VCO's can be manually programmed, the user is recommended to use the default automatic settings as these provide optimum performance.

Bit Field	Name	Default	Type	Description
7	FLF	-	R	Full Lock Flag
6:0	-	0X20	R/W	Test Modes

Table 14 - Register 8

The FLF bit is the VCO tuning controller lock output and is set when PLL is locked and the automatic VCO tuning is optimised and complete.

Register 9 to Register E are for test modes only. It is however important that these registers are programmed with the values shown.

Bit Field	Name	Default	Type	Description
7:0	-	0XA2	R/W	Test Modes

Table 15 - Register 9

Bit Field	Name	Default	Type	Description
7:0	-	0XF1	R/W	Test Modes

Table 16 - Register A

Bit Field	Name	Default	Type	Description
7:6	-	-	R	Test Modes (read only)
5:0	-	0X38	R/W	Test Modes

Table 17 - Register B

Bit Field	Name	Default	Type	Description
7:0	-	0XD0	R/W	Test Modes

Table 18 - Register C

Bit Field	Name	Default	Type	Description
7:5	-	-	R	Test Modes (read only)
4:0	-	0X10	R/W	Test Modes

Table 19 - Register D

Bit Field	Name	Default	Type	Description
7:6	-	-	R	Test Modes (read only)
5:0	-	0X30	R/W	Test Modes

Table 20 - Register E

2.5 General Control Register

This register controls powerdown and general control functions:

Bit Field	Name	Default	Type	Description
7	PD	1	R/W	Power Down
6	CLR	0	R/W	Clear and reset logic
5	P0	0	R/W	Port 0 control
4	-	0	R/W	Test Mode
3:0	-	-	R	Test Modes (Read only)

Table 21 - Register F

The PD bit is the 'software' power down control. When this bit is set to 1, all the analogue blocks are powered down with the exception of the Crystal Oscillator. The I^2C interface will remain active and can still be used to enable the RF Bypass.

Setting the SLEEP input pin high also invokes 'software' power down with the addition of powering down the Crystal Oscillator to produce 'hardware' power down. The RF Bypass will remain active if it has been previously programmed on the I^2C bus. Note that in 'hardware' power down, the I^2C interface does not operate.

The CLR bit re-triggers the power-on-reset function. This resets all register values to their power-on reset default value. The CLR bit is itself cleared. Note that the chip-wide reset will reset the I^2C Interface and the current write sequence used to set this bit will not be acknowledged.

The P0 bit controls the state of the output port according to Table 22.

P0	Output Port State
0	Off, high impedance
1	On, current sinking

Table 22 - Output Port States

3.0 Applications Information

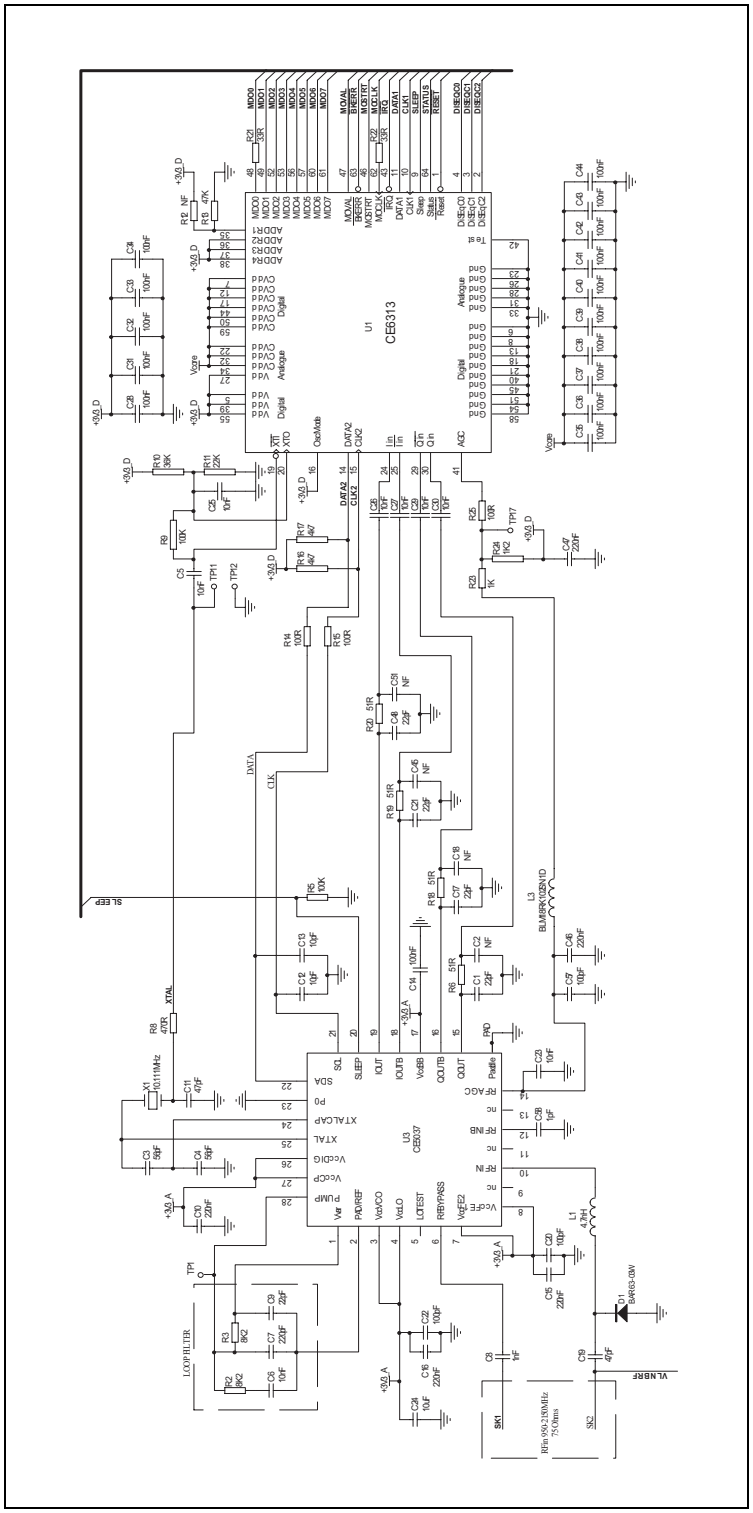


Figure 4 - Typical Application with CE6313 Demodulator

3.1 General Design Guidelines

Figure 4 shows a typical application using a CE6313 as a demodulator. This is available as a reference design (CE9542) from Intel Corporation.

The design uses a standard two layer board. All components are mounted on the upper surface with the lower surface as a ground plane. The RF input requires a coupling capacitor and series inductor for optimum matching. The RF bypass output requires a coupling capacitor. Good decoupling should be used - these components should be mounted as close to the device as practicable.

All ground contact to the CE5037 is to the ground 'paddle' on the underside of the package. This must be soldered fully to the board to achieve best thermal and electrical contact. It is recommended that an array of vias (4 x 4) is used to achieve good contact to the ground plane underneath the device

A common crystal reference can be used for the tuner and demodulator. The crystal oscillator capacitors are optimised for a 10.111 MHz reference.

Sensitivity is optimised by minimizing interaction from digital signal activity in the demodulator. This is achieved by filtering in the agc control, and filter networks in the baseband I and Q signals between the demodulator and CE5037. These networks should be mounted as close to the CE5037 as possible.

The typical performance from the reference design is shown in the table below:

Parameter	Typ.	Units	Notes
Sensitivity	-83	dBm	QEF 27.5MS/s rate 7/8 No added noise
C/N 27.5MS/s rate 7/8 2e-4 post Viterbi BER	8.3 8.1 8.1	dB dB dB	Input = -69 dBm -45 dBm -23 dBm
C/N 2MS/s rate 7/8 2e-4 post Viterbi BER	8.2 8.0 8.0	dB dB dB	Input = -81dBm -45 dBm -23 dBm
Interference Rejection Ratio 27.5 MS/s rate 7/8. Interferers at -25 dBm	32 35 45 35	dB dB dB dB	N+1 N+4 N+10 2 Interferers at -25dBm

Table 23 - Typical Performance using CE5037 and CE6313

Further information is provided in CE9542 user guides.

The CE5037 can also be used with other demodulators. If the demodulator has a single-ended input then the CE5037 can be used with a single-ended outputs ie IOUT and QOUT. The unused outputs should be loaded with an equivalent load to the demodulator input to maintain a good balanced configuration. The optimum output level for the demodulator can be achieved by adjusting the post filter baseband gain.

3.2 DVB-S2 Applications

The excellent performance of the CE5037 makes the device also suitable for the higher level modulation schemes (8PSK) used for DVB-S2. In the critical areas of quadrature accuracy and phase noise, typical performance is shown in the following table.

Parameter	Value	Notes
Quadrature Amplitude Matching	< 0.5 dB	Filter bandwidth = 26.5 MHz
Quadrature Phase Matching	< 2 °	
Integrated Phase Noise LO = 950MHz	0.40 °rms	PLL Loop Bandwidth = 10kHz
Integrated Phase Noise LO = 1500MHz	0.62 °rms	Phase noise integrated over 1kHz to 10 MHz
Integrated Phase Noise LO = 2150MHz	0.83 °rms	

Table 24 - Typical Performance for DVB-S2 Applications

3.3 Baseband Filter Bandwidth Calculation

The bandwidth of the baseband filter is given by the following expression:

$$fbw = \frac{fxtal}{BR \times 5.088} \times (BF + 1) \quad \textit{Equation 1}$$

where:

fbw = the filter bandwidth in MHz within the range 8 MHz to 43 MHz.

fxtal = crystal oscillator frequency in MHz.

BR = decimal value of the bits BR[4:0], range 1-31.

(BR = 0 is not allowed)

BF = decimal value of the register bits BF[7:0], range 0 - 255.

The above equation can be re-arranged as follows

$$BF = \left[fbw \times 5.088 \times \frac{BR}{fxtal} \right] - 1 \quad \textit{Equation 2}$$

It is recommended that BR should be set so that $\frac{fxtal}{BR}$ is approximately 1 MHz

This sets the bandwidth resolution to approximately 200kHz

The value of BF can now be calculated from Equation 2 and rounded to the nearest integer:

Example

Conditions: fxtal = 10.111 MHz, fbw = 26.5 MHz

Choose BR = 10

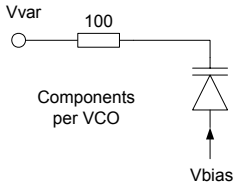
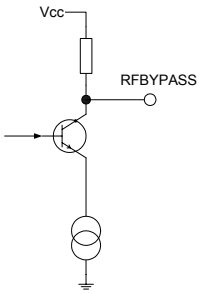
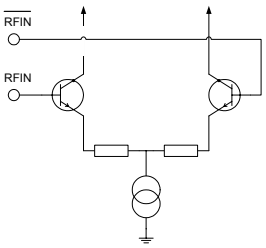
$$BF = \frac{26.5 \times 5.088 \times 10}{10.111} - 1 = 132.35$$

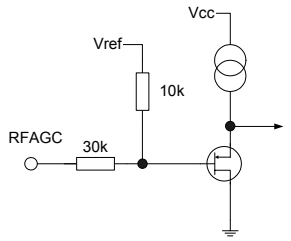
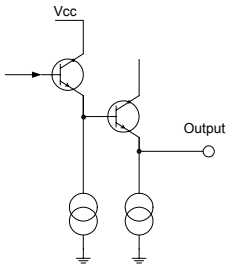
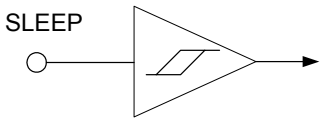
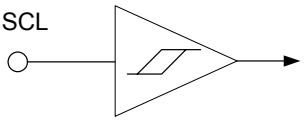
BF = 132

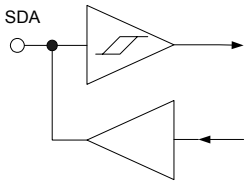
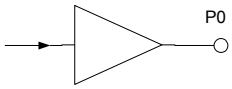
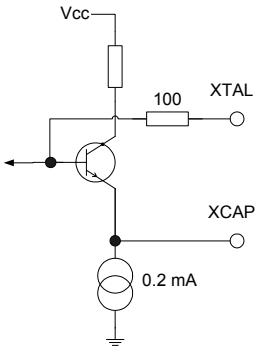
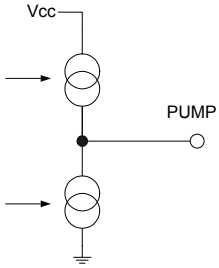
The actual filter bandwidth is therefore given by:

$$fbw = \frac{10.111}{10} \times (132 + 1) \times \frac{1}{5.088} = 26.43\,MHz$$

4.0 Pin Descriptions

Pin#	Name	Description	Schematic
1	Vvar	LO voltage tuning input.	
2	PAD/REF	Bonded to paddle. Production continuity test for paddle soldering and also ground reference for loop filter.	
3	VccVCO	+3.3 V voltage supply for VCO's.	
4	VccLO	+3.3 V voltage supply for LO circuits.	
5	LOTEST	For Intel testing only. Must not connect.	
6	RFBYPASS	RF bypass output. AC couple. Matching circuitry as shown in applications diagram. Do not connect in applications where RF bypass is not required.	
7	VccRF2	+3.3 V voltage supply for RF.	
8	VccRF1	+3.3 V voltage supply for RF.	
9	N/C	Not connected.	
10 12	RFIN $\overline{\text{RFIN}}$	RF input. AC couple. See applications diagram.	
11	N/C	Not connected.	
13	N/C	Not connected.	

Pin#	Name	Description	Schematic
14	RFAGC	RF analog gain control input.	
15 16	$\overline{\text{QOUT}}$ QOUT	Q channel baseband differential outputs. AC couple as shown in application diagram.	
17	VccBB	+3.3 V voltage supply for Baseband.	
18 19	$\overline{\text{IOUT}}$ IOUT	I channel baseband differential outputs. AC couple as shown in application diagram.	Same as pin 15,16
20	SLEEP	Hardware power down input. Logic '0' normal mode. Logic '1' - analog sections are powered down including crystal oscillator.	 CMOS Digital input
21	SCL	I^2C serial clock input	 CMOS Digital input

Pin#	Name	Description	Schematic
22	SDA	I^2C serial data input/output	 CMOS Digital input/output
23	P0	Switching port output. Open Drain '0' = disabled (high impedance) '1' = enabled.	 CMOS Digital output
24 25	XCAP XTAL	Reference oscillator crystal inputs. XTAL pin can be used for external reference via 10nF capacitor. See applications diagram for recommended external components (10.111 MHz)	
26	VccDIG	+3.3 V voltage supply for digital logic.	
27	VccCP	+3.3 V voltage supply for varactor tuning.	
28	PUMP	Charge pump output.	

5.0 Absolute Maximum Ratings

Parameter	Min.	Max.	Units	Notes
Maximum voltage on any Vcc pin	-0.3	3.6	V	
Maximum voltage between any two Vcc pins		0.3	V	
Maximum voltage on any other pin	-0.3	Vcc + 0.3	V	The voltage on any pin must not exceed 3.6 V
Maximum voltage between RFIN and $\overline{\text{RFIN}}$	-1	1	V	
P0 Output current		20	mA	
Maximum RF Input		10	dBm	
Storage temperature	-55	150	°C	
Junction temperature		125	°C	
Package thermal resistance		34	°C/W	Package ground paddle soldered to ground
ESD Protection - all pins except 10,12		1.75	kV	Mil std 883B method 3015 cat1
ESD Protection - pins 10,12 RFIN, $\overline{\text{RFIN}}$		0.75	kV	Mil std 883B method 3015 cat1

6.0 Operating Conditions

Parameter	Min.	Max.	Units	Notes
Supply Voltage	3.15	3.45	V	
Operating Temperature	-10	+85	°C	
RF Input Frequency	950	2150	MHz	
Baseband I/Q Output load	4.7	 15	kΩ pF	

7.0 Electrical Characteristics

Test conditions (unless otherwise stated)

T_{amb} = 25°C, Vee= 0V, All Vcc supplies = 3.3 V+-5%

Baseband Gain = 9 dB, RFG = 0

Baseband filter bandwidth 26.5 MHz

All power levels are referred to 75 Ω (0 dBm = 109 dBμV)
Specifications refer to total cascaded system of converter/AGC stage and baseband amplifier/filter stage.

Output amplitude of 0.5 Vp-p differential.

Characteristic	Min.	Typ.	Max.	Units	Conditions
Supply Current		 145 155	 200 215	 mA mA	Outputs unloaded. Max Filter bandwidth RF Bypass disabled RF Bypass enabled
Hardware Power Down Software Power Down		0.2 1.7	 3	mA mA	 No RF input. Crystal oscillator remains operational
System					
Input Return Loss		9		dB	Zo = 75 Ω with external matching. Bypass enabled or disabled
Noise Figure DSB		8 8.5	10 10 13	dB dB dB	At max gain At -70 dBm operating level At -60 dBm operating level
Variation in NF with RF gain adjust			-1	dB/dB	Above -60dBm operating level
Operating dynamic range		-92	-10	dBm	1MS/s
Operating dynamic range		-84	-10	dBm	27.5MS/s
Conversion Gain Max Min	 72	 78 -6	 10	 dB dB	 RFagc = 0.2V RFagc = 2.8V
AGC Control Range	68	72		dB	AGC monotonic for RFagc from Vee to Vcc
RFAGC input current	-150		150	μA	Vee <= RFagc<= Vcc
System IM2			-28 -40	dBc dBc	Baseband defined, note 1 RF front-end defined, note 2
System IM3			-24 -30	dBc dBc	Note 3 Note 4
IIP2	15	22		dBm	At -40 dBm input, note 2
IIP3	5	13		dBm	At -25 dBm input, note 3

Characteristic	Min.	Typ.	Max.	Units	Conditions
LO second harmonic interference level			-35	dBc	Note 5, all gain settings
LNA second harmonic interference level			-20	dBc	Note 6
Quadrature gain match	-1		1	dB	1.5 to 18 MHz
Quadrature phase match	-3 -5		3 5	deg deg	Baseband Signal = 1.5 MHz Baseband Signal = 18 MHz
I & Q channel in band ripple			1	dB	1.5 to 18 MHz
LO reference sideband spur level on I & Q outputs			-40	dBc	synthesizer phase detector comparison frequency 500 - 2000 kHz
In band local oscillator leakage to RF input			-65 -55	dBm dBm	950 - 2150 MHz 30 - 950 MHz
Channel lock time			50	ms	Worst case channels
Local Oscillator					
VCO Gain		27		MHz/V	LO = 2 GHz. Note 7
SSB Phase Noise		-83	-76 -96 -110	dBc/Hz dBc/Hz dBc/Hz	10 kHz offset 100 kHz offset 1 MHz offset
Phase Noise floor			-132	dBc/Hz	
Integrated phase jitter			3	deg	10 kHz to 15 MHz
Varactor input current	-10		10	nA	Vvar = 0.5 to 1.3 V
Baseband Filters					
Bandwidth	6		43	MHz	Max specified load
Bandwidth Tolerance	-1		+1	MHz	All bandwidth settings
Time to change filter bandwidth			10	ms	
Total Harmonic Distortion			-30	dBc	1 Vpp differential output at 43 MHz filter bandwidth
RF Bypass					Output load = 75 ohms
Gain	-2	1.5	4	dB	
Noise Figure		8.5	10	dB	
OPIP3		9		dB	Note 8
OPIP2	20			dBm	Note 9
Output return loss	9			dB	
Forward Isolation		30		dB	950-2150 MHz. Bypass disabled

Characteristic	Min.	Typ.	Max.	Units	Conditions
Reverse Isolation		30		dB	950-2150 MHz. Bypass enabled or disabled
In band LO leakage			-65	dBm	950-2150 MHz. Bypass enabled or disabled
synthesizer					
Charge Pump Current	304 422 578 762	400 550 750 1000	552 759 1035 1380	µA µA µA µA	
Charge Pump Matching		2		%	Vpin = 0.5 to 1.3 V
Charge Pump Leakage	-10	+/-3	+10	nA	Vpin = 0.5 to 1.3 V
Charge Pump Compliance	0.4		Vcc - 0.4	V	
Crystal Frequency	4		20	MHz	
Recommended crystal series resistance	12	25	50	ohms	10 MHz crystal
Crystal power dissipation		100	500	µW	Note 10
Crystal load capacitance		16		pF	Note 10
Crystal oscillator startup time			10	ms	
External reference input frequency	4		20	MHz	ac coupled sinewave
External reference drive level	0.5		2.0	Vpp	ac coupled sinewave
Phase detector comparison frequency	0.5		2	MHz	
Equivalent phase noise at phase detector		-148		dBc/Hz	10 MHz crystal SSB within PLL loop bandwidth
Interface					
SDA, SCL Input high voltage Input low voltage Hysteresis Input current	 2.3 0 -10	 0.4 	 3.6 1 10	 V V µA	 Input = Vee to VccDIG +0.3 V
SDA Output Voltage			0.4	V	Isink = 3 mA
SCL clock rate			100	kHz	

Characteristic	Min.	Typ.	Max.	Units	Conditions
External Port P0					
Sink Current	3			mA	Vo = 0.7 V
Leakage Current			10	μA	Vo = Vcc
SLEEP Input					
Input high voltage	1.9		3.6	V	
Input low voltage	Vee		1.0	V	
Input Current			10	μA	Vin = Vee to VccDIG

Note 1: AGC set to deliver an output of 0.5Vp-p with an input CW @ frequency fc of -30 dBm, undesired tones at fc+146 and fc+155 MHz @ -15 dBm, generating output IM spur at 9 MHz. Measured relative to unwanted signal.

Note 2: LO set to 2145 MHz and AGC set to deliver a 5 MHz output of 0.5Vp-p with an input CW @ frequency 2150 MHz of –40 dBm. Undesired tones at 1.05 and 1.1 GHz at -25 dBm generating IM spur at 5 MHz baseband. Measured relative to unwanted signal.

Note 3: AGC set to deliver an output of 0.5Vp-p with an input CW @ frequency fc of -30 dBm. Two undesired tones at fc+205 and fc+405 MHz at -12 dBm, generating output IM spur at 5 MHz.

Note 4: AGC set to deliver an output of 0.5Vp-p with an input CW @ frequency fc of -30 dBm. Two undesired tones at fc+55 and fc+105 MHz at -15 dBm, generating output IM spur at 5 MHz.

Note 5: The level of 2.01 GHz down converted to baseband relative to 1.01 GHz with the oscillator tuned to 1 GHz.

Note 6: The level of second harmonic of 1.01 GHz at -20dBm downconverted to baseband relative to 2.01 GHz desired signal at -35dBm with agc set to give 0.5Vp-p output. LO frequency = 2 GHz.

Note 7: Reference VCO gain value for loop filter calculations. Using this recommended value then takes into account VCO switching and automatic charge pump current variations.

Note 8: Two input tones at fc+50 and fc+100 MHz at -12 dBm, generating output IM product at fc.

Note 9: IM2 product from two input tones at 1.05 and 1.1 GHz at -16 dBm, generating IM product at 2150 MHz.

Note 10: Crystal specifications vary considerably and significantly effect the choice of external oscillator capacitor values. Each application may require separate consideration for optimum performance.

8.0 Typical Performance Data

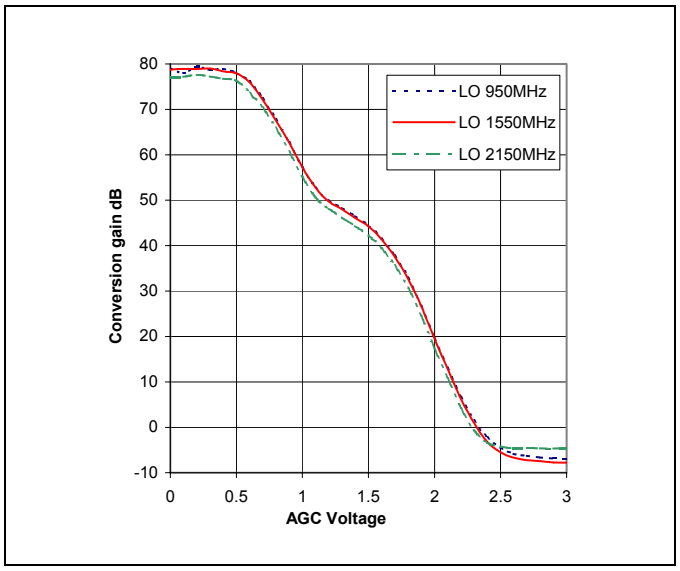


Figure 5 - Gain v. RFAGC at 25°C

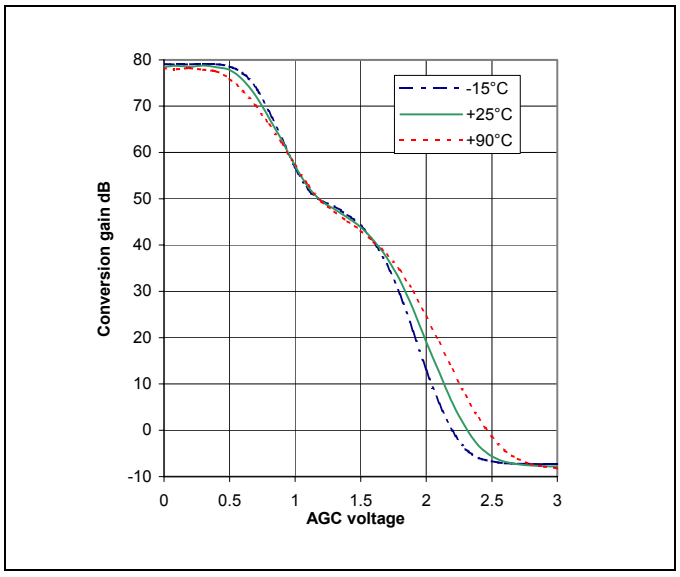


Figure 6 - Gain v RFAGC v. Temperature

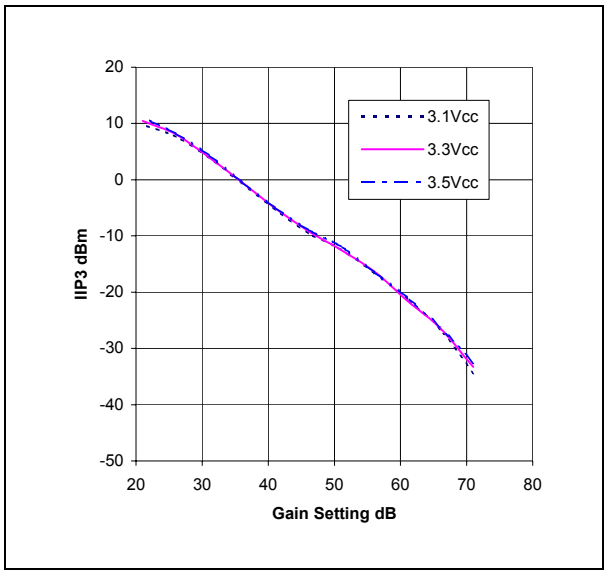


Figure 7 - IIP3 v Gain at 25°C

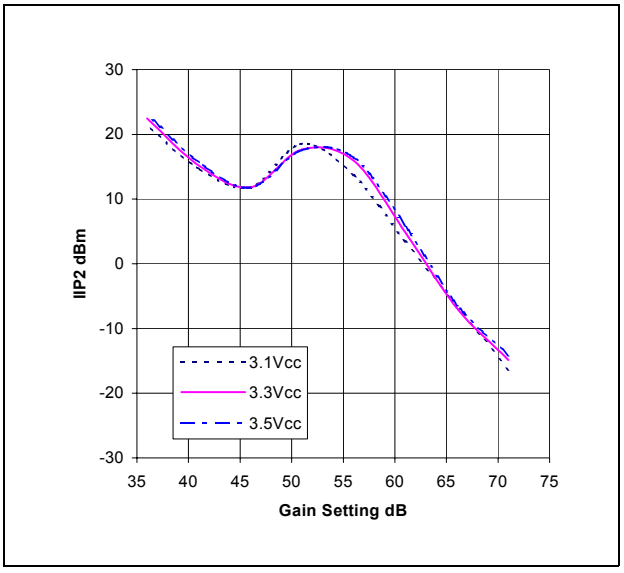


Figure 8 - IIP2 v Gain at 25°C

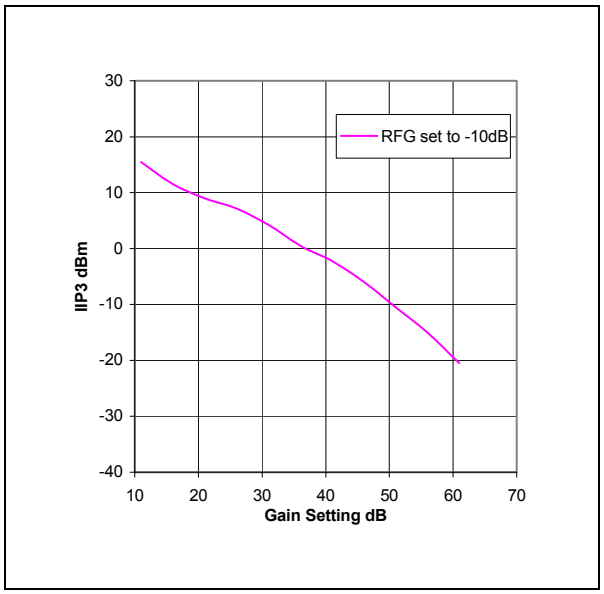


Figure 9 - IIP3 v Gain at 25°C (RFG = 1)

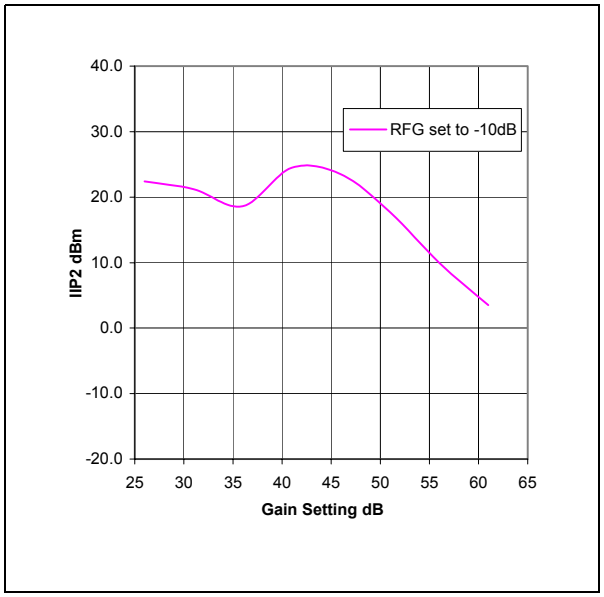


Figure 10 - IIP2 v Gain at 25°C (RFG = 1

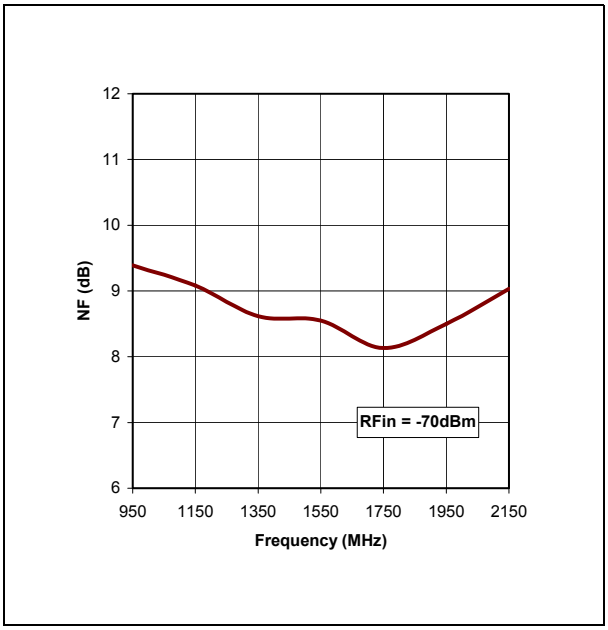


Figure 11 - Noise Figure v Freq at 25°C

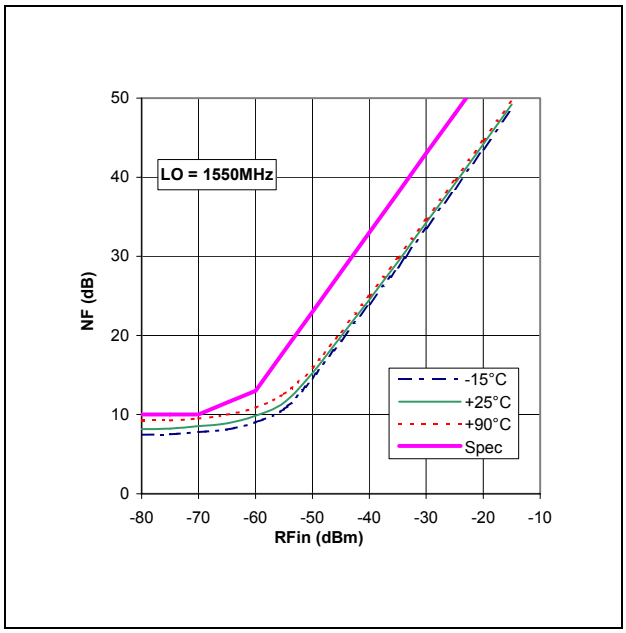


Figure 12 - Noise Figure v RFin v Temperature

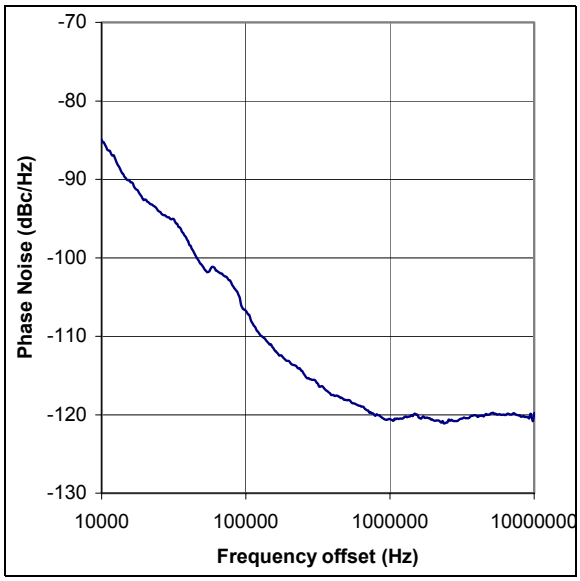


Figure 13 - LO Phase Noise at 25°C

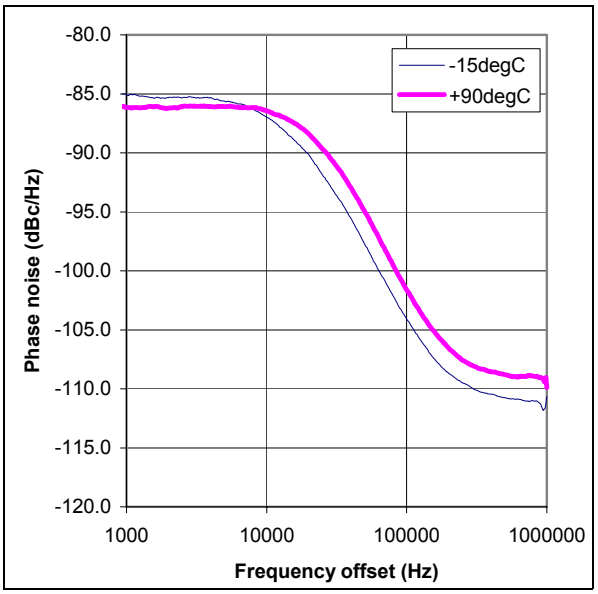


Figure 14 - LO Phase Noise v Temperature

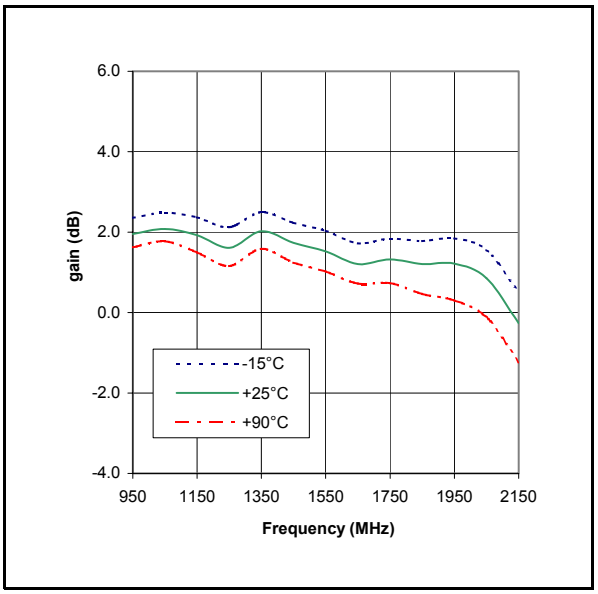


Figure 15 - RF Bypass Gain v Temperature

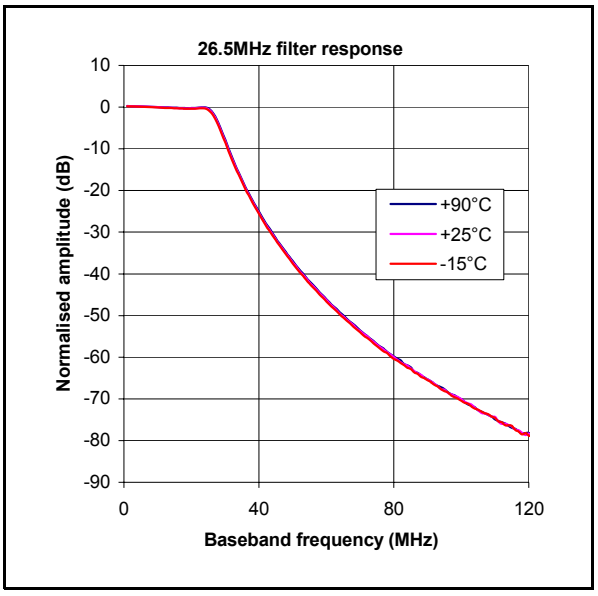


Figure 16 - Baseband Filter Response 26.5 MHz