AT86RF211S
FSK Transceiver for ISM Radio Applications

(Not Intended for Automotive or Medical Applications)

Datasheet

1. Features

- Up-compatibility with the AT86RF211
  - Same Features as AT86RF211 after Power-on Reset
  - New Features Activated by a Bit (ADDFEAT)
- Shrink Version with a Current Consumption Reduction of 20%
- Direct Replacement in Production
- Migration Documentation/Kit Available for AT86RF211 Users
- Multiband Transceiver: 400 to 950 MHz
- Monochip RF Solution: Transmitter-Receiver-Synthesizer
- Integrated PLL and VCO: No External Coil
- Design Highly Resistant to Interference
- Digital Channel Selection (200 Hz Steps)
- Data Rates Up to 100 kbps
- Transparent Asynchronous or Synchronous Modes thanks to Built-in Clock Recovery
- Three Data Slicer Modes Available: *External, Internal, Charge and Hold*
- High Output Power Enabling Use of Low-Cost Printed Antennas:
  - +14 dBm in 915 MHz Frequency Band
  - +15 dBm in 868 MHz Frequency Band
  - +16 dBm in 433 MHz Frequency Band
- FSK Modulation: Integrated Modulator and Demodulator
- Meets Wideband Application Requirements in the USA (250 kHz)
- Power Saving:
  - Stand-alone *Sleep* Mode and *Wake-up* Procedures
  - Eight Selectable Digital Levels for Output Power
  - High Data Rate and Fast Settling Time of the PLL
  - Low Power Oscillator Running Mode
- 100% Digital Interface through R/W Registers Including:
  - Fast Digital RSSI for Quick Channel Scanning
  - V_{CC} Readout
  - Digital Clock Output to Drive the Companion Microcontroller
- Pb-Free and RoHS Compliant

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for the latest version of the datasheet

2. Description

The AT86RF211S is a shrink version of the AT86RF211. In addition to cost reduction, the use of the latest RF e2v process provides a high level of robustness and performance (high output power) and significantly improves some technical features such as power consumption. The AT86RF211 is a fully compatible product that can be directly replaced in production, without redesigning the hardware or software. New features are also available through the software (activated by the ADDFEAT bit).

Like the AT86RF211, this is a single-chip transceiver dedicated to low-power wireless applications, optimized for licence-free ISM band operations from 400 to 950 MHz. Its flexibility and unique level of integration make it a natural choice for any system related to telemetry, remote controls, alarms, radio modems, Automatic Meter Reading, hand-held terminals or high-tech games and appliances. The AT86RF211S makes bidirectional communications affordable for applications such as secured transmissions with hand-shake procedures, new features and services.

The AT86RF211S can easily be configured to provide the optimal solution for your application: choice of external filters versus technical requirements (bandwidth, selectivity, immunity, range, etc), and software protocol (single channel, frequency agility, listen before transit, FHSS). The AT86RF211S is also well adapted to battery-operated systems, as it can be powered with as little as 2.4V. It also offers a *wake-up* receiver feature to save power by alerting the associated microcontroller only when a valid inquiry is detected.

3. General Overview

The AT86RF211S is a microcontroller RF peripheral. The chip's setup is done by writing or reading the registers (for example, frequency selection) or by obtaining information on the parameters such as RSSI level, Vbattery or PLL lock state. These operations are all carried out via a three-wire serial interface.

3.1 List of New Features

The AT86RF211S now replaces the AT86RF211, and offers numerous new features.

The AT86RF211S can operate in two different modes, described in the following table.

Table 3-1. Modes Description

Mode Name	Choice Made By	Compatibility	Additional Features	Recommended
RF211	ADDFEAT = CTRL1[0] = 0	Yes	No	For existing applications: direct replacement
RF211S	ADDFEAT = CTRL1[0] = 1	At reset state of DTR register	Yes	For new applications or upgrades: new functions

3.1.1 Data Rate

The AT86RF211S has a data rate of up to 100 kbps. The modulator and demodulator have been optimized to increase the speed of the RF links while maintaining a high performance level.

The receiver's bandwidth has been increased to 250 kHz for very wide band applications in the US.

3.1.2 Low-current XTAL Running Mode

It is now possible to run the XTO alone; this is useful for real-time demanding applications. The sinked current is 150 µA, increasing according to the load capacitance when the XTO signal is buffered, to be fed to a companion microcontroller (thus saving on the cost of the crystal for the MCU).

3.1.3 Faster RSSI

The ADC clock period can now be decreased from 12 µs to 1.5 µs. Faster channel scanning in multi-channel applications or LBT (Listen Before Transmit) is then possible, as well as ASK demodulation for low data rates.

3.1.4 Digital Signal Output DIGOUT

Pin 17 was previously reserved and not connected, but can now deliver several signals:

- Divided XTAL reference clock
- Carrier detection when RSSI is above predefined TRSSI
- XTO running flag
- 455 kHz signal from the discriminator PLL
- Receive mode flag
- 1 kHz reference clock of the wake-up timer
- Lock detect flag *PLLL* of the main PLL

3.1.5 Charge and Hold Data Slicer Mode

After a *charge* phase, the comparison threshold of the data slicer is stored in the external SKFILT capacitor. This is an additional and very easy way to implement a transparent NRZ UART mode, for instance.

3.2 Low-power Standby Modes

3.2.1 PDN Mode

This is a very low power mode. Only the control interface is powered and I_{CC} is as low as 500 nA typical.

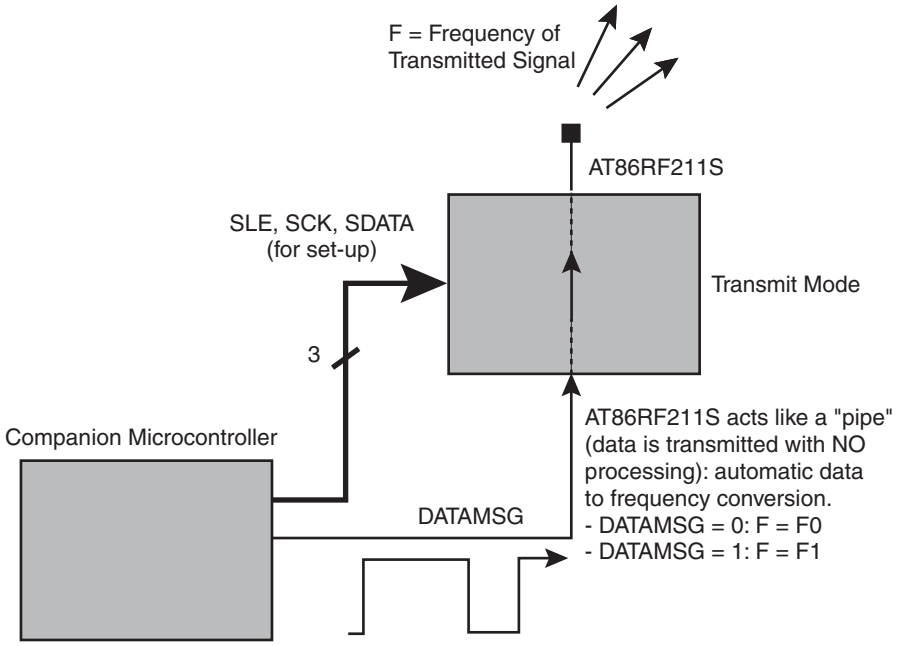
3.2.2 XTAL Running

The XTO remains active for short start-up-time applications at 150 µA, rising to 950 µA typical if the 10.245 MHz signal is buffered on the DIGOUT pin, assuming that the load is 10 pF.

3.3 Asynchronous Transparent Transmit Mode

The chip is set-up by the MCU to act as transmitter. It then acts like a *pipe* in which any data entering DATAMSG is immediately radiated on the antenna. No data is stored or processed on the chip. The transmission is asynchronous.

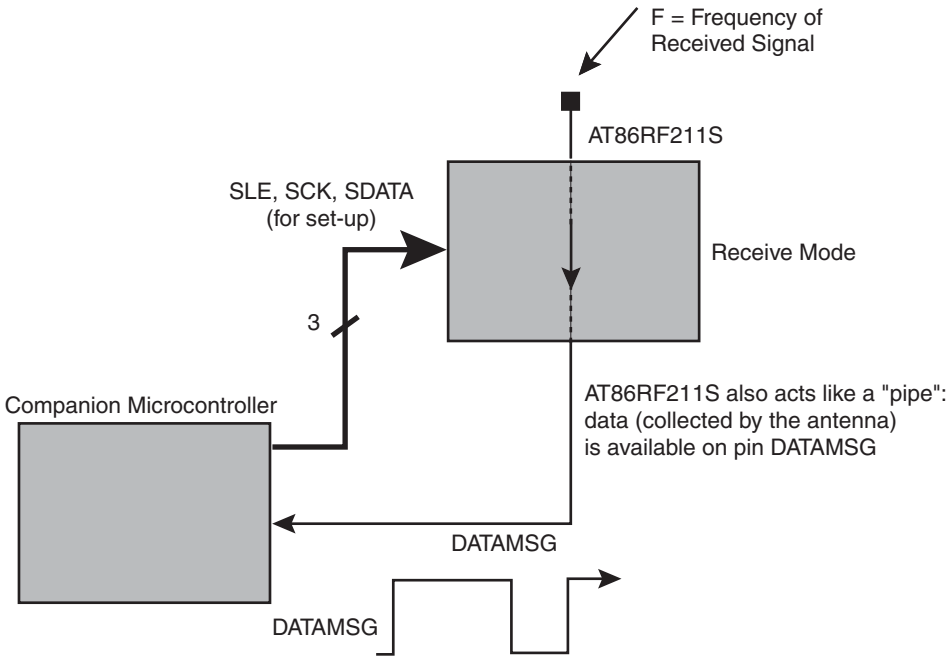
Figure 3-1. Asynchronous Transparent Transmit Mode



3.4 Asynchronous Transparent Receive Mode

Set up by the MCU in receive mode, the AT86RF211S demodulates any data available on the antenna. The data is given on the DATAMSG pin in real-time with no processing and no synchronization clock.

Figure 3-2. Asynchronous Transparent Receive Mode



Using a UART controller is a good solution in this case. NRZ or Manchester coding is possible, but is to be held by the MCU itself.

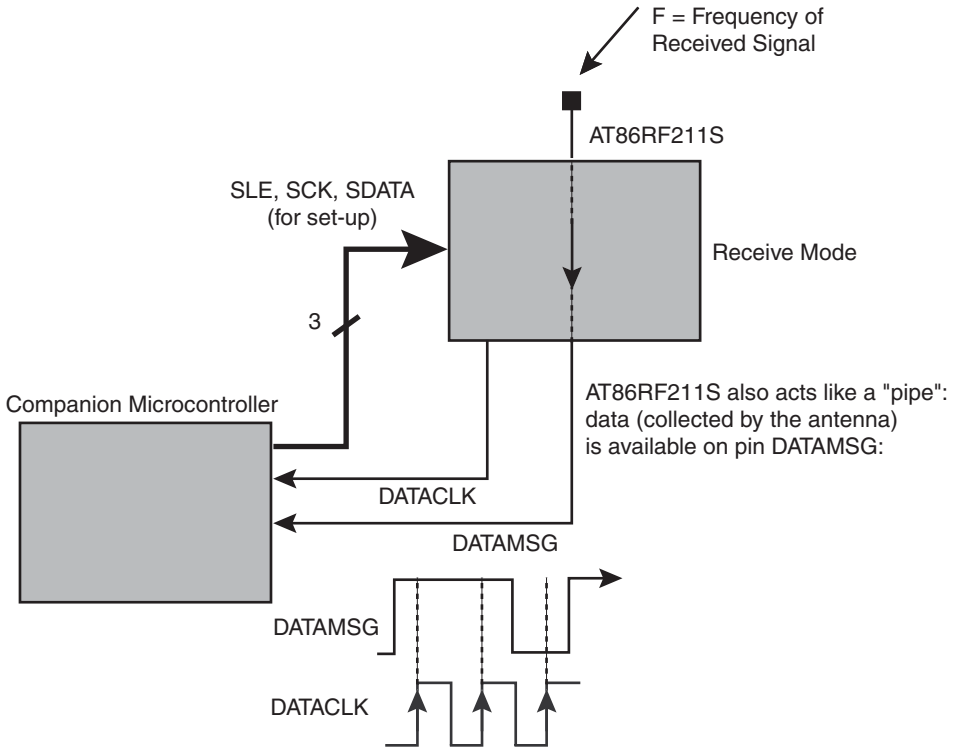
3.5 Synchronous Receive Modes

In addition to the modes described above, the AT86RF211S provides a clock signal that facilitates recovery of data by any low-cost MCU (no UART controller, for instance).

The data can also be synchronized on this clock signal; the benefits of this are:

- Bit decision is done on-chip
- Jitter is removed
- Processing time constraints on the MCU are eliminated

Figure 3-3. Synchronous Receive Mode



3.6 Wake-up Mode

The chip is set-up in a special Rx mode called *sleep* mode. The chip wakes up periodically thanks to its internal timer (in a stand-alone procedure, the microcontroller is in power-down mode), and waits for an expected message defined previously. If no correct sequence is received, the periodic scan continues.

If a correct message is detected, its data field is stored into the AT86RF211S (up to 32 bits) and an interrupt is generated on the WAKEUP pin.

Please refer to Figure 3-3 on page 5.

Figure 3-4. Wake-up Overview

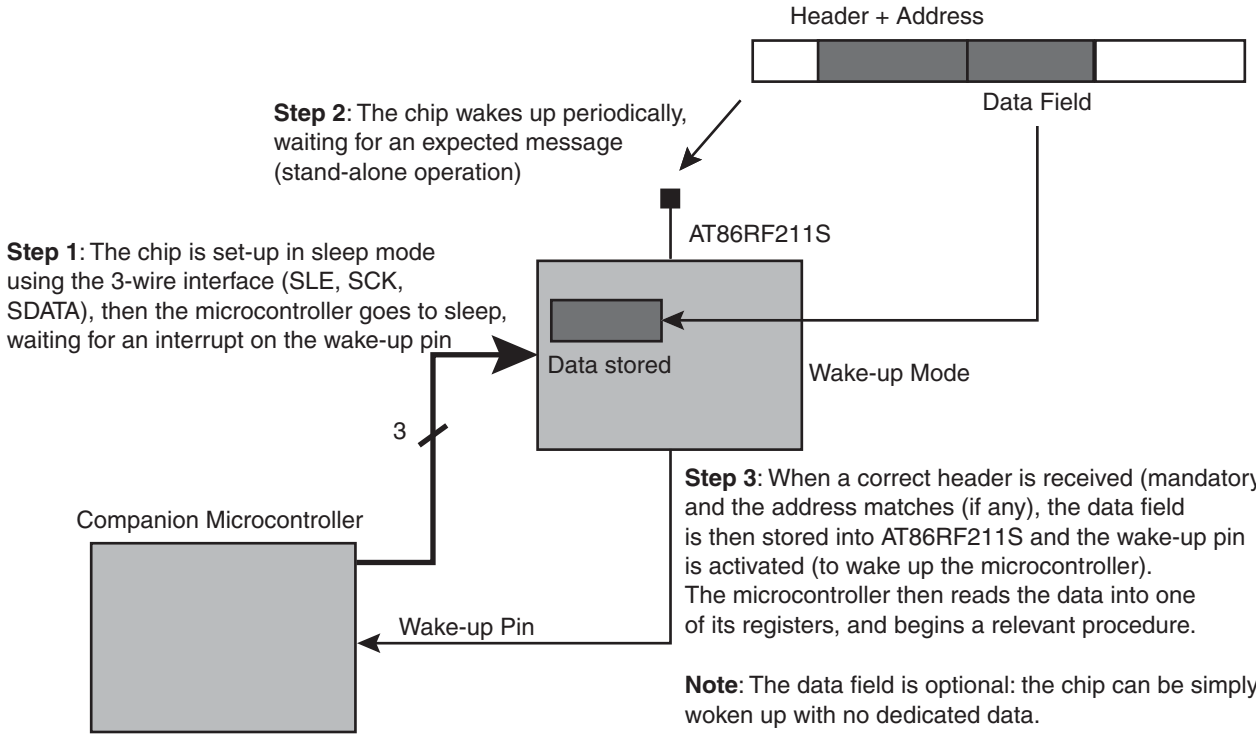
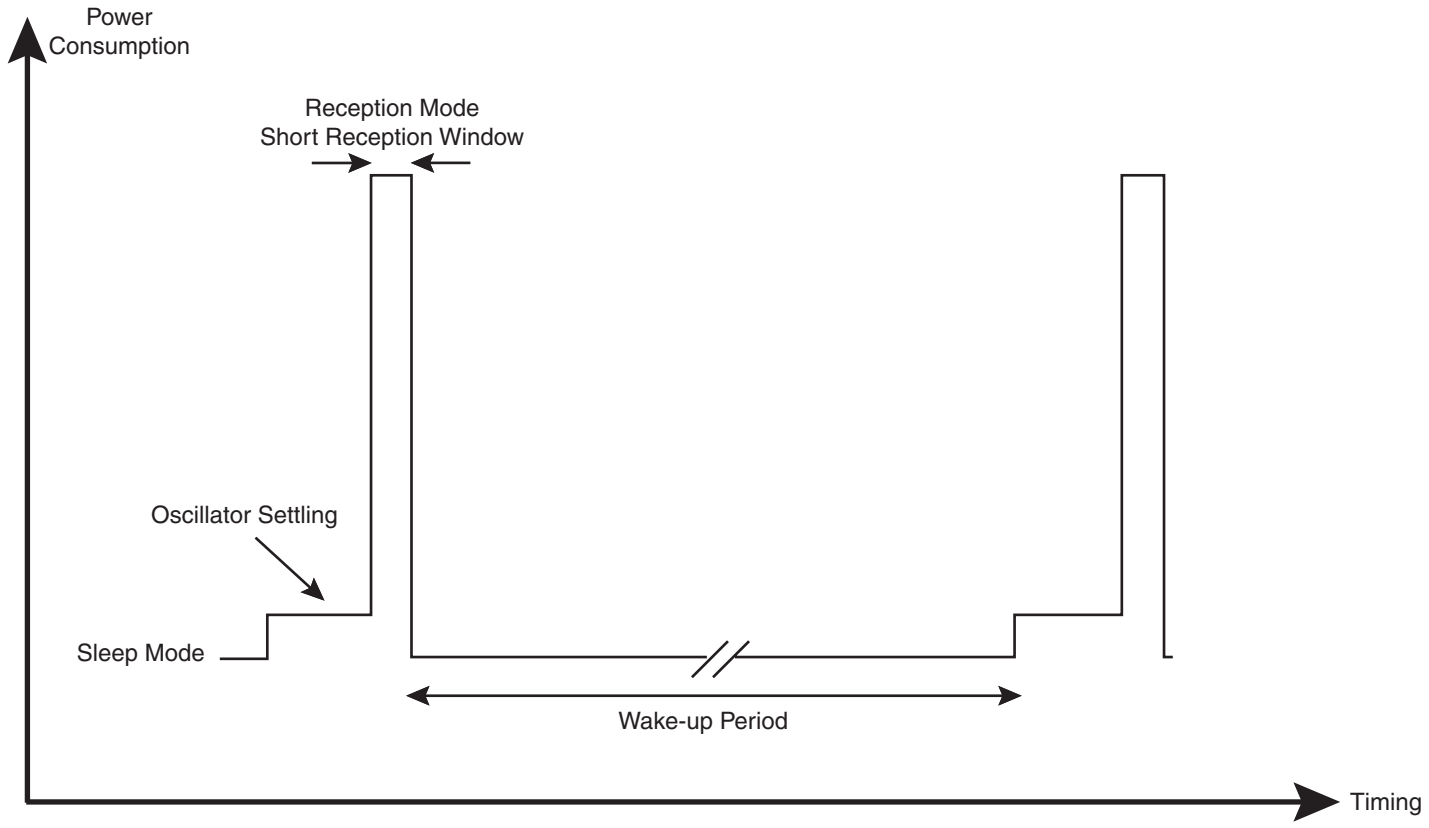
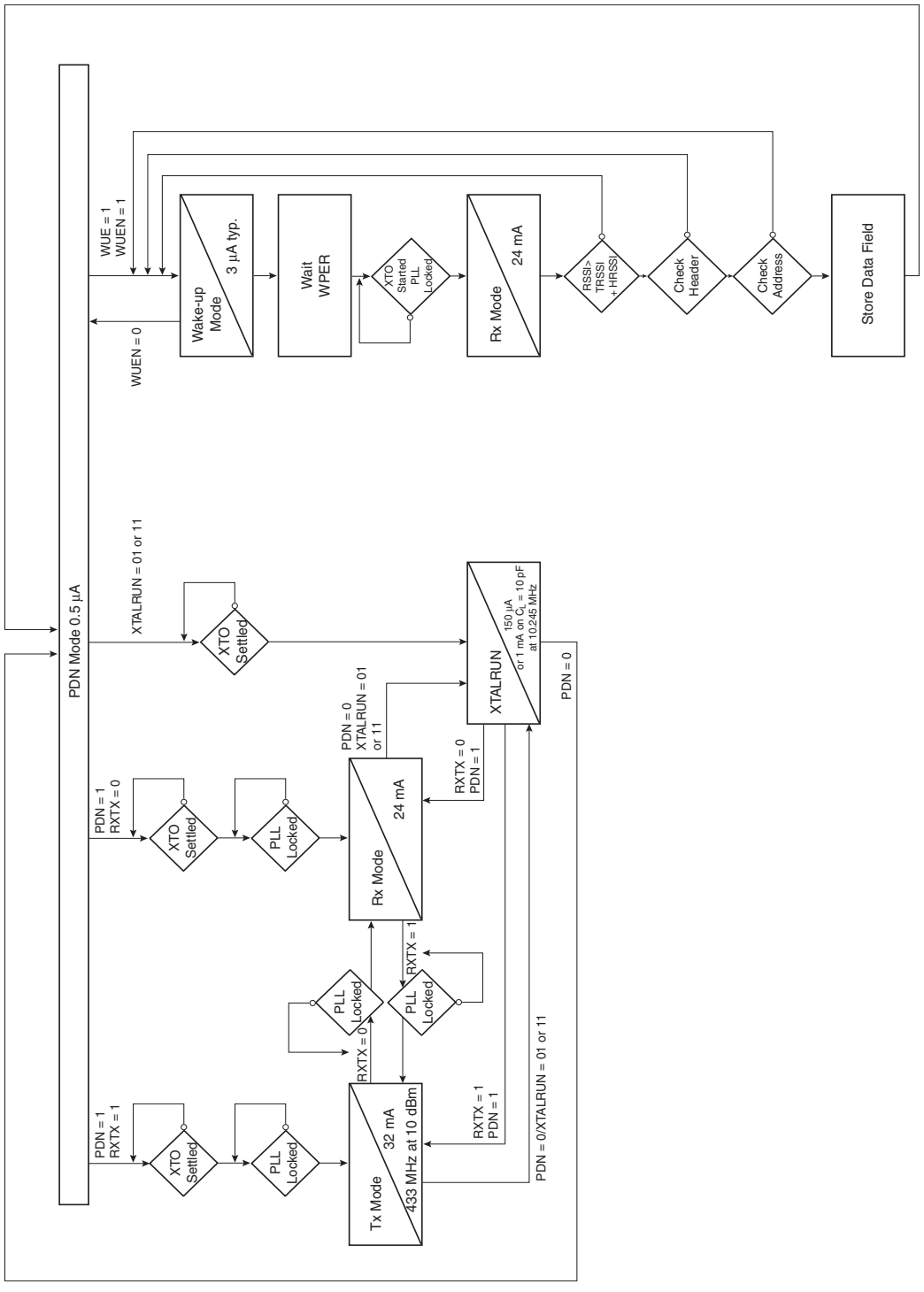


Figure 3-5. Periodical Scan



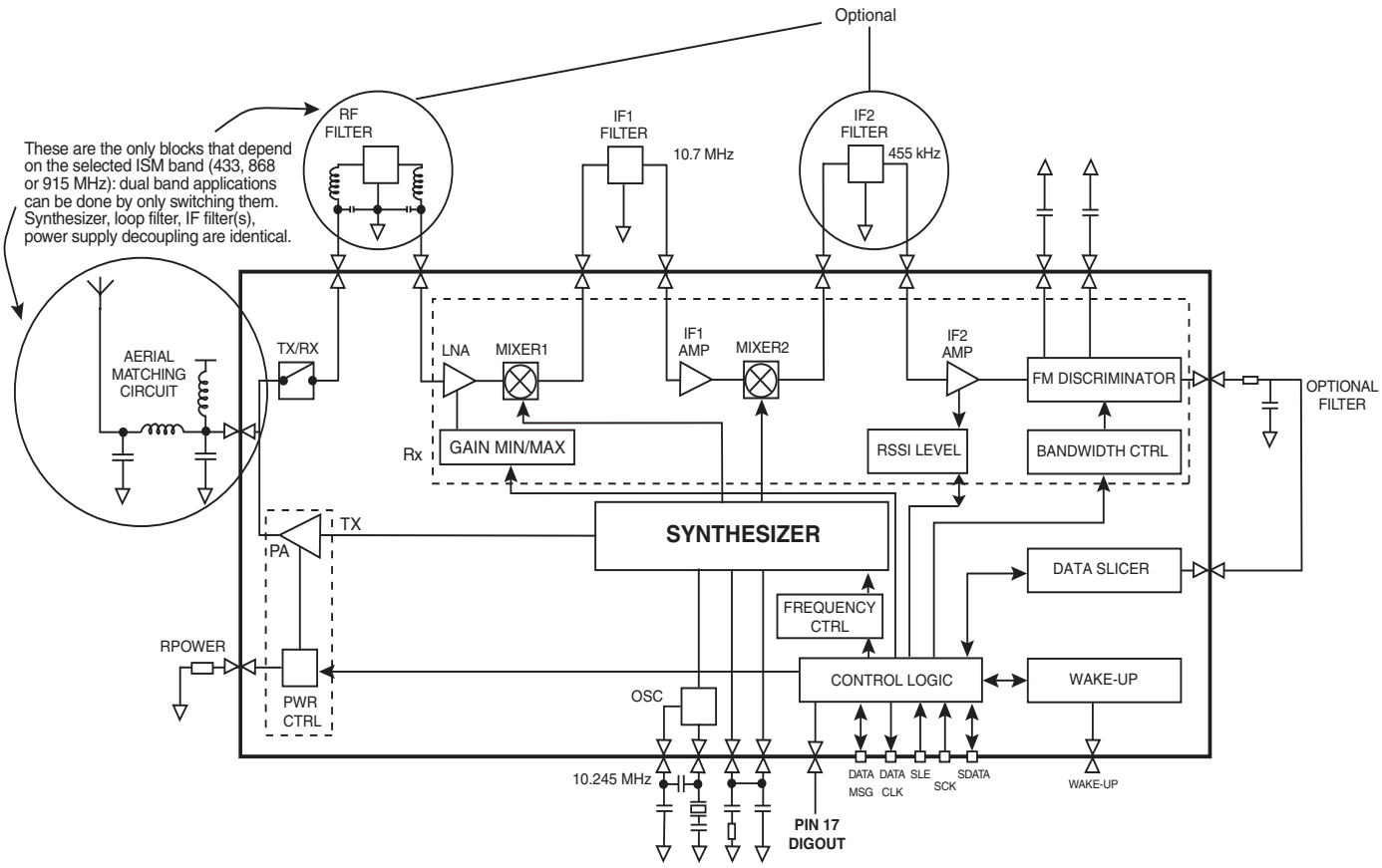
3.7 Selecting the Operating Mode

Figure 3-6. Flowchart



3.8 Block Diagram

Figure 3-7. AT86RF211S Block Diagram



3.9 Pin Description

Table 3-2. Pinout

Pin	Name	Comments	Pin	Name	Comments
1	RPOWER	Full-scale output power resistor	25	SKFILT	Threshold for data slicer
2	TXGND1	GND	26	DSIN	Data slicer input
3	RF	RF input/output	27	DISCOUT	Discriminator output
4	TXGND2	GND	28	IF2VCC	VCC
5	TXGND3	GND	29	IF2GND	GND
6	TXGND4	GND	30	IF2IN	IF2 amplifier input
7	TXVCC	VCC	31	IF2DEC	2.2 nF to ground
8	TXGND5	GND	32	DISCFILT	Discriminator bypass
9	DIGND	GND	33	IF2OUT	IF2 mixer output
10	DIVCC	VCC	34	IF1DEC	4.7 nF to ground
11	DATAMSG	Input/output digital message	35	IF1IN	IF1 amplifier input
12	SLE	Serial interface enable	36	IF1OUT	IF1 mixer output
13	SCK	Serial interface clock	37	AGND	GND
14	SDATA	Serial interface data	38	AVCC	VCC
15	WAKEUP	Wake-up output	39	CVCC2	VCC
16	DATACLK	Data clock recovery	40	CGND2	GND
17	TEST2	In RF211 Mode, do not connect	41	FILT1	Synthesizer output
	DIGOUT	Additional digital features (RF211S mode)	42	VCOIN	Synthesizer input (VCO)
18	EVCC1	VCC	43	EVCC2	VCC
19	EGND1	GND	44	EGND2	GND
20	–	Test pin: do not connect	45	RXIN	LNA input from SAW filter
21	CGND1	GND	46	RXVCC	VCC
22	CVCC1	VCC	47	RXGND	GND
23	XTAL1	Crystal input	48	SWOUT	Switch output
24	XTAL2	Crystal output			

Notes:
1. All V_{CC} pins must be connected in each of the functional modes (Tx, Rx, wake-up, PDN).
2. To be connected:
   Rx mode only, all but 1, 3, 20 and 48
   Tx mode only, all but 15, 20, 25 to 27, 30 to 36, 45 and 48
3. Pin 20 must remain disconnected or connected to ground.
4. To monitor pin 17, refer to “Control Logic” on page 33.

4. Detailed Description

4.1 Frequency Synthesis

4.1.1 Crystal Reference Oscillator

The reference clock is based on a classic Colpitts architecture with three external capacitors.

The bias circuitry of the oscillator is optimized to produce a low drive level for the XTAL. This reduces XTAL aging.

Note: The PLL is only activated when the oscillator is stabilized.

Figure 4-1. Crystal Oscillator Inputs

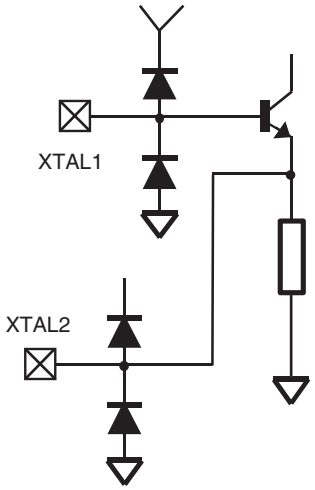
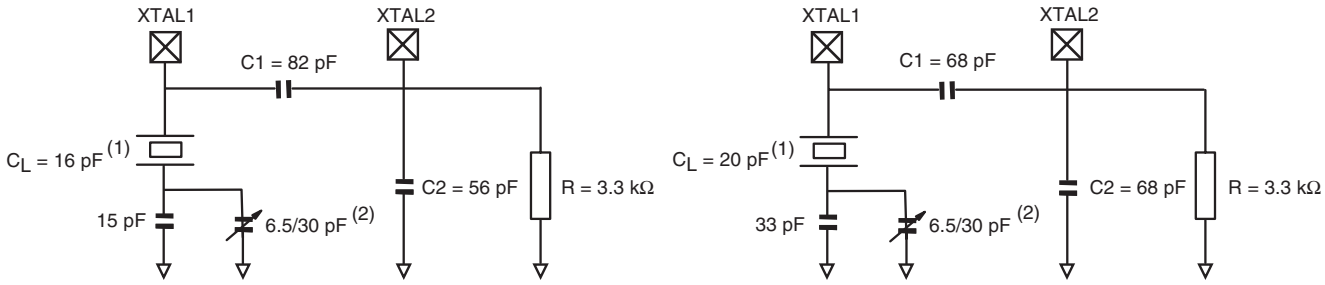


Figure 4-2. Typical Networks



Notes:
1. Various load capacitance (C_L) crystals can be used. If C_L differs from 16 or 20 pF, the surrounding network (C1, C2) must be re-calculated.
2. Thanks to the synthesizer's fine steps (200 Hz), the trimmer capacitor can be replaced by adjusting the software.

Any parallel-mode 10.245 MHz crystal can be used. Its load capacitance must be between 10 pF and 20 pF.

Table 4-1. XTO Frequencies

Reference Clock Frequency	IF1 Frequency	Possible IF1 Bandwidth	Comments
10.245 MHz	10.7 MHz	Up to 380 kHz	Cheap ceramic filters available at 10.7 MHz

It is preferable to add a resistor (3.3 kΩ) between XTAL2 and GND. This decreases the settling time of the XTO to typically 8 ms with an extra power consumption of only a few hundred µA. For applications in which XTO is always *active*, we suggest that you remove this resistor to save battery life.

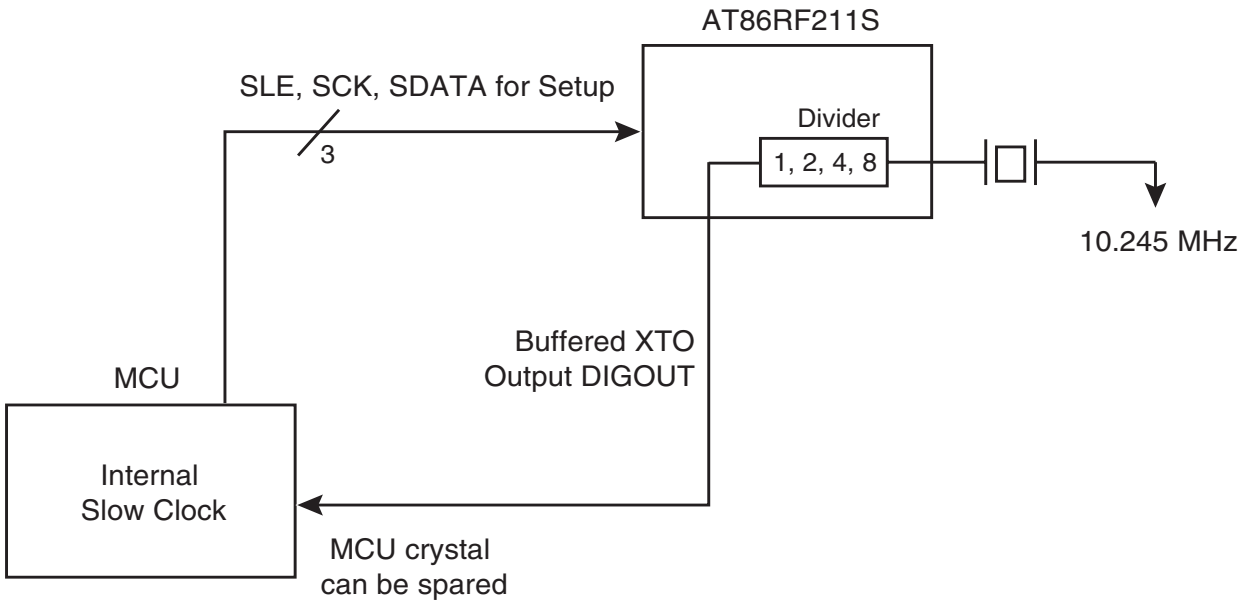
If an external frequency reference is used together with the AT86RF211S, it must be applied to pin 23 XTAL1. A coupling capacitor is recommended if the source is not DC-free qualified. Pin 24 XTAL2 should remain *Not Connected*.

4.1.2 Microcontroller Clocking Capability

The microcontroller can be provided with a calibrated clock, derived from the clock of the AT86RF211S, at 10.245 MHz. Therefore, as detailed in “Control Logic” on page 33, this feature is only activated once and CTRL1[0] is set to *1* to access the additional features.

Through internal buffers and multiplexers, the AT86RF211S can clock its companion controller. The frequency fed to the microcontroller can be adjusted by programming the DTR[20:14] bits, thus activating a set of dividers. This clock’s reference signal is available on the DIGOUT pin.

Figure 4-3. MCU Clocking Capability

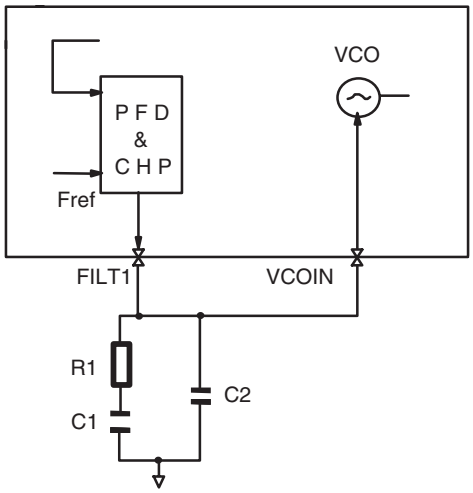


Refer to “Control Logic” on page 33 for more information.

4.1.3 Synthesizer

A high-speed, high-resolution multi-loop synthesizer is integrated. The synthesizer can operate within two frequency bands: 400 to 480 MHz and 800 to 950 MHz. All channels within these two bands can be selected by programming registers F0 to F3. All circuitry is on-chip with the exception of the PLL loop filter. The phase comparison is made thanks to a charge pump topology. The typical charge pump current is 225 µA.

Figure 4-4. Synthesizer Loop Filter Schematic



The PLL loop filter can be designed to optimize the phase noise around the carrier. A few configurations for the application and channel spacing can be suggested.

Figure 4-5. Choosing the Loop Filter Values

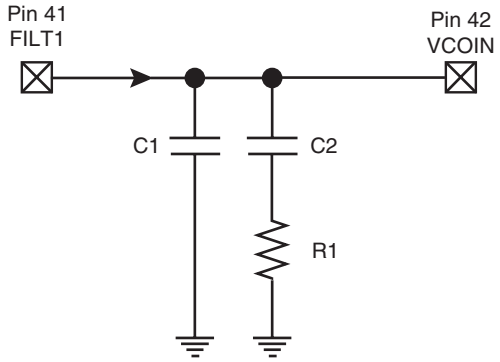


Table 4-2. PLL Loop Filter Examples

Data Rate	C1	C2	R1	Comments
Low	220 pF	2.2 nF	14.7 kΩ	For improvement of phase noise
Medium	560 pF	5.6 nF	3.3 kΩ	Typical
High	100 pF	1 nF	10 kΩ	For high modulation rate

4.2 Receiver Description

4.2.1 Intermediate Frequencies

For selectivity and flexibility purposes, a classic and robust 2 IF super-heterodyne architecture has been selected for the AT86RF211S. To minimize the cost of the external components, the most popular IF values has been chosen that is 10.7 MHz. The impedances of the input/output of the mixing stages have been internally matched to the most common ceramic filter impedances.

Note: IF1 can be any frequency but must match available ceramic filters.

4.2.2 Rx/Tx Switch

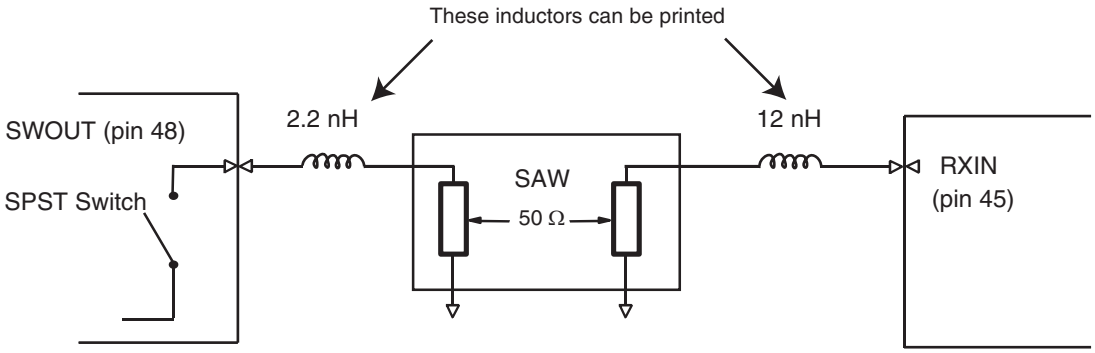
An SPST switch is integrated. In transmission mode, it protects the LNA input from the large voltage swings of the Power Amplifier (PA) output (up to several volts peak-to-peak), which is switched to a high impedance state. The SPST switch is automatically turned *on* or *off* by the Rx/Tx control bit. The insertion loss is approximately 4 dB and the reverse isolation about 30 dB in a 300Ω environment.

4.2.3 Image Rejection and RF Filter

The immunity of the AT86RF211S can be improved with an external band-pass filter.

For example, when using a SAW filter, it must be matched with the LNA input and the output of the switch. The following diagram gives the typical implementation for an
868 MHz application with a 50Ω/50Ω SAW filter.

Figure 4-6. Typical 50Ω SAW Filter Implementation in the 868 MHz Bandwidth



See Table 4-3 on page 14 for precise matching information and the Application Note “AT86RF211S Transceiver for ISM Radio Applications - RF BOM versus. Application Requirements”, for suggested matching filters.

4.2.4 First LNA/Mixer

The LNA mixer exhibits a gain of approximately 17 dB (13 dB if the reduced gain is selected) over a 1.2 GHz bandwidth. Its noise figure is typically 9 dB at 900 MHz (10 dB with a minimum gain) when optimum matching is realized on pin 45.

Table 4-3. Matching Information

Frequency Band	RXIN[1]	SWOUT[2]
433 MHz	35 + j 170Ω	24 - j 43 Ω
868 MHz	37 + j 85 Ω	50 - j 42 Ω
915 MHz	30 + j 85 Ω	50 - j 42 Ω

Notes: 1. RXIN: impedance to be seen by LNA input for NF optimization purposes
2. SWOUT: output impedance of the RF switch

The gain is programmable through the CTRL1[25] register (6 dB attenuation when the minimum gain is selected). The matching choice of the switch and LNA depends mainly on the choice of SAW filter. Usually the in/out impedance of the SAW filter is 50Ω, but other SAW filters can be implemented and the matching network recalculated by using the impedance information in Table 4-3.

The LNA is directly coupled to the first mixer. The inputs and outputs of the LNA and mixer respectively must be connected through a capacitive link because of their internal DC coupling. A SAW or ceramic filter provides such a link.

Figure 4-7. Schematic Input of the LNA

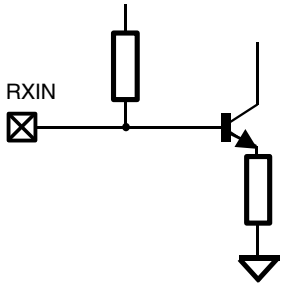
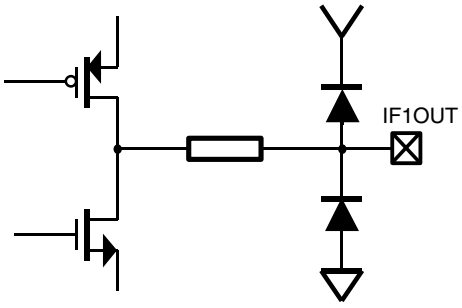


Figure 4-8. Schematic Output of the Mixer



The first mixer translates the input RF signal down to 10.7 MHz.

The local oscillator is provided by the same synthesizer that generates a local frequency 10.7 MHz away from the Tx carrier frequency.

The output impedance of the mixer is 330Ω with a 20% accuracy, so that low-cost, standard 10.7 MHz ceramic filters can be directly driven. Other IFs may be chosen thanks to the mixer's high bandwidth (50 MHz).

4.2.5 IF1 Filtering

A popular ceramic filter is used to reject the second image frequency and provide a first level of filtering.

The IF1 filter can be removed however; it leads to a sensitivity reduction of about 3 dB (the substitution coupling capacitor should be greater than 100 pF).

4.2.6 IF1 Gain and Second Mixer

The input impedance of the IF1 amplifier is naturally 330Ω to match the input filter. The voltage gain, that is the gain at 10.7 MHz added to the conversion gain at 455 kHz, is typically 14 dB when loaded with 1700Ω. The second mixer operates at a fixed LO frequency of 10.245 MHz. Its output impedance is 1700Ω in parallel to 20 pF.

Figure 4-9. IF1 Filtering

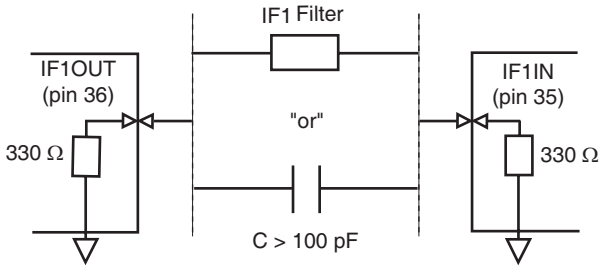


Figure 4-10. Schematic Input of the IF1 Amplifier

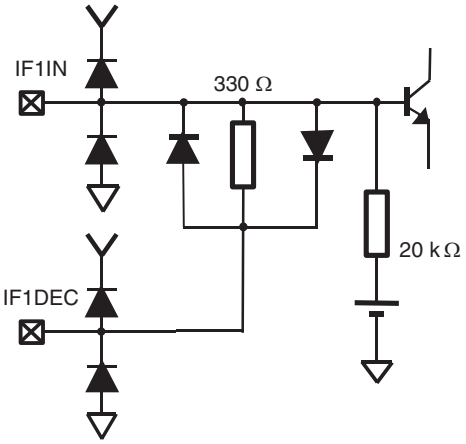
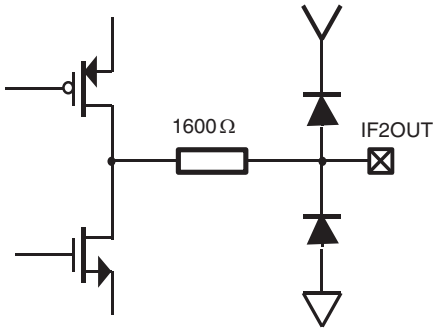


Figure 4-11. Schematic Output of the Second Mixer



4.2.7 IF1 Narrow Bandwidth Filters

IF1 and IF2 filters can be replaced by a single narrowband 10.7 MHz crystal filter. This solution has the following advantages:

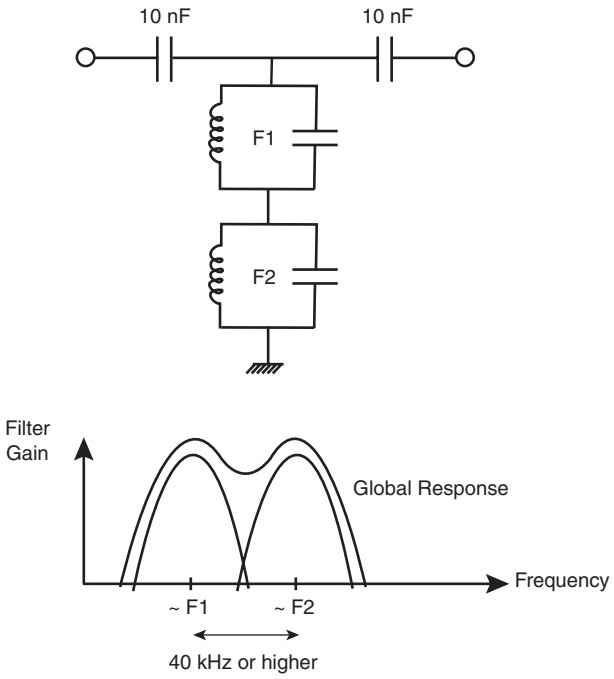
- Only one cheap IF1 filter is used, reducing costs
- Size is optimized
- Selectivity remains good, even if a very narrow 455 kHz filter is not used

4.2.8 IF2 Filtering and Gain

IF2 filtering provides a narrow channel selection. If an IF2 filter is not used, it should be replaced by a coupling capacitor superior to 1 nF, the IF1 filter therefore being the only part achieving the channel selection. Available commercial filters with a 35 kHz bandwidth provide data rates up to 19.6 kbps if crystal temperature drifts are very low.

For faster communication and/or wider channelization, this ceramic filter can be replaced by an LC band-pass filter as suggested in Figure 4-12 on page 16.

Figure 4-12. LC Band-pass Filter



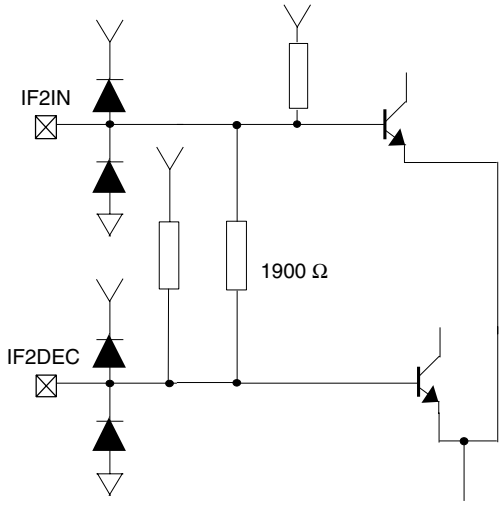
The 10 nF capacitors cut the DC response. The first network has the low cut-off frequency and the second network the high cut-off frequency.

4.2.9 IF2 Amplifier Chain

The input impedance of the IF2 amplifier is 1700Ω. This value permits use of popular filters with an impedance between 1500Ω and 2000Ω. The IF2 amplifier is directly connected to the FSK demodulator. The bandwidth is internally limited to 1 MHz to minimize noise entering the discriminator.

The IF2 amplifier acts like a band pass filter centered at 455 kHz with capacitive coupling between the different stages of the amplifier and mixer. The total voltage gain is typically 86 dB. Thanks to the capacitive coupling, no slow DC feedback loop is needed, thus enabling the IF2 amplifier to be activated rapidly. IF2DEC must be decoupled with at least 2.2 nF.

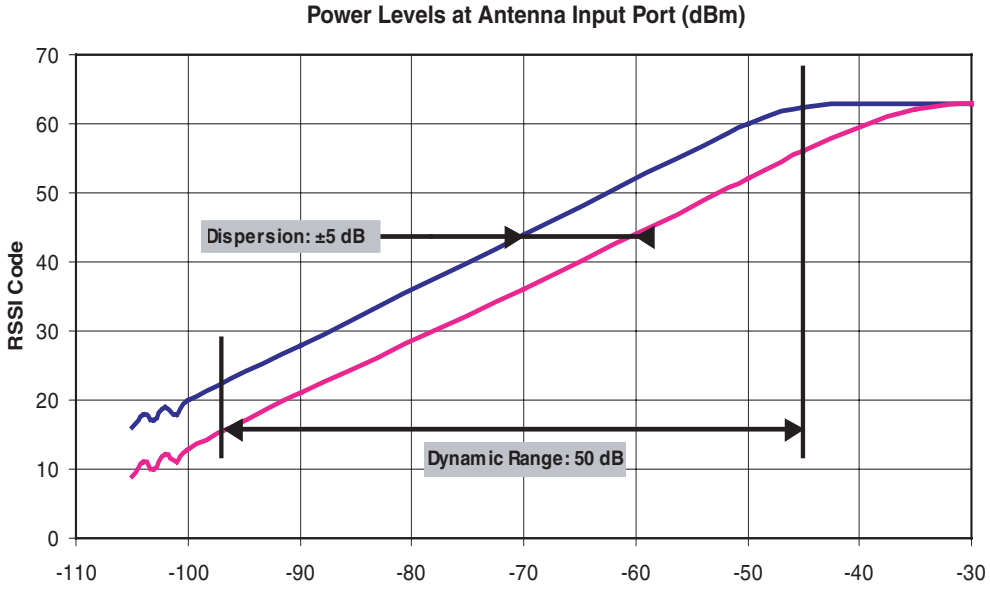
Figure 4-13. Input of the IF2 Amplifier



4.2.10 RSSI Output

The RSSI value can be read as a 6-bit word in the *Status* register. Its value is given in dB and is linear as shown in Figure 4-14 on page 18.

Figure 4-14. Typical RSSI Output (Board Implementation, T = 25°C, V_{CC} = 3V)

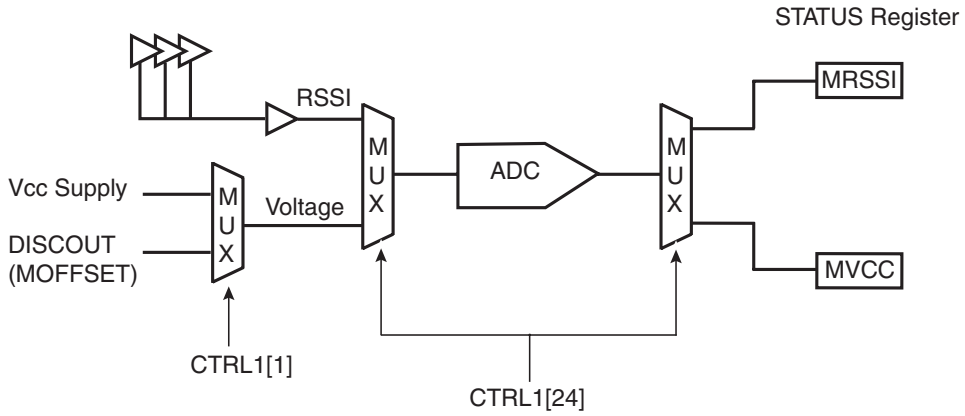


Note: Should the RSSI be required for accurate measurement purposes (for precision above 5 dB), then one value should be measured with a calibrated RF source and stored into the microcontroller during production testing.

The RSSI's dynamic range is 50 dB from a -95 dBm to -45 dBm RF input signal power, over temperature and power supply ranges. The value of the RSSI's LSB weighs approximately 1.3 dB in the linear area. The RSSI value is measured from the IF2 chain.

As the successive approximation ADC is shared by the RSSI, V_{CC} voltage and discriminator offset measurements, some bits of the CTRL1 register must be selected for a correct measurement, as illustrated in Figure 4-15.

Figure 4-15. ADC Converter Input Selection



Note: For voltage measurement, the LSB weighs 85 mV and the reference voltage is 1.25V.
In Reception mode, please remember that both RSSI and V_{CC} measurements use the same ADC.

The clocking period on the AT86RF211S is as short as 1.5 µs. This gives a data readout at least every 100 µs. The clock speed can, however, be reduced (for compatibility reasons for instance).

Table 4-4. RSSI Clocking Options

Mode	Bits RSSICLK	Clock Frequency	Worst Case Settling Time(Note:)	Comments
RF211S only	11	640 kHz	100 µs	Recommended
RF211S only	10	320 kHz	200 µs	
RF211S only	01	160 kHz	400 µs	
RF211 or RF211S	00	80 kHz	800 µs	Compatible with AT86RF211 This is the only clock speed available with the AT86RF211

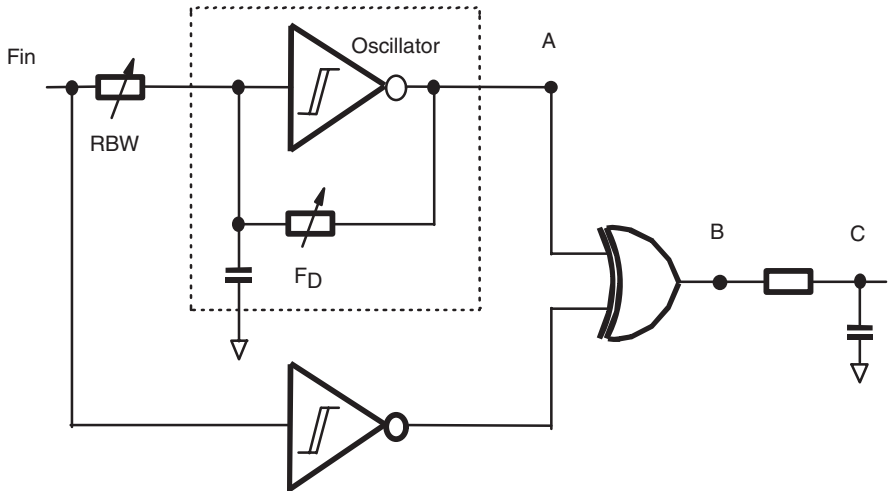
Note: From 0 to 63.

Refer to “Control Logic” on page 33 for additional programming details.

4.2.11 FSK Demodulator

The structure of the FSK demodulator is based on an oscillator.

Figure 4-16. FSK Demodulator Schematic



The oscillator's natural frequency is F_D and it actually oscillates at the Fin frequency. The signal at the oscillator's output (point A in Figure 4-16 is proportional to the frequency difference between Fin and F_D. The XOR function translates the difference into a pulse duty cycle (point B). Thereafter, by low-pass filtering of the signal, a mean voltage of the signal is obtained (point C).

This demodulation's architecture is thereby analog and as the output voltage is proportional to the input frequency, enables transmission of a continuous stream of data of the same value. It is not therefore mandatory to use Manchester encoding; the first bit is correctly demodulated.

The oscillator's feedback resistor controls the center frequency F_D. It is adjusted according to the output of a dummy FSK demodulator driven by a 455 kHz internal reference frequency, which is a division of the reference crystal. The discrete components connected to pin 32 DISCFILT constitute the loop filter of the PLL stabilizing the 455 kHz signal.

The input RBW resistor controls the discriminator bandwidth. Table 4-5 outlines some possible choices:

Table 4-5. Discriminator Bandwidth Selection

Name	Applicable Mode	Maximum FSK Deviation (kHz)	Conversion Gain at 2.4V (mV/kHz)	Conversion Gain at 3V (mV/kHz)	Bit Configuration	Comments
NDB	RF211	±25 kHz	28	34	FSKBW = 0	Compatible with AT86RF211
	RF211S				DISCRANGE = 11	
SDB	RF211	±50 kHz	14	17	FSKBW = 1	
	RF211S				DISCRANGE = 10	
MDB	RF211S	±75 kHz	9	11	DISCRANGE = 01	AT86RF211S only
WDB	RF211S	±125 kHz	5	6.5	DISCRANGE = 00	

Note: Please refer to the Application Note "Data Demodulation and Crystal Selection for the AT86RF211S".

Given below are examples of possible configurations in the 600 kHz-wide 868 to 868.6 MHz European sub-band, in which the European standard EN 300 220 is applicable:

- SDB: 4 channels at 19.200 bps
- MDB: 2 channels at 5.000 bps
- WDB: 1 channel at 100.000 bps

For further details, please refer to the Application Note “Data Demodulation and Crystal Selection for the AT86RF211S”.

4.2.12 Data Slicer

The analog signals at the discriminator’s output (DISCOUT, pin 27) are converted into CMOS level data by a high resolution comparator called a *data slicer*.

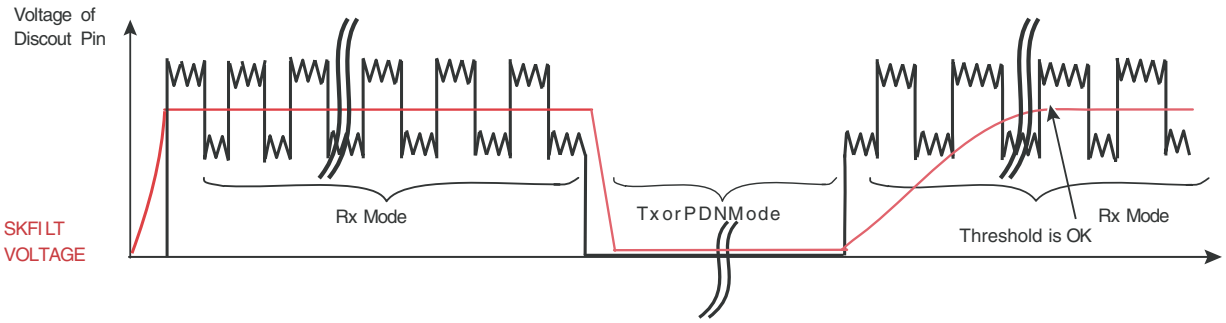
The data slicer has a reference for its comparator that can be chosen using CTRL1[4]. The reference sets the comparator’s comparison level. One option is to extract the average value of the demodulated signal on the SKFILT pin (pin 25), described below as the *external* mode. The other option is to set an absolute value for this reference, described below as the *internal* mode.

4.2.12.1 External Mode

The external mode takes the average value of the demodulated signal as the comparison level for the comparator. There must be sufficient transitions in the message to ensure that the average value remains between the 0 and 1 levels. Manchester encoding can be used in this mode as well as DC-free encoding schemes. The choice of SKFILT capacitor value is a trade-off between the maximum duration of a constant bit (whether 0 or 1) and the maximum allowed settling time to charge this capacitor after power-up.

When switching from Rx mode to Tx mode or PDN mode: the pin 25 is shorted to ground, with an internal switch. The result is a fast discharge of SKFILT capacitor. Switching back to Rx mode: as the SKFILT cap has been fully discharged, the user should take into account the relevant time to be ready for receiving data. For instance, a preamble might be received to settle the comparison threshold at the right level.

Figure 4-17. Example of Rx Timing with Discharge

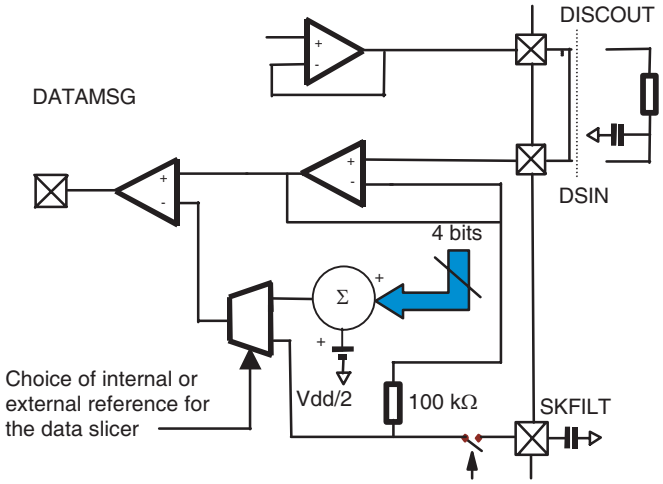


Notes:
1. It is possible to *hold* the level on SKFILT capacitor thanks to the *charge and hold* capability that has been implemented on the AT86RF211S. Please contact the technical support for further information.
2. Internal data slicer threshold can also be implemented. In this mode, the comparison level is generated internally with a DAC. Please refer to Section 4.2.12.2 and the Application Note, “Data Demodulation and Crystal Selection for the AT86RF211S” (reference 5418) to implement this in the best way.

4.2.12.2 *Internal Mode*

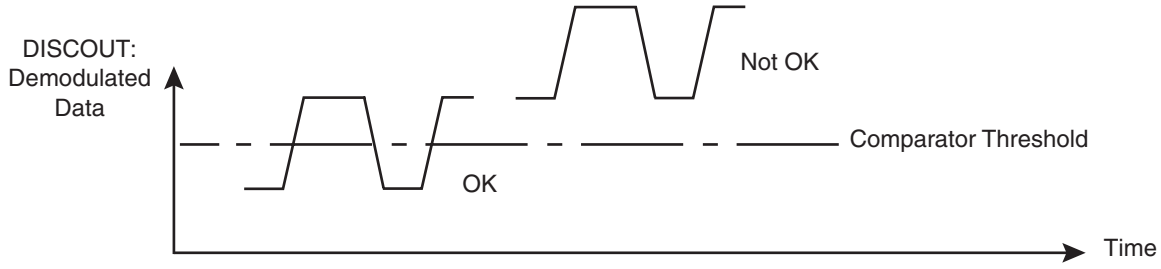
The internal mode uses the output of a DAC as the comparison level. Once this threshold has been correctly set, an *absolute* data slicing of the demodulated signal is possible; there is no need for a DC-free modulation scheme (it is possible to send a 0 or a 1 infinitely).

Figure 4-18. Data Slicer Schematics



To operate this way, one must make sure that the 0 and 1 levels at the output of the discriminator appear *on both sides* of the comparison level in order for the decision to be made properly.

Figure 4-19. Data Slicing Parameters Setup Example



To set the discriminator and data slicer accordingly:

- The output DC level of the discriminator DISCOUT can be measured (using the A/D embedded converter)
- The DC level can be shifted up or down at the output of the discriminator through the DTR[1:0] bit:
  - DTR[1] = 1: +180 mV + 77 × (V_{CC} - 2.4V)
  - DTR[0] = 1: -180 mV - 77 × (V_{CC} - 2.4V)
- The comparison threshold can be tuned around V_{CC}/2 through the DTR[5:2] bit. 16 levels are possible, with an LSB equal to 15 mV per volt of supply voltage. V_{CC}/2 corresponds to DTR[5:2] = 0111, and the RESET value is 1000.

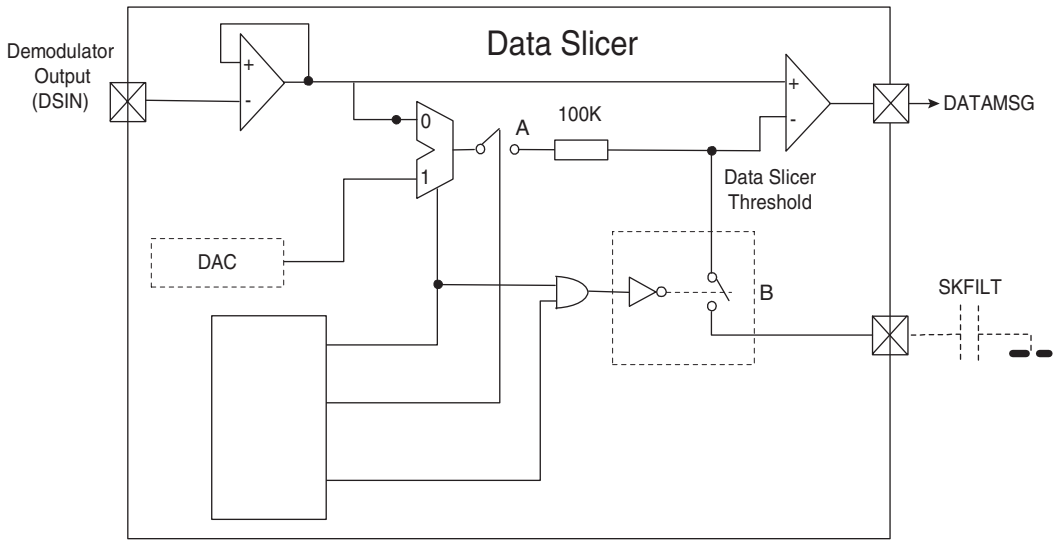
These procedures are made automatically by the software. Refer to the Application Note “Data Demodulation and Crystal Selection with the AT86RF211S” reference 5418.

4.2.12.3 Charge and Hold Mode

After a single *charge* phase (for example, during a preamble), the comparison threshold of the data slicer is stored in the external SKFILT capacitor. Once the threshold is stored, the bits that follow can be directly demodulated. Please contact e2v for further information.

.

Figure 4-20. Charge and Hold Mode Schematics



Note: This mode is very similar to the external mode and differs only in that the SKFILT voltage value can be held.

As a subdivision of the external mode (previously described) the Charge and Hold allows the following settings:

- Charge: switches A and B are closed. The SKFILT capacitor charges through a 100 kΩ resistor. An efficient charge or pre-charge can be done on white noise or on a preamble.
- Pre-charge: to obtain a faster charging time, it is possible to keep the SKFILT capacitor charged to $V_{CC}/2$. To do so, the user shall use the charge mode while selecting the internal reference for the data slicer.
- Hold: A and B are opened so as to keep SKFILT charged. The leakage current is very low, enabling receipt of a long set of 0 or 1, while maintaining an appropriate data slicer threshold.

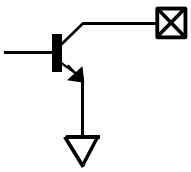
Please refer to the Application Note “Data Demodulation and Crystal Selection for the AT86RF211S” reference 5418, for details.

4.3 Transmitter Description

4.3.1 Power Amplification

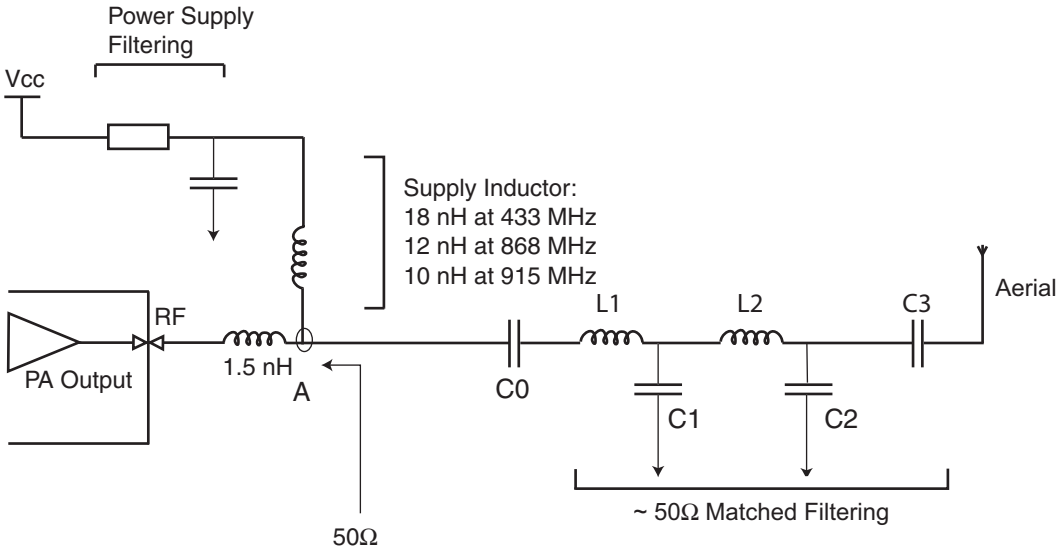
The Power Amplifier has been built to deliver more than 14 dBm (25 mW in the three most common frequency bands). This power level is intended to be measured on the aerial port with a correct output matching network. Note that correct calculation of the matching network guarantees optimal power efficiency.

Figure 4-21. Output of the Power Amplifier



The PA must be correctly matched to deliver the best output power and current consumption. Figure 4-22 on page 24 gives an example of the typical recommended output network in the 868 MHz band.

Figure 4-22. Output Matching of the Power Amplifier



Note: The filter is designed to meet relevant regulations. Refer to the Application Note "AT86RF211S Transceiver for ISM Radio Applications - RF BOM versus Application Requirements" reference 5305, for details.

This network has the benefit of filtering the output signal's harmonic levels; hence it can be designed to meet a particular regulation.

It is mandatory to implement low impedance grounding techniques. Excessive inductor values to ground can not only limit the PA output voltage swing, but can also trigger RF instability. Board design is vital to avoid parasitic loss when a high output power is needed (a direct short connection to a single low impedance ground plane).

An Automatic Level Control (ACL) loop is integrated to minimize the PA's sensitivity to temperature, process and power supply variations. For instance, at 85°C, the output power is approximately 2 dB less than at 25°C. At -40°C, the output power is higher than at 25°C. The ALC is controlled by a generated current as shown in Figure 4-23 on page 25.

Figure 4-23. ALC of the Power Amplifier

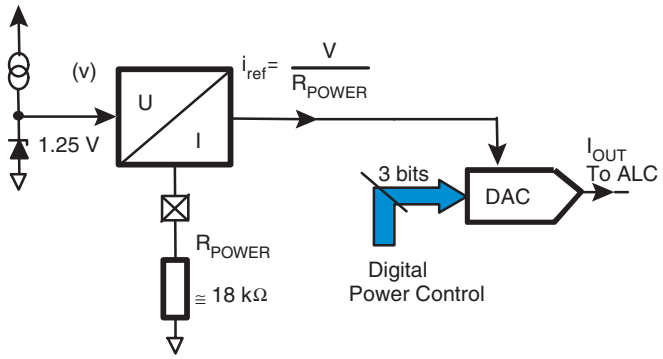
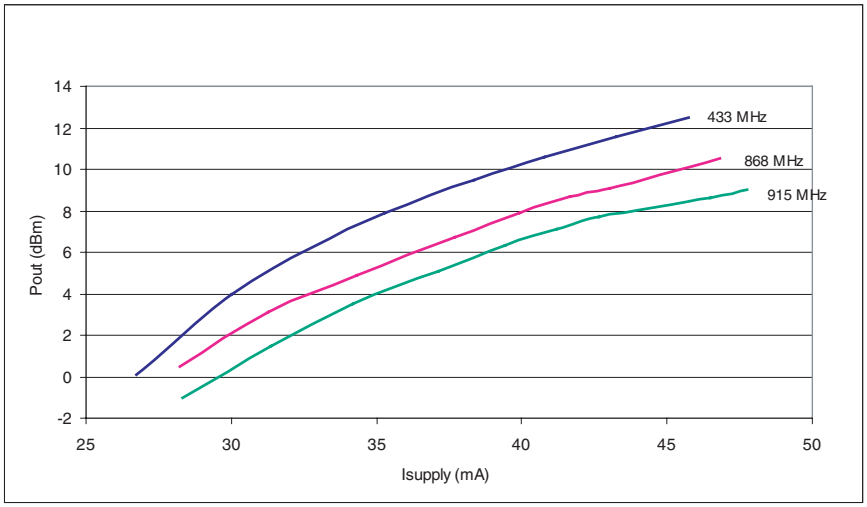


Figure 4-24. Typical Output Power of the PA for T = 25°C and V_{CC} = 3V



4.3.2 Hardware Control

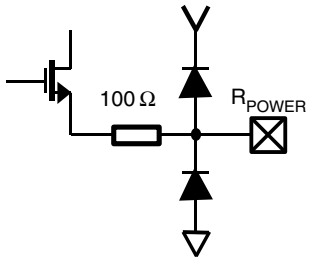
R_{POWER} sets the maximum power delivered by the internal Power Amplifier by limiting the current it sinks. The PA performs well if R_{POWER} ranges from 10 KΩ (highest power level) to 33 kΩ (lowest power level).

Table 4-6. Power Levels According to R_{POWER}

	Typical Output Power (dBm)		
RPOWER	433 MHz	868 MHz	915 MHz
5.6 kΩ	+16	+15	+14
18 kΩ	+13	+10	+9
33 kΩ	+9	+8	+7

Note: Figures are given for V_{CC} = 3V, temperature = 25°C, TXLVL = 111, best matching.

Figure 4-25. R_{POWER} Output Schematic



Note: Keeping the PA output matched guarantees maximum power efficiency.

4.3.3 Software Control

The power can then be adjusted from the value set by R_{POWER} down to a maximum of 12 dB below this value, by programming bits 6 to 8 of the CTRL1 register. Eight levels are therefore digitally selectable with a variation of the output power. The minimum regulated output power is set to -10 dBm.

Table 4-7. Power Level Software Control

TXLVL (CTRL1)	P_{out} at 433 MHz (dBm)	P_{out} at 868 MHz (dBm)	P_{out} at 915 MHz (dBm)
000	0	-2	-3
001	+4	0	0
010	+6	+3	+2
011	+8	+5	+4
100	+10	+7	+5
101	+11	+8	+7
110	+12	+9	+8
111	+13	+10	+9

Note: Unless otherwise specified, typical data given for R_{POWER} is 18 kΩ, T = 25°C, V_{CC} = 3V.

4.4 Digital Features

4.4.1 Clock Recovery Function

4.4.1.1 Preamble

The clock recovery algorithm in the AT86RF211S has been improved and the new algorithm must be used. To use the new algorithm:

1. Put the device into RF211S mode: ADDFEAT = CTRL1[0] = 1
2. Select the improved algorithm by setting bit NEWDATACLK = DTR[13] = 1

For compatibility purposes *only*, it is nevertheless possible to run the former algorithm, (the algorithm of the AT86RF211). This algorithm is automatically activated in the RF211 mode or if bit NEWDATACLK is kept in reset state in RF211S mode.

It is now possible, in RF211S mode only, to inhibit the clock recovery when RSSI is too low, leaving the MCU in sleep mode. This is performed by the DATACLKEN bit in the DTR register.

4.4.1.2 Algorithm Overview

The clock recovery function is activated by setting the DATACLK bit of the CTRL1 register to 1.

The clock recovery function provides the data clock on the DATACLK pin, synchronized on the received data flow. The targeted position for the rising edge of the clock is the middle of the data bit, eliminating synchronization problems and facilitating readout by the microcontroller.

The clock's recovery mechanism is based on the generation of a basic data clock with a period given by the DATARATE of CTRL2 with a step of approximately 100 ns. This basic clock is synchronized on the received data flow. The phase correction step is fixed by DATATOL of the CTRL2 register (steps of approximately 100 ns also).

Therefore, DATATOL can:

- Compensate for the difference between the read data rates from the transmitter and the receiver (fixed by DATARATE).
- Allow fast initial synchronization of the data clock, avoiding bit transition times, and converge towards the middle of the bit.
- Keep the appropriate data rate (no additional and no removed bit) when noisy data with a bad bit transition position arrives.

The best DATATOL value is a a balance of the above three points.

  – If the tolerance is too high, the rate value is reached earlier, and could be unstable (too big a step).
  – If the tolerance is too low, it could be difficult to catch up with the data and the function may be lost.
  – The tolerance is able to compensate for the difference of datarate generators between Rx and Tx.

The synchronization mechanism is explained by the chronogram in Figure 4-26. Synchronization is done for the first bit. In worst case scenarios, when the data and clock arrive at the same time, synchronization begins at the second bit. Notice that the DATACLK signal is available as soon as the DATACLK bit is programmed, regardless of the state of the DATAMSG pin.

The programmed data rate enables the creation of a basic clock at the programmed DATARATE frequency at the beginning of reception. The clock is then shifted if necessary from the tolerance value,

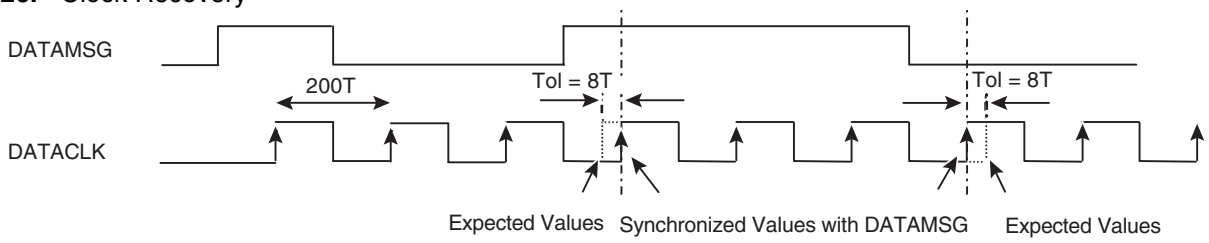
depending on the previous DATA transition; the clock is moved later or sooner, depending on the gap between CLOCK and DATA.

For example:

If DATARATE = 50 kbps, which is equivalent to a duration of 200 × T for 1 bit, with T = 100 ns = base clock period.

If DATATOL = 4% × DATARATE = 8 × T.

Figure 4-26. Clock Recovery



4.4.2 Data Rate Programming

This value must only be programmed when the DATA clock is needed on the chip's DATACLK output pin.

The DATA rate can be programmed from 1 to 100 kbps with 14 bits of the CTRL2 register.

DATARATE is the period of the data rate and can be programmed with a resolution given by the crystal oscillator period:

- 10.245 MHz oscillator, period = T = 97.6 ns

Table 4-8 provides examples of data rate values with the 10.245 MHz oscillator:

Table 4-8. Data Rate Values with an 10.245 MHz Oscillator

DATARATE[13:0]	Rate	Period
$(102)_{10}$	100 kbps	1 bit ~ 102 × T
$(205)_{10}$	50 kbps	1 bit ~ (205-1) × T
$(\text{even number})_{10}$		1 bit ~ (even number) × T
$(\text{odd numbers})_{10}$		1 bit ~ (odd numbers -1) × T
$(534)_{10}$	19.2 kbps	1 bit ~ 534 × T
$(1024)_{10}$	10 kbps	1 bit ~ 1024 × T
$(1067)_{10}$	9.6 kbps	1 bit ~ (1067-1) × T
$(2135)_{10}$	4.8 kbps	1 bit ~ (2135-1) × T
$(4269)_{10}$	2.4 kbps	1 bit ~ (4269 -1)× T
$(10246)_{10}$	1 kbps	1 bit ~ 10246 × T

4.4.3 Data Tolerance Programming

Table 4-9 provides some examples of tolerance values with tolerance = 4% × DATARATE.

Table 4-9. Tolerance Values with Tolerance Equal to 4% × Data Rate

DATATOL[7:0]	Rate	Period
$(4)_{10}$	100 kbps	1 bit ~ 4 x T
$(8)_{10}$	50 kbps	1 bit ~ 8 x T
$(vv)_{10}$		1 bit ~ vv x T
$(41)_{10}$	10 kbps	1 bit ~ 41 x T
$(43)_{10}$	9.6 kbps	1 bit ~ 43 x T
$(85)_{10}$	4.8 kbps	1 bit ~ 85 x T
$(171)_{10}$	2.4 kbps	1 bit ~ 171 x T
$(410)_{10}$	1 kbps	1 bit ~ 410 x T

4.4.4 Recommended Values

You can select DATATOL. This parameter decides upon:

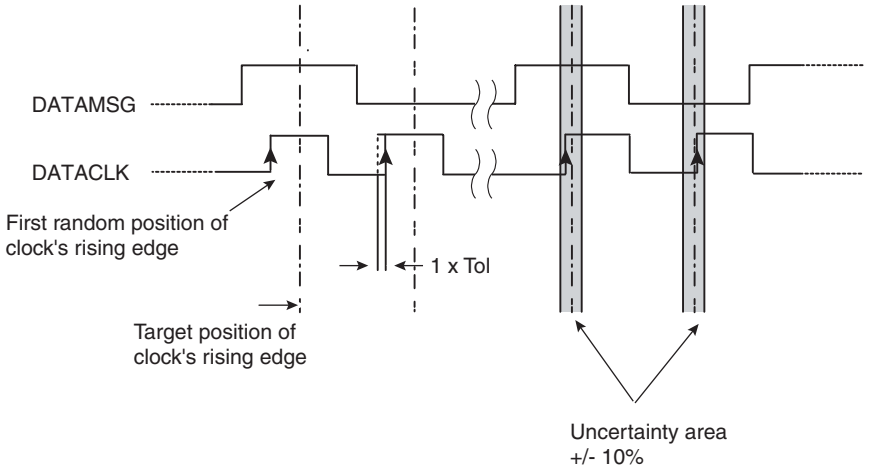
- The stability of the clock and its jitter
- The number of bits that are required to synchronize the data

Table 4-10. Clock Recovery Recommended Settings

DATATOL	Maximum Number of Preamble Bytes for Sync(Note:)	From…	To…
2%	4 bytes of $55	The duty cycle time of the demodulated preamble is better than 25 to 75%	The clock is settled at the center of the bit with an accuracy of ±10%
4% - recommended	2 bytes of $55		
8%	1 byte of $55		

Note: The clock's "settling time" depends on the random first occurrence of the clock edge compared to the data edge. This means that in most cases, the number of bits required to obtain synchronization will be far smaller.

Figure 4-27. Clock Recovery Target Position



Note: Use the above settings to ensure a good trade-off between the settling time and the jitter of the clock. The clock remains correct, regardless of the number of transitions in the received stream, as long as the reference clocks of Tx and Rx are the same. Example: if D (Rx - Tx) = 20 ppm, the clock is centered at ±20% for at least $0.2/20.10^{-6}$ = 10 Kbits.

4.4.5 Data Resynchronization

As the AT86RF211S can provide a synchronization signal together with the demodulated data on pins DATAMSG and DATACLK, it is also possible to *reshape* the data received.

In resynchronization mode the signals provided to the companion MCU are filtered; the jitter of the generated clock remains the only concern. The bit decision is then fully performed on the chip, thus removing real-time constraints on the MCU. This facilitates the data transfer, independently of the chosen protocol (UART, USART, SPI etc.)

Note: Resynchronizations add a short latency time on the data; this does not affect transmission.

Figure 4-28. Benefits of Resynchronization

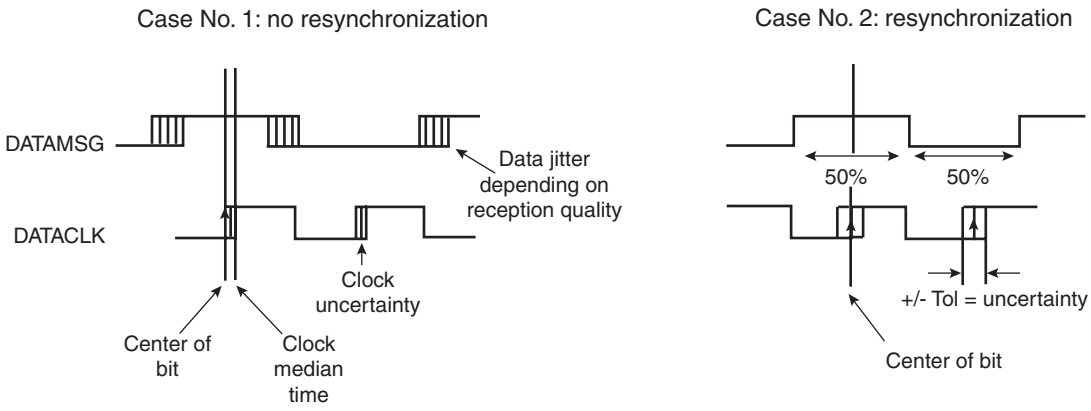


Figure 4-28 shows that the data provided to the MCU has a perfect bit period, with the synchronization clock centered on the half bit.

4.4.6 PLL Lock Detect

The PLL lock function uses up and down signals from the internal phase detector. These signals are analyzed synchronously with a clock frequency, depending on the LDCK bit programming:

- N0LD2 triggers the PLL's unlock condition
- N1LD2 triggers the PLL's lock condition

Except in cases where compatibility with the former AT86RF211 is mandatory, please use the PLL lock bit in RF211S mode.

We recommend using the default values indicated in Table 4-19 on page 40.

4.5 Wake-up Mode

The data rate (in bps) and the decimal value to be coded in the register are related by the equation:

$$\text{RATE} = \frac{64000}{rate(bps)}$$

The following table gives the programming values of commonly used rates:

Table 4-11. Programming Values of Commonly Used Rates

Rate	WUR RATE
1200 bits/sec	$(533)_{10}$
2400 bits/sec	$(267)_{10}$
4800 bits/sec	$(133)_{10}$
9600 bits/sec	$(67)_{10}$

4.5.1 WPER Programming

WPER can be set from 10 ms to 328 seconds with an accuracy of ±20%. A 10 ms period clock is used for generating this period.

Bits 8 and 7 give a period multiplication factor of 1, 16 or 256 (with two serial by 16 clock prescalers).

Bits 6 to 0 give the number of cycles of the divided clock from 1 to 128 (counter).

Table 4-12. Wake-up Period Programming

WPER[8:0]	WPER[8:7]	WPER[6:0]	Period	Prescaler	Comments
$(000)_{16}$	$(00)_2$	$(00)_{16}$	10 ms	1	1 × 10 ms
$(001)_{16}$	$(00)_2$	$(01)_{16}$	20 ms	1	(1+1) × 10 ms
–	$(00)_{10}$	$(vv)_{10}$	–	1	(vv + 1) × 10 ms
$(07e)_{16}$	$(00)_2$	$(7e)_{16}$	1270 ms	1	1 × 1270 ms
$(07f)_{16}$	$(00)_2$	$(7f)_{16}$	1280 ms	1	1 × 1280 ms
$(101)_{16}$ or $(081)_{16}$	$(10)_2$ or $(01)_2$	$(01)_{16}$	170 ms	16	([16 × 1] +1) × 10 ms
$(102)_{16}$ or $(082)_{16}$	$(10)_2$ or $(01)_2$	$(02)_{16}$	330 ms	16	([16 × 2] +1) ×10 ms
–	$(10)_2$ or $(01)_2$	$(vv)_{10}$	–	16	([16 × vv] +1) × 10 ms
$(17e)_{16}$ or $(0fe)_{16}$	$(10)_2$ or $(01)_2$	$(7e)_{16}$	20.2 sec	16	([16 × 126] +1) × 10 ms

Table 4-12. Wake-up Period Programming (Continued)

WPER[8:0]	WPER[8:7]	WPER[6:0]	Period	Prescaler	Comments
$(17f)_{16}$ or $(0ff)_{16}$	$(10)_2$ or $(01)_2$	$(7f)_{16}$	20.3 sec	16	([16 × 127] +1) × 10 ms
$(181)_{16}$	$(11)_2$	$(01)_{16}$	2.57 sec	256	([256 × 1] +1) × 10 ms
$(182)_{16}$	$(11)_2$	$(02)_{16}$	5.13 sec	256	([256 × 2] +1) ×10 ms
–	$(11)_2$	$(vv)_{10}$	–	256	([256 × vv] +1) × 10 ms
$(1fe)_{16}$	$(11)_2$	$(7e)_{16}$	323 sec	256	([256 × 126] +1) × 10 ms
$(1ff)_{16}$	$(11)_2$	$(7f)_{16}$	325 sec	256	([256 × 127] +1) × 10 ms

4.5.2 WL1 Programming

WL1 can be set from 1 ms to 1.024 seconds. A 1 ms period clock is used for generating this delay.

Bit 6 gives a period multiplication factor of 1 or 16 (by a 16-clock prescaler). Bits 5 to 0 give the number of cycles of the divided clock from 1 to 64 (counter).

Table 4-13. WL1 Programming

WL1[6:0]	WL1[6]	WL1[5:0]	Period	Prescaler	Comments
$(00)_{16}$	0	$(00)_{16}$	1 ms	1	1 × 1 ms
$(01)_{16}$	0	$(01)_{16}$	2 ms	1	(1+1) × 1 ms
$(vv)_{10}$	0	$(vv)_{10}$	vv + 1 ms	1	1× (vv +1) ms
$(3e)_{16}$	0	$(3e)_{16}$	63 ms	1	1 × 63 ms
$(3f)_{16}$	0	$(3f)_{16}$	64 ms	1	1 × 64 ms
$(40)_{16}$	1	$(00)_{16}$	16 ms	16	16 × 1 ms
$(41)_{16}$	1	$(01)_{16}$	32 ms	16	16 × 2 ms
–	1	$(vv)_{10}$	–	16	16 × (vv +1) ms
$(7e)_{16}$	1	$(3e)_{16}$	1.008 sec	16	16 × 63 ms
$(7f)_{16}$	1	$(3f)_{16}$	1.024 sec	16	16 × 64 ms

4.5.3 WL2 programming

WL2 can be set as a multiple of WL1 from 0 to 31 WL1.

Table 4-14. WL2 Programming

WL2[2:0]	Period	Comments
$(000)_2$	0	Simultaneous test of the RSSI and header
$(001)_2$	1 × WL1	
$(010)_2$	2 × WL1	
$(011)_2$	3 × WL1	
$(100)_2$	4 × WL1	
$(101)_2$	8 × WL1	
$(110)_2$	16 × WL1	
$(111)_2$	31 × WL1	

More information is given in the Application Note “Power Management Using the Embedded Stand-alone Wake-up Mode protocol” reference 2186.

4.6 Control Logic

4.6.1 Serial Data Interface

The application microcontroller can control and monitor the AT86RF211S through a synchronous, bidirectional 3-wire serial interface, comprising three signals:

- SLE signal: enable input
- SCK signal: clock input
- SDATA signal: data in/out

When SLE = 1, the interface is inhibited and the SCK and SDATA (in) values are not propagated into the IC, reducing power consumption and preventing any risk of parasitic write or read cycle.

A *read* or *write* cycle starts when SLE is set to 0 and stops when SLE is set to 1. Only one operation can be performed during one access cycle, meaning that only one register can be either read or written.

4.6.1.1 Register Interface Format

A message comprises three fields:

- Address A[3:0]: 4 bits (MSB first)
- R/W: read/write selection
- Data D[31:0]: up to 32 bits (MSB first)

ADDRESS				R/W	DATA up to 32 bits (Variable Length)		
A[3]	A[2]	A[1]	A[0]	R/W	MSB	D[nbit-1:0]	LSB

A variable register length and partial read or write cycles are supported. In the case of partial read or write cycles, the first data (in or out) is always the register’s MSB.

4.6.1.2 *WRITE Mode (R/W = 1)*

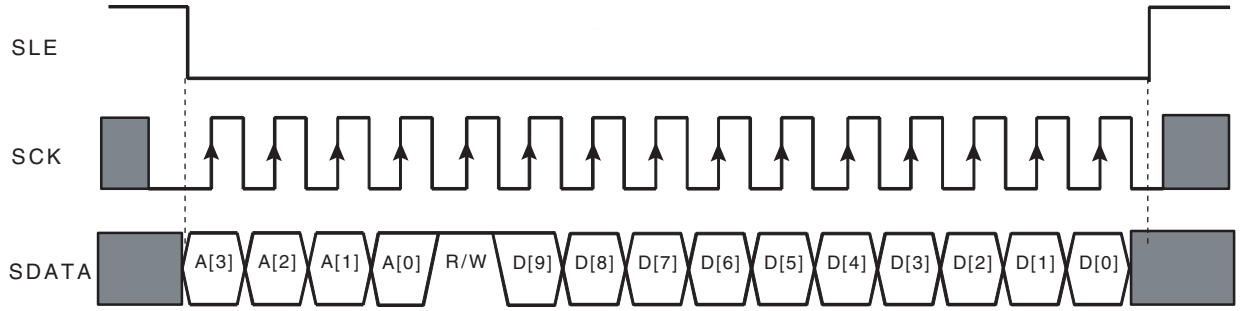
The address, R/W and data bits are clocked on the rising edge of SCK.

If the number of data bits is lower than the register capacity, the LSB bits retain their former value, allowing a safe partial write. If the number of data bits is greater than the register capacity, the extra bits are ignored.

The data is actually written into the register on the rising edge of SLE when the data length is less or equal to the register length.

When trying to write more data than the register length, a data field is written on the first extra rising clock edge of the register length.

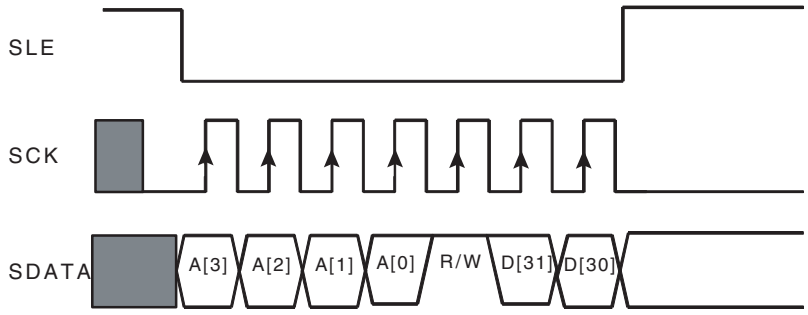
Figure 4-29. Write Chronogram: Complete Write Cycle in a 10-bit Register



Note: The SCK signal must be at a logic level 0 when SLE toggles up or down.

The complete 10-bit register is updated on a rising edge of SLE.

Figure 4-30. Write Chronogram: Partial Write Cycle, Writing 2 bits



Only the 2 MSBs are updated on the rising edge of SLE; other register bits remain unchanged.

4.6.1.3 *READ Mode (R/W = 0)*

The address and R/W bits are clocked on the rising edge of SCK and the data bits are changed on the falling edge of SCK. The register's MSB is the first bit read.

The SDATA I/O pin is switched from input to output on the edge following the *1* clocking the R/W bit.

It is possible to stop reading a register (by reverting SLE to 1) at any time.

If an attempt is detected to read more bits than the register capacity, SDATA is clamped to 0.

If the address of a register is not valid, SDATA is set to 1 during the first 32 SCK periods, and then to 0 during all the extra periods.

SDATA is switched back to the input state when SLE reverts to 1.

Figure 4-31. Read Chronogram: Complete Read Cycle from a 10-bit Register

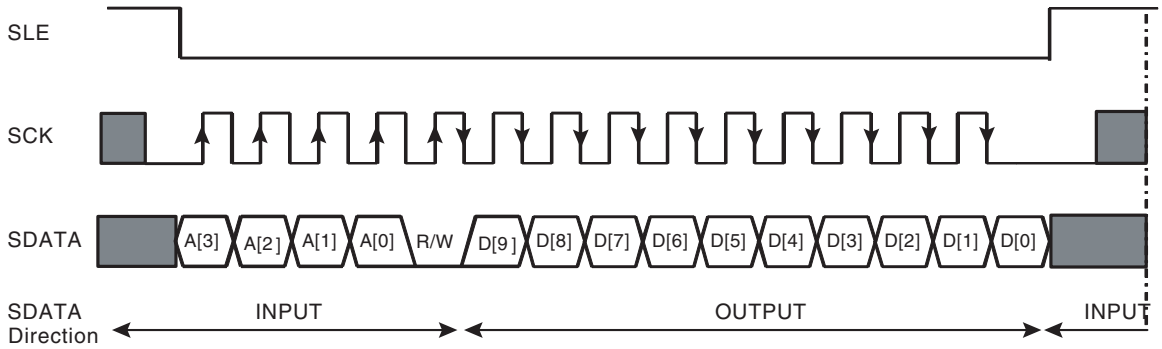


Figure 4-32. Read Chronogram: Partial Read Cycle, Reading 2 Bits

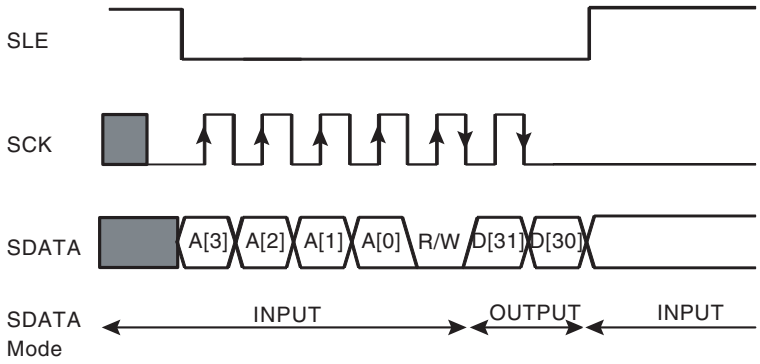
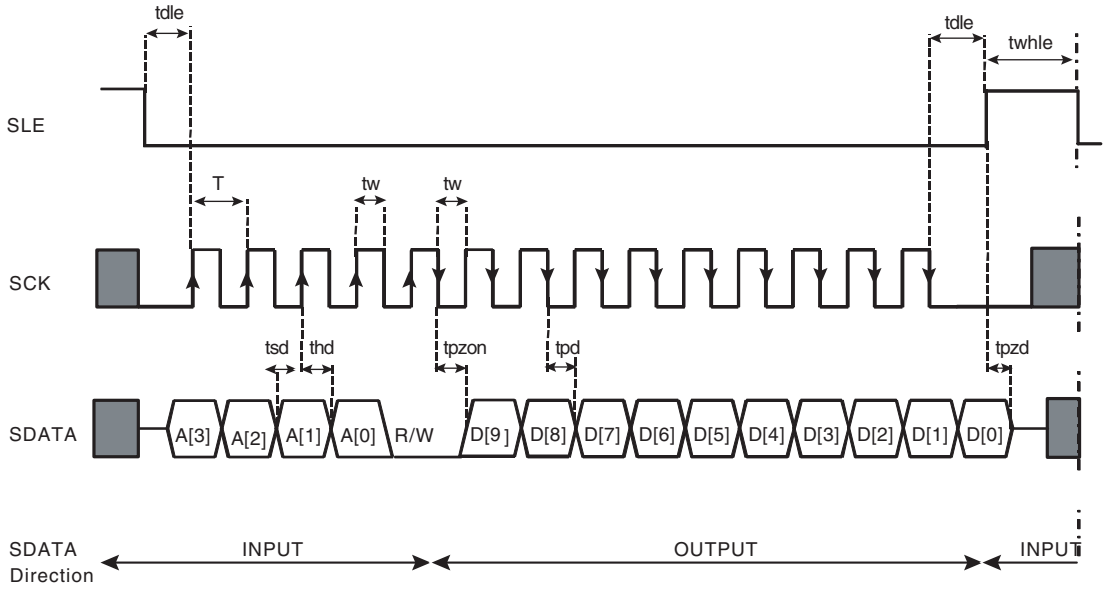


Figure 4-33. Chronogram with Timing



Note: For timing specifications, refer to Table 5-3 on page 52.

4.6.2 Registers

Table 4-15. Register Overview

Name	Address A[3:0]	Nbits	Read-Write	Comments
F0	$(0000)_2$	32	R-W	F0 frequency code
F1	$(0001)_2$	32	R-W	F1 frequency code
F2	$(0010)_2$	32	R-W	F2 frequency code
F3	$(0011)_2$	32	R-W	F3 frequency code
CTRL1	$(0100)_2$	32	R-W	Main control register
STAT	$(0101)_2$	31	R	Status register
DTR	$(0110)_2$	32	R-W	RF211 mode
	$(0110)_2$	32	R-W	RF211S mode
WUC	$(0111)_2$	32	R-W	Wake-up control register
WUR	$(1000)_2$	18	R-W	Wake-up data rate register
WUA	$(1001)_2$	25	R-W	Wake-up address register
WUD	$(1010)_2$	32	R	Wake-up data register
RESET	$(1011)_2$	1	W	Reset
-	$(1100)_2$			Reserved
-	$(1101)_2$			Reserved
-	$(1110)_2$			Reserved
CTRL2	$(1111)_2$	32	R-W	Control register (lock detect - clock recovery)

Note: All the registers must be reprogrammed after the voltage supply has been removed, otherwise they will remain in the default state

4.6.2.1 Reset Register (RESET)

Name	Bit Number
Reset	0

Writing in this register (0 or 1) triggers an asynchronous reset. This register can only be written.

All registers return to the reset state. The chip returns to power-down mode. All the following blocks are reset:

- Registers revert to their default value, therefore the device is compatible with the AT86RF211
- Wake-up function
- Clock recovery function

And in the power-down state, reset is applied to the following blocks:

- Synthesizer dividers
- Clock recovery function
- PLL lock detect
- RSSI detection block
- Discriminator clock (455 kHz)

From powering up the supplies, it takes about 10 µs or at least 1.8V before the reset state is established (power-on reset). From resetting the device, one should wait about 10 µs before re-programming.

Please note that for compatibility reasons, any reset triggered by a power-on sequence or an access to the RESET register sets the device to RF211 mode.

4.6.2.2 Control Register (CTRL1)

Table 4-16. CTRL1 Overview

Name	PDN	RXTX	DATACLK	TXLOCK	PAPDN	WUEN	LNAGSEL	MVCC	TRSSI	HRSSI
nbit	31	30	29	28	27	26	25	24	23-18	17-15
init	0	0	0	1	0	0	0	0	$(000000)_2$	$(000)_2$

CTRL1 Overview (Continued)

Name	TXLVL	TXFS	-	RXFS	XTALFQ	FSKBW	FSKPOL	DSREF	-	-	MOFFSET	ADDFEAT
nbit	14-12	11	10	9-8	7	6	5	4	3	2	1	0
init	$(000)_2$	0	0	$(10)_2$	0	1	1	1	0	0	0	0

Register reset value = $(10000270)_{16}$

Table 4-17. CTRL1 Detailed Description[1][2][3][4]

Name	Number of Bits	Comments
PDN	1	General power-down 0: power down mode; only the serial interface is active 1: AT86RF211S activated *Reset* value: 0
RXTX	1	Reception or transmission selection 0: Rx mode 1: Tx mode *Reset value: 0*
DATACLK	1	DATA clock recovery selection 0: no signal on DATACLK output pin, clock recovery is disabled 1: Clock recovery active: DATACLK activated *Reset value: 0*
TXLOCK	1	Transmission on PLL lock 0: transmission enabled, regardless of the PLL lock status 1: PA *ON* only when the PLL is locked *Reset value: 1* Note: the PLL status is stored in the PLLL bit of the STATUS register
PAPDN	1	Power amplifier power down 0: Tx Power Amplifier power down mode 1: Tx Power Amplifier activated (only if PDN = 1) *Reset value: 0*
WUEN	1	Wake-up function enable 0: Wake-up function disabled, whatever the content of the wake-up control registers 1: Wake-up function activated, depending on the content of wake-up control registers *Reset value: 0*
LNAGSEL	1	LNA gain selection 0: maximum gain 1: minimum gain *Reset value: 0*
MVCC	1	RSSI or V_{CC} power supply measurement selection 0: RSSI voltage measurement, value is stored in STAT register: MRSSI bits 1: V_{CC} voltage measurement, value is stored in STAT register: MVCC bits *Reset value: 0*
TRSSI	6	RSSI value threshold DATAMSG validated if RSSI ≥ TRSSI + HRSSI (high RSSI level) DATAMSG inhibited if RSSI < TRSSI - HRSSI (low RSSI level) *Reset value: $(000000)_2$*
HRSSI	3	Value RSSI hysteresis *Reset value: $(000)_2$*
TXLVL	3	Tx PA output power selection $(000)_2$: minimum transmission level $(111)_2$: maximum transmission level Reset value: $(000)_2$
TXFS	1	Tx frequency selection 0: F0 & F1 1: F2 & F3 *Reset value: 0*

Table 4-17. CTRL1 Detailed Description[1][2][3][4] (Continued)

Name	Number of Bits	Comments
–	1	reserved, must be kept to reset value: 0
RXFS	2	RX frequency selection $(00)_2$: F0 $(10)_2$: F2 $(01)_2$: F1 $(11)_2$: F3 *Reset value: $(10)_2$*
XTALFQ	1	Crystal frequency 0: 10.245 MHz (when IF1 = 10.7 MHz) 1: 20.945 MHz (when IF1 = 21.4 MHz); *option not available* *Reset value: 0*
FSKBW	1	Discriminator range, inactive in AT86RF211S mode: report to DISCRANGE bits of DTR register 0: Narrow Discriminator BW 1: Standard Discriminator BW *Reset value: 1*
FSKPOL	1	Polarity of DATAMSG 0: inverted signal 1: direct signal *Reset value: 1*
DSREF	1	Data slicer reference voltage 0: external reference: SKFILT pin voltage 1: internal reference: DAC level voltage *Reset value: 1*
–	1	reserved, must be kept to reset value 0
–	1	reserved, must be kept to reset value: 0
MOFFSET	1	0: internal ADC sets to V_{CC} measurement 1: internal ADC sets to DISCOUT DC level measurement *Reset value: 0*
ADDFEAT	1	0: no additional feature, RF211 mode 1: additional digital features selected, RF211S mode, in which the DTR length is extended to 32 bits, giving access to new additional features *Reset value: 0*

Notes:
1. The same ADC is used to measure the RSSI or V_{CC} voltage. When the V_{CC} voltage is measured, the RSSI measurement is stopped (the previously-measured RSSI is kept in the STATUS register). This can disturb the reception process (if a threshold is used for DATAMSG validation).Therefore, it is not recommended to measure V_{CC} in reception mode.
2. The V_{CC} measurement cannot be done when the AT86RF211S is in power-down mode.
3. While V_{CC} is being measured, it is possible to measure the DC output of the discriminator.
4. Description of RSSI measurement with hysteresis mechanism: if the RSSI measurement is higher than the high RSSI level, DATAMSG is validated (high RSSI level = TRSSI + HRSSI). If the RSSI measure is lower than the low RSSI level, DATAMSG is inhibited (low RSSI level = TRSSI - HRSSI). Between these two levels, DATAMSG validation depends on the previous measurement.
   Example:
   TRSSI = 32 and HRSSI = 4 implies high RSSI level = 36 and Low RSSI level = 28

Table 1. RSSI Working Example

MRSSI Sequence	27	32	35	36	35	32	29	28	27	25
RSSI level	NOK	NOK	NOK	OK	OK	OK	OK	OK	NOK	NOK
DATAMSG				valid	valid	valid	valid	valid		

4.6.2.3 Control Register (CTRL2)

Table 4-18. CTRL2 Overview

Name	DATARATE	DATATOL	LDCK	N0LD1	N1LD2
nbit	31-18	17-10	9	8-5	4-0
init	$(0000)_{16}$	$(00)_{16}$	0	$(0010)_2$	$(10111)_2$

Register reset value = $(00000057)_{16}$

Table 4-19. CTRL2 Detailed Description

Name	Number of bits	Comments
DATARATE	14	Received DATAMSG rate This value must be programmed to have the DATACLK activated. (selected with DATACLK bit in CTRL1 register). Value from 1 kbps to 100 kbps *Reset value: $(0000)_{16}$*
DATATOL	8	Step size of the synchronization algorithm *Reset value: $(00)_{16}$*
LDCK	1	Clock frequency is doubled to increase precision of PLL lock detection 0: 10 MHz clock frequency, recommended value 1: doubled clock frequency *Reset value: 0*
N0LD2	4	PLL unlock condition trigger Recommended values are reset values *Reset value: $(0010)_2$*
N1LD2	5	PLL lock condition trigger Recommended values are reset values *Reset value: $(10111)_2$*

4.6.2.4 *Frequency Registers*

Table 4-20. Overview

Name	Number of Bits
F0, F1, F2, F3	31-0

Table 4-21. Detailed Description

Name	Number of bits	Comments
F0	32	Frequency code value F0 default register in TX mode (*0* code in FSK modulation)
F1	32	Frequency code value F1 default register in TX mode (*1* code frequency in FSK modulation)
F2	32	Frequency code value F2 default register in RX mode
F3	32	Frequency code value F3

Note: 1. F0, F1, F2 and F3 registers must be programmed before using the device.

There is no simple relationship between the frequency registers and the exact frequency. e2v provides a tool to program them on a production bench.

4.6.2.5 *Selection of Frequency Registers*

The FSK modulation is completely integrated. Two registers must be programmed (default F0 and F1) to allow *0* and *1* transmission.

The frequency register selection depends on the control register programming and on the DATAMSG pin.

Table 4-22. Frequency Register Settings

RXTX	RXFS	TXFS	DATAMSG	Mode
0	00	X	X	Receive LO is F0
0	01	X	X	Receive LO is F1
0	10	X	X	Receive LO is F2
0	11	X	X	Receive LO is F3
1	XX	0	0	Transmit *0* on F0
1	XX	0	1	Transmit *1* on F1
1	XX	1	0	Transmit *0* on F2
1	XX	1	1	Transmit *1* on F3

in reception mode, only frequency need to be programmed. In transmission mode, two different registers F0 and F1 or F2 and F3 must be programmed for *0* code and *1* code transmission. The DATAMGS pin value actually selects the used register. The four registers can also be set to define two channels so that the AT86RF211S may switch quickly from one channel to another.

Table 4-23. Programmed Frequency

Mode	Programmed Frequency
RX	FCHANNEL ± IF1
TX	FCHANNEL ± deviation

Example:

FCHANNEL = 868.3 MHz
IF1 = 10.7 MHz
Deviation = ±4 kHz

Table 4-24. Programmed Frequency Example

Mode	FSK
RX	868.3 ± 10.7 = 879 MHz or 857.6 MHz programmed in F2
TX	868.3 ± 0.004 = 868.304 MHz programmed in F1 when DATAMSG = 1 and 868.296 MHz programmed in F0 when DATAMSG = 0

Notes: 1. In reception mode, one of the two frequencies (879 or 857.6 MHz) can be chosen, taking into account the external parameters (for example, the noise that brings the image frequency).
2. Two frequencies are used to transmit data: 868.304 MHz for *1* transmission and 868.296 MHz for *0* transmission. The polarity of DATAMSG can be swapped using bit 5 of CTRL1.

4.6.2.6 Status Register

The STATUS register is used to read the status of the internal functions (including the wake-up function) or the output value of the internal ADC. This register is read-only.

Table 4-25. Overview

Name	PLLL	MRSSI	MVCC	WAKEUP	-	MSGERR
nbit	30	29-24	23-18	17	16	15

Overview (Continued)

Name	MSGDATL	MSGMRATE
nbit	14-10	9-0

Table 4-26. Detailed Description

Name	Number of Bits	Comments
PLLL	1	PLL Lock flag 0: PLL unlocked 1: PLL locked *Reset value: 0*
MRSSI	6	Measured RSSI level *Reset value: $(00)_{16}$*
MVCC	6	Measured V_{CC} power supply voltage or discriminator output when MOFFSET = 1 *Reset value: $(00)_{16}$*
WAKEUP	1	WAKEUP flag Copy of the WAKEUP pin, but not affected by polarity selection. 0: no wake-up message received 1: wake-up message received *Reset value: 0*
-	1	Reserved *Reset value: 0*
MSGERR	1	Wake-up message error in test message mode 0: no error detected in the received message 1: message received with error *Reset value: 0*
MSGDATL	5	Wake-up message data length length of the data stored in WUD (received message). *Reset value: 0*
MSGMRATE	10	Wake-up message measured data rate bit period extracted from message header of the wake-up message. Measured as a multiple of 1.56 µs (like RATE in WUR register). 0: 1 × 1.56 µs $(vv)_{10}$: vv × 1.56 µs $(3ff)_{16}$: 1024 × 1.56 µs *Reset value: $(000)_{16}$*

4.6.2.7 *DTR Register*

DTR contains the bits corresponding to the new features of the AT86RF211S.

Depending on the CTRL1[0] value, DTR has two different sizes:

- CTRL1[0] = 0 - DTR[5:0] - (same as AT86RF211)
- CTRL1[0] = 1 - DTR[31:0] - (extended DTR)

The DTR register enables the data slicer input offset to be precisely adjusted.

Table 4-27. Overview in RF211 Mode

Name	DSREF[3:0]	DISCHIGH	DISCLOW
nbit	5-2	1	0
init	$(1000)_2$	0	0

The register's reset value = $(20)_{16}$

Note: When CTRL1[0] is left to the default value, AT86RF211S' programming and features are the same as for the AT86RF211.

Table 4-28. Detailed Description in RF211 Mode

Name	Number of Bits	Comments
DSREF	4	Data Slicer reference tuning, when reference is said to be internal $(0000)_2$ to $(1111)_2$ *Reset value: $(1000)_2$*
DISCHIGH	1	Discriminator offset shift (high) 0: no shift 1: output level shifted up *Reset value: 0*
DISCLOW	1	Discriminator offset shift (low) 0: no shift 1: output level shifted down *Reset value: 0*

The DTR register also allows you to take advantage of the additional digital features when CTRL1[0] has been set to 1 (ADDFEAT). If CTRL1[0] = 1 and DTR is left to the default value, the AT86RF211S has the same features as the RF211 (with one exception explained in Note 5 on page 47).

Table 4-29. DTR Overview in RF211S Mode

Name	XTALRUN	SELCH	HOLDMODE	XTAL205M	DISCRANGE	DISCLPF	RSSICLK	–
nbit	31-30	29	28	27	26-25	24	23-22	21
init	00	0	0	0	$(10)_2$	0	10	0

DTR Overview in RF211S Mode (Continued)

Name	PORTEN	PORTPOL	PORTSEL	CLKOUTPUT	NEWDATACLK	SYNCDATAMSG	DATACLKEN
nbit	20	19	18-16	15-14	13	12	11
init	0	0	$(000)_2$	$(00)_2$	0	0	0

DTR Overview in RF211S Mode (Continued)

Name	WUSYNC	WUHEAD	-	DSREF	DISCHIGH	DISCLOW
nbit	10	9	8-6	5-2	1	0
init	0	0	$(000)_2$	$(1000)_2$	0	0

Table 4-30. DTR Detailed Description in RF211S Mode

Name	Number of Bits	Comments
XTALRUN	2	*XTAL running mode* control 00: normal mode 01: XTAL oscillator running with no possibility to output the clock on the DIGOUT pin 10: unused 11: XTAL oscillator running, with possibility to output the clock on the DIGOUT pin *Reset value: $(00)_2$*
SELCH	1	*Charge and hold* mode control 0: internal or external mode as specified by CTRL1[4] 1: *charge and hold* mode selection *Reset value: 0*
HOLDMODE	1	Hold control in *charge and hold* mode if SELCH = '1' 0: remains in the Charge mode 1: holds the capacitor voltage *Reset value: 0*
XTAL205M	1	*20.5 MHz crystal and 10.7 MHz IF1* mode control 0: selection as specified by CTRL1[7] 1: 20.5 MHz crystal with 10.7 MHz IF1; *option not available* *Reset value: 0*
DISCRANGE	2	Discriminator range choice 11: narrow DB ± 25 kHz.... ..... 10: standard DB, ± 50 kHz 01: medium DB ± 75 kHz.. ..... 00: wide DB, ± 125 kHz Reset value: $(10)_2$
DISCLPF	1	Discriminator low-pass filter frequency cut-off control 0: discriminator LPF kept to 50 kHz 1: discriminator LPF set to 70 kHz... *Reset value: 0*

Table 4-30. DTR Detailed Description in RF211S Mode (Continued)

Name	Number of Bits	Comments
RSSICLK	2	RSSI clock selection control 00: 80 kHz clock (12 µs) 01: 160 kHz clock (6 µs) 10: 320 kHz clock (3 µs) 11: 640 kHz clock (1.5 µs) *Reset value: $(10)_2$*
–	1	Reserved. Must be kept to reset value 0
PORTEN	1	DIGOUT pin enable 0: no signal on DIGOUT 1: DIGOUT selected for output signal *Reset value: 0*
PORTPOL	1	DIGOUT pin polarity 0: low level for '0' 1: low level for '1', inverted output *Reset value: 0*
PORTSEL	3	DIGOUT signal selection 000: divided XTAL reference clock (see CLKOUTPUT below) 001: carrier Sense on RSSI over TRSSI 010: XTAL oscillator running flag 011: 455 kHz reference clock from the discriminator PLL 100: Receive mode flag during “wake-up mode” (WUEN =1) 101: Receive mode flag (other modes) 110: 1 kHz reference clock of the Wake-up timer 111: Lock Detect flag of the main PLL *Reset value: $(000)_2$*
CLKOUTPUT	2	DIGOUT output clock division ratio 00: no division .... 01: divided by 2 10: divided by 4 .... 11: divided by 8 *Reset value: $(10)_2$*
NEWDATACLK	1	Clock recovery improved algorithm 0: standard clock recovery state machine, same as AT86RF211 for compatibility 1: improved clock recovery state machine, recommended *Reset value: 0*
SYNCDATAMSG	1	DATAMSG resynchronization 0: no resynchronization, as AT86RF211 1: DATAMSG resynchronized by DATACLK *Reset value: 0*
DATACLKEN	1	DATACLK with RSSI inhibition 0: no inhibition ..... 1: DATACLK inhibited if RSSI < TRSSI *Reset value: 0*
WUSYNC	1	Improved wake-up header synchro detection (during “wake-up mode”) 0: standard header synchro, as AT86RF211 1: improved header synchro with wider duty cycle acceptance *Reset value: 0*

Table 4-30. DTR Detailed Description in RF211S Mode (Continued)

Name	Number of Bits	Comments
WUHEAD	1	Wake-up header detection 0: header detection on 9 ½ bits, as AT86RF211 1: header detection on 10 bits *Reset value: 0*
–	3	Reserved, must be kept to reset value: (000)2
DSREF	4	Data slicer reference tuning, when internal $(0000)_2$ to $(1111)_2$ Reset value: $(1000)_2$
DISCHIGH	1	Discriminator offset shift (high)' 0: no shift 1: output level shifted up *Reset value: 0*
DISCLOW	1	Discriminator offset shift (low) 0: no shift 1: output level shifted down *Reset value: 0*

Notes:
1. The hold time on the SKFILT capacitor depends on the value of this capacitor. This is detailed in the Application Note “AT86RF211S FSK Transceiver for ISM Radio Applications - RF BOM versus Application Requirements”.
2. SDB and NDB are like the CTRL1[6] selection. Medium DB offers a slope (mV / kHz) that is one third of the NDB one, and wide DB a slope of one fifth of the NDB one, allowing wider deviations.
3. The reference clock used for the DIGOUT output clock is the crystal frequency, in relation with the chosen division ratio.
4. DSREF, DISCHIGH and DISCLOW are unchanged compared to the AT86RF211 selection.
5. If CTRL1[0] = '1' (ADDFEAT) and DTR is left to the default setting, then the AT86RF211S has the same features as the AT86RF211. Exception: if CTRL1[6] is NDB, it is then set to SDB which is the default value of DTR[26-25] .

4.6.2.8 Wake-up Control Register

Table 4-31. WUC Overview

Name	WUE	DATA	STOP	DATL	ADD	–	WPER	WL1
nbit	31	30	29	28-24	23	22	21-13	12-6
init	0	1	1	$(11111)_2$	1	0	$(001011111)_2$	$(0000100)_2$

WUC Overview (Continued)

Name	WL2	ISTU	–	–
nbit	5-3	2	1	0
init	$(010)_2$	0	0	0

Register reset value = $(7f8be110)_{16}$

Table 4-32. WUC Detailed Description

Name	Number of Bits	Comments
WUE	1	Wake-up function enable Returns to “0” when a valid message is received. 0: wake-up disable 1: wake-up enable *Reset value: 0*
DATA	1	Data content 0: message without data field 1: message with data field *Reset value: 1*
STOP	1	STOP field usage 0: fixed data length: data length set from 1 to 32 by DATL 1: variable data length: data length given by the STOP field location; DATL must be set to $(11111)_2$ *Reset value: 1*
DATL	5	Data length Valid in fixed data length mode (STOP = 0). $(00000)_2$: 1 bit (minimum data length value) ---------- $(11110)_2$: 31 bits $(11111)_2$: 32 bits (max data length value) *Reset value: $(11111)_2$*
ADD	1	Address content 0: message without address field 1: message with address field *Reset value: 1*
MSGTST	1	Message error test 0: no error detection mode 1: error detection enabling for debugging Reset value: 0
WPER	9	Wake-up period Variable from 10 ms to 328 sec with an accuracy of ±20%.(on-chip RC oscillator) *Reset value: 960 ms* *Reset value: $(5f)_{16}$*
WL1	7	Minimum delay before TEST1 (check of RSSI level) Variable from 1ms to 1.024 sec Delay calculation starts when the reference oscillator starts *Reset value: 5 ms* *Reset value: $(04)_{16}$*

Table 4-32. WUC Detailed Description (Continued)

Name	Number of Bits	Comments
WL2	3	Minimum delay between TEST 1 and TEST 2 (check of header detection) Variable as multiple of WL1 from 0 to 31 × WL1 *Reset value: 2 × WL1* *Reset value: $(2)_{10}$*
ISTU	1	Inhibit stuff mechanism 0: stuff is used for wake-up message 1: no stuff used in the wake-up message *Reset value: 0*
-	2	Reserved, must be kept to reset value *Reset value: 0*

4.6.2.9 Wake-up Data Rate Register (WUR)

Table 4-33. WUR Overview

Name	WUOP	RATECHK	RATE	RATETOL
nbit	17-16	15	14-5	4-0
init	$(01)_2$	0	$(0000010000)_2$	$(01000)_2$

Table 4-34. WUR Detailed Description

Name	Number of Bits	Comments
WUOP	2	WAKEUP output polarity $(00)_2$: Wake-up pin active low $(01)_2$: Wake-up pin active high $(1\times)_2$: Wake-up pin open drain (active low, inactive tri-state) *Reset value: $(01)_2$*
RATECHK	1	Data rate check the data rate is automatically extracted from the HEADER field. the data rate can be compared to RATE with a tolerance of plus or minus RATETOL. Data rate is computed from a unit of 1.56 µs (Reference clock divided by 16). 0: data rate not checked. 1: data rate check done (header ignored if check fails). *Reset value: 0*
RATE	10	Data rate value 0d: min value = 1 × 1.56 µs $(1023)_{10}$: max value = 1024 × 1.56 µs *Reset value: 64 × 1.56 µs* *Reset value: $(63)_{10}$*
RATETOL	5	Data rate tolerance 0d: min value = 0 × 1.56 µs $(31)_{10}$: max value = 31 × 1.56 µs *Reset value: 8 × 1.56 µs* *Reset value: $(8)_{10}$*

4.6.2.10 Wake -up Address Register (WUA)

Table 4-35. WUA Overview

Name	ADDL	ADD
nbit	24-20	19-0
init	$(01001)_2$	$(0f0f0)_{16}$

Table 4-36. WUA Detailed Description

Name	Number of Bits	Comments
ADDL	5	Wake-up address length 0: wake-up address length = 1 bit 1: wake-up address length = 2 bits $(19)_{10}$: wake-up address length = 20 bits $>(19)_{10}$: forbidden *Reset value: 10 bits*
ADD	20	Wake-up address If wake-up address length is less than 20 bits, MSB bits are ignored *Reset value: $(0f0f0)_{16}$*

In this register, the last bit of the address field is not taken into account the address field that is received is being tested. Thus, the last bit must be programmed and counted in the address length but it can be either 0 or 1.

4.6.2.11 Wake-up Data Register (WUD)

Table 4-37. WUD Overview

Name	WUD
nbit	(data length -1) - 0

Table 4-38. WUD Detailed Description

Name	Number of bits	Comments
WUD	Length	Wake-up message data Warning: the length of this register is variable: * case fixed data length (STOP = 0 of WUC) data length is given by DATL of WUC. * case variable data length (STOP = 1 of WUC) data length is given by MSGDATL of STAT register. Warning: the first bit of data received is the LSB: WUD[0].

Note: To use this mode, refer to the corresponding Application Note "*Power Management Using the Embedded Stand-alone Wake-up Mode Protocol*".

5. Electrical Specification

This device is sensitive to electro-static discharge (ESD). Storage or handling of the device must be carried out according to usual protection rules.

Table 5-1. Absolute Maximum Ratings

Temperature	95°C	Stresses beyond the conditions listed above may cause permanent damage to the device. Exposure to Absolute Maximum Ratings for an extended period may affect device reliability
Storage temperature	-65 to 150°C	
Supply voltage	0 to 3.95V	
Digital input voltage	-0.3 to V_{CC} +0.3V	
RXIN input power	0 dBm	

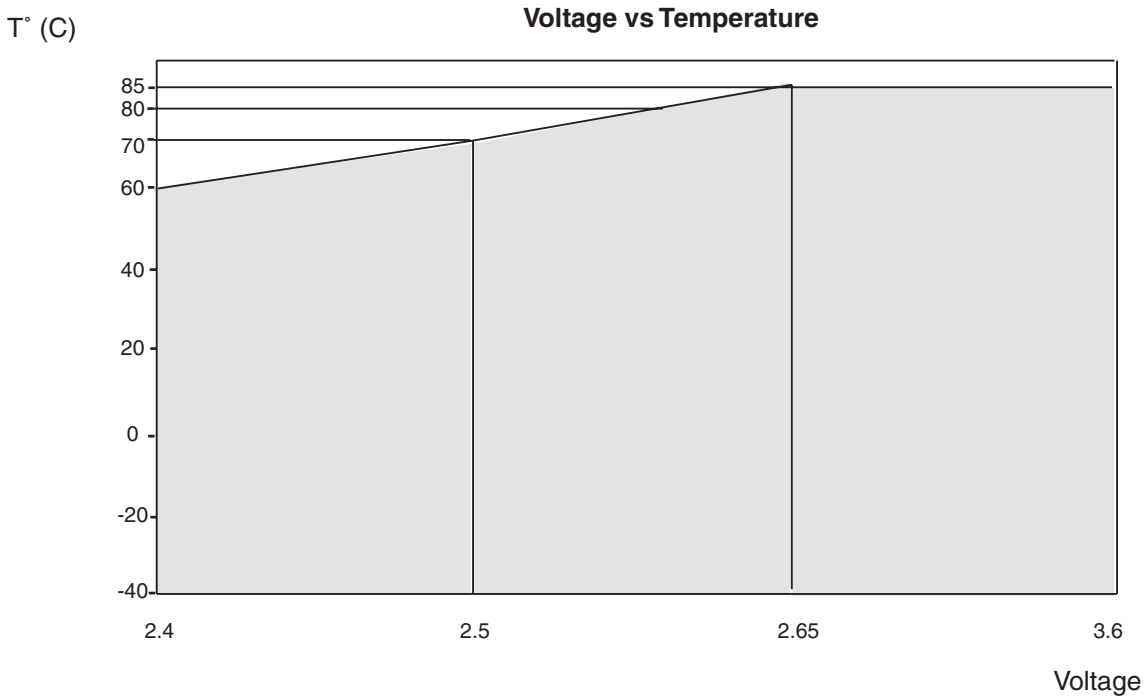
Table 5-2. DC Characteristics (unless otherwise specified, data is given for T = 25°C and V_{SUPPLY} = 2.7V)

Parameter	Min	Typ	Max	Unit	Comments
Supply voltage	2.4		3.6	V	Qualified at 3.75V for 6 months maximum
Supply current		0.5		µA	Power-down
Supply current		3		µA	Wake-up mode
Supply current(1)		150		µA	XTALRUN mode, 10.245 MHz reference
Supply current(1)(2)		950		µA	XTALRUN with output on DIGOUT pin, 10.245 MHz
Supply current		24		mA	Rx mode
Supply current		35		mA	Tx mode, Pout = +10 dBm at 433 MHz
Supply current		42		mA	TX mode, Pout = +10 dBm at 868 MHz
Supply current		43		mA	TX mode, Pout = +10 dBm at 915 MHz
Supply current		15		mA	Tx mode, PDN-PA on
Operating temperature	-40		85	°C	

Notes: 1. Values given if no 3.3 kΩ resistor is mounted between XTAL2 and GND; otherwise add 200 µA.

2. C_{LOAD} = 10 pF, F_{DIGOUT} = 10.245 MHz.

Figure 5-1. Voltage vs. Temperature



Note: The utilization range of the product described in Figure 5-1 is shown in grey.

Table 5-3. Digital CMOS DC Characteristics (unless otherwise specified, data is given for T = 25°C and V_{SUPPLY} = 2.7V)

Name	Parameter	Conditions	Min	Typ	Max	Units
Vil	CMOS low level input voltage Normal input(2) Schmitt trigger input(3)				 0.3*Vcc 0.2*Vcc	 V V
Vih	CMOS high level input voltage Normal input(2) Schmitt trigger input(3)		 0.7*Vcc 0.85*Vcc			 V V
Vol	CMOS low level output voltage(1)	Iol = 1 mA			0.2*Vcc	V
Voh	CMOS high level output voltage(1)	Ioh = - 1 mA	0.8*Vcc			V
Iil	Low level input current without pull-up(4)	Vi = 0V	-1		1	µA
Iih	High level input current without pull-down(4)	Vi = V_{CC}	-1		1	µA
Iioz	Tri-state output leakage without pull-up/-down(4)	Vi = 0V or V_{CC}	-1		1	µA

Notes:
1. For digital CMOS pins : SDATA, DATAMSG, DATACLK, WAKEUP, DIGOUT.
2. For digital CMOS pins: SLE, SCK, SDATA
3. For digital CMOS pins: DATAMSG
4. For digital CMOS pins: SLE, SCK

Table 5-4. Timings

Name	Parameter	Conditions	Min	Typ	Max	Units
tr = tf	CMOS rise/fall times	C_L = 50 pF; 20 – 80%			30	ns
F	SCK frequency		0		5	MHz
T	SCK period		200			ns
tw	SCK low or high time		60			ns
tsd	SDATA setup before SCK rising		40			ns
thd	SDATA hold after SCK rising		40			ns
tpd	SDATA output propagation delay after SCK falling (read mode) (C_L = 30 pF)		2		50	ns
tpzon	Delay to switch SDATA to output after SCK falling (read mode)		3		50	ns
tdle	Minimum delay between an edge of SLE and an edge of SCK		40			ns
twhle	Minimum delay between two accesses to the registers		100			ns
tpzd	Delay to switch SDATA to input (tri-state) after SLE rising (read mode)				40	ns
C_L (1)	Max load for CMOS output pins				50	pF

Note: These timings refer to Figure 4-33 on page 36.

Table 5-5. Synthesizer Specification (unless otherwise specified, data is given for T = 25°C, V_{SUPPLY} = 2.7V)

Parameter	Min		Max	Unit	Comments
Frequency range	400		480	MHz	Digital programming
Frequency range	800		950	MHz	Digital programming
Crystal frequency	10.235	10.245	10.255	MHz	With IF1 = 10.7 MHz(1)
Crystal load impedance	10		20	pF	Parallel mode
XTO settling time	5	8		ms	Depending on crystal specification, with R = 3.3 kΩ
XTO settling time		30		ms	If R = 3.3 kΩ not connected
Clock signal P-P voltage		700		mV	Steady state
Lock time(2)		1200		µs	From oscillator settling to Fc ±10 kHz
Lock time(2)(3)		30		µs	±10 kHz
Rx to Tx toggle time(2)		150		µs	For a 100 kHz shift, ±10 kHz
Phase noise at 10 kHz		-82/-76		dBc/Hz	434/868 or 915 MHz
Phase noise at 50 kHz		-95/-91		dBc/Hz	434/868 or 915 MHz
Phase noise at 100 kHz		-103/-100		dBc/Hz	434/868 or 915 MHz
Phase noise at 1 MHz		-123/-118		dBc/Hz	434/868 or 915 MHz

Notes:
1. The crystal frequency can be slightly changed but since IF2 = IF1 - crystal frequency, IF2 can shift and must remain within the IF2 filter and discriminator bandwidth.
2. With the “typical implementation” loop filter.
3. This must be understood as a channel swap, not applicable in case of modulation.

Table 5-6. Receiver Specification (unless otherwise specified, data is given for T = 25°C and V_{SUPPLY} = 2.7V)

Parameter	Min	Typ	Max	Unit	Comments
FSK sensitivity		-107		dBm	Typical performance with a BER of 1% at input pin RXIN (45). BW = ±10 kHz, dF = ±7.5 kHz, Brate = 4800 bps (1)
Noise figure		13		dB	Input matched, whole Rx chain
Input IP3		-15		dBm	Whole Rx chain
LO leakage			-60	dBm	
Co-channel rejection		-6		dB	Measured as specified in EN 300 220-1
Image frequency rejection		35			Measured on evaluation board
LNA-mixer gain		17		dB	Best matching, see “First LNA/Mixer” on page 14
LNA-mixer noise figure		9		dB	Best matching, see “First LNA/Mixer” on page 14
1dB compression point		-20		dBm	At LNA input pin 45
Optimum load of RXIN 433 MHz		35 + j170		Ω	Impedance for best trade-off noise figure/gain
Optimum load of RXIN 868 MHz		37 + j85		Ω	
Optimum load of RXIN 915MHz		30 + j85		Ω	
Internal switch insertion loss		4.5		dB	
Internal switch isolation		30		dB	
Impedance of internal switch 433 MHz		24-j43		Ω	For matching to SAW filter
Impedance of internal switch 868 MHz		50-j42		Ω	For matching to SAW filter
Impedance of internal switch 915 MHz		50-j42		Ω	For matching to SAW filter
Immunity, no shielding(2)		3		V/m	Without SAW filter
Immunity, no shielding(2)		10		V/m	With SAW filter
1 MHz blocking 433/868/915 MHz		60/51/56		dB	Measured specified in EN 300 220-1, section 9-3 SAW filter used
2 MHz blocking 433/868/915 MHz		73/62/62		dB	
5 MHz blocking 433/868/915 MHz		78/70/72		dB	
10 MHz blocking 433/868/915 MHz		92/86/74		dB	

Table 5-6. Receiver Specification (unless otherwise specified, data is given for T = 25°C and V_{SUPPLY} = 2.7V) (Continued)

Parameter	Min	Typ	Max	Unit	Comments
1 MHz blocking 433/868/915 MHz		40/40/40		dB	Measured specified in EN 300 220-1, section 9-3 No SAW filter mounted
2 MHz blocking 433/868/915 MHz		54/52/52		dB	
5 MHz blocking 433/868/915 MHz		66/63/63		dB	
10 MHz blocking 433/868/915 MHz		67/65/64		dB	
ACR 100kHz		29		dB	Using a 35 kHz 3 dB BW filter in IF2
ACR 200kHz		38		dB	Using a 35 kHz 3 dB BW filter in IF2
ACR 300kHz		31		dB	Using a 150 kHz 3 dB BW IF1 filter
ACR 500kHz		40		dB	Using a 150 kHz 3 dB BW IF1 filter
IF1		10.7		MHz	XTO frequency of 10.245 or 20.5 MHz
IF1 filter impedance		330		ohm	
IF2		455		kHz	
IF2 filter impedance		1700		ohm	
RSSI accuracy		±5		dB	
RSSI dynamic range		50		dB	
Max peak-to-peak frequency deviation		300		kHz	Receiver BW is limited by external filters

Notes: 1. The overall sensitivity depends on the measurement conditions and external components i.e.-102 dBm for BW = ±10 kHz, ΔF = ±7.5 kHz, Brate = 4800 bps with RF switch used and external SAW filter

2. No shielding, 2-layer board, layout respecting the standard EMC rules of thumb, also depending on application software.

Figure 5-2. Detailed Current in Rx Mode

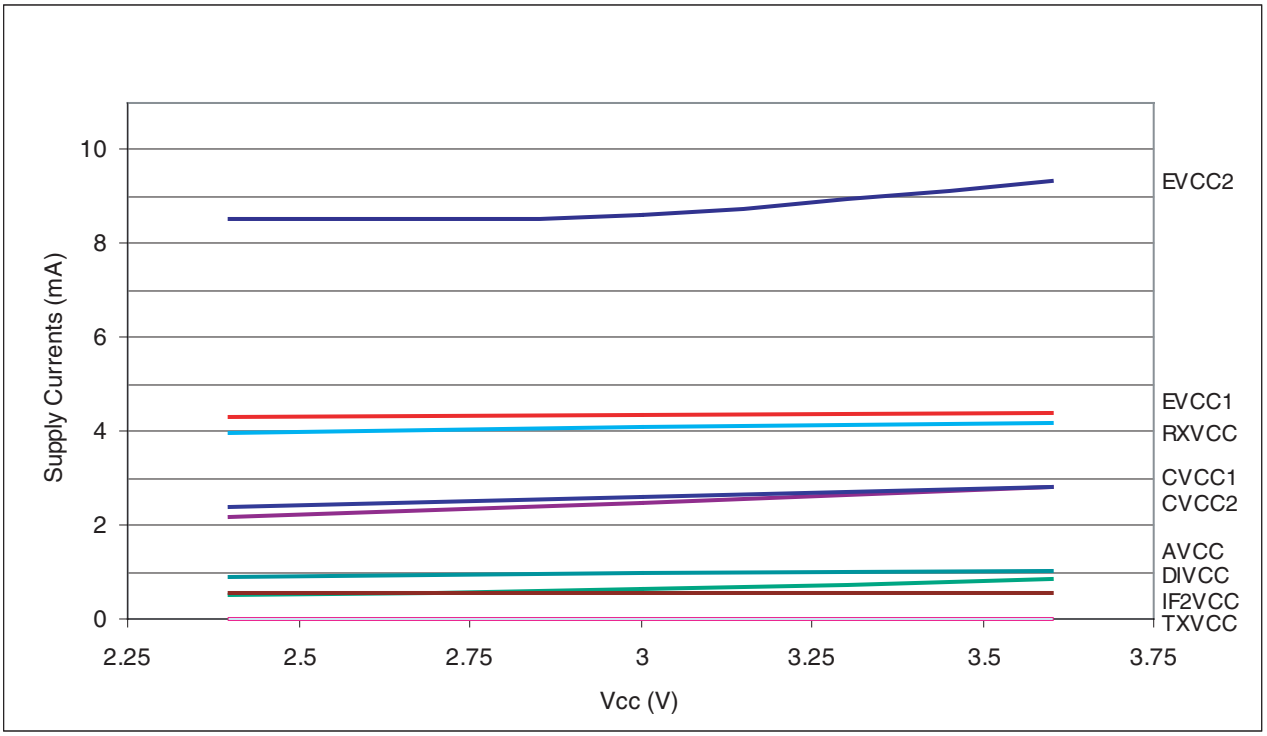


Figure 5-3. Typical Supply Current in Rx Mode

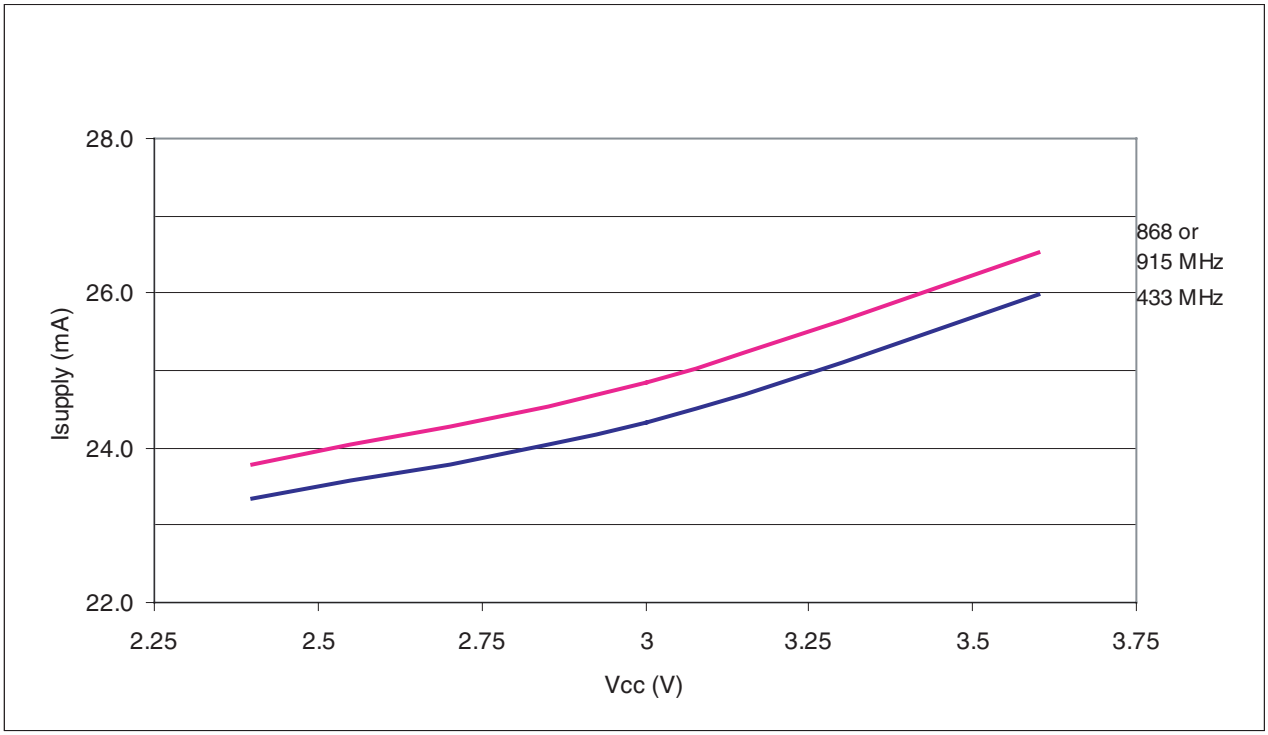


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Table 5-7. Transmitter Specification (unless otherwise specified, data is given for T = 25°C, V_{SUPPLY} = 2.7V, and R_{POWER} = 18 kΩ)

Parameter	Min	Typ	Max	Unit	Comments
Output power		+16		dBm	433 MHz band(1)
Output power		+15		dBm	868 MHz band(1)
Output power		+14		dBm	915 MHz band(1)
Harmonic 2 at 433 MHz		-38		dBm	Output power = +14 dBm measured on evaluation board
Harmonic 3 at 433 MHz		-54		dBm	
Harmonic 2 at 868/915 MHz		-56		dBm	Output power = +12 dBm measured on evaluation board
Harmonic 3 at 868/915 MHz		-52		dBm	
Optimum load impedance of PA		50		Ω	Refer to "Power Amplification" on page 24
Output power dynamic range		12		dB	Digital programming(2)
Automatic level control accuracy		1		dB	Constant conditions
Automatic level control accuracy		±2		dB	Against V_{CC}, T°(3)
FSK data rate			100	kbps	NRZ encoding
FSK data rate			50	kbps	Manchester encoding
FSK deviation	±1		±125	kHz	Selected by F0,...F3
Range of modulation bandwidth		100		kHz	Δ F = ±10 kHz, 9600 bps NRZ with P_{OUT} = +10 dBm
Spurious emissions			-55	dBm	All restricted bands
Spurious emissions			-36	dBm	All other frequencies <1 GHz
Spurious emissions			-30	dBm	Frequencies >1 GHz

Notes:
1. Output power for R_{power} = 5.6 kΩ and TXLVL = 111
2. The maximum power is set by an external resistor, connected to pin R_{POWER}. The output power can be digitally programmed/re-programmed, up to -12 dB below this limit, by means of a 3-bit word: TXLVL of CTRL1 register.
3. The output power is regulated against process, temperature and power supply variations by an internal ALC loop.
4. Measured with P_{OUT} = +10 dBm

Figure 5-4. Typical Expected Supply Current in Tx Mode

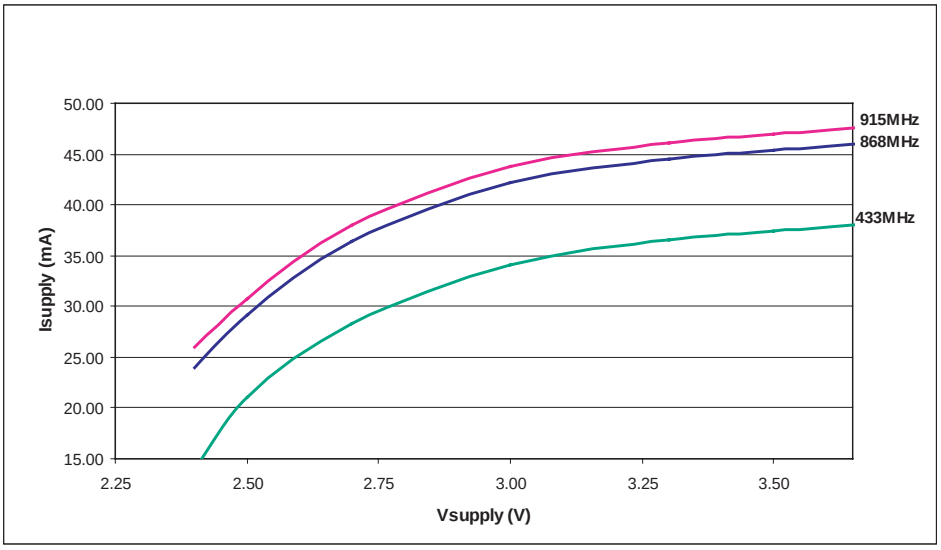
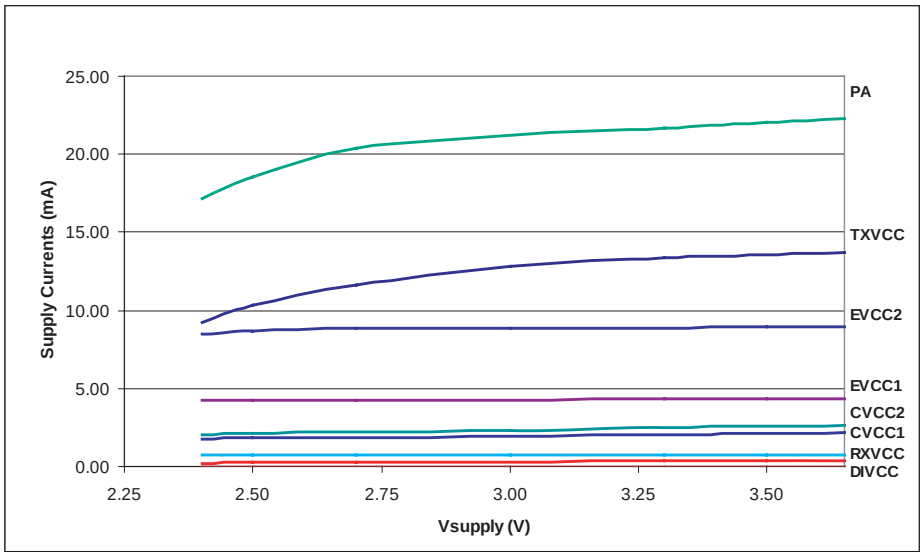


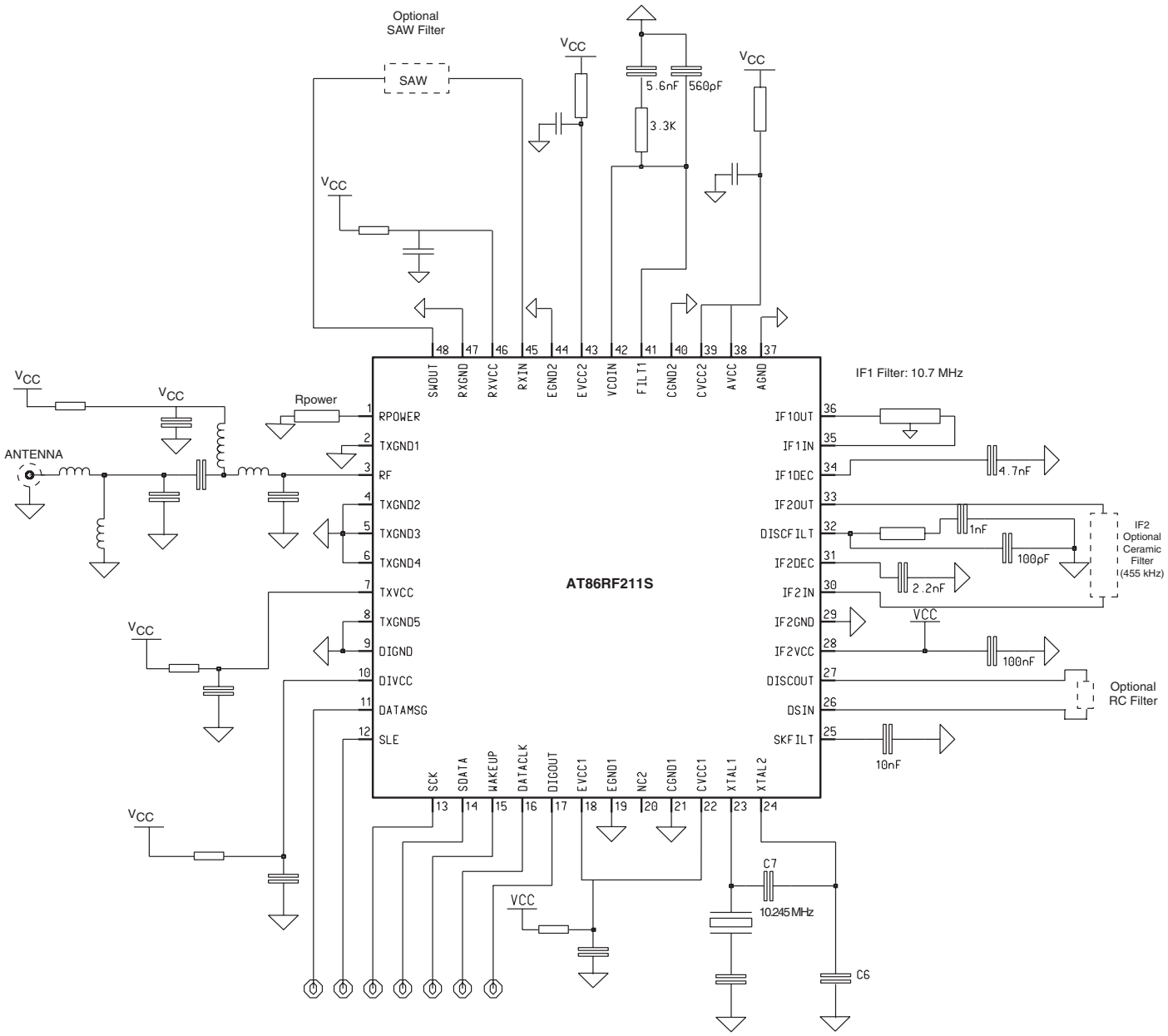
Figure 5-5. Typical Expected Detailed Current in Tx Mode at F = 434 MHz



6. Typical Application

6.1 Implementation

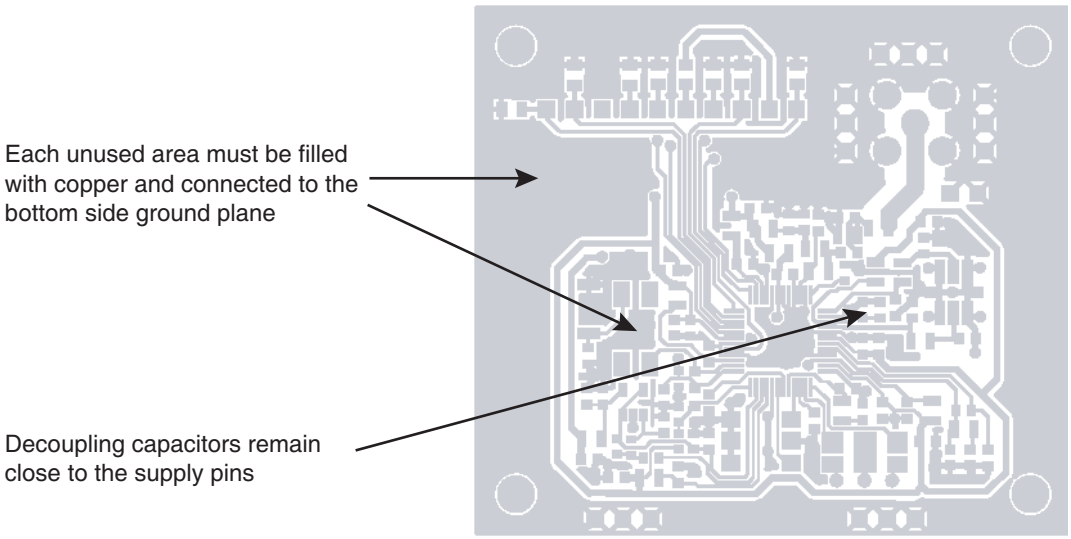
Figure 6-1. Full Example Schematic



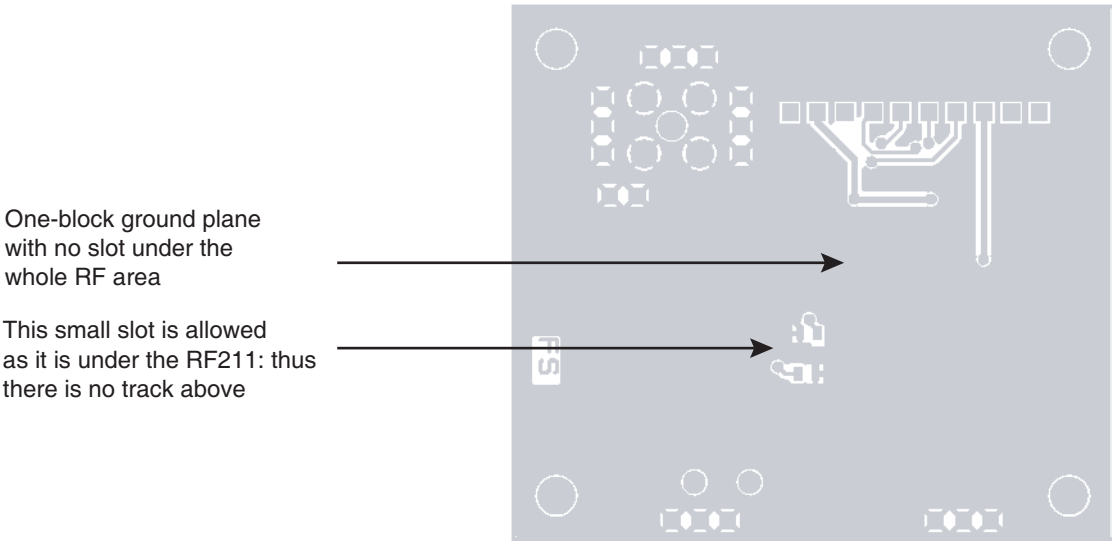
Note: Accurate information regarding the parts and values of the components to be used with the AT86RF211S is described in our Application Note “AT86RF211S Transceiver for ISM Radio Applications - RF BOM versus Application Requirements”.

6.2 Layout

6.2.1 Reference Design – Top Layer



6.2.2 Reference Design – Bottom Layer



7. Packaging Information

Figure 7-1. 48-lead TQFP

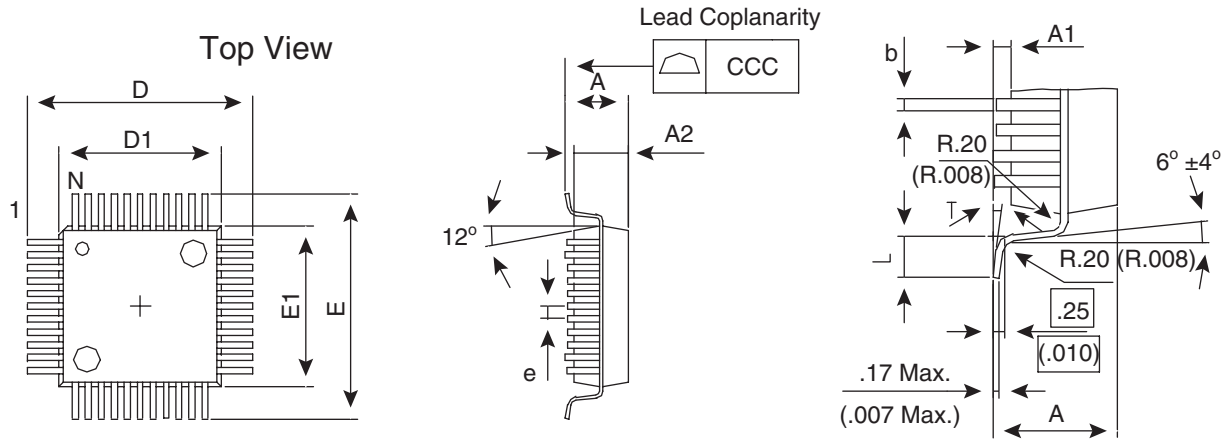


Table 7-1. Packaging Description

Dimension	Nominal Value (mm)	Tolerance	Dimension	Nominal Value (inch)	Tolerance
A	1.60	max	A	0.063	max
A1	0.05 min/0.15 max		A1	0.002 min/0.006 max	
A2	1.40	±0.05	A2	0.055	±0.002
D	9.00	±0.20	D	0.354	±0.008
D1	7.00	±0.10	D1	0.275	±0.004
E	9.00	±0.20	E	0.354	±0.008
E1	7.00	±0.10	E1	0.275	±0.004
L	0.60	+0.15/-0.10	L	0.024	+0.006/-0.004
e	0.50	basic	e	0.020	basic
b	0.22	±0.05	b	0.009	±0.002
ccc	0.1	max	ccc	0.003	max

8. Ordering Information

Full Part Number	Package	Minimum Order Qty	Conditioning
AT68RF211SAHW	TQFP48	250	Tray
AT86RF211SAHW-R	TQFP48	2 000	Tape & reel

The AT86RF211S can be delivered in die form. Please contact your local e2v sales office. Tape & reel may be delivered in one or two different reels tied up together and may also come from two different lots.

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