ST70137

UNICORN™ PCI & USB CONTROLLERLESS ADSL DMT TRANSCEIVER

ST70137 HARDWARE FEATURES

- SUPPORT DIGITAL SIGNAL PROCESSING REQUIREMENTS FOR ONE ADSL CPE CHANEL (ITU-R)
- COMPLIANT WITH ITU 992.1 (ADSL FULL RATE) ANNEXE A (ADSL OVER POTS) AND ANNEXE B (ADSL OVER ISDN) AND ITU 922.2 (G.LITE) AND ANSI T1.413.
- DIRECT INTERFACE TO PCI BUS (PCI RELEASE 2.2 AND COMPLIANT WITH MICROSOFT PC99 & PC2001 SPECIFICATION)
- DIRECT INTERFACE TO USB (USB RELEASE 1.1 SPECIFICATION)
- DIRECT INTERFACE TO THE EXTERNAL SERIAL MEMORY TO SUPPORT PCI/USB USER'S CONFIGURATION
- DIRECT ANALOG FRONT END INTERFACE FOR ST70136 OR ST70134
- 4 TO 8 GPIO DEPENDING ON SELECTED AFE AND EXTERNAL MEMORY CONFIGURATION USED
- CLOCK & RESET INTERFACE
- 1.8V AND 3.3V POWER SUPPLY
- TTL LOGIC LEVELS COMPATIBLE (DEPENDING ON PADS)
- POWER MANAGEMENT
- LOW POWER CONSUMPTION : 0.4W
- TQFP 144

ST70137 SOFTWARE FEATURES

- RFC 2364 PPP OVER ATM
- UNI 3.0, 3.1, 4.0 SIGNALING
- UBR, CBR
- AAL0, AAL5
- NDIS5.0 PCI DRIVER AND USB DRIVER

DESCRIPTION

ST70137 is STMicroelectronics UNICORN™ chipset ADSL DMT transceiver for controllerless ADSL CPE modem.

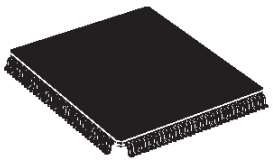
UNICORN™ allows to develop easily and quickly low cost ADSL CPE modem for PC environment.

UNICORN™ is made of two devices, ST70137 and ST70136 or ST70134 (CPE ADSL Analog Front End). ST70137 provides PCI and USB interface. PCI is used to build ADSL CPE modem bundled in the PC, USB interface is used to build external bus powered ADSL modem.

ST70137 is compliant with ITU 992.1 Annexe A and B, with ITU 992.2 and with ANSI T1.413.

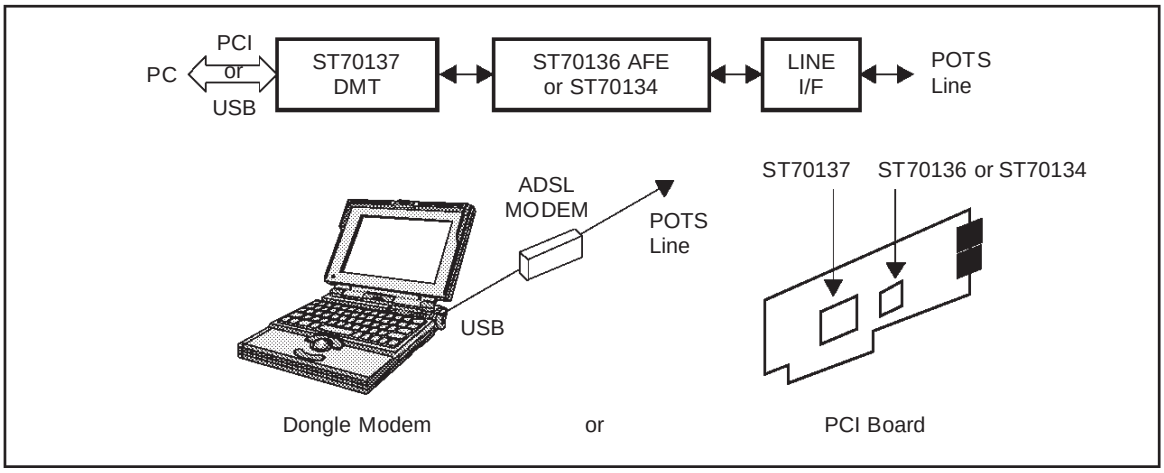
UNICORN™ chipset is delivered with a complete PC software suite for Microsoft Windows 98, Windows 2000 and Windows NT. NDIS5.0 PCI driver and USB driver with ADSL modem control and ATM device driver are provided assuring full ATM support. Configuration and diagnostic tools are also provided.

UNICORN™ chipset and PC software ensure interoperability with the most deployed DSLAM.

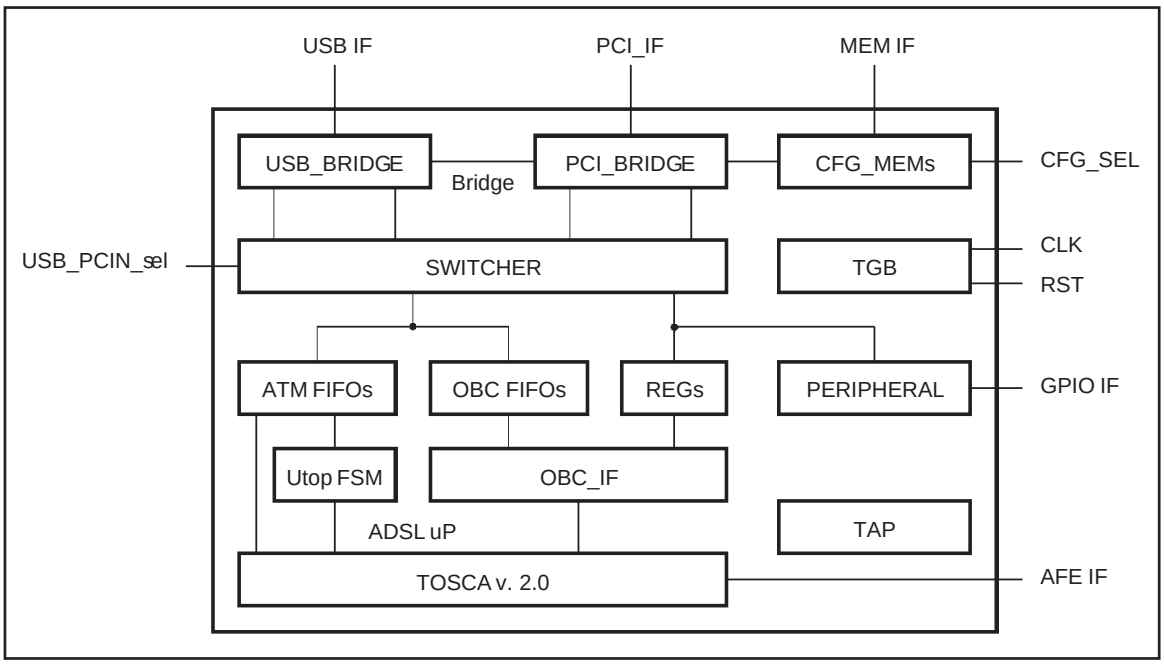


TQFP144
ORDER CODE: ST70137TQFP

TYPICAL APPLICATION

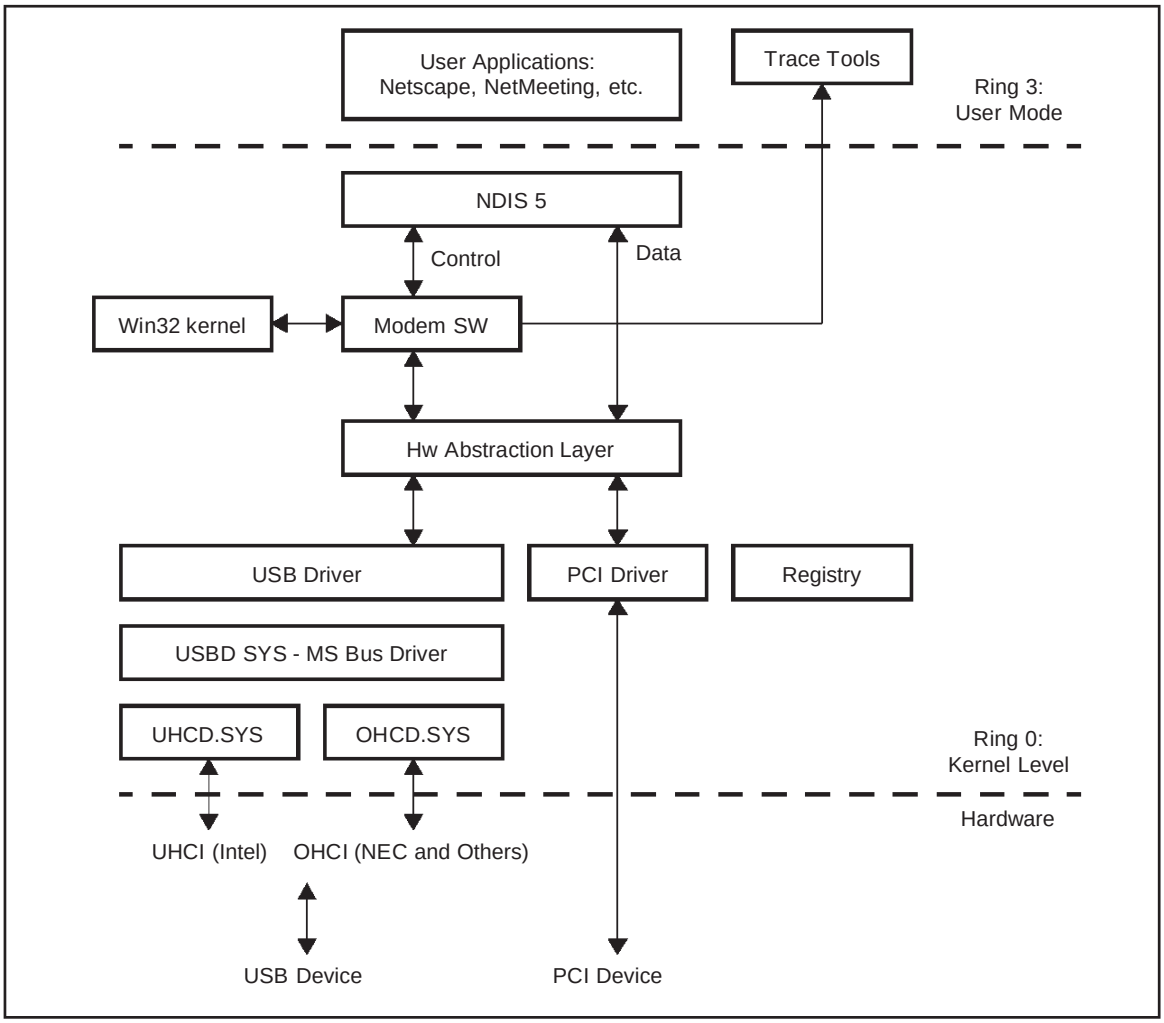


BLOCK DIAGRAM

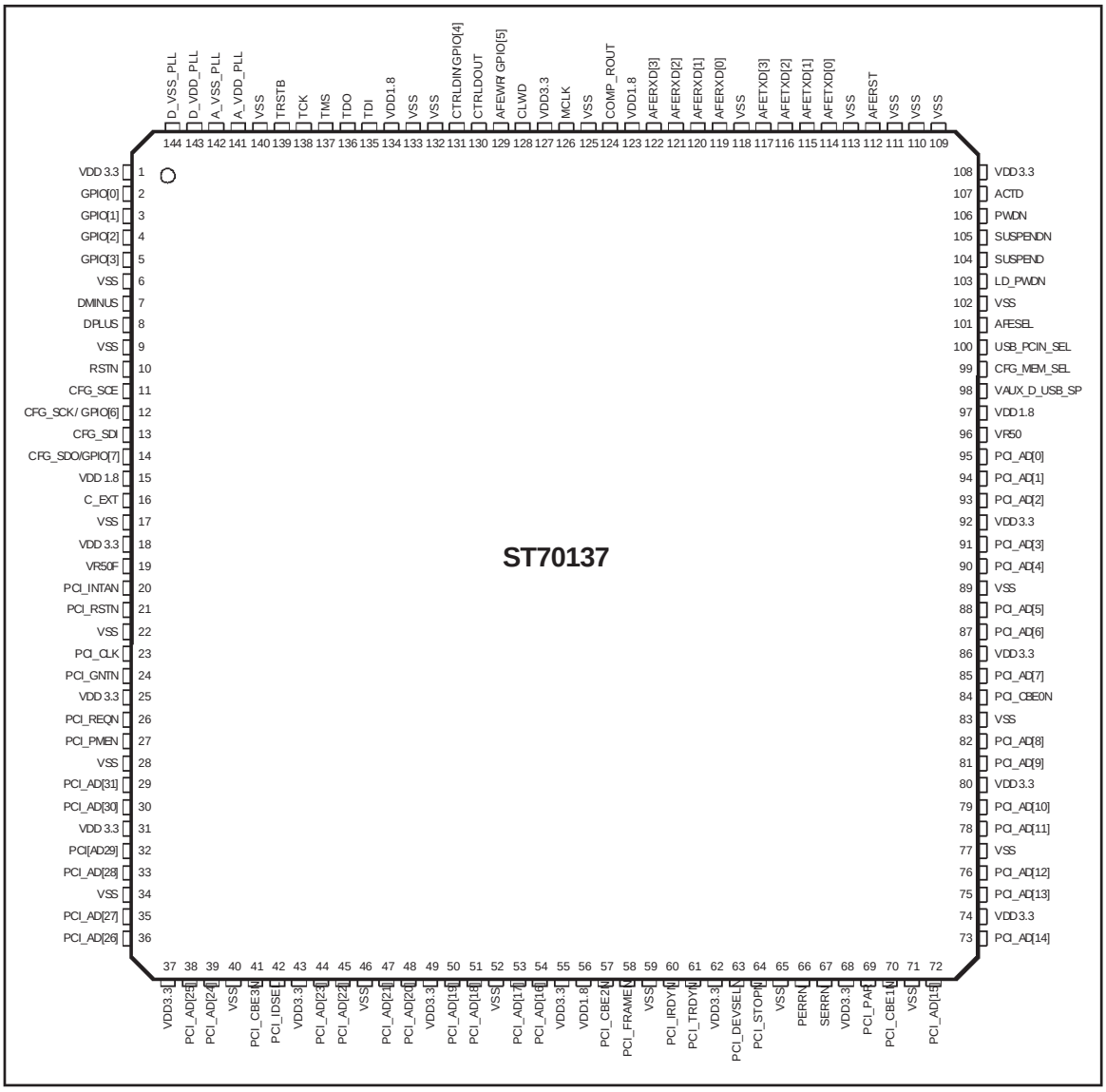


OBC: On Board Controller
TGB: Time Generation Block
TAP: Test Access Protocol
Utop FSM: Utopia Finite State Machine

SOFTWARE ARCHITECTURE



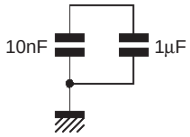
PIN CONNECTIONS



PIN LIST

PIN	NAME	TYPE	DRIVE	DESCRIPTION
1	VDD3.3	P		Power supply pins 3.3V for I/O pads (not PCI)
2	GPIO[0]	I/O	4mA	
3	GPIO[1]	I/O	4mA	
4	GPIO[2]	I/O	4mA	
5	GPIO[3]	I/O	4mA	
6	VSS	P		Ground
7	DATA_MINUS	I/O		
8	DATA_PLUS	I/O		
9	VSS	P		Ground
10	RSTN	I		
11	CFG_SCE	O	4mA	
12	CFG_SCK/GPO[6]	O	4mA	
13	CFG_SDI	I		
14	CFG_SDO/GPO[7]	O	4mA	
15	VDD 1.8	P		Power supply pins 1.8V for Core
16	C_EXT	P		External Capacitor to reduce ripple of the internal DC regulator [1]
17	VSS			Ground
18	VDD3.3	P		Power supply pins 3.3V for PCI I/O pads ESD protection
19	VR50F	P		Power Supply for DC regulator (3.3V)
20	PCI_INTAN	OD	8mA	Low, High Impendance
21	PCI_RSTN	I		
22	VSS	P		Ground
23	PCI_CLK	I		
24	PCI_GNTN	I		
25	VDD3.3	P		Power supply pins 3.3V for PCI I/O pads ESD protection
26	PCI_REQN	O	8mA	
27	PCI_PMEN	OD	8mA	
28	VSS	P		Ground
29	PCI_AD[31]	I/O	8mA	
30	PCI_AD[30]	I/O	8mA	
31	VDD3.3	P		Power supply pins 3.3V for PCI I/O pads
32	PCI_AD[29]	I/O	8mA	
33	PCI_AD[28]	I/O	8mA	
34	VSS	P		Ground

Note 1. Pin C_EXT must be connected:



PIN LIST (continued)

PIN	NAME	TYPE	DRIVE	DESCRIPTION
35	PCI_AD[27]	I/O	8mA	
36	PCI_AD[26]	I/O	8mA	
37	VDD3.3	P		Power supply pins 3.3V for PCI I/O pads ESD Protection
38	PCI_AD[25]	I/O	8mA	
39	PCI_AD[24]	I/O	8mA	
40	VSS	P		Ground
41	PCI_CBE_N[3]	I/O	8mA	
42	PCI_IDSEL	I		
43	VDD3.3	P		Power supply pins 3.3V for PCI I/O pads ESD Protection
44	PCI_AD[23]	I/O	8mA	
45	PCI_AD[22]	I/O	8mA	
46	VSS	P		Ground
47	PCI_AD[21]	I/O	8mA	
48	PCI_AD[20]	I/O	8mA	
49	VDD3.3	P		Power supply pins 3.3V for PCI I/O pads ESD Protection
50	PCI_AD[19]	I/O	8mA	
51	PCI_AD[18]	I/O	8mA	
52	VSS	P		Ground
53	PCI_AD[17]	I/O	8mA	
54	PCI_AD[16]	I/O	8mA	
55	VDD3.3	P		Power supply pins 3.3V for PCI I/O pads
56	VDD1.8	P		Power supply pins 1.8V for Core
57	PCI_CBE_N[2]	I/O	8mA	
58	PCI_FRAMEN	I/O	8mA	
59	VSS	P		Ground
60	PCI_IRDYN	I/O	8mA	
61	PCI_TRDYN	I/O	8mA	
62	VDD3.3	P		Power supply pins 3.3V for PCI I/O pads ESD Protection
63	PCI_DEVSELN	I/O	8mA	
64	PCI_STOPN	I/O	8mA	
65	VSS	P		Ground
66	PCI_PERRN	I/O	8mA	
67	PCI_SERRN	I/O	8mA	
68	VDD3.3	P		Power supply pins 3.3V for PCI I/O pads ESD Protection
69	PCI_PAR	I/O	8mA	
70	PCI_CBE_N[1]	I/O	8mA	
71	VSS	P		Ground
72	PCI_AD[15]	I/O	8mA	
73	PCI_AD[14]	I/O	8mA	

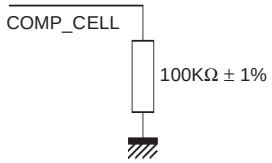
PIN LIST (continued)

PIN	NAME	TYPE	DRIVE	DESCRIPTION
74	VDD3.3	P		Power supply pins 3.3V for PCI I/O pads ESD Protection
75	PCI_AD[13]	I/O	8mA	
76	PCI_AD[12]	I/O	8mA	
77	VSS	P		Ground
78	PCI_AD[11]	I/O	8mA	
79	PCI_AD[10]	I/O	8mA	
80	VDD3.3	P		Power supply pins 3.3V for PCI I/O pads ESD Protection
81	PCI_AD[9]	I/O	8mA	
82	PCI_AD[8]	I/O	8mA	
83	VSS	P		Ground
84	PCI_CBE_N[0]	I/O	8mA	
85	PCI_AD[7]	I/O	8mA	
86	VDD3.3	P		Power supply pins 3.3V for PCI I/O pads
87	PCI_AD[6]	I/O	8mA	
88	PCI_AD[5]	I/O	8mA	
89	VSS	P		Ground
90	PCI_AD[4]	I/O	8mA	
91	PCI_AD[3]	I/O	8mA	
92	VDD3.3	P		Power supply pins 3.3V for PCI I/O pads ESD Protection
93	PCI_AD[2]	I/O	8mA	
94	PCI_AD[1]	I/O	8mA	
95	PCI_AD[0]	I/O	8mA	
96	VR50	P		3.3V Power supply for DC regulator
97	VDD1.8	P		Power
98	VAUX_D/USB_SP	I		
99	CFG_MEM_SEL	I		
100	USB_PCIN_sel	I		
101	AFESEL	I		
102	VSS	P		Ground
103	LPDWDN	O	4mA	
104	SUSPEND	O	4mA	
105	SUSPENDN	O	4mA	
106	PWDN	O	4mA	
107	ACTD	I		
108	VDD3.3	P		Power supply pins 3.3V for I/O pads (not PCI)
109	TEST	I/O		Test Reserved - Must be fixed to ground
110	TEST	I/O		Test Reserved - Must be fixed to ground
111	TEST	I/O		Test Reserved - Must be fixed to ground
112	AFERST	O	4mA	

PIN LIST (continued)

PIN	NAME	TYPE	DRIVE	DESCRIPTION
113	VSS	P		Ground
114	AFETXD[0]	O	8mA	
115	AFETXD[1]	O	8mA	
116	AFETXD[2]	O	8mA	
117	AFETXD[3]	O	8mA	
118	VSS	P		Ground
119	AFERXD[0]	I		
120	AFERXD[1]	I		
121	AFERXD[2]	I		
122	AFERXD[3]	I		
123	VDD1.8	P		Power supply pins 1.8V for Core
124	COMP_CELL	O		Compensation cell resistor [1]
125	VSS	P		Ground
126	MCLK	I		
127	VDD3.3	P		Power supply pins 3.3V for I/O pads (not PCI)
128	CLWD	I		
129	AFEWR/GPIO[5]	I/O	4mA	
130	CTRLDOUT	O	4mA	
131	CTRLDIN/GPIO[4]	I/O	4mA	
132	VSS	P		Ground
133	TEST	I/O		Test Reserved - Must be fixed to ground
134	VDD1.8	P		Power supply pins 1.8V for Core
135	TDI	I		
136	TDO	O	4mA	
137	TMS	I		
138	TCK	I		
139	TRSTB	I		
140	VSS	P		Ground
141	VDD_APLL	P		PLL Analog power supply 1.8V
142	VSS_APLL	P		PLL Analog Ground
143	VDD_DPLL	P		PLL digital power supply 1.8V
144	VSS_DPLL	P		PLL digital Ground

Note 1.



Note: PCI section from pin 16 to pin 96 (included): all the power supply pins (at 3.3V) included in this section are intented for PCI I/O pads.

PIN DESCRIPTION

Signal Name	Direction	Init Status	Polarity	Signal Description
PCI INTERFACE				
PCI_CLK	I	-	-	**PCI Clock. (33 MHz)** The rising edge of this signal is the reference upon which all the other PCI signals are based except for PCI_RSTN and PCI_INTAN. The maximum PCI_CLK frequency for ST70137 is 33MHz and the minimum is DC.
PCI_RSTN	I	I	L	**PCI Reset** Reset bring ST70137 in a known state: - All PCI bus output signal tri-stated - All open drain signals floated - All registers set to their factory defaults - All FIFOs emptied - GPIO signals tri-stated - Sachem Macrocell initialized - Clock of Adsl_Up stopped - AFE set in Power down mode
PCI_REQN	O	H	L	**PCI Request** This signal is sourced by an agent wishing to become a bus master. It is a point to point signal and each master has its own PCI_REQN.
PCI_GNTN	I	I	L	**PCI Grant** The PCI_GNTN signal is a dedicated, point-to-point signal provided to each potential bus master and signifies that access to the bus has been granted.
PCI_AD[31:0]	I/O	I	-	**PCI Multiplexed Address/Data Bus** Address and data are multiplexed on the same PCI bus pins. A PCI bus transaction consists of an address phase followed by the one or more data phase. An address phase occurs on the PCLK cycle in which PCI_FRAMEN is asserted. A data phase occurs on PCLK cycles in which PCI_IRDYN and PCI_TRDYN are both asserted.

PIN DESCRIPTION (continued)

Signal Name	Direction	Init Status	Polarity	Signal Description
PCI_CBE_N[3:0]	I/O	I	L	**PCI Multiplexed Bus Command Mode** Bus command and byte enables are multiplexed on the same pins. These pins define the current bus command during an address phase. During a data phase, these pins are used as Byte Enables, with PCI_CBE_N[0] (LSB) enabling byte 0 and PCI_CBE_N[3] enabling byte 3 (MSB). **C/BE[3:0]=Command Type** 0000 = Interrupt Acknowledge 0001 = Special Cycle 0010 = I/O Read 0011 = I/O Write 0100 = Reserved 0101 = Reserved 0110 = Memory Read 0111 = Memory Write 1000 = Reserved 1001 = Reserved 1010 = Configuration Read 1011 = Configuration Write 1100 = Memory Read Multiple 1101 = Memory Write Multiple 1110 = Memory Read line 1111 = Memory Write and Invalidate
PCI_PAR	I/O	I	H	**PCI Parity (even)** Parity is always driven as even from all PCI_AD[31:0] and PCI_CBE[3:0] signals. The parity is valid during the clock following the address phase and is driven by the bus master. During a data phase for write transactions, the bus master sources this signal on the clock following PCI_IRDYN active; during data phase for read transactions, this signal is driven by the target and is valid on the clock following PCI_TRDYN active. The PCI_PAR signal has the same timing as PCI_AD[], delayed by one clock.
PCI_FRAMEN	I/O	I	L	**PCI Cycle Frame** This signal is driven by current bus master to indicate the beginning and duration of a bus transaction. When PCI_FRAMEN is first asserted, it indicates a bus transaction is beginning with a valid addresses and bus command present on PCI_AD[31:0] and PCI_CBE[3:0]. Data transfer continue until PCI_FRAMEN is asserted. PCI_FRAMEN de-assertion indicates the transaction is in final data phase or has completed.
PCI_DEVSELN	I/O	I	L	**PCI Device Select** This signal is driven by a target decoding and recognizing its bus address. This signal informs a bus master whether an agent has decoded a current bus cycle.
PCI_IRDYN	I/O	I	L	**PCI Initiator Ready** This signal is always driven by the bus master to indicate its ability to complete the current data phase. During write transactions it indicates PCI_AD[] contains valid data.
PCI_IDSEL	I	I	H	**PCI Initialization Device Select** This pin is used as chip select during configuration read or write transactions.

PIN DESCRIPTION (continued)

Signal Name	Direction	Init Status	Polarity	Signal Description
PCI_TRDYN	I/O	I	L	**PCI Target Ready** This signal is driven by the select target to indicate the target is able to complete the current data phase. During read transactions, it indicates PCI_AD[] contains valid data. Wait states occur until both PCI_TRDYN and PCI_IRDYN are asserted togheter.
PCI_PERRN	I/O	I	L	**PCI Parity Error** Only for reporting data parity errors for all bus transactions except for special cycles. It is driven by the agent receiving data two clock cycles after the parity was detected as an error. This signal is driven inactive (high) for one clock cycle prior to returning to the tri-state condition.
PCI_SERRN	O	Z	L	**PCI System Error** Used to report address and data parity errors on special cycle commands and any other error condition having a catastrophic system impact.
PCI_INTAN	O	Z	L	**PCI Interrupt A** This signal is defined as optional and level sensitive. Driving it low will interrupt to the host. The PCI_INTAN interrupt is to be used for any single function device requiring an interrupt capability.
PCI_PMEN	O	Z	L	**PCI Power Management Event** This signal is used to indicate that a power management event has been detected. The PCI_PMEN signal is asynchronous with respect to the PCI clock; it is set (if enabled) by the low to high transition of the ACTD signal.
PCI_STOPN	I/O	I	L	**PCI Stop** This signal indicates the current target is requesting the master to stop the current transaction.
USB INTERFACE				
DPLUS	I/O	I	+	Differential positive USB data input/output.
DMINUS	I/O	I	-	Differential negative USB data input/output.
MISCELLANEOUS INTERFACE				
GPIO[3:0]	I/O	I	-	**General Purpose I/O Bus** These signals are controlled by internal registers located inside ADSL uP block. At the Power-up, Hardware or Software Reset the input direction is chosen.
CFG_MEM_SEL	I	I	-	Select Internal [1] or External [0] PCI/USB configuration memory.
USB_PCIN_sel	I	I	-	**Select PCI [0] or USB [1] Interface** Selecting USB interface and if all Test Pins are set to default value, all the PCI Pads are deactivated. The power supply for this section can be not provided. The PCI section is frozen. Selecting PCI interface the DMINUS and DPLUS has to be set to the low level (reset mode). The PLL is in power down and no any clock will be provided to the USB section.
VAUX_D / USB_SP	I	I	-	VAUX Detect when USB_PCIN_sel = [0] or USB SELF POWERED when USB_PCIN_sel = [1].

PIN DESCRIPTION (continued)

Signal Name	Direction	Init Status	Polarity	Signal Description
CLOCK & RESET INTERFACE				
MCLK	I	I	-	35.328 MHz Master Input Clock.
RSTN	I	I	L	Asynchronous Master Input Reset (active if USB_PCI_SEL = '1').
AFE INTERFACE				
AFETXD[3:0]	O	L	-	**AFE Transmit Data Nibble Bus** The signal changes are synchronized to the rising edge of MCLK clock signal.
AFERXD[3:0]	I	I	-	**AFE Receive Data Nibble Bus** The signal changes are synchronized to the rising edge of MCLK clock signal.
CLWD	I	I	H	**Start of word indication** This signal is the word clock used to enable shift of data. It occurs on CTRLDOUT signal to indicate the first data of the nibble sequence. The CLWD frequency is equal to MCLK/4.
CTRLDOUT	O	H	L	**Transmit Control Word Data to AFE** The data is shifted out from internal register on the rising edge of MCLK during CLWD assertion.
AFESEL	I	I	-	Select ST-70136 [0] or ADSL_C [1].
AFERST	O	L	L	**AFE Reset** This signal is connected to the internal PCFW (USB_PCIN_SEL = [0]) or UCFW registers (USB_PCIN_SEL = [1]) if AFESEL = [0], or to the Sachem GPOUT register if AFESEL = [1]. Not usable in USB mode.
AFEWR / GPIO[5]	I/O	I	L/-	**AFE Write control output signal** (AFESEL = 0), or General Purpose I/O pin. The selection is performed writing the proper bit in the PCFW or UCFW (depending on status of USB_PCIN_SEL pin) registers. At the power-on or hardware reset the GPIO[5] function is selected.
CTRLDIN / GPIO[4]	I	I	L/-	**Receive Control word data from AFE** (AFESEL = 0), or General Purpose I/O pin. The selection is performed writing the proper bit in the PCFW or UCFW (depending on status of USB_PCIN_SEL pin) registers. At the power-on or hardware reset the GPIO[4] function is selected ACTD I I H Activation Tone Detect [1] (or Wake Up signal). When PCI IF has been selected, the Low to High transition of ACTD asserts the PCI_PMEN signal (if this last has been enabled) and generates an interrupt event. When USB IF has been selected, the Low to High transition of ACTD de-asserts the SUSPEND signal and re-enable the internal ST70137 activity.
SUSPEND	O	L	H	Suspend Mode Indication.
SUSPENDN	O	H	L	Suspend Mode Indication Negated.
PWDN	O	H	H	AFE Power Down.
LDPWDN	O	H	H	Line Driver Power Down [1].

PIN DESCRIPTION (continued)

Signal Name	Direction	Init Status	Polarity	Signal Description
CFG_MEM INTERFACE				
CFG_SCE	O	L	H	**Chip Enable** This pin is designed to directly interface to a serial EEPROM that use the 93C66 EEPROM interface protocol. This pin has to be connected directly to the EEPROM's chip select pin.
CFG_SCK/GPO[6]	O	L	-	**Serial Clock** or General Purpose Output Pin 6 depending on the internal selection. The selection is performed writing the proper bit inside the PCFW or UCFW register. At the power-on or hardware reset the CFG_CLK functionality is selected. This pin is designed to directly interface to a serial EEPROM that use the 93C66 EEPROM interface protocol.
CFG_SDI	I	I	H	**Serial Data Input** Data going into this pin has to be generated on the rising edge of CFG_SCK. This pin is designed to directly interface to a serial EEPROM that use the 93C66 EEPROM interface protocol.
CFG_SDO/GPO[7]	O	L	-	**Serial Data/Address Output** General Purpose Output Pin 7 depending on the internal selection. The selection is performed writing the proper bit inside the PCFW or UCFW register. At the power-up or hardware reset the CFG_SDO functionality is selected. The CFG_SDO data change is synchronous with the falling edge of CFG_SCK. This pin is designed to directly interface to a serial EEPROM that use the 93C66 EEPROM interface protocol.
JTAG INTERFACE				
TDI	I	IH	-	JTAG Test Data Input.
TDO	O	-	-	JTAG Test Data Output.
TMS	I	IH	L	JTAG Test Mode Select.
TCK	I	IL	-	JTAG Test Clock.
TRSTB	I	IL	L	JTAG Reset (active Low).

TEST CONDITION

All Ouputs have been loaded with.

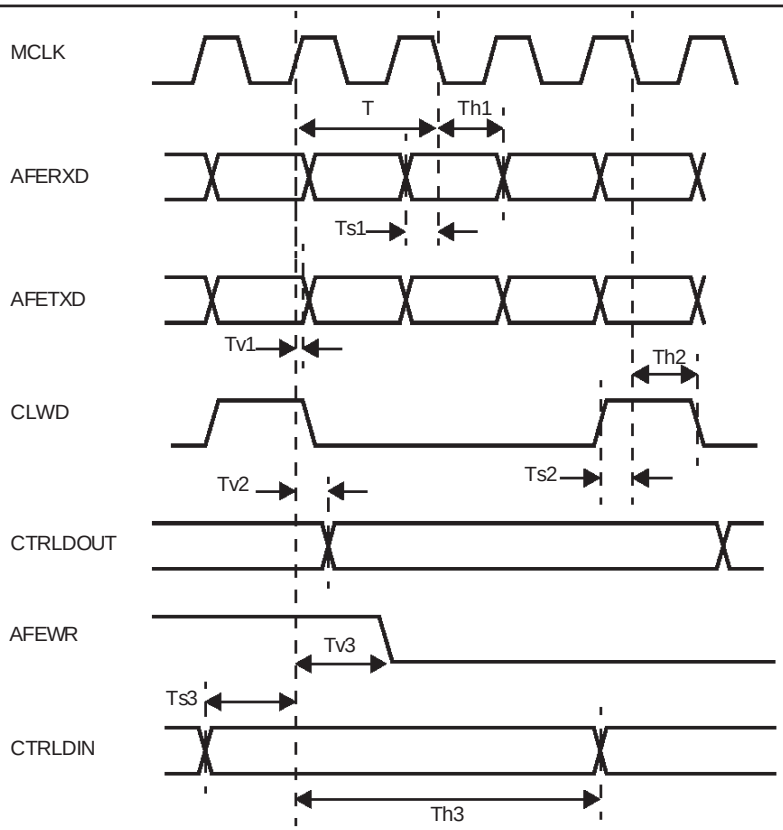
Outputs	Minimum	Maximum	Unit
PCI	0	50	pF
USB *	0	50	pF
Others	0	15	pF

** See text scheme at page 20.*

TIMING SPECIFICATION

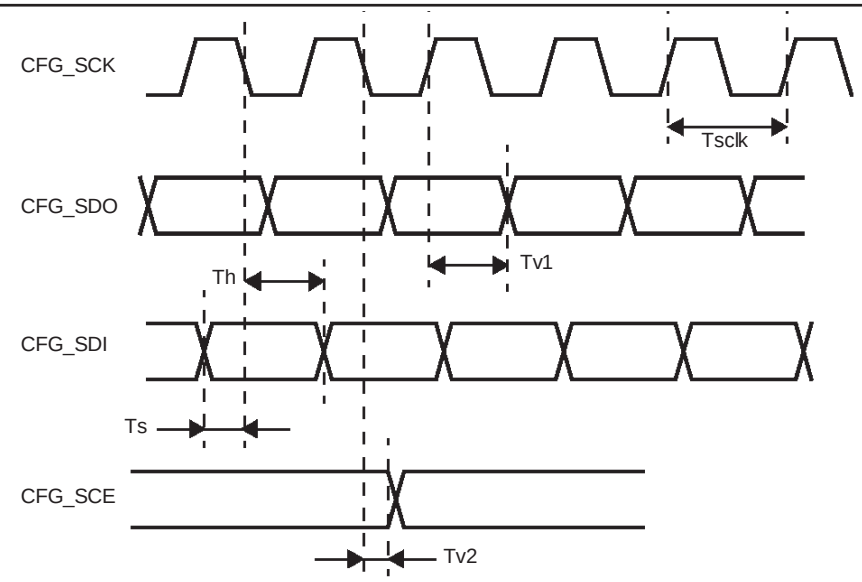
MCLK Master Clock					
Symbol	**Parameter**	**Minimum**	**Typical**	**Maximum**	**Unit**
F	Clock frequency		35.328		MHz
T	Clock Period		28.3		ns
Th	Clock Duty cycle	40		60	%

AFE IF Transmit & Receive Signals



AFE IF Transmit & Receive signals					
Ts1	Data Setup Time	5			ns
Th1	Data Hold Time	7			ns
Tv1	Data Valid Time			13	ns
Ts2	Data Setup Time	5			ns
Th2	Data Hold Time	6			ns
Tv2	Data Valid Time			18	ns
Ts3	Data Setup Time	20			ns
Th3	Data Hold Time	1			ns
Tv3	Data Valid Time			18	ns

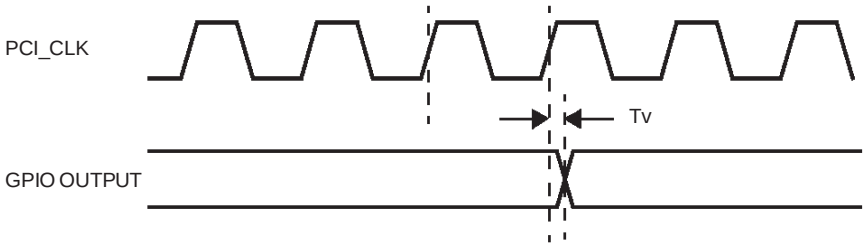
CFG_MEM IF Signals with PCI = 30.3ns



CFG_MEM IF signals with PCI = 30.3ns *					
Symbol	**Parameter**	**Minimum**	**Typical**	**Maximum**	**Unit**
Ts	Data Setup Time	45			ns
Th	Data Hold Time	0			ns
Tv1	Data Valid Time			970	ns
Tv2	Data Valid Time			160	ns
Tsck	SCK Clock period: - USB 48MHz - PCI 33MHz		USB_CLK / 64 PCI_CLK / 64		ns

** PCI conditions are more restrictive than USB conditions.*

GPIO IF



GPIO IF					
Symbol	**Parameter**	**Minimum**	**Typical**	**Maximum**	**Unit**
Tv	Output Data Valid from PCI_CLK			22	ns

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Description	Minimum	Typical	Maximum	Units
V_{DD} 3.3	Supply Voltage	3.0	3.3	3.6	V
V_{DD} 1.8	Supply Voltage	1.62	1.8	1.98	V
Ptot	Total Power Dissipation			450	mW
Tamb	Ambient Temperature 1.5ml airflow	0		70	°C
Tstg	Storage Temperature	-65		+150	°C
V_{ESD}	ESD Protection (HBM)	2000			V

PCI Interface DC Specifications

Parameter	Description	Condition	Minimum	Typical	Maximum	Units
Vilp	Input LOW Voltage		-0.5		$0.3V_{DD}$	V
Vihp	Input HIGH Voltage		$0.5V_{DD}$		V_{DD}+0.5	V
Iip	Input Leakage Current	$0<Vin<V_{DD}$	-10		10	µA
Volp	Output LOW Voltage	Iout = 1.5mA			$0.1V_{DD}$	V
Vohp	Output HIGHT Voltage	Iout = 0.5mA	$0.9V_{DD}$			V
Cinp	Input Pin Capacitance *				10	pF
Cclkp	CLK Pin Capacitance *		5		12	pF
Cidsel	IDSEL Pin Capacitance *				8	pF
Lpinp	Pin Inductance *		N/A		20	nH

** Guaranted by design.*

USB Interface DC Specifications

Nominal DC Characteristics (DPLUS, DMINUS)

Parameter	Description	Minimum	Typical	Maximum	Units
V_{DI}	Differential Input Sensitivity [(D+) - (D-)]	0.2			V
V_{CM}	Differential Common Mode Range	0.8		2.5	V
V_{SE}	Single Ended Receiver Threshold	0.8		2	V
V_{OH} V_{OL}	High Level Output Static Voltage (RL of 15KΩ to GND Low Level Output Static Voltage (RL of 1.5KΩ to 3.6V)	2.8		3.6 0.3	V V
I_{LO}	Hi-Z State Data Line Leakage Current (0V < Vin < 3.3V)			30	µA
C_{IN}	Transceiver Capacitance (Pin to GND) *			10	pF
R_D	Driver Output Resistance (steady state drive)	28		44	Ω

** Guaranted by design.*

Other Signals DC Characteristics

The values presented in the following table apply for all inputs and/or outputs unless otherwise specified. All voltages are referenced to V_{SS}, unless otherwise specified, positive current is towards the device.

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Units
I_{IN}	Input Leakage Current	Vin = V_{SS}, V_{DD} no pull up/pull down	-4		+4	µA
I_{OZ}	Tristate Leakage Current	Vin = V_{SS}, V_{DD} no pull up/pull down	-4		+4	µA
I_{PU}	Pull Up Current	Vin = V_{SS}	-15	-40	-125	µA
I_{PD}	Pull Down Current	Vin = V_{DD}	+15	+30	+125	µA

Suspend Mode Current Consumption

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Units
I_{518}	Suspend Mode Current Consumption on 1.8V	Temperature = 25°C		350		µA
I_{533}	Suspend Mode Current Consumption on 3.3V	Temperature = 25°C		150		µA

AC Specifications

PCI Signaling AC Specifications

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Units
Ioh	Switching Current High	0 < Vout ≤ 0.3V_{DD}	-12V_{DD}			mA
		Vout = 0.7V_{DD}			-32V_{DD}	mA
Iol	Switching Current Low	V_{DD} > Vout ≥ 0.6V_{DD}	16V_{DD}			mA
		Vout = 0.18V_{DD}			38V_{DD}	mA
Icl	Low Clamp Current *	-3 < Vin ≤ -1V	-25 + (Vin + 1) / 0.015			mA
Ich	High Clamp Current *	V_{DD} + 4 > Vin ≥ V_{DD} + 1	25 + (Vin - V_{DD} - 1) / 0.015			mA
Tr	Unloaded Output Rise Time *	0.2V_{DD} to 0.6V_{DD}	1		4	V/ns
Tf	Unloaded Output Fall Time *	0.6V_{DD} to 0.2V_{DD}	1		4	V/ns

** Guaranted by design.*

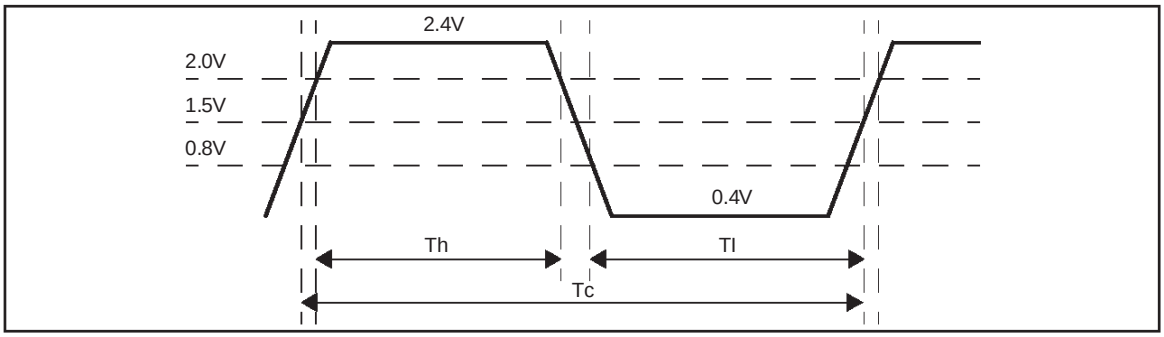
Timing Specifications

PCI Clock Specifications

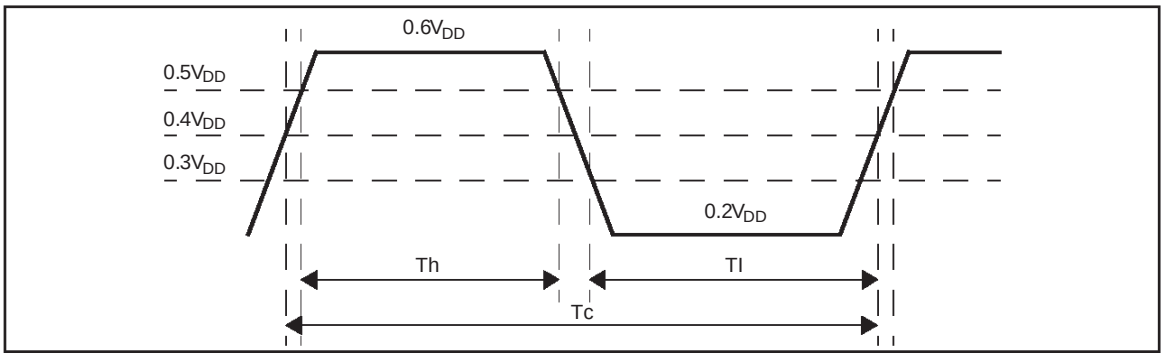
Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Units
Tc	Clock Cycle Time		30		50	ns
Th	Clock High Time		11			ns
Tl	Clock Low Time		11			ns
	Clock Slew Rate *		1		4	V/ns

** Guaranted by design.*

PCI Clock Waveform 5V



PCI Clock Waveform 3.3V

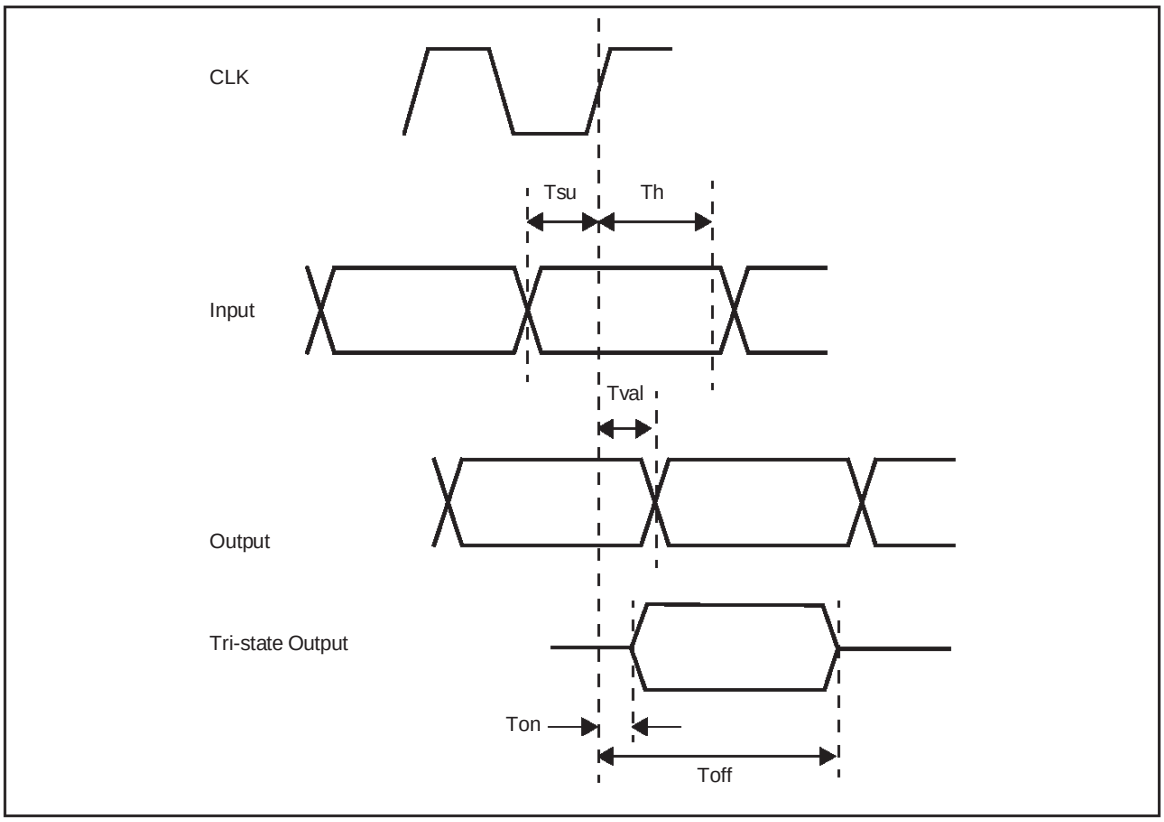


PCI Timings

Symbol	Parameter	Minimum	Typical	Maximum	Units
Tval	Clock to Signal Valid Delay (bused signals)	2		11	ns
Tval(ptp)	Clock to Signal Valid Delay (point to point)	2		12	ns
Ton	Float to Active Delay	2			ns
Toff	Active to Float Delay			28	ns
Tsu	Input Set up Time to Clock (bused signals)	7			ns
Tsu(ptp)	Input Set up Time to Clock (point to point) *	10, 12 *			ns
Th	Input Hold Time from Clock	0			ns
Trst	Reset Active Time after Power Stable	1			ms
Trst-clk	Reset Active Time after CLK Stable **	100			µs
Trst-off	Reset Active to Output Float Delay **			40	ns

** PCI REQN and GNTN are point-to-point signals and have different output valid delay and input setupt times than do bused signals. REQN has set up of 12ns and GNTN of 10ns. All other signals are bused.*

*** Guaranted by design.*

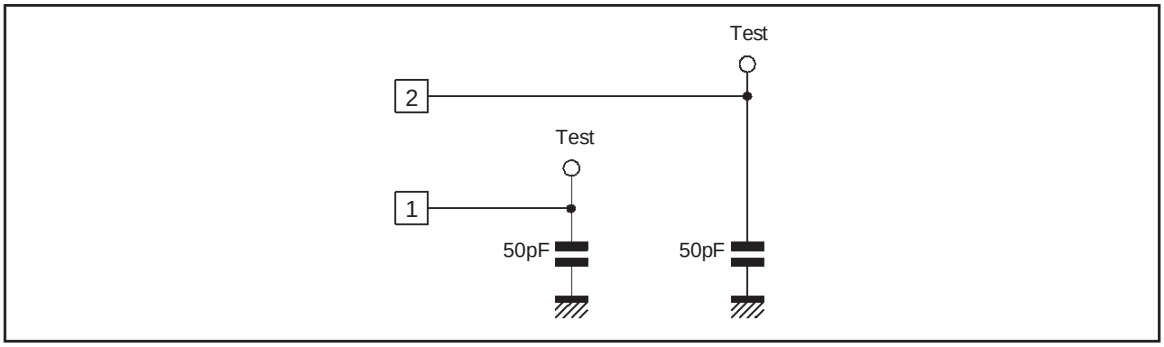


USB Interface AC Specifications (1.1 version)

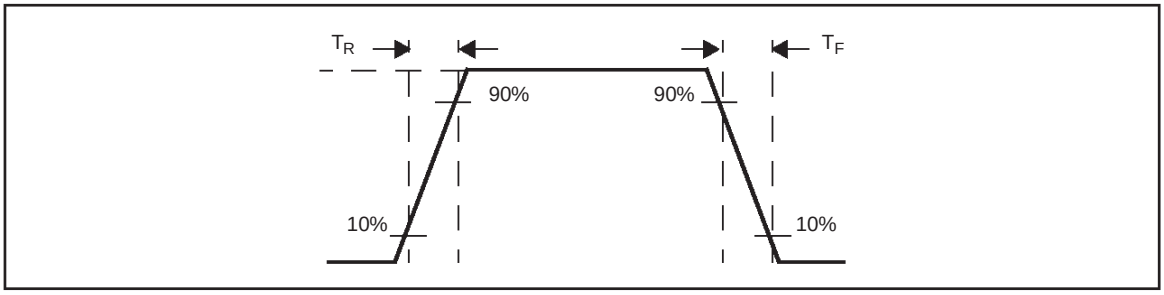
AC Characteristics (D+, D-)

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Units
t_{DR}	Average bit rate (12 M/s ±0.05%)		11.97		12.03	Mbps
t_R	Rise Time between 10% and 90% (see Figure Rise and Fall Time Measures)		4		20	ns
t_F	Fall Time 10% and 90% (see Figure Rise and Fall Time Measures)		4		20	ns
V_{CRS}	Output Signal Crossover Voltage		1.3		2	V

USB Test Scheme



Rise and Fall Time Measures



Input / Output TTL Generic Characteristics

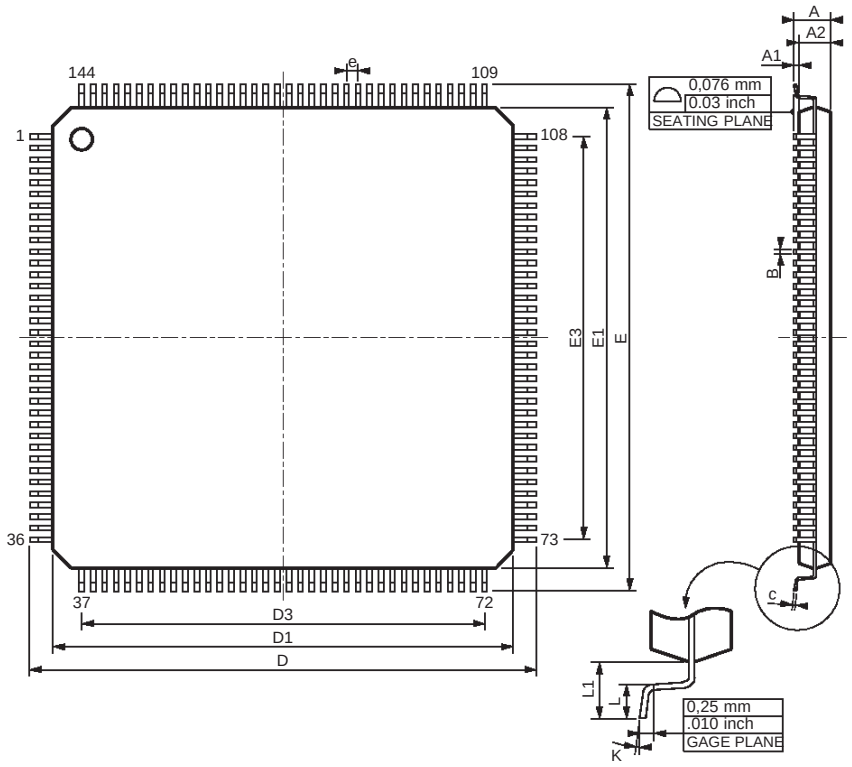
The value presented in the following table apply for all TTL inputs and/or outputs unless otherwise specified.

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Units
V_{IL}	Low Level Input Voltage				0.8	V
V_{IH}	High Level Input Voltage		2.0			V
V_{ILHY}	Low Level Threshold, falling *	Slow edge < 1V/µs	0.9		1.35	V
V_{IHHY}	Low Level Threshold, rising *	Slow edge < 1V/µs	1.3		1.9	V
V_{HY}	Schmitt Trigger Hysteresis *	Slow edge < 1Vµs	0.4		0.7	V
V_{OL}	Low Level Output Voltage	I_{OUT} = XmA (see Note)			0.4	V
V_{OH}	High Level Output Voltage	I_{OUT} = XmA (see Note)	2.4			V

** Guaranted by design.*

Note: The reference current is dependent on the exact buffer chosen and is a part of the buffer name. The available values are 2, 4 and 8mA.

PACKAGE MECHANICAL DATA (TQFP144 - 20 x 20 x 1.40 mm)



Dimension	Millimeters			Inches		
	Minimum	Typical	Maximum	Minimum	Typical	Maximum
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.0067	0.0087	0.011
C	0.09		0.20	0.0035		0.008
D		22.00			0.866	
D1		20.00			0.787	
D3		17.50			0.689	
e		0.50			0.020	
E		22.00			0.866	
E1		20.00			0.787	
E3		17.50			0.689	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0° (Min.), 7° (Max.)					