CY7C185A

8K x 8 Static RAM

Features

- **High speed**
  - **— 20 ns**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 743 mW**
- **Low standby Power**
  - **— 220 mW**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}_1$, CE_2 and $\overline{OE}$ features**
- **Automatic power-down when deselected**

Functional Description

The CY7C185A is a high-performance CMOS static RAM organized as 8192 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}_1$), an active HIGH chip enable (CE_2), an active LOW output enable ($\overline{OE}$), and three-state drivers. The device has an automatic power-down feature ($\overline{CE}_1$), reducing the power consumption by over 70% when deselected. The CY7C185A is in the standard 300-mil-wide DIP package and leadless chip carrier.

Writing to the device is accomplished when the chip enable one ($\overline{CE}_1$) and write enable ($\overline{WE}$) inputs are both LOW, and the chip enable two (CE_2) input is HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is written into the memory location specified on the address pins (A_0 through A_{12}).

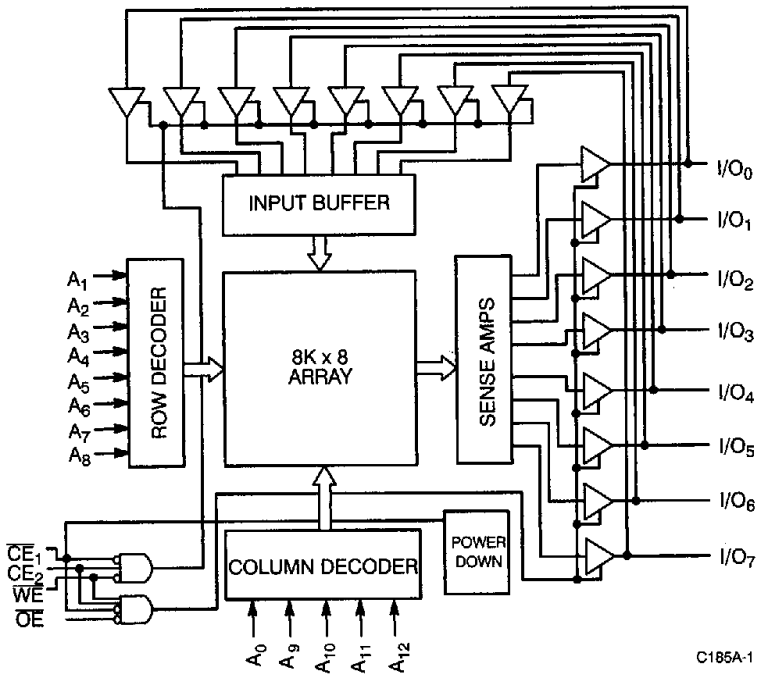
Reading the device is accomplished by taking chip enable one ($\overline{CE}_1$) and output enable ($\overline{OE}$) LOW, while taking write enable ($\overline{WE}$) and chip enable two (CE_2) HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the I/O pins.

The I/O pins remain in a high-impedance state when chip enable one ($\overline{CE}_1$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) or chip enable two (CE_2) is LOW.

A die coat is used to ensure alpha immunity.

2

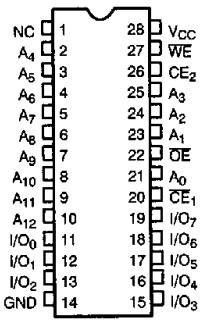
Logic Block Diagram



C185A-1

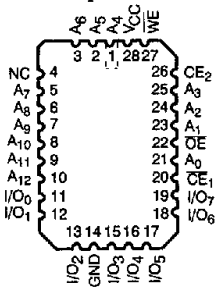
Pin Configurations

DIP
Top View



C185A-2

LCC
Top View



C185A-3

Selection Guide[1]

		7C185A–15	7C185A–20	7C185A–25	7C185A–35	7C185A–45
Maximum Access Time (ns)		15	20	25	35	45
Maximum Operating Current (mA)	Military	170	135	125	125	125
Maximum Standby Current (mA)	Military	40/20	40/20	40/20	30/20	30/20

Shaded area contains advanced information.

Note:

1. For commercial specifications, see the CY7C185 datasheet.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[2] ..... −0.5V to +7.0V

DC Input Voltage[2] ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL−STD−883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Military[3]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[4]

Parameter	Description	Test Conditions		7C185A−15 Min.	7C185A−15 Max.	7C185A−20 Min.	7C185A−20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]			−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			−350		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Military		170		135	mA
I_{SB1}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{IH}, Min. Duty Cycle = 100%	Military		40		40	mA
I_{SB2}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} − 0.3V V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≥ 0.3V	Military		20		20	mA

Shaded area contains advanced information.

Notes:

2. V_{IL} (min.) = − 3.0V for pulse durations less than 30 ns.
3. T_A is the "instant on" case temperature.
4. See the last page of this specification for Group A subgroup testing information.
5. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Electrical Characteristics Over the Operating Range[4] (continued)

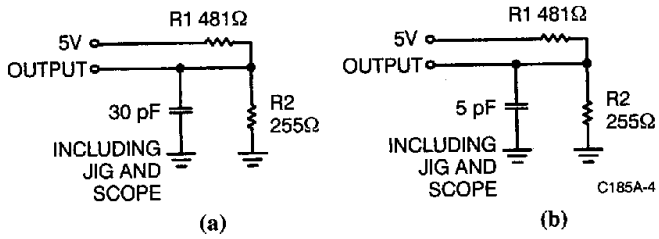
Parameter	Description	Test Conditions		7C185A–25 Min.	7C185A–25 Max.	7C185A–35, 45 Min.	7C185A–35, 45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[2]			−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Military		125		125	mA
I_{SB1}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{IH}, Min. Duty Cycle = 100%	Military		40		30	mA
I_{SB2}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≥ 0.3V	Military		20		20	mA

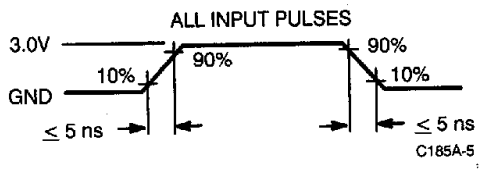
Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

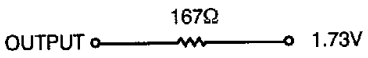
Note:
6. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3, 7]

Parameter	Description	7C185A–15		7C185A–20		7C185A–25		7C185A–35		7C185A–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	15		20		25		35		45		ns
t_{AA}	Address to Data Valid		15		20		25		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		3		ns
t_{ACE1}	$\overline{CE}_1$ LOW to Data Valid		15		20		25		35		45	ns
t_{ACE2}	CE_2 HIGH to Data Valid		15		20		25		35		30	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		7		10		12		15		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[8]		8		8		10		12		15	ns
t_{LZCE1}	$\overline{CE}_1$ LOW to Low Z[9]	3		5		5		5		5		ns
t_{LZCE2}	CE_2 HIGH to Low Z	3		3		3		3		3		ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High Z[8, 9] CE_2 LOW to High Z		8		8		10		15		15	ns
t_{PU}	$\overline{CE}_1$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH to Power-Down		15		20		20		20		25	ns
WRITE CYCLE[10]												
t_{WC}	Write Cycle Time	15		20		20		25		40		ns
t_{SCE1}	$\overline{CE}_1$ LOW to Write End	10		15		20		25		30		ns
t_{SCE2}	CE_2 HIGH to Write End	10		15		20		25		30		ns
t_{AW}	Address Set-Up to Write End	10		15		20		25		30		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		15		15		20		20		ns
t_{SD}	Data Set-Up to Write End	7		10		10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8]		7		7		7		10		15	ns

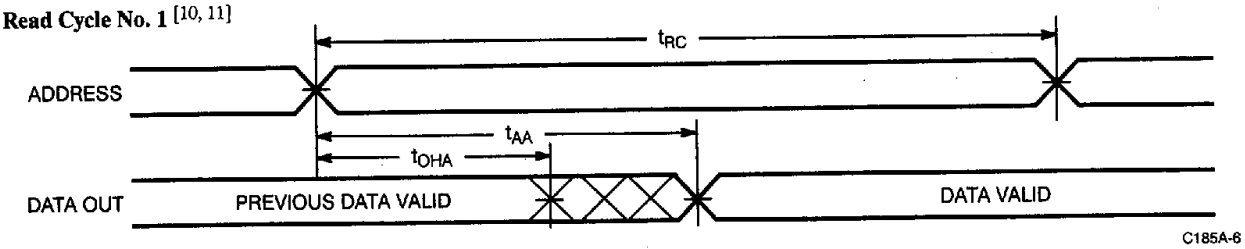
Shaded area contains advanced information.

Notes:

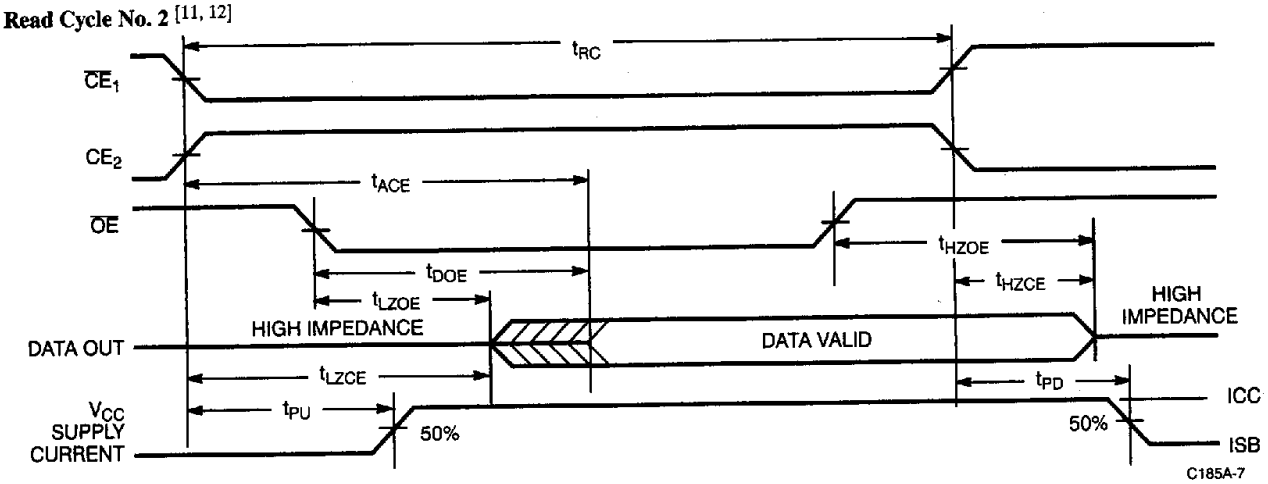
7. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
8. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
10. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}. CE_2 = V_{IH}.

Switching Waveforms

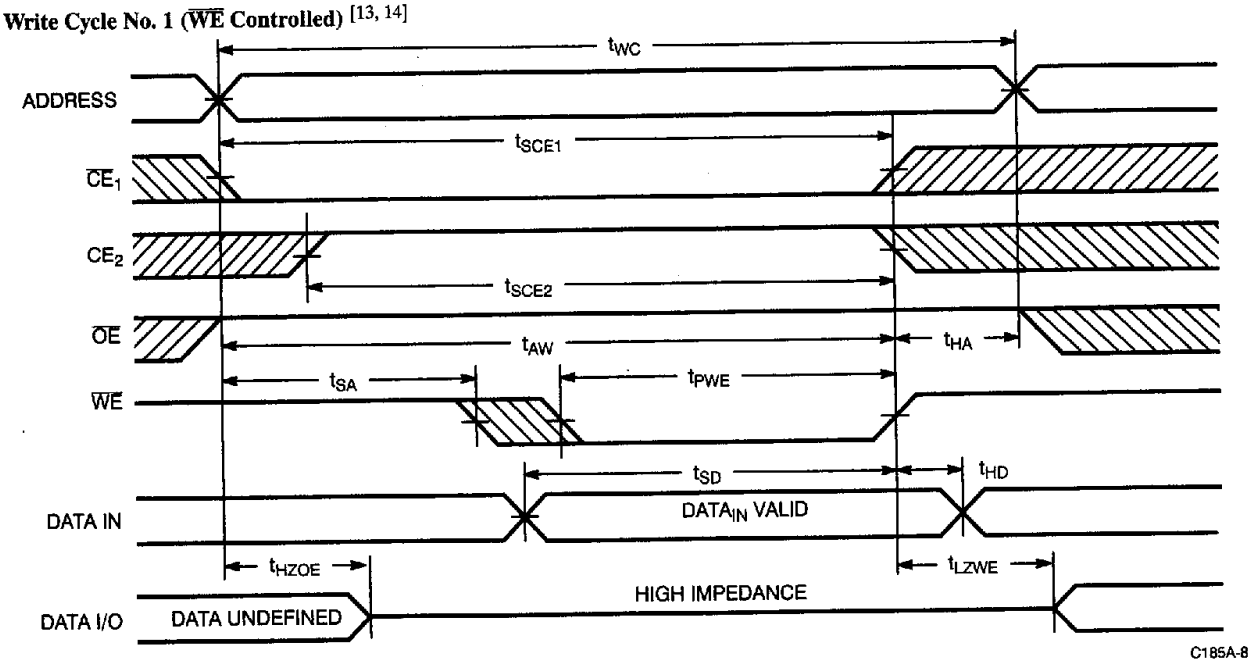
Read Cycle No. 1 [10, 11]



Read Cycle No. 2 [11, 12]



Write Cycle No. 1 ($\overline{WE}$ Controlled) [13, 14]

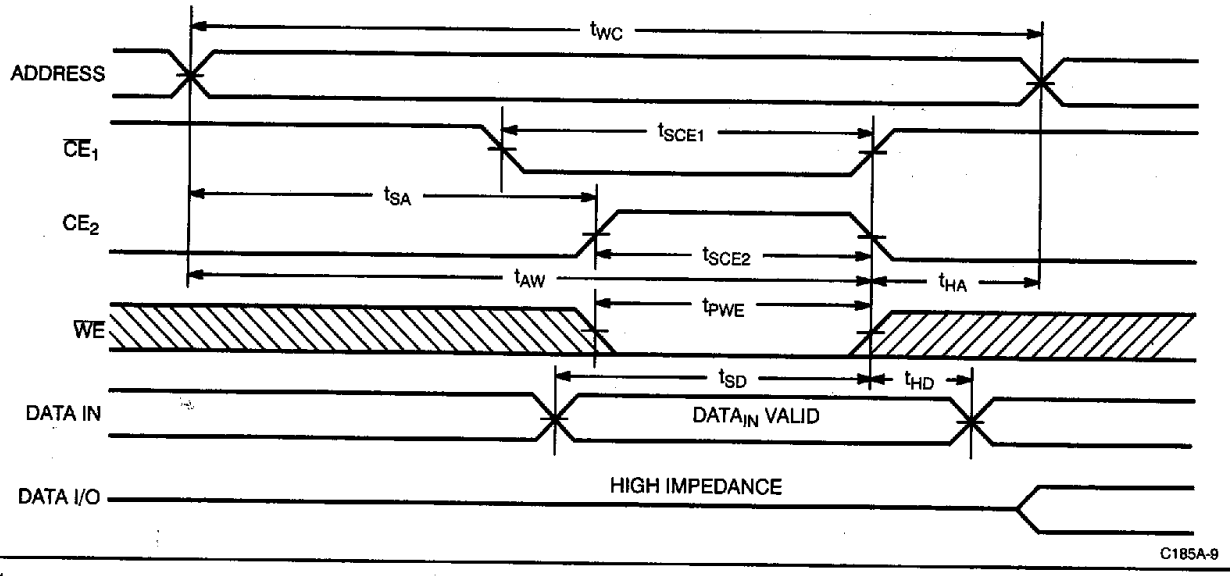


Notes:

11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
12. $\overline{WE}$ is HIGH for read cycle.
13. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
14. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.

Switching Waveforms (continued)

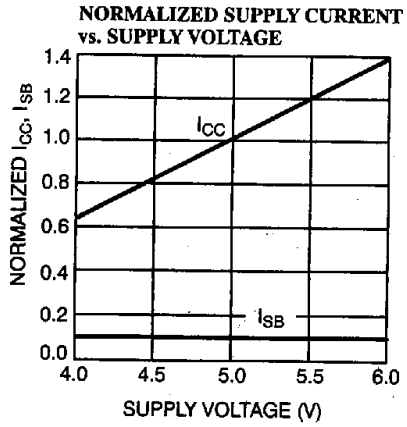
Write Cycle No. 2 ($\overline{CE}$ Controlled) [13, 14, 15]

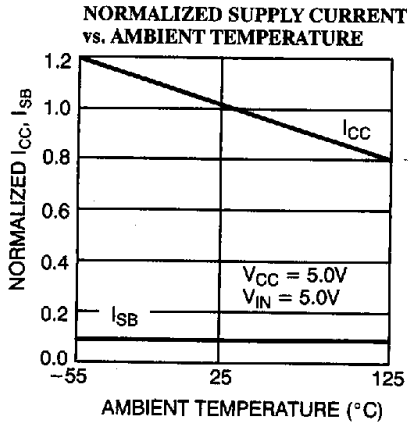


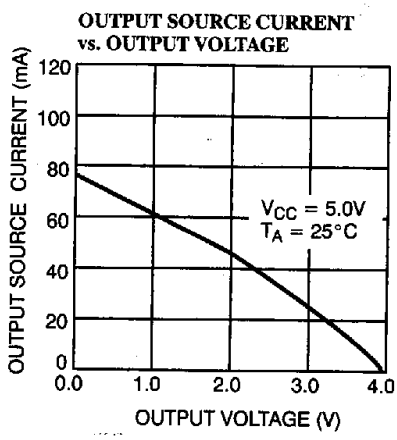
Note:

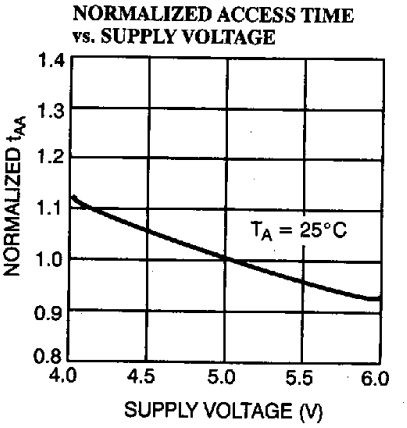
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

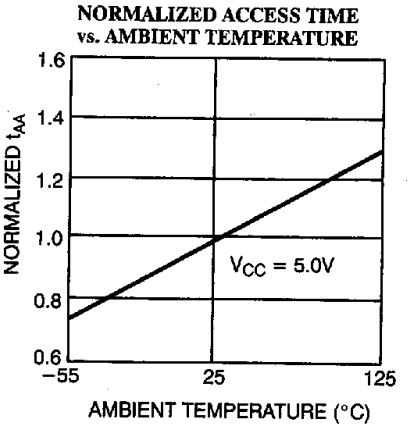
Typical DC and AC Characteristics

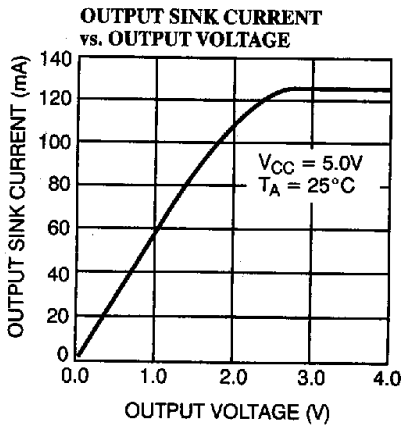






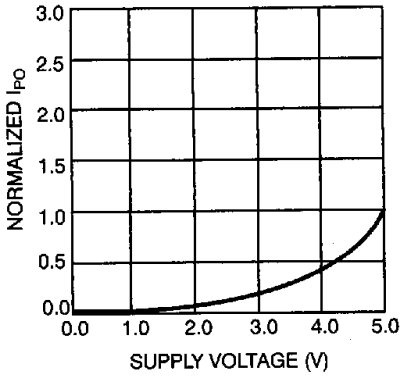




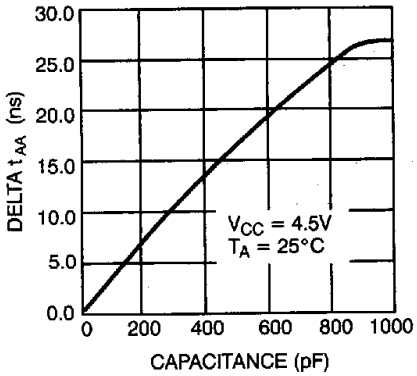


Typical DC and AC Characteristics (continued)

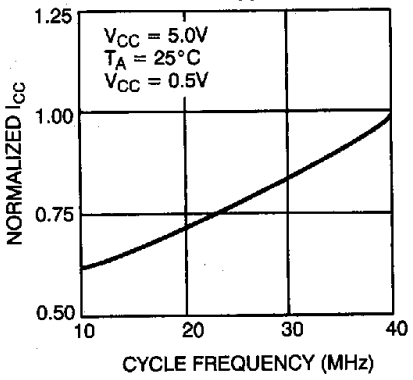
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Truth Table

$\overline{CE}_1$	CE_2	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode
H	X	X	X	High Z	Deselect/Power-Down
X	L	X	X	High Z	Deselect
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselect

Address Designators

Address Name	Address Function	Pin Number
A4	X3	2
A5	X4	3
A6	X5	4
A7	X6	5
A8	X7	6
A9	Y1	7
A10	Y4	8
A11	Y3	9
A12	Y0	10
A0	Y2	21
A1	X0	23
A2	X1	24

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C185A–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C185A–15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
20	CY7C185A–20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C185A–20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
25	CY7C185A–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C185A–25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
35	CY7C185A–35DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C185A–35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
45	CY7C185A–45DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C185A–45LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Shaded area contains advanced information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE1}	7, 8, 9, 10, 11
t_{ACE2}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE1}	7, 8, 9, 10, 11
t_{SCE2}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

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