TL3M Device
Triple Level 3 Mapper
TXC-03453B

DATA SHEET

FEATURES

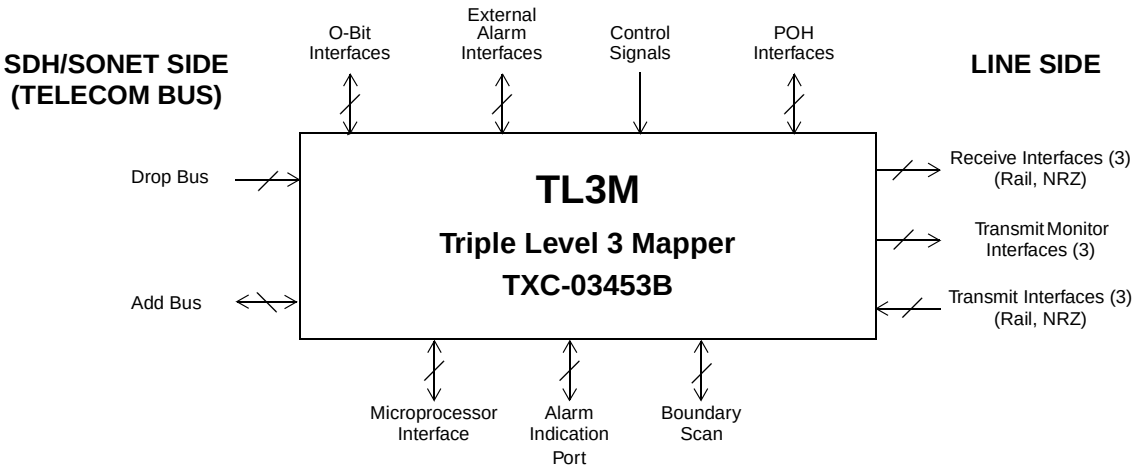
- Maps up to three independent DS3/E3 line formats into SDH/SONET formats as follows:
  - DS3 to/from STM-1/TUG-3
  - DS3 to/from STS-3/STS-1
  - E3 to/from STM-1/TUG-3
- SDH/SONET bus access:
  - Byte-wide drop and Add buses
  - Drop bus timing mode (Add bus timing derived from Drop bus)
  - Add bus timing mode (independent timing for drop/Add buses)
- Path overhead byte processing:
  - Microprocessor access
  - External interface
  - B3 generation/detection with test mask
  - B3 bit/block performance counters
  - REI bit/block performance counters
  - C2 mismatch detection
  - C2 unequipped detection and generation
- Alarm indication port
  - Path REI count and RDI status for APS applications
- O-bit channel access via external interface
- Digital desynchronizer with internal pointer leak algorithm
- Line interface:
  - NRZ or P/N rail option for transmit and for receive
  - Monitor NRZ transmit data
- Microprocessor access:
  - Motorola or Intel compatible
  - Hardware interrupt with mask bits
  - Software polling bits
- Testing:
  - Facility or line loopback
  - PRBS generator/analyzer
  - Boundary scan (IEEE 1149.1 standard)
- A fully tested device driver is available
- 3.3 volt power supply, 5 volt tolerant inputs
- 324-lead plastic ball grid array package (23 mm x 23 mm)

DESCRIPTION

Each of the three channels of the TL3M can map a DS3 line signal into an STM-1 TUG-3 or STS-3 STS-1 SPE SDH/SONET signal. An E3 signal can be mapped only into an STM-1 TUG-3. The TL3M interfaces to an STM-1 or STS-3 SDH/SONET signal using a byte- wide parallel interface in the TranSwitch Telecom Bus format. The TL3M supports Drop bus and Add bus SDH/SONET timing modes. Drop bus timing provides the timing signals for the add side. Timing for both buses is independent for the Add bus timing mode. Individual POH bytes are mapped into a RAM interface for microprocessor access and to an external interface for external processing if required. In the add direction (except for the B3 byte) POH bytes may be inserted individually from RAM locations, from the external interface, or from the local side/alarm indication port. An option is provided to generate an unequipped channel or AIS. An external interface is provided for accessing the O-bits. An alarm indication port is provided for ring operation. The TL3M also uses internal digital desynchronizers that have a built-in pointer leak algorithm. The line side can be configured for a NRZ or positive/negative rail interface. For testing purposes, the TL3M provides boundary scan, PRBS generators and analyzers, a BIP error mask, and DS3/E3 line and facility loopbacks. The TL3M provides either Motorola or Intel microprocessor access. The interrupt has programmable mask bits. A software polling register is also provided.

APPLICATIONS

- Add/drop multiplexers
- Digital cross connect systems
- Broadband switching systems
- Transmission equipment



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LIST OF FIGURES

FEATURES

The TL3M supports the following features. Please note that the convention used here is that the transmit (or add) direction is from the DS3/E3 line signal (rail or NRZ) to the SDH/SONET format (Telecom Bus), while the receive (or drop) direction is from the SDH/SONET format to the DS3/E3 line.

Bus Timing (Telecom Bus):

The TL3M provides the following bus timing modes for the Telecom Bus modes of operation:

- Drop bus timing
  - Add bus timing is derived from the Drop bus timing input signals
    - Drop bus: C1J1, SPE, optional C1, data, clock, and parity signals leads are inputs
    - Add bus: data, parity, and add indication signal leads are outputs
- Add bus timing
  - Add bus timing is supplied and is independent of the Drop bus timing
    - Drop bus: C1J1, SPE, optional C1, data, clock and parity signal leads are inputs
    - Add bus: clock, C1J1, and SPE signal leads are inputs; data, parity, and add indication signal leads are outputs

Mappings:

The TL3M provides the following mapping features:

- Maximum of three channels for either E3 or DS3 line signals
- STM-1 AU-4 VC-4 format
  - Each E3 or DS3 signal into TUG-3 format
- STS-3 format
  - Each DS3 signal into STS-1 format
- Same drop and Add bus for all channels
- Add bus contention indication (same channel assignment)
  - Add Bus: high impedance Add bus if there is contention
- Broadcast mode
  - Drop Bus: multiple channel assignment to the same TUG-3

SDH/SONET Rates:

The TL3M provides the following Telecom Bus rates and format mappings:

- STS-3 STS-1s (19.44 Mbyte/s)
- STM-1 VC-4 (19.44 Mbyte/s)

Other Telecom Bus Features:

The TL3M provides the following additional bus features:

- SDH/SONET interface Drop bus
  - Input parity check with alarm monitoring
    - Odd parity
    - Bus signals
  - Input loss of clock detection
    - Stuck high or low
  - Loss of J1 reference

    - Positive/negative justification count for J1 pulse
  - External path AIS and other alarm (e.g., LOP) indication
- SDH/SONET interface Add bus
  - Output parity generation
    - Odd parity
  - Bus indication (active low to indicate bus activity)
  - Ability to High-Z the output bus signals
    - Under processor control
  - Input loss of clock detection
    - Stuck high or low

SDH/SONET Processing Features

- In-band upstream path AIS detection
  - TOH E1 bytes
    - Majority vote
- TUG-3 pointer tracking
  - ETSI-based state machine
    - 8-bit PJ and NJ counters
    - NDF, LOP, and AIS alarm detection
- TUG-3 pointer generation
  - Slaved to drop or Add bus J1 pulse
  - Adjusts pointer accordingly
- POH byte processing (TUG-3, STS-1)
  - All receive POH bytes accessible
    - Microprocessor access
    - POH interface
  - J1 byte
    - 64-byte host processor read
  - B3 parity error check
    - Bit or block count
  - G1 byte
    - Single-bit RDI alarm detection with a 5 or 10 event option
    - REI (FEBE) counter (16 bits)
  - C2 byte
    - Signal label mismatch and unequipped detection
- POH byte Insertion (TUG-3, STS-1)
  - All POH bytes
    - Microprocessor access
    - POH interface
      - Control bits to determine source of input bytes
  - J1 byte
    - 64-byte message

  - G1 byte
    - Receive side or alarm indication port
      - REI (FEBE) insertion from B3 byte errors
      - Single-bit RDI insertion
  - C2 byte
    - Path label insertion
- SDH/SONET AIS generation
  - TUG-3s
- Unequipped channel generation
  - TUG-3s
- Desynchronizer
  - Meets ITU, ETSI, and ANSI performance requirements
    - Pointer test sequence
    - Jitter
  - Internal
    - Digital
    - Internal pointer leak algorithm or microprocessor control

O-Bit (Overhead Communications) Channel Access:

- Microprocessor access (two-bit field)
- Option for two reserved bits in the E3 format
- External serial bit interface (clock and data)
  - Gapped clock
  - Asynchronous

Line AIS Detection:

  - Transmit E3 AIS detection per ITU G.775

Line AIS Generation:

- Transmit and receive sides
- Generate as a result SDH/SONET alarms or line level alarms
  - Mask enable bits
  - Global enable bit
  - Microprocessor control

Line Interface:

- Rail interface
  - Clock, positive and negative rail signals
  - DS3/E3 loss of signal detection in transmit direction
  - BPV counter
  - DS3 B3ZS or E3 HDB3 codec function
  - Loss of clock detector
  - Invert clock polarity (receive and transmit)

- NRZ interface
  - Clock and data
  - Loss of Clock Detector
  - External interface for loss of signal (transmit direction)
  - Invert clock polarity (receive and transmit)
- High-Z output leads
  - Receive Line Outputs
  - Transmit Monitor Outputs
  - Per channel control via host
- Transmit Monitor Port
  - Clock and data

Test Features:

- Boundary Scan that meets IEEE 1149.1 standard
- High-Z all output leads option
- Loopbacks per channel
  - DS3/E3 line with generate receive AIS output option
  - DS3/E3 facility
- Pseudo-random test generator and analyzer per channel
  - 2^{15}-1, or 2^{23}-1
  - Uses CV counter to count errors
- B3 BIP-8 error mask
  - RAM value substituted
  - Column error control

Microprocessor Interface:

- Microprocessor
  - Split address/data buses
  - Selectable Intel or Motorola

Alarms And Interrupts:

- Hardware interrupt option
  - Mask bits
  - Positive level
- Software polling bit
- Latched and unlatched alarms
- Saturating or rollover counters option

Device Driver:

- Device configuration
- Fault monitoring
- Performance monitoring

APPLICATION EXAMPLES

The TL3M can be used in a wide range of telecommunications applications, such as:

- Add/drop multiplexers
- Digital cross connect systems
- Router systems
- Transmission systems

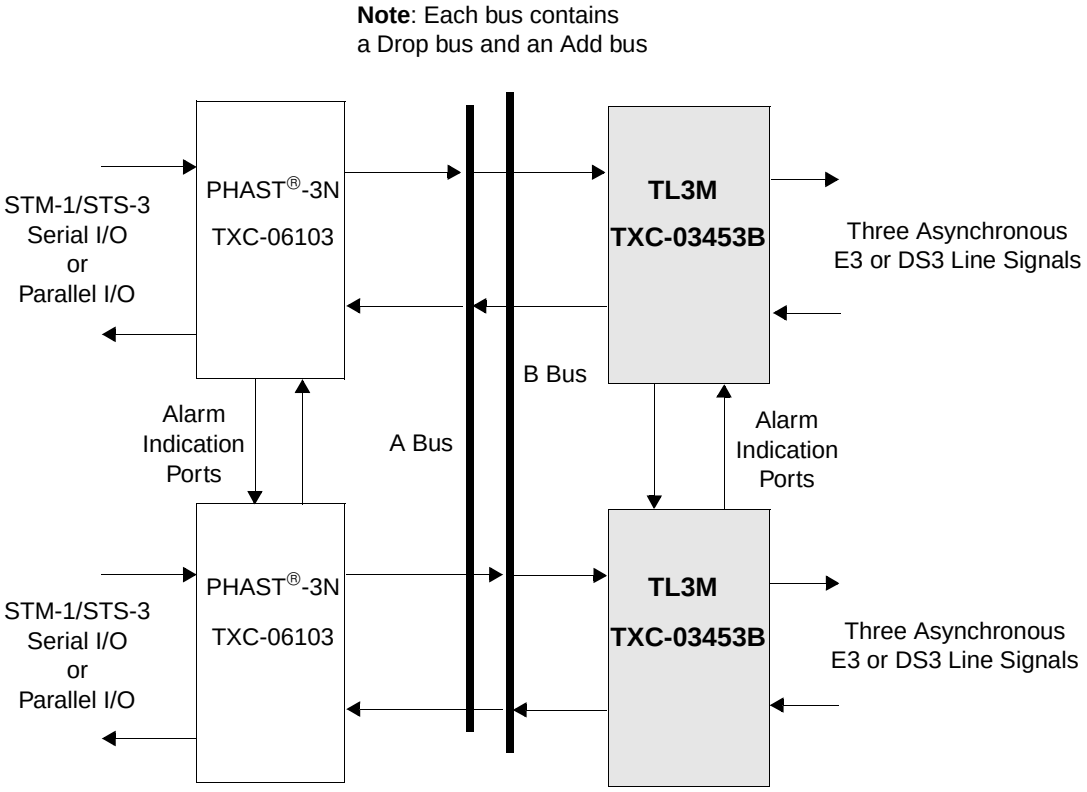


Figure 1. Typical Application using the TL3M and PHAST-3N Devices

Figure 1 shows a Telecom Bus bidirectional E3/DS3 add/drop STM-1/STS-3 multiplexer. The three E3's or DS3's may be dropped from either direction with full time slot reuse in both directions. If required, the asynchronous line interfaces for the two TL3M devices may be tied together. An option is provided in which the output line interface can be forced to the high impedance state.

BLOCK DIAGRAM

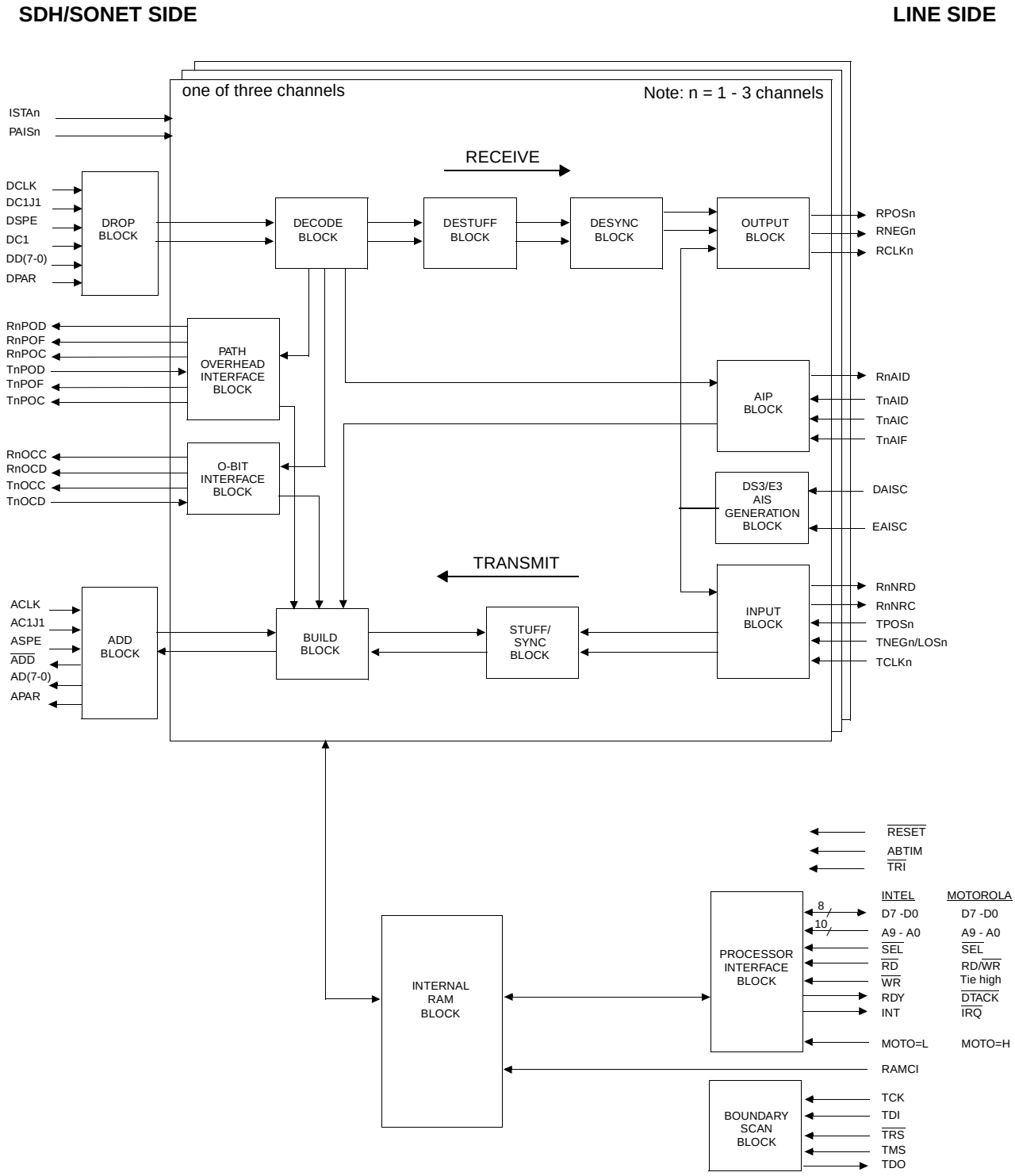
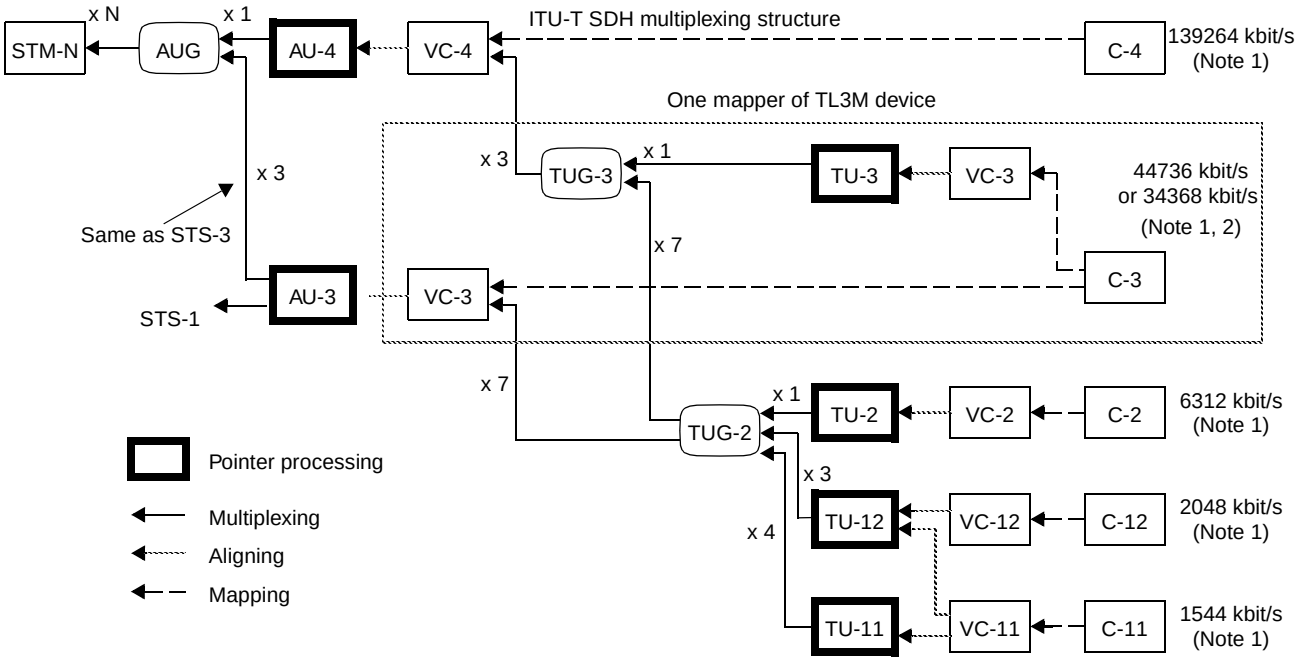


Figure 2. TL3M TXC-03453B Block Diagram

BLOCK DIAGRAM DESCRIPTION

A functional block diagram of the TL3M is shown in Figure 2. The portion of the ITU-T SDH multiplexing structure implemented by each Level 3 Mapper within the TL3M device is shown in Figure 3. Each of the three Level 3 mappers is multiplexed/demultiplexed from a SDH/SONET Telecom Bus interface which is carrying the three STS-3 STS-1s or STM-1 VC-4 TUG-3s.



Note 1: G.702 tributaries associated with containers C-x are shown. Other signals (e.g., ATM) can also be accommodated.
Note 2: AU-3/VC-3 is for DS3 only.

Figure 3. TL3M Multiplexing Structure

In the receive direction the drop side parallel Telecom Bus interface uses a bus signaling rate of 19.44 MHz. The parallel interface at the drop block consists of byte-wide input data (DD(7-0)), a C1J1 input indication (DC1J1), an SPE input indication (DSPE), input clock (DCLK), and input parity (DPAR). The C1 (J0) pulse, which is required, is used in conjunction with an active low SPE indication to determine the start of the SDH/SONET frame. The J1 pulse (in the DC1J1 signal) and an active high SPE indication determine the starting location of the VC-4 within the STM-1 format and also the start of each of the STS-1s in the STS-3 format. There are three J1 pulses required for the STS-3 format, and a single J1 pulse required for the STM-1 VC-4 format. The Drop bus clock (DCLK) is also monitored for a stuck high or low state. The data leads and other bus leads are calculated for odd parity and compared against the incoming input parity lead (DPAR) to determine if there is a parity error. Other than a parity error indication, no action is taken by the TL3M. The C1J1 pulse is also monitored for a loss of J1 pulse. An option is provided in which the C1 pulse can be supplied on a separate lead from the DC1J1 lead (DC1 lead).

The Decode block contains the logic for performing the pointer interpretation and tracking for each of the three TUG-3s, when the STM-1 VC-4 format is selected. The H1/H2 pointer bytes in each of the TUG-3s are monitored for loss of pointer, AIS, and a New Data Flag (NDF) indication. The pointer state machines are implemented using the algorithms specified in ETSI and ANSI documents. Performance counters are provided for justification events. The TL3M does not perform pointer tracking for the STS-1 signals, or for the VC-4 formats. Instead, the J1 indication is used as the start of format indication.

This block also performs SDH/SONET E1 byte AIS detection, which may be carrying an upstream in-band AIS indication. The TranSwitch PHAST-3N and SOT-3 devices have an option to generate an in-band line/path AIS indication for the downstream mappers, such as the TL3M, which enables line AIS to be generated without having to perform an additional pointer AIS detection. In addition, two leads are provided for an out-of-band upstream AIS indication, using either the PAISn or ISTAn leads.

The POH bytes from the TUG-3 or the STS-1 format are provided at the POH Interface block for external processing, if required. Each of the three mappers' POH interfaces consists of an output data lead (RnPOD), framing pulse (RnPOF) and a clock signal (RnPOC), where n represents each of three level 3 mappers, starting with channel 1. All the POH bytes in each of the STS-1s and TUG-3s are supplied, including the B3 byte.

All POH bytes from each of the TUG-3s or STS-1s are also written into Internal RAM block segments for microprocessor access. In addition, the J1 byte is written into a 64-byte RAM segment on an arbitrary address rotating basis. Each mapper section also performs POH byte processing, which includes RDI detection, C2 mismatch detection and unequipped detection.

The received O-bits for the DS-3 format are provided at the O-Bit Interface block and are also written into a 2-bit RAM location for microprocessor access. Two reserved bits in the E3 format have been designated as an O-bit channel, if required. The bits in the RAM location are updated each frame by the TL3M. There is no synchronous relationship between the SDH/SONET frame and the bits written into these RAM locations. The external interface consists of a serial data lead (RnOCD) and a clock lead (RnOCC).

An Alarm Indication Port block is provided for ring configurations. The alarm indication port consists of a data lead (RnAID), which is used with the corresponding POH interface framing pulse (RnPOF) and clock signal (RnPOC). The information on the data lead consists of the REI count and the path RDI alarm summary status. In a ring configuration, this information is inserted from the mate TL3M mapper channel into the local TL3M mapper channel G1 byte for transmission.

The Destuff block works in conjunction with the Desync block to remove the stuff columns in the payloads, and also performs the majority logic voting for the DS3 and E3 formats. The majority voting logic uses the justification control bits to determine if the S-bit (or bits) is carrying a stuffing state or data.

The Desync block, using a digital desynchronizer, is responsible for removing the effects on the output of the DS3 or E3 signals of systemic jitter due to signal mapping and pointer movements. Each of the three desyncronizers has a built-in TranSwitch proprietary pointer leak algorithm, which is transparent to the user. An option is provided in which the pointer leak rate can be programmed by the host processor. The output has an average frequency equal to the source frequency and has jitter characteristics that meet both ITU and ANSI standards.

A line DS3/E3 AIS generator is provided, which enables line AIS to be generated for the various upstream alarms, such as loss of pointer. A control bit is also provided which enables the microprocessor to send line AIS independent of the alarm states. An option is provided which enables line AIS to be generated when a channel is placed in line loopback.

The Output block provides either a positive (RPOSn) and negative (RNEGn) rail line signal, or an NRZ line signal (RPOSn), and a clock signal (RCLKn). The receive E3 HDB3 and DS3 B3ZS coder operates independent of the transmitter side. A control bit is provided for inverting the clock output, if required. Also provided is a control bit which enables the receive data and clock leads to be forced to a high impedance state, independent of interface type (rail or NRZ) selected. This permits two interfaces from two different devices to be tied together for ring configurations.

In the transmit direction (towards the Add bus), the Input block supports either a positive (TPOSn) and negative (TNEGn) rail line signal, or an NRZ line signal (TPOSn), and a clock signal (TCLKn). A control bit enables the transmit input clock to be inverted. The Input block performs either the E3 HDB3 or DS3 B3ZS decoder function. Bipolar violations are counted in a 16-bit counter. A choice of bipolar violation sequence detection is also provided. The rail interface also detects an E3 or DS3 loss of signal. The input clock is also monitored for a stuck high or low condition. When the NRZ interface is selected, the unused negative rail input lead can be used to clock in an external loss of signal (LOS) indication from a downstream codec.

Control bits are provided which enable line AIS to be sent when either a loss of signal or input clock failure is detected. A control bit also enables the microprocessor to send line AIS, independent of alarms. Separate NRZ data (RnNRD) and clock (RnNRC) output signals are also provided which may be used for monitoring.

The line signal is connected to the Stuff/Sync block. This block basically consists of a FIFO into which the data is written from the line and is read out by a SDH/SONET clock which is either derived from the Add bus (i.e., Add bus timing), or from the Drop bus (i.e., Drop bus timing). The stuffing algorithm for the DS3 signal uses one set of five control bits (C-bits) with one stuffing opportunity bit (S-bit) for frequency justification per subframe (nine subframes). The E3 format uses five pairs of control bits (C1 and C2 bits) to control two stuff opportunity bits (S1 and S2) per subframe (one subframe per three rows for a total of three subframes per frame). FIFO underflow and overflow alarm indications are provided. Should an underflow or overflow condition occur, the FIFO will immediately reset to a preset value. The FIFO also tracks an incoming line signal having an average frequency deviation as high as ± 20 ppm, and can simultaneously accept the signal with up to 5 UI peak-to-peak jitter (where 1 UI = 1/f).

The Build block formats the data bits into either a SONET STS-3 STS-1 SPE format (see Figure 4) or an STM-1 VC-4 TUG-3 format (see Figure 5). The STS-1 format has two stuff columns and payload plus a column of POH bytes, while the TUG-3 format consists of the payload, plus a column of POH bytes and H1/H2 pointer bytes. The TUG-3 pointer bytes define the start of the J1 POH byte within the TUG-3. A fixed pointer value of 6800 hex is used as the initial value when building a TUG-3 format. There are two levels of pointer movements in the TUG-3 build process. In either drop or add timing, the transmit pointer value will increment or decrement when there is an STM-1 VC-4 increment or decrement based on the relative position of the J1 pulse in the C1J1. The pointer movement for the TUG-3s will be in the opposite direction. This feature can be disabled.

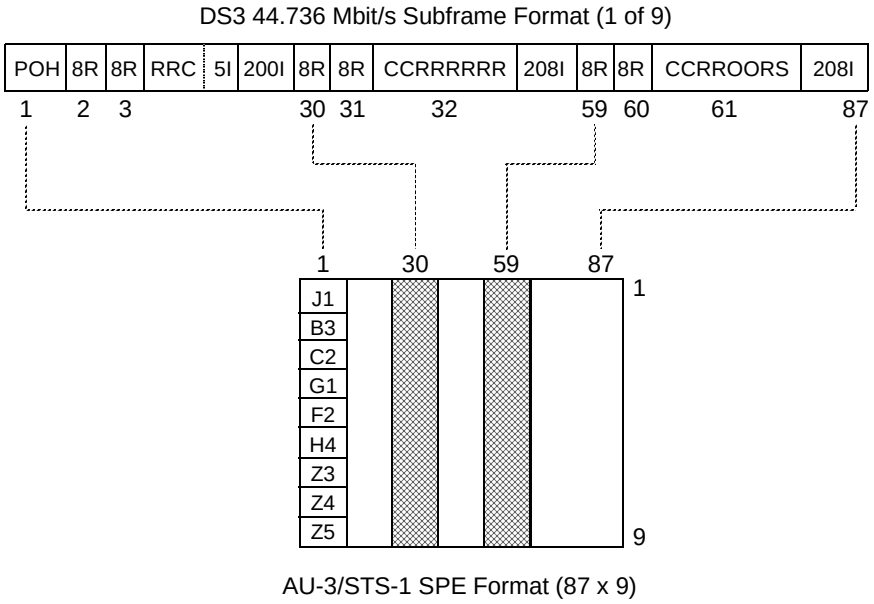


Figure 4. SONET AU-3/STS-1 SPE Build Format

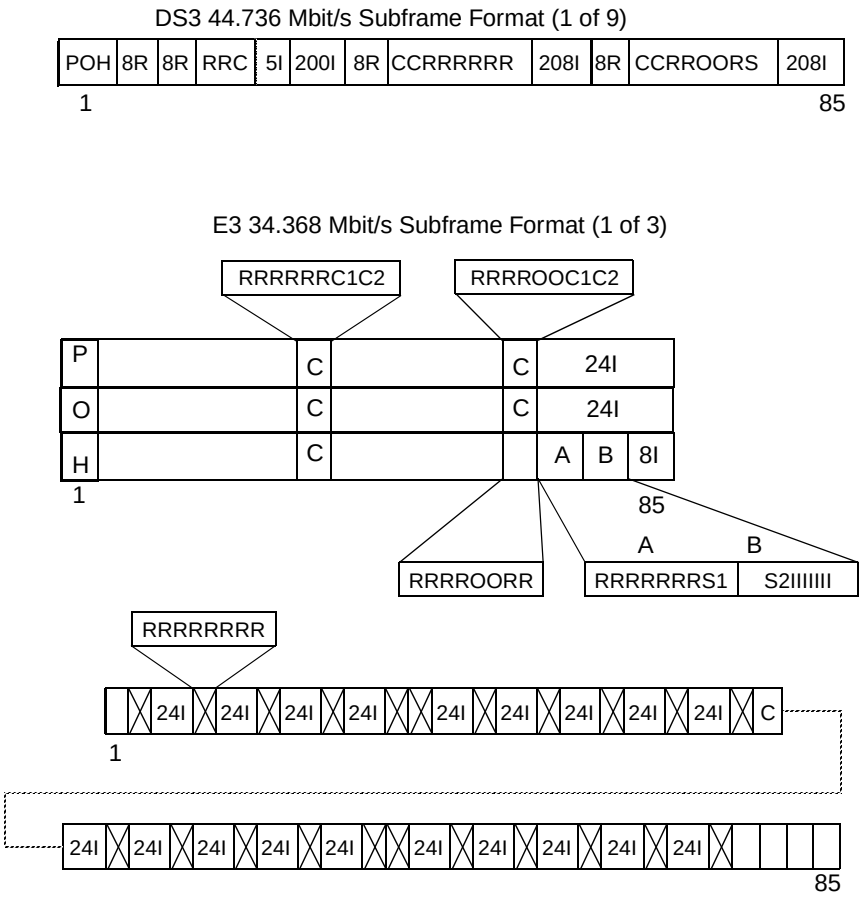


Figure 5. ITU-T TUG-3 Build Format

An O-bit interface value or a value written into RAM by the microprocessor is mapped into the two O-bit positions in the DS3 format. The O-bit interface consists of an output clock signal (TnOCC) and an input data lead (TnOCD). The relationship between the O-bit channel and the SDH/SONET frame in both directions is asynchronous.

The nine individual POH bytes (except the B3 byte) can be inserted into the TUG-3 or STS-1 POH bytes from values written to RAM by the microprocessor or from the transmit POH interface. The POH interface consists of an input data lead (TnPOD), output framing pulse (TnPOF), and an output clock signal (TnPOC), where n represents each of three level 3 mappers. A control bit enables the POH interface bytes to be written into RAM for microprocessor access when transmitted. In the case of the G1 byte, the value can also be inserted from the local receive side or from the alarm indication port. A test mask is provided for the calculated B3 byte, which permits up to eight errors to be transmitted.

For ring operation, an alarm indication port is provided in the AIP block. The alarm indication port consists of an input data lead (TnAID), input framing pulse (TnAIF), and input clock signal (TnAIC). The information on the data lead consists of the REI count, and the path RDI alarm summary status. In ring operation, this information is inserted into the G1 byte for transmission.

The Add block uses either the add or drop timing signals. Add bus timing is enabled by placing a high on control lead ABTIM. When Add bus timing is selected, the timing for the two buses, add and drop, is supplied by separate inputs for add and drop. When Add bus timing is selected, the output Add bus signals consist of byte-wide data (AD(7-0)), add indication (ADD), and odd parity (APAR). The Add bus input timing signals consist of a 19.44 MHz clock (ACLK), C1J1 indication (AJ1C1) and a SPE active indication (ASPE). The output Add bus signals consist of byte-wide data (AD(7-0)), add indication (ADD), and odd parity (APAR). The active low add indication (ADD) indicates the location of all time slots being added to the Add bus. The Add bus clock is also monitored for a stuck high or low state when Add bus timing is selected. A bus contention alarm is provided if more than one channel is assigned to the same TUG-3 or STS-1.

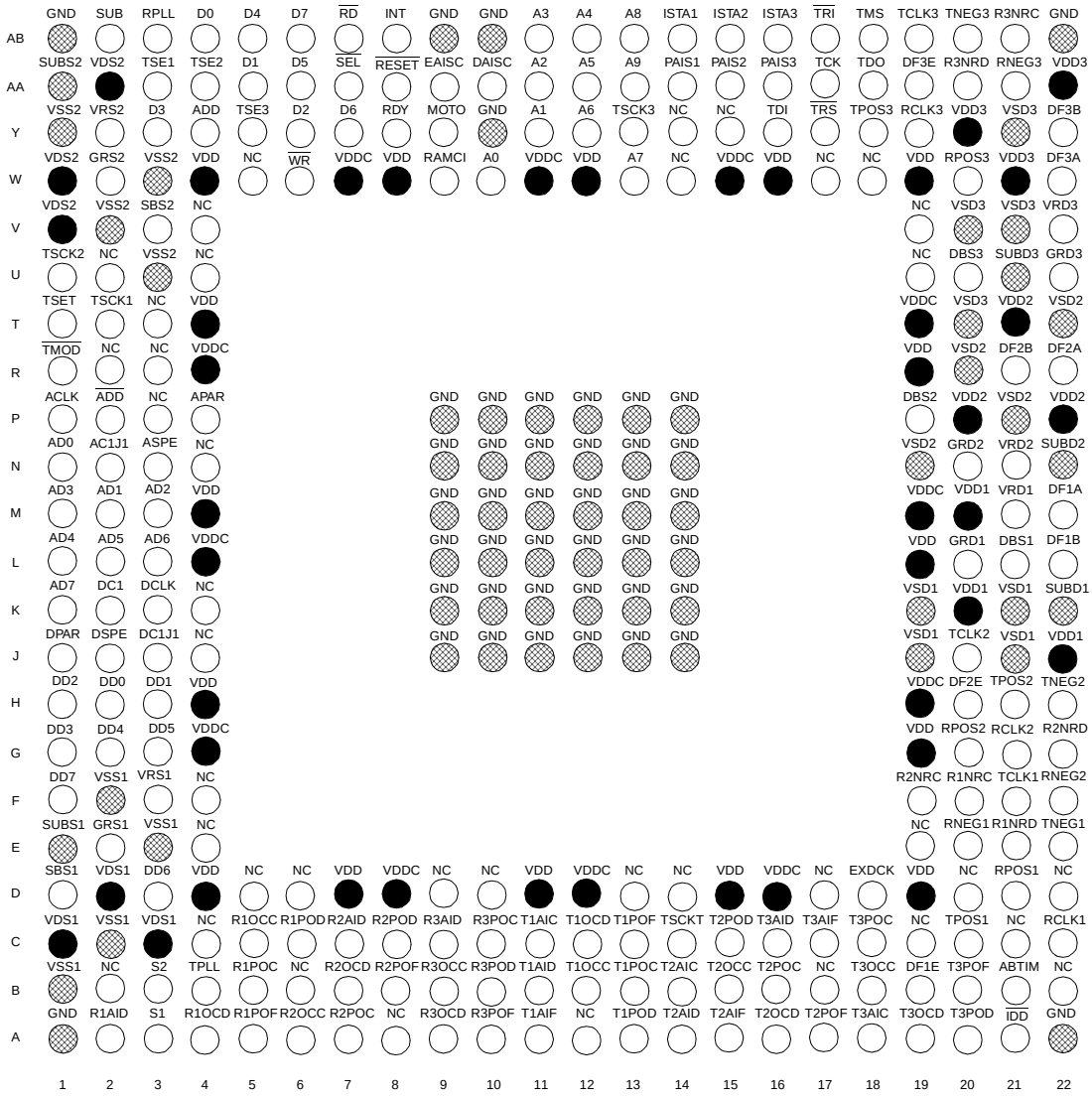
Drop bus timing is enabled by placing a low on control lead ABTIM. When Drop bus timing is selected, the timing for the Add bus depends upon the Drop bus input signals for operation. When Drop bus timing is selected, the output Add bus signals consist of byte-wide data (AD(7-0)), add indication (ADD), and odd parity (APAR).

All of the control registers and performance counters, as well as the status and alarm indications, are accessible via a microprocessor interface. The TL3M supports either Intel or Motorola microprocessor bus interfaces, with hardware and software interrupts. Mask bits are provided for the latched status and alarm indications, to control whether each of them will generate an interrupt when active. The counters may be configured as either rollover or saturating. Saturating counters are cleared automatically when they are read.

For board testing, boundary scan and the ability to force all the output signals to a high impedance state are provided. For network and device debugging, facility and line loopbacks are provided at the line interfaces. Each channel also has a PRBS test analyzer and generator (not shown in Figure 2).

LEAD DIAGRAM

BOTTOM VIEW



Notes:

1. This is the bottom view. The leads are solder balls. See Figure 38 for package information. This view is rotated relative to the bottom view in Figure 38.
2. Lead symbols are described in the “Lead Descriptions” section.
3. Power supply leads are shown as solid black circles, ground leads as cross-hatched circles.

Figure 6. TL3M TXC-03453B Lead Diagram

LEAD DESCRIPTIONS

POWER SUPPLY, GROUND AND NO CONNECTS

Symbol	Lead No.	I/O/P*	Name/Function
VDDC	D8, D12, D16, G4, H19, L4, M19, R4, T19, W7, W11, W15	P	**Core VDD:** +3.3 volts, ± 5% power supply
VDD	D4, D7, D11, D15, D19, G19, H4, L19, M4, R19, T4, W4, W8, W12, W16, W19		**VDD:** +3.3 volts, ± 5% power supply
VDS1	C1, C3, D2	P	**VDD Analog:** +3.3 volts, ± 5% power supply
VDS2	V1, W1, AA2	P	**VDD Analog:** +3.3 volts, ± 5% power supply
VDD1	J22, K20, M20	P	**VDD Analog:** +3.3 volts, ± 5% power supply
VDD2	P20, P22, T21	P	**VDD Analog:** +3.3 volts, ± 5% power supply
VDD3	W21, Y20, AA22	P	**VDD Analog:** +3.3 volts, ± 5% power supply
GND	J9 - J14 K9 - K14 L9 - L14 M9-M14 N9 - N14 P9 - P14	P	**Core Ground:** 0 volts reference
GND	A1, Y10, A22, AB1, AB9, AB10, AB22		**Ground:** 0 volts reference
VSS1	B1, C2, E3, F2	P	**VSS (Analog Ground):** 0 volts reference
VSS2	U3, V2, W3, Y1	P	**VSS (Analog Ground):** 0 volts reference
VSD1	J19, J21 K19, K21	P	**VSS (Analog Ground):** 0 volts reference
VSD2	N19, P21, R20, T22	P	**VSS (Analog Ground):** 0 volts reference
VSD3	T20, V20, V21, Y21	P	**VSS (Analog Ground):** 0 volts reference
NC	A8, A12, B2, B6, B17, B22, C4, C19, C21, D5, D6, D9, D10, D13, D14, D17, D20, D22, E4, E19, F4, J4, K4, N4, P3, R2, R3, T3, U2, U4, U19, V4, V19, W5, W14, W17, W18, Y14, Y15		**No Connect:** NC leads are not to be connected, not even to another NC lead, but must instead be left floating. Connection of these leads may impair performance or cause damage to the device.

* Note: I = Input; O = Output; P = Power; T = Tristate:

DROP BUS INTERFACE

Symbol	Lead No.	I/O/P	Type*	Name/Function
DD(7-0)	F1, D3, G3, G2, G1, H1, H3, H2	I	LVTTL	**Drop Bus Data Byte:** 19.44 Mbyte/s byte-wide data that corresponds to the STM-1 or STS-3 signal from the Drop bus. Lead F1 is DD7. Data that may be present on the bus, other than the TUG-3s, or the STS-3 STS-1 SPEs, is ignored.
DCLK	K3	I	LVTTL	**Drop Bus Clock:** This clock operates at a 19.44 MHz rate. Drop bus byte-wide data (DD(7-0)), parity (DPAR), payload indicator (DSPE), and C1/J1 (DC1J1 and DC1) are clocked in on falling edges of this clock. This signal will provide timing for the add direction when the Drop bus timing mode is selected (lead ABTIM is low).
DC1	K2	I	LVTTL	**Drop C1 Pulse:** External positive C1 pulse that may be provided on this lead instead of in the DC1J1 signal. This signal is internally or-gated with the DC1J1 signal to form a composite C1J1 signal. If this lead is not used it must be grounded. This signal will provide timing for the add direction when the Drop bus timing mode is selected (lead ABTIM is low).
DC1J1	J3	I	LVTTL	**Drop Bus C1 and J1 Indicator:** The C1 pulse is an active high, one clock cycle-wide (DCLK) timing pulse that indicates the location of the first C1 (J0) time slot in the STM-1 or STS-3 frame. If the C1 pulse is not present in this signal, it must be provided at the DC1 lead. One or three J1 pulses, also one clock cycle wide, identify the starting location of the J1 byte in the VC-4 format or the starting locations of the J1 bytes in each of the three STS-1s. This signal will provide timing for the add direction when the Drop bus timing mode is selected (lead ABTIM is low).
DSPE	J2	I	LVTTL	**Drop Bus SPE Indicator:** A signal that is active high during the STM-1 VC-4 format, and for each of the STS-3 STS-1 SPE periods. It is active low during the STS-3 TOH and STM-1 RSOH/MSOH byte times. This signal will provide timing for the add direction when the Drop bus timing mode is selected (lead ABTIM is low).
DPAR	J1	I	LVTTL	**Drop Bus Parity Bit:** Odd parity input for the data byte, the DSPE signal, and the composite DC1J1 pulse.

* Note: See the "Input, Output and Input/Output Parameters" section for Type definitions.

ADD BUS INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
AD(7-0)	K1, L3, L2, L1, M1, M3, M2, N1	O(T)	LVCMOS 4mA	**Add Bus Data Byte:** 19.44 Mbytes/s byte-wide data that corresponds to the time slots that are placed on the Add bus by the TL3M. Lead K1 is AD7. The first bit transmitted (MSB) corresponds to bit 7. These leads are forced to a high impedance state when: - Data is not present - Hardware or software reset occurs - Drop Bus Loss Of Clock (DLOC) occurs when the Drop bus timing mode is selected (ABTIM lead is low) - When control bit ADDEN (bit 1 in 0C2H) is set to 0.
ACLK	P1	I	LVTTL	**Add Bus Clock:** This input clock operates at 19.44 MHz. The add clock is used when the Add bus timing mode is selected (ABTIM lead is high). Add bus byte-wide data (AD(7-0)), the ASPE signal, and the AC1J1 signal are clocked in on its falling edges. The parity (APAR) signal, and add indicator ($\overline{ADD}$) are clocked out on its rising edges. This lead is disabled, and should be grounded, when the drop timing mode is selected (ABTIM lead is low).
ASPE	N3	I	LVTTL	**Add Bus SPE Indicator:** An input signal that must be high to indicate the STM-1 VC-4 period, and each of the three STS-3/STS-1 SPE periods, when Add bus timing is selected. This lead is disabled, and should be grounded, when the drop timing mode is selected (ABTIM lead is low).
AC1J1	N2	I	LVTTL	**Add Bus C1 and J1 Indicator:** The C1 pulse is an active high, one clock cycle-wide (ACLK) input timing pulse that identifies the location of the first C1 (J0) time slot in the STM-1 or STS-3 frame. A single J1 pulse, also one clock cycle wide, identifies the starting location of the J1 byte in the STM-1 VC-4 signal. Three J1 pulses are used to identify the starting location of the J1 bytes in each of the three STS-3 STS-1 SPEs. This lead will carry only J1 pulse information when the DC1 lead is used. This lead is disabled, and should be grounded, when the drop timing mode is selected (ABTIM lead is low).
$\overline{ADD}$	P2	O	LVCMOS 4mA	**Add Indicator:** An active low signal that identifies the position of the TUG-3 and STS-1 bytes that are being mapped to the Add bus. This signal will be high when - Data is not present - Hardware or software reset occurs - Drop Bus Loss Of Clock (DLOC) occurs when the Drop bus timing mode is selected (ABTIM lead is low) - When control bit ADDEN (bit 1 in 0C2H) is set to 0.

Symbol	Lead No.	I/O/P	Type	Name/Function
APAR	P4	O(T)	LVCMOS 4mA	**Add Bus Parity Bit:** This output bit represents an odd parity calculation for each data byte that is mapped to the Add bus in the add timing and Drop bus timing modes. This lead is forced to a high impedance state when - Data is not present - Hardware or software reset occurs - Drop Bus Loss Of Clock (DLOC) occurs when the Drop bus timing mode is selected (ABTIM lead is low) - When control bit ADDEN (bit 1 in 0C2H) is set to 0.

LINE INTERFACE

Where n represents the channel (mapper) number, for channels 1 through 3.

Symbol	Lead No.	I/O/P*	Type	Name/Function
RPOS1 RPOS2 RPOS3	D21 G20 W20	O (T)	LVCMOS 4mA	**Receive Line Positive Rail/NRZ Data for Channel n:** When control bit CODE (bit 6 in XC1H) is a 0 for the corresponding channel, this lead provides the received NRZ output for the 44.736 (DS3) or 34.368 Mbit/s (E3) asynchronous line data. When control bit CODE is a 1, a positive rail output signal is provided. This lead is forced to a high impedance state when - Control bit L3EN (bit 0 in 0C2H) is set to 0 - Control bit L3OEN (bit 0 in XC2H) is set to 0 for the corresponding channel - Hardware reset (lead $\overline{\text{RESET}}$) or software reset (RESETS, bit 0 in 0C7H) occurs - RESETn (bits 1-3 in 0C7H) is set to 1 for the corresponding channel.
RNEG1 RNEG2 RNEG3	E20 F22 AA21	O (T)	LVCMOS 4mA	**Receive Negative Rail Data for Channel n:** When control bit CODE (bit 6 in XC1H) is a 0, the corresponding lead is set to low. When control bit CODE is a 1, a negative rail output is provided. This lead is forced to a high impedance state when - Control bit L3EN (bit 0 in 0C2H) is set to 0 - Control bit L3OEN (bit 0 in XC2H) is set to 0 for the corresponding channel - Hardware reset (lead $\overline{\text{RESET}}$) or software reset (RESETS, bit 0 in 0C7H) occurs - RESETn (bits 1-3 in 0C7H) is set to 1 for the corresponding channel.

Symbol	Lead No.	I/O/P*	Type	Name/Function
RCLK1 RCLK2 RCLK3	C22 G21 Y19	O (T)	LVCMOS 4mA	**Receive Line Clock for Channel n:** The 44.736 or 34.368 Mbit/s line signals on the RPOSn/RNEGn signal leads are clocked out on falling edges of this clock when control bit INVCO (bit 4 in XC1H) is set to 0 for the corresponding channel. These signals are clocked out on rising edges when control bit INVCO is set to 1. This lead is forced to a high impedance state when - Control bit L3EN (bit 0 in 0C2H) is set to 0 - Control bit L3OEN (bit 0 in XC2H) is set to 0 for the corresponding channel - Hardware reset (lead $\overline{\text{RESET}}$) or software reset (RESETS, bit 0 in 0C7H) occurs - RESETn (bits 1-3 in 0C7H) is set to 1 for the corresponding channel.
TPOS1 TPOS2 TPOS3	C20 H21 Y18	I	LVTTL	**Transmit Line Positive Rail/NRZ Data: for Channel n.** When control bit DECODE (bit 7 in XC1H) is set to 0 for the corresponding channel, this lead is used as the NRZ input for the 44.736 (DS3) or 34.368 Mbit/s (E3) asynchronous line signal. When control bit DECODE is a 1, the corresponding lead provides the positive rail data input for the internal decoder.
TNEG1/ LOS1 TNEG2/ LOS2 TNEG3/ LOS3	E22 H22 AB20	I	LVTTL	**Transmit Negative Rail Data or LOS Input:** When control bit DECODE (bit 7 in XC1H) is a 1, the corresponding lead provides the negative rail data input for the internal decoder. When control bit DECODE is set to 0 for the corresponding channel, this lead can be used to input an external loss of signal alarm. If a lead is not used, it must be tied to ground.
TCLK1 TCLK2 TCLK3	F21 J20 AB19	I	LVTTL	**Transmit Line Clock:** The NRZ or rail signal for a corresponding channel is clocked in on rising edges of this clock when control bit INVCI (bit 5 in XC1H) is set to 0. NRZ or rail data is clocked in on falling edges when control bit INVCI is set to 1.
R1NRD R2NRD R3NRD	E21 G22 AA20	O (T)	LVCMOS 4mA	**Monitor Transmit Line Data:** Output provided for an optional external performance monitoring circuit. This serial NRZ output is provided after the line decoder in the transmit direction, and is independent of whether the transmit line input is configured for a NRZ or rail interface. Data is clocked out on rising edges of clock (RnNRC). This lead is forced to a high impedance state when - Control bit L3EN (bit 0 in 0C2H) is set to 0 - Control bit L3OEN (bit 0 in XC2H) is set to 0 for the corresponding channel - Hardware reset (lead $\overline{\text{RESET}}$) or software reset (RESETS, bit 0 in 0C7H) occurs - RESETn (bits 1-3 in 0C7H) is set to 1 for the corresponding channel.

Symbol	Lead No.	I/O/P*	Type	Name/Function
R1NRC R2NRC R3NRC	F20 F19 AB21	O (T)	LVCMOS 4mA	**Monitor Transmit Line Clock:** Data (RnNRD) for the performance monitoring circuits is clocked out on rising edges of the corresponding clock. This lead is forced to a high impedance state when - Control bit L3EN (bit 0 in 0C2H) is set to 0 - Control bit L3OEN (bit 0 in XC2H) is set to 0 for the corresponding channel - Hardware reset (lead $\overline{\text{RESET}}$) or software reset (RESETS, bit 0 in 0C7H) occurs - RESETn (bits 1-3 in 0C7H) is set to 1 for the corresponding channel.

OVERHEAD COMMUNICATIONS CHANNEL (O-BIT) INTERFACE

Where n represents the channel number, channels 1 through 3.

Symbol	Lead No.	I/O/P	Type	Name/Function
R1OCD R2OCD R3OCD	A4 B7 A9	O	LVCMOS 4mA	**Receive Overhead Communications Channel Data:** Unaligned data output for the overhead communications channel (O-bits) defined in the DS3 format and two reserved bits defined in the E3 format are provided. The O-bits for channel n are clocked out on falling edges of the RnOCC clock signal.
R1OCC R2OCC R3OCC	C5 A6 B9	O	LVCMOS 4mA	**Receive Overhead Communications Channel Clock:** A gapped 720 kHz output clock that has an average frequency of 144 kHz, that is used for clocking out the received overhead communications channel bits (RnOCD) to external circuitry.
T1OCD T2OCD T3OCD	C12 A16 A19	I	LVTTL	**Transmit Overhead Communications Channel Data:** Data input for transmitting the overhead communications channel in the DS3 format, and two defined reserved bits in the E3 format. This input is enabled when a 1 is written to control bit EXOO (bit 7 in XC4H) for the corresponding channel. Data is clocked in on rising edges of the TnOCC clock signal. The bits are transmitted unaligned regarding bit position and subframe number within the payload.
T1OCC T2OCC T3OCC	B12 B15 B18	O	LVCMOS 4mA	**Transmit Overhead Communications Channel Clock:** A gapped 720 kHz output clock that has an average frequency of 144 kHz, which is used for clocking in the transmit overhead communications channel bits (TnOCD) from external circuitry when enabled.

PATH OVERHEAD BYTE INTERFACE

Where n represents the channel number, channels 1 through 3.

Symbol	Lead No.	I/O/P	Type	Name/Function
R1POD R2POD R3POD	C6 C8 B10	O	LVCMOS 4mA	**Receive Path Overhead Byte Data:** These leads provide a serial output for the nine path overhead bytes associated with each of the three TUG-3s or STS-1s. The nine POH bytes are clocked out on falling edges of the corresponding clock signal (RnPOC).
R1POF R2POF R3POF	A5 B8 A10	O	LVCMOS 4mA	**Receive Path Overhead Byte Framing:** A positive one (RnPOC) clock cycle-wide output framing pulse that is synchronous to the J1 byte location in the receive path overhead data signal (RnPOD). This signal is also used as the framing pulse for the receive alarm indication port output data signal (RnAID).
R1POC R2POC R3POC	B5 A7 C10	O	LVCMOS 4mA	**Receive Path Overhead Byte Clock:** A gapped clock used for clocking out the receive path overhead bytes (RnPOD), and receive alarm indication port data (RnAID) for each channel.
T1POD T2POD T3POD	A13 C15 A20	I	LVTTL	**Transmit Path Overhead Byte Data:** A serial input for the following path overhead bytes: J1, C2, G1, F2, H4, F3, K4, and N1 bytes. The POH bytes are clocked in on rising edges of the clock signal (TnPOC). The bit times corresponding to the B3 byte are ignored.
T1POF T2POF T3POF	C13 A17 B20	O	LVCMOS 4mA	**Transmit Path Overhead Byte Framing:** A positive one (TnPOC) clock cycle-wide output framing pulse that determines the start of the J1 byte in transmit path overhead byte data signal (TnPOD).
T1POC T2POC T3POC	B13 B16 C18	O	LVCMOS 4mA	**Transmit Path Overhead Byte Clock:** A gapped output clock used for clocking in the transmit path overhead bytes from an external circuit.

ALARM INDICATION PORT

Where n represents the channel number, channels 1 through 3

Symbol	Lead No.	I/O/P	Type	Name/Function
R1AID R2AID R3AID	A2 C7 C9	O	LVCMOS 4mA	**Receive Alarm Indication Port Data:** Serial output leads that provide a 4-bit REI (FEBE) count based on the received B3 error count, and a Path RDI alarm indication for a mate TL3M device in a ring configuration, from each channel. These leads are normally connected to the corresponding Transmit alarm indication port data leads (TnAID) at the mate TL3M device. The receive path overhead byte clock (RnPOC) signal is used to clock out this signal. The receive path overhead frame signal (RnPOF) provides the frame reference. The bits are sent according to the following format and are repeated every eight bit times. Bit 1 is the MSB and is the first bit sent. Bits: 1 2 3 4 | 5 | 6 7 8 REI Count | RDI | 0 0 1
T1AID T2AID T3AID	B11 A14 C16	I	LVTTL	**Transmit Alarm Indication Port Data:** These serial input leads are normally connected to the receive alarm indication port data output leads (RnAID) at the mate TL3M device for a ring configuration. Provides an input for the four bit REI count (received B3 error count), and the Path RDI alarm indication. The format is shown above.
T1AIC T2AIC T3AIC	C11 B14 A18	I	LVTTL	**Transmit Alarm Indication Port Clock:** These clock input leads are normally connected to the receive path overhead byte clock output leads (RnPOC) at the mate TL3M device for a ring configuration. Transmit alarm indication port data (TnAID) is clocked in on rising edges of TnAIC.
T1AIF T2AIF T3AIF	A11 A15 C17	I	LVTTL	**Transmit Alarm Indication Port Framing Pulse:** Normally connected to receive path overhead byte framing pulse output leads (RnPOF) at the mate TL3M device for a ring configuration. Used to indicate the location of the first bit in the byte.

ADDITIONAL SIGNALS

Symbol	Lead No.	I/O/P	Type	Name/Function
DAISC	AA10	I	LVTTL	**DS3 AIS Clock Input:** Input clock for the DS3 AIS generator. This clock must be present for the DS3 AIS generator to function. The clock must have the operating line rate of 44.736 MHz, and a frequency stability of ± 20 ppm. This clock is also used as a backup clock for the transmit and receive PRBS generators in DS3 applications, in the event that the transmit or receive DS3 signal clocks are absent. Clock duty cycle of 45 to 55% is required. If this clock input is not used, it should be grounded.
EAISC	AA9	I	LVTT	**E3 AIS Clock Input:** Input clock for the E3 AIS generator. This clock must be present for the E3 AIS generator to function. The clock must have the operating line rate of 34.368 MHz, and a frequency stability of ± 20 ppm. This clock is also used as a backup clock for the transmit and receive PRBS generators in E3 applications, in the event that the transmit or receive E3 signal clocks are absent. Clock duty cycle of 45 to 55% is required. If this clock input is not used, it should be grounded.
ABTIM	B21	I	LVTTL	**Add Bus Timing Mode:** A high placed on this lead selects the Add bus timing mode. In Add bus timing mode, Drop and Add buses function with independent timing. A low placed on this lead selects Drop bus timing mode. In this mode of operation, the Drop bus signals provide timing information for the add (transmit) section.
$\overline{\text{RESET}}$	AA8	I	LVTTLp	**Hardware Reset:** A low clears all counters, presets internal logic, and forces the Add bus output signals and line interfaces to a high impedance state for all three channels. The reset signal must be low for a minimum of 200 nanoseconds. The bus clocks, line clocks, and microprocessor clock must also be present during the reset signal. This lead is provided with an internal pull-up resistor.
PAIS1 PAIS2 PAIS3	AA14 AA15 AA16	I	LVTTL	**External Path AIS Indication:** A high on this lead may be used to indicate an external Path AIS has occurred. It causes the XPAIS status bit (bit 0 in XB4H/XB5H) to be set to 1. This lead is enabled when control bit XALM2AIS (bit 7 in XC2H) is a 1. When enabled, the in-band upstream AIS indication provided via the TOH E1 byte is disabled. If a lead is not used it should be grounded.
ISTA1 ISTA2 ISTA3	AB14 AB15 AB16	I	LVTTL	**External STS-1 Alarm Indication:** A high on this lead may be used to indicate an external SDH/SONET alarm has occurred. It causes the XISTAT status bit (bit 1 in XB4H/XB5H) to be set to 1. If a lead is not used it should be grounded.
$\overline{\text{TRI}}$	AB17	I	LVTTLp	**High Impedance Enable:** A low causes all TL3M digital outputs and bidirectional leads to be set to a high impedance state for board testing. This lead is provided with an internal pull-up resistor.

DIGITAL DESYNCHRONIZERS

Symbol	Lead No.	I/O/P	Type	Name/Function
DF1A DF1B	M22 L22	I	Analog	**Digital Desynchronizer PLL External Capacitor - Channel 1:** An external 1.0 µF ± 10% capacitor (alternate capacitor value 4.7 µF) is connected between the two leads, as shown in the PLL connections diagram (Figure 27).
DF2A DF2B	R22 R21	I	Analog	**Digital Desynchronizer PLL External Capacitor - Channel 2:** An external 1.0 µF ± 10% capacitor (alternate capacitor value 4.7 µF) is connected between the two leads, as shown in the PLL connections diagram (Figure 27).
DF3A DF3B	W22 Y22	I	Analog	**Digital Desynchronizer PLL External Capacitor - Channel 3:** An external 1.0 µF ± 10% capacitor (alternate capacitor value 4.7 µF) is connected between the two leads, as shown in the PLL connections diagram (Figure 27).
VRD1 DBS1 GRD1	M21 L21 L20	I	Analog	**Digital Desynchronizer PLL Bias Components - Channel 1:** An external 30.1 kΩ 1% resistor is connected between the GRD1 lead and the DBS1 lead, as shown in the PLL connections diagram (Figure 27). VRD1 should be left unconnected.
VRD2 DBS2 GRD2	N21 P19 N20	I	Analog	**Digital Desynchronizer PLL Bias Components - Channel 2:** An external 30.1 kΩ 1% resistor is connected between the GRD2 lead and the DBS2 lead, as shown in the PLL connections diagram (Figure 27). VRD2 should be left unconnected.
VRD3 DBS3 GRD3	V22 U20 U22	I	Analog	**Digital Desynchronizer PLL Bias Components - Channel 3:** An external 30.1 kΩ 1% resistor is connected between the GRD3 lead and the DBS3 lead, as shown in the PLL connections diagram (Figure 27). VRD3 should be left unconnected.
SUBD1 SUBD2 SUBD3	K22 N22 U21	I	Analog	**Digital Desynchronizer Dedicated Substrate Connections.** These leads are normally connected to ground.
DF1E DF2E DF3E	B19 H20 AA19	O	LVCMOS 4mA	**FIFO Reset Indication.** These leads are used to indicate a reset condition from their corresponding desynchronizer. The indication will be high for a minimum of 125 microseconds and a maximum of 250 microseconds for any of the following - Hardware Reset ($\overline{\text{RESET}}$ lead goes low) - RESET (bit 0 in 0C7H) is a 1 - RESETn (0C7H) is set to 1 for the corresponding channel. - FIFO overflow or underflow

TRANSMIT AND RECEIVE SYNTHESIZERS

Symbol	Lead No.	I/O/P	Type	Name/Function
VRS1 SBS1 GRS1	F3 D1 E2	I	Analog	**Transmit Synthesizer Bias Components:** An external 30.1 kΩ 1% resistor is connected between the GRS1 lead and the SBS1 lead. A 220 pF bypass capacitor is connected between the SBS1 node and ground, as shown in the Synthesizer connections diagram (Figure 28). VRS1 should be left unconnected.
VRS2 SBS2 GRS2	Y2 V3 W2	I	Analog	**Receive Synthesizer Bias Components:** An external 30.1 kΩ 1% resistor is connected between the GRS2 lead and the SBS2 lead. A 220 pF bypass capacitor is connected between the SBS2 node and ground, as shown in the Synthesizer connections diagram (Figure 28). VRS2 should be left unconnected.
SUBS1 SUBS2	E1 AA1	I	Analog	**Dedicated Substrate Connections:** These leads are normally connected to ground.

MICROPROCESSOR INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
A(9-0)	AA13, AB13, W13, Y12, AA12, AB12, AB11, AA11, Y11, W10	I	LVTTL	**Address Bus:** Used by the microprocessor for accessing a specific memory location in the TL3M for a read/write cycle. A9 is defined as the most significant bit (lead AA13).
D(7-0)	AB6, Y7, AA6, AB5, Y3, Y6, AA5, AB4	I/O	LVTTL/ LVCMOS 8mA	**Data Bus:** Bidirectional data lines used for transferring data between the TL3M and the external microprocessor. D7 (lead AB6) is defined as the most significant bit.
$\overline{WR}$	W6	I	LVTTL	**Write (I mode):** Intel Mode - An active low signal generated by the microprocessor for writing to the TL3M. Motorola Mode - Not used. This lead should be tied high.
$\overline{RD}$ or RD/$\overline{WR}$	AB7	I	LVTTL	**Read (I mode) or Read/Write (M mode):** Intel Mode - An active low signal generated by the microprocessor for reading the TL3M memory map. Motorola Mode - A high signal generated by the microprocessor for reading the TL3M memory map. A low signal is used for writing to the TL3M.
$\overline{SEL}$	AA7	I	LVTTLp	**Select:** A low enables data transfers between the microprocessor and the TL3M during a read/write cycle.

Symbol	Lead No.	I/O/P	Type	Name/Function
RDY/ DTACK	Y8	O (T)	LVCMOS 8mA	**Ready (I mode) or Data Transfer Acknowledge (M mode):** Intel Mode - A high is an acknowledgment from the addressed memory map location that the transfer can be completed. A low indicates that the TL3M has not completed the transfer cycle, and the microprocessor must wait before latching read data or completing the write cycle. Motorola Mode - During a read cycle, a low signal indicates the information on the data bus is valid. During a write cycle, a low signal acknowledges the acceptance of data.
INT/IRQ	AB8	O (T)	LVCMOS 4mA	**Interrupt:** Intel Mode - A high on this output lead signals an interrupt request to the microprocessor (active high). Motorola Mode - A low on this lead signals an interrupt request to the microprocessor (active low). The interrupt lead state is also controlled by the control bit states listed in the following table INTZN (OC2H, bit 3) / INTEN (OC2H, bit 2) / Interrupt Lead X / 0 / High impedance state 0 / 1 / Interrupt lead held to the high-z state only when inactive 1 / 1 / Interrupt lead enabled for normal operation
RAMCI	W9	I	LVTTL	**RAM Clock Input:** Clock input for the internal RAM. This clock supports an arbitrator function for accessing the internal RAM structure. This clock must operate between 19 and 35 MHz with a duty cycle of (50±10) percent. This clock and the microprocessor timing signals may operate asynchronously with respect to each other.
MOTO	Y9	I	LVTTL	**Motorola/Intel Microprocessor Select:** A high selects the Motorola microprocessor compatible bus interface. A low selects the Intel microprocessor compatible bus interface.

BOUNDARY SCAN

Symbol	Lead No.	I/O/P	Type	Name/Function
TDO	AA18	O(T)	LVCMOS 4mA	**Boundary Scan Test Data Output:** Serial data clocked out on falling edges of TCK.
TDI	Y16	I	LVTTLp	**Boundary Scan Test Data Input:** Serial data input for boundary scan test messages.
TCK	AA17	I	LVTTL	**Boundary Scan Test Clock:** The input clock for boundary scan testing. The TDI and TMS states are clocked in on its rising edges.
TMS	AB18	I	LVTTLp	**Boundary Scan Test Mode Select:** The signal present on this lead is used to control test operations.
$\overline{\text{TRS}}$	Y17	I	LVTTLp	**Boundary Scan Test Reset:** This lead must be asserted low for at least 250 nanoseconds in order to reset the TL3M device's Test Access Port (TAP) controller. The TAP controller may also be reset by holding the TMS signal lead high for at least five clock cycles of TCK. In applications which will not be using the boundary scan feature, this lead must be tied low, thereby holding the TAP controller reset.

TRANSWITCH TEST LEADS

Symbol	Lead No.	I/O/P	Type	Name/Function
TPLL	B4	I/O	LVTTL/ LVCMOS 8mA	**Test Lead - Transmit PLL:** Do not connect.
RPLL	AB3	I/O	LVTTL/ LVCMOS 8mA	**Test Lead - Receive PLL:** Do not connect.
$\overline{\text{IDD}}$	A21	I	LVTTLp	**Test Lead:** Do not connect.
EXDCK	D18	I	LVTTL	**Test Lead:** Tie lead to ground.
$\overline{\text{TMOD}}$	R1	I	LVTTLp	**Test Lead:** Do not connect.
TSE1 TSE2 TSE3	AA3 AA4 Y5	I	LVTTLpd	**Test Leads:** These leads must be grounded.
TSET TSCK1 TSCK2 TSCK3 TSCKT	T1 T2 U1 Y13 C14	I	LVTTLpd	**Test Leads:** These leads must be grounded.
S1 S2 SUB ADD	A3 B3 AB2 Y4	O	LVCMOS 4mA	**Test Leads:** These leads provide test outputs when enabled. Do not connect.

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{DD}	-0.3	+3.9	V	Note 1
DC input voltage	V_{IN}	-0.5	+5.5	V	Note 1
Storage temperature range	T_S	-55	150	^oC	Note 1
Ambient Operating Temperature	T_A	-40	+85	^oC	0 ft/min linear airflow
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative Humidity, during assembly	RH	30	60	%	Note 2
Relative Humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD	absolute value 2000		V	Note 3

Notes:

1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the “CAUTION” label on the drypack bag in which devices are supplied.
3. Test method for ESD per MIL-STD-883E, Method 3015.7.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance: junction to ambient			23	$^oC/W$	0 ft/min linear airflow

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	3.15	3.30	3.45	V	
I_{DD}		318		mA	
Power Dissipation, P_{DD}		1050	1320	mW	At max VDD, -40 to $+85^oC$ (see Note 1)

Note 1. Maximum power dissipation does not show strong temperature dependency.

INPUT, OUTPUT AND INPUT/OUTPUT PARAMETERS

INPUT PARAMETERS FOR LVTTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.15 \le V_{DD} \le 3.45$
V_{IL}			0.8	V	$3.15 \le V_{DD} \le 3.45$
Input leakage current	-10		+10	µA	0 to 5.25 V input
Input capacitance		5.0		pF	

INPUT PARAMETERS FOR LVTTLp (LVTTL WITH INTERNAL PULL-UP)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.15 \le V_{DD} \le 3.45$
V_{IL}			0.8	V	$3.15 \le V_{DD} \le 3.45$
Input leakage current	-100		0.0	µA	0 to 5.25 V input
Input capacitance		5.0		pF	

INPUT PARAMETERS FOR LVTTLpd (LVTTL WITH INTERNAL PULL-DOWN)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.15 \le V_{DD} \le 3.45$
V_{IL}			0.8	V	$3.15 \le V_{DD} \le 3.45$
Input leakage current	0.0		100	µA	0 to 5.25 V input
Input capacitance		5.0		pF	

OUTPUT PARAMETERS FOR LVCMOS 4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 3.15; I_{OH} = -4.0
V_{OL}			0.4	V	V_{DD} = 3.15; I_{OL} = 4.0
I_{OL}	4.0			mA	
I_{OH}			-4.0	mA	
Leakage Tristate	-10		+10	µA	0 to 5.25 V input
Output Capacitance		7.5		pF	
t_{RISE}			10	ns	C_{LOAD} = 15pF
t_{FALL}			10	ns	C_{LOAD} = 15pF

OUTPUT PARAMETERS FOR LVCMOS 8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 3.15; I_{OH} = -8.0
V_{OL}			0.4	V	V_{DD} = 3.15; I_{OL} = 8.0
I_{OL}	8.0			mA	
I_{OH}			-8.0	mA	
Leakage Tristate	-10		+10	µA	0 to 5.25 V input
Output Capacitance		7.5		pF	
t_{RISE}			10	ns	C_{LOAD} = 25pF
t_{FALL}			5.0	ns	C_{LOAD} = 25pF

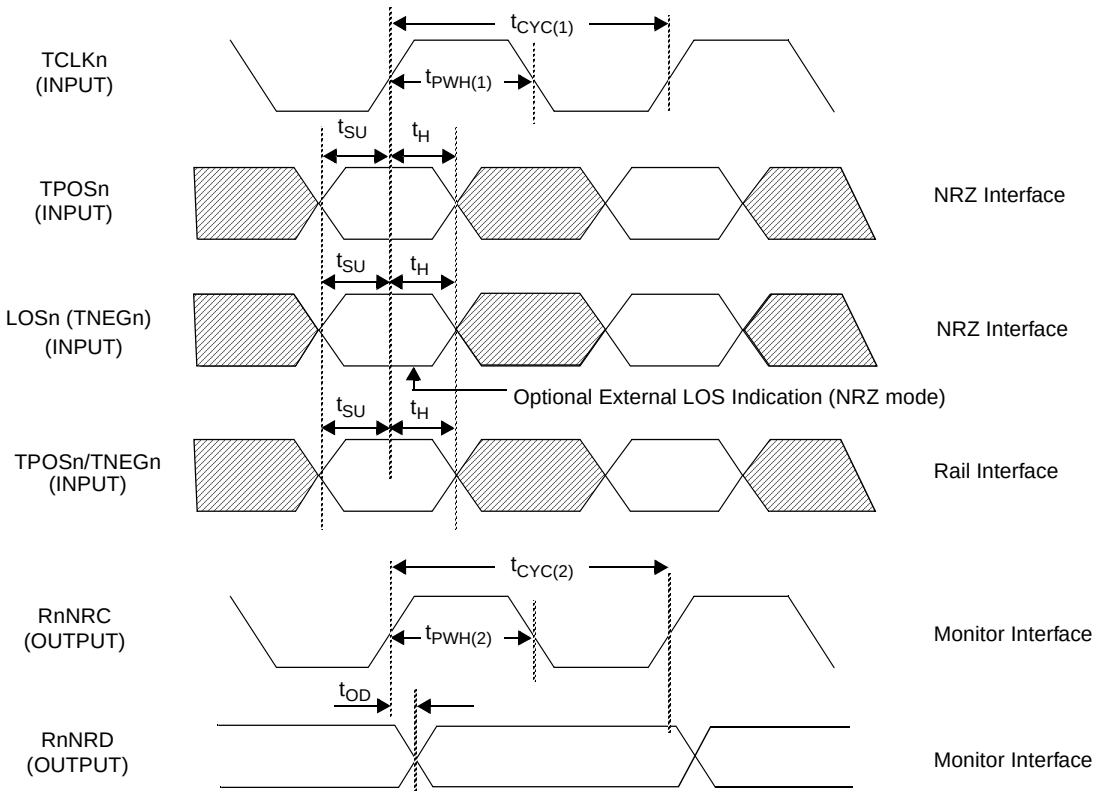
INPUT/OUTPUT PARAMETERS FOR LVTTL/LVCMOS 8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	3.15 ≤ V_{DD} ≤ 3.45
V_{IL}			0.8	V	3.15 ≤ V_{DD} ≤ 3.45
Input leakage current	-10		+10	µA	0 to 5.25 V input
Input capacitance		7.0		pF	
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 3.15; I_{OH} = -8.0
V_{OL}			0.4	V	V_{DD} = 3.15; I_{OL}= 8.0
I_{OL}	8.0			mA	
I_{OH}			-8.0	mA	
t_{RISE}			10	ns	C_{LOAD} = 25pF
t_{FALL}			5.0	ns	C_{LOAD} = 25pF

TIMING CHARACTERISTICS

Detailed timing diagrams for the TL3M device are illustrated in Figures 7 through 26, with values of the timing intervals tabulated below the diagrams. All output times are measured with a maximum 25 pF load capacitance. Timing parameters are measured at voltage levels of $(V_{IH} + V_{IL})/2$ for input signals or $(V_{OH} + V_{OL})/2$ for output signals.

Figure 7. Line Side Transmit Timing for Channel n

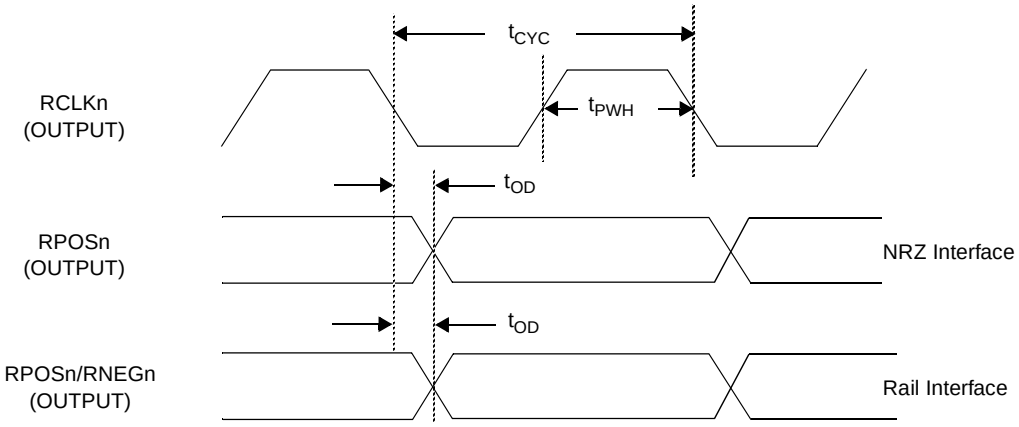


Note: Shown for control bit INVCI (bit 5 in XC1H) equal to 0; data is clocked in on the falling edge when INVCI equals 1. RnNRD is always clocked out on the rising edges of RnNRC. The delay between the input clock TCLKn and output clock RnNRC is not specified.

Parameter	Symbol	Min	Typ	Max	Unit
TCLKn clock period	$t_{CYC(1)}$		See Note 1		ns
TCLKn duty cycle, $t_{PWH(1)}/t_{CYC(1)}$	--	40	50	60	%
TPOSn/TNEGn setup time before TCLKn↑	t_{SU}	2.0			ns
TPOSn/TNEGn hold time after TCLKn↑	t_H	3.0			ns
RnNRC clock period	$t_{CYC(2)}$		See Note 1		ns
RnNRC duty cycle, $t_{PWH(2)}/t_{CYC(2)}$	--	40	50	60	%
RnNRD output delay after RnNRC↑	t_{OD}	0.0		5.0	ns

Note 1: 22.35 ns (DS3) or 29.10 ns (E3).

Figure 8. Line Side Receive Timing for Channel n

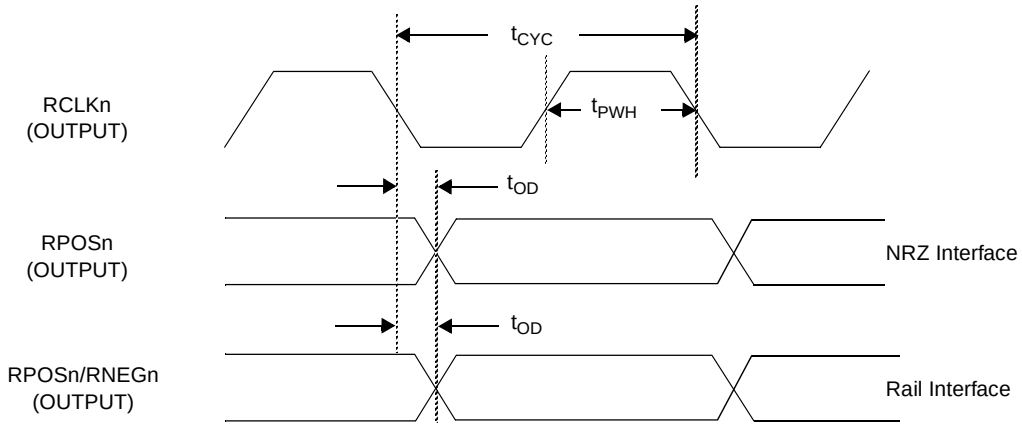


Note: Shown for control bit INVCO (bit 4 in XC1H) equal to 0; data is clocked out on the rising edge when control bit INVCO equals 1. The three signals for all channels are forced to a high impedance state when control bit L3EN (bit 0 in 0C1H) is set to 0, or when a hardware or software reset occurs. Each channel's output is forced to a high impedance state when control bit L3OEN (bit 0 in XC2H) is set to 0.

Parameter	Symbol	Min	Typ	Max	Unit
RCLKn clock period	t_{CYC}		See Note 1		ns
RCLKn duty cycle, t_{PWH}/t_{CYC}	---	45	50	55	%
RPOSn/RNEGn data output delay after RCLKn↓	t_{OD}	0.0		2.0	ns

Note 1. 22.35 ns (DS3) or 29.10 ns (E3).

Figure 9. Line Side Receive Timing in Facility Loopback for Channel n

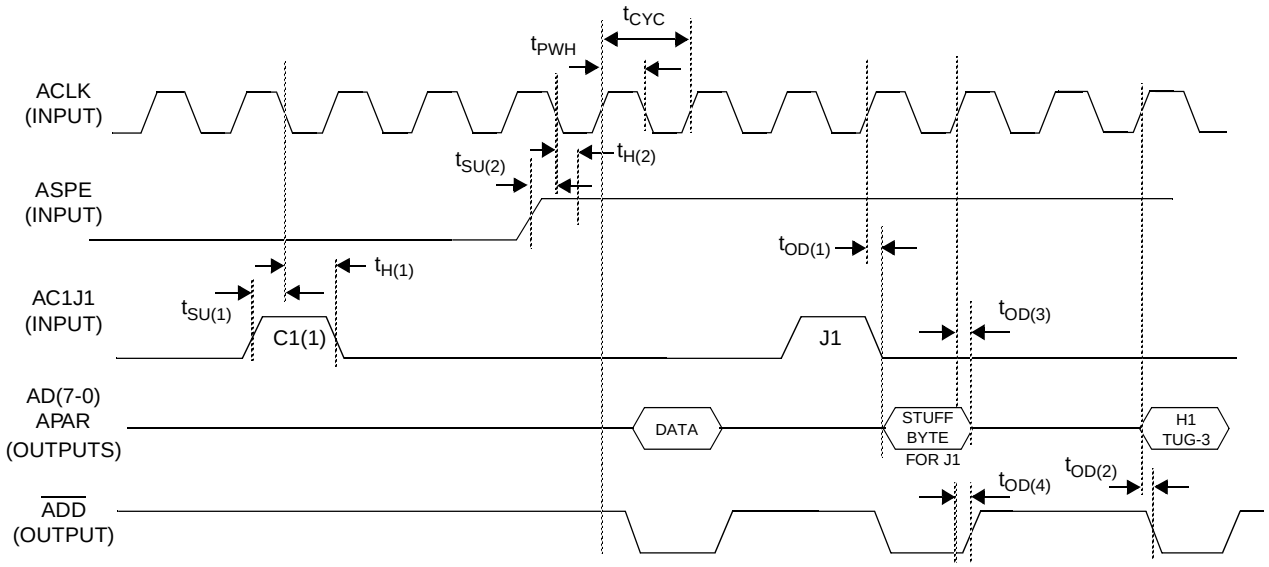


Note: Control bit INVCO (bit 4 in XC1H) has no effect on which edge the data is transmitted. The three signals for all channels are forced to a high impedance state when control bit L3EN (bit 0 in 0C1H) is set to 0, or when a hardware or software reset occurs. Each channel's output is forced to a high impedance state when control bit L3OEN (bit 0 in XC2H) is set to 0. Facility loopback is enabled when control bit FLBK (bit 2 in XC1H) is set to 1.

Parameter	Symbol	Min	Typ	Max	Unit
RCLKn clock period	t_{CYC}		See Note 1		ns
RCLKn duty cycle, t_{PWH}/t_{CYC}	---	45	50	55	%
RPOSn/RNEGn data output delay after RCLKn edge (same relation as on TCLKn to TPOSn/ TNEGn in facility loopback).	t_{OD}	0.0		4.0	ns

Note 1: 22.35 ns (DS3) or 29.10 ns (E3).

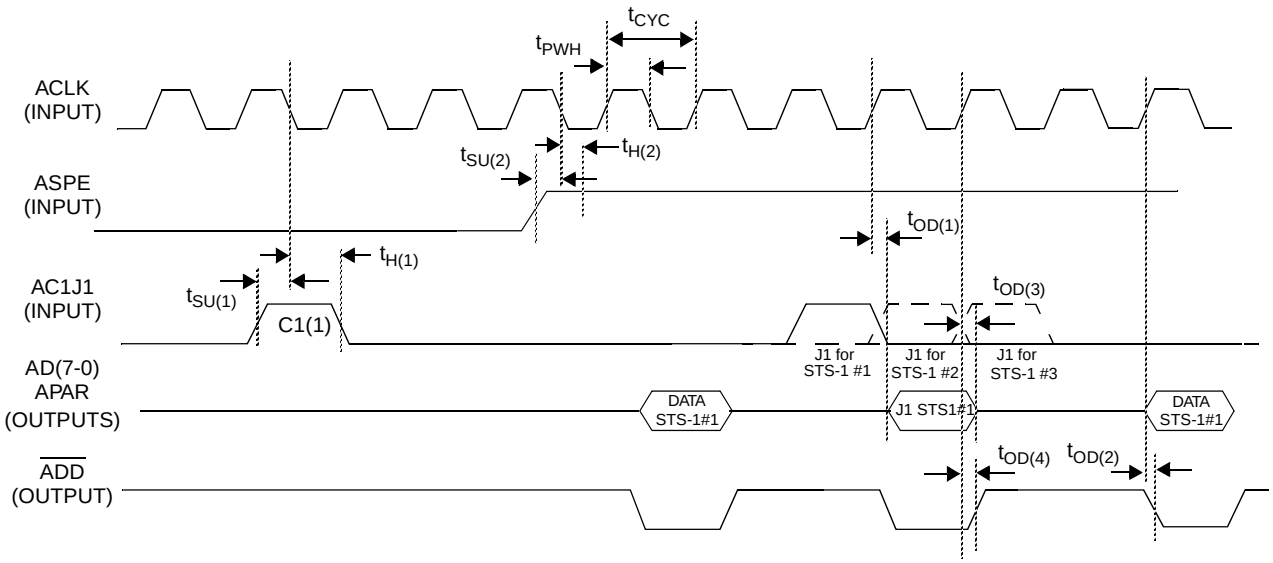
Figure 10. STM-1 Add Bus Derived Interface Timing



Note: The relationship between the J1 and the SPE signals is shown for illustration purposes only. For the STM-1 format, there will be one J1 pulse, which indicates the start of the VC-4 that carries the three TUG-3s. The TUG-3 added to the bus is shown for the TUG-3 designated as A. TUG-3 B will occur one clock cycle later. TUG-3 C will occur two clock cycles later. There is always a one byte delay between the AC1J1/ASPE input signals and the AD(7-0) output leads.

Parameter	Symbol	Min	Typ	Max	Unit
ACLK clock period	t_{CYC}		51.44		ns
ACLK duty cycle, t_{PWH}/t_{CYC}	--	40	50	60	%
AC1J1 setup time before ACLK↓	$t_{SU(1)}$	1.0			ns
AC1J1 hold time after ACLK↓	$t_{H(1)}$	4.0			ns
ASPE setup time before ACLK↓	$t_{SU(2)}$	1.0			ns
ASPE hold time after ACLK↓	$t_{H(2)}$	4.0			ns
AD(7-0) and APAR output delay from ACLK↑	$t_{OD(1)}$	5.0		12.0	ns
$\overline{ADD}$ low output delay from ACLK↑	$t_{OD(2)}$	7.0		13.0	ns
AD(7-0) and APAR tristate delay from ACLK↑	$t_{OD(3)}$	6.0		14.0	ns
$\overline{ADD}$ high output delay from ACLK↑	$t_{OD(4)}$	5.0		12.0	ns

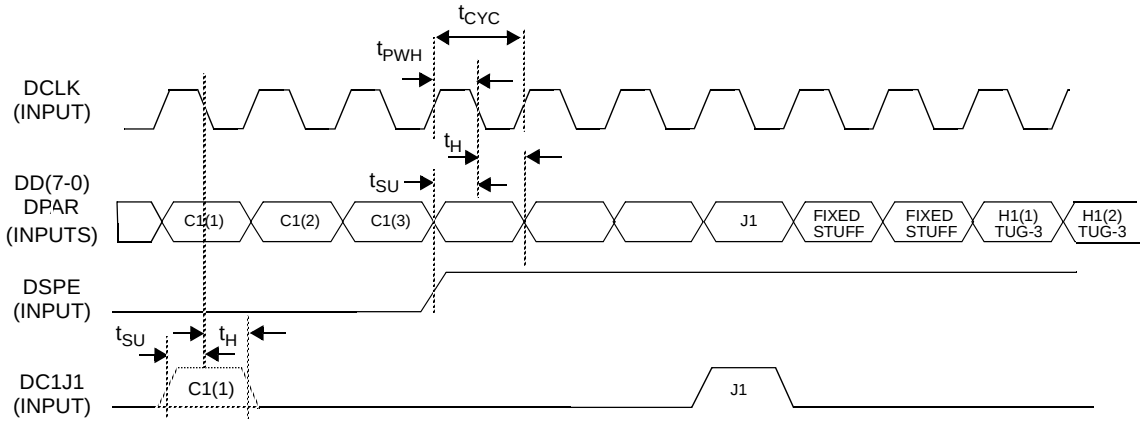
Figure 11. STS-3 Add Bus Derived Interface Timing



Note: The relationship between the J1 and the SPE signals is shown for illustration purposes only. For the STS-3 format, there will be three J1 pulses, which indicate the start of each of the STS-1 SPEs. The STS-1 SPE added to the bus is shown for STS-1 number 1. STS-1 number 2 will occur one clock cycle later. STS-1 number 3 will occur two clock cycles later. There is always a one byte delay between the AC1J1/ASPE input signals and the AD(7-0) output leads.

Parameter	Symbol	Min	Typ	Max	Unit
ACLK clock period	t_{CYC}		51.44		ns
ACLK duty cycle, t_{PWH}/t_{CYC}	--	40	50	60	%
AC1J1 setup time before ACLK↓	$t_{SU(1)}$	1.0			ns
AC1J1 hold time after ACLK↓	$t_{H(1)}$	4.0			ns
ASPE setup time before ACLK↓	$t_{SU(2)}$	1.0			ns
ASPE hold time after ACLK↓	$t_{H(2)}$	4.0			ns
AD(7-0) and APAR output delay from ACLK↑	$t_{OD(1)}$	5.0		12.0	ns
$\overline{\text{ADD}}$ low output delay from ACLK↑	$t_{OD(2)}$	7.0		13.0	ns
AD(7-0) and APAR tristate delay from ACLK↑	$t_{OD(3)}$	6.0		14.0	ns
$\overline{\text{ADD}}$ high output delay from ACLK↑	$t_{OD(4)}$	5.0		12.0	ns

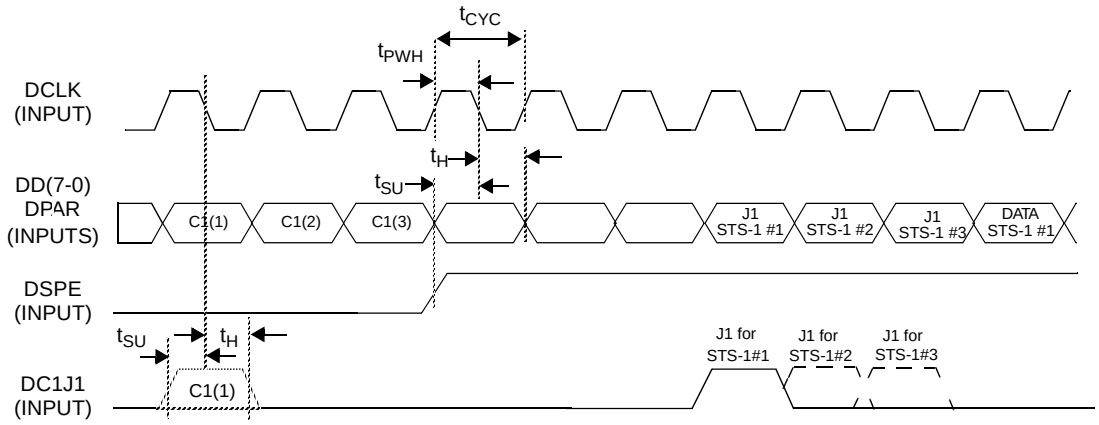
Figure 12. STM-1 Drop Bus Interface Timing



Note: The relationship between J1 and the SPE signals is shown for illustration purposes only, and will be a function of the pointer offset. For the STM-1 format, there will be one J1 pulse which indicates the start of the VC-4 that carries the three TUG-3s. The C1 pulse is shown dotted because the C1 pulse may be provided on the DC1 signal lead. If the DC1 signal lead is not used, it must be grounded.

Parameter	Symbol	Min	Typ	Max	Unit
DCLK clock period	t_{CYC}		51.44		ns
DCLK duty cycle, t_{PWH}/t_{CYC}	--	40	50	60	%
DD(7-0) data/DPAR/DC1J1/DC1/DSPE setup time before DCLK↓	t_{SU}	4.0			ns
DD(7-0) data/DPAR/DC1J1/DC1/DSPE hold time after DCLK↓	t_H	4.0			ns

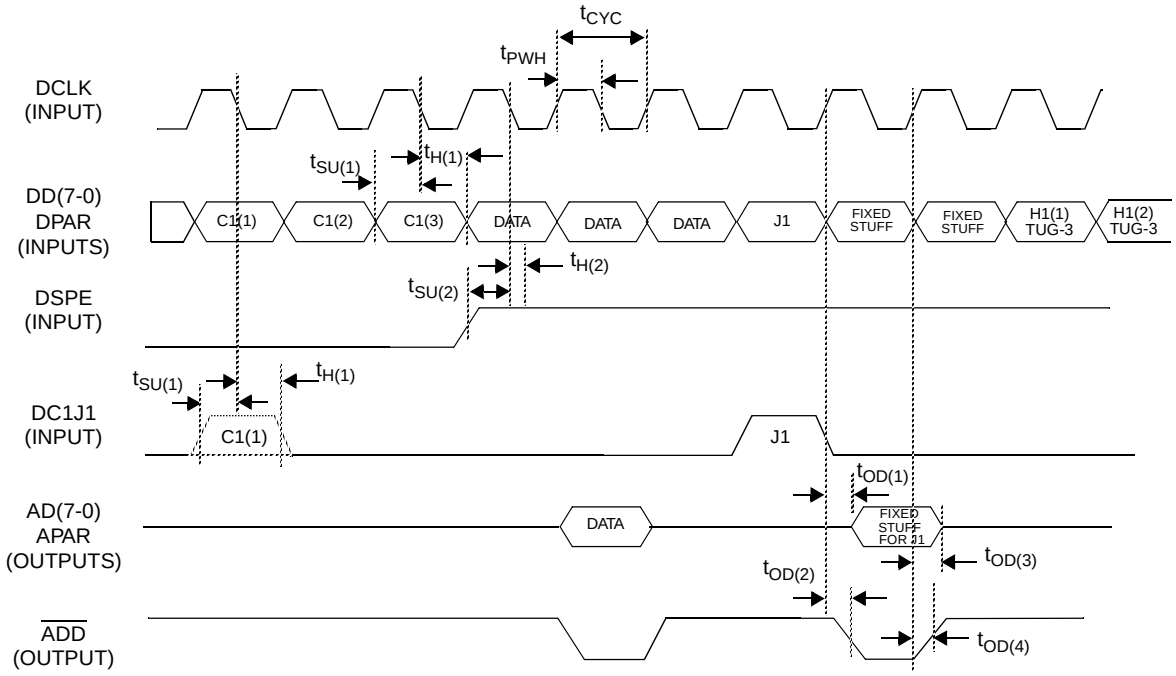
Figure 13. STS-3 Drop Bus Interface Timing



Note: The relationship between J1 and the SPE signals is shown for illustration purposes only, and will be a function of the pointer offset. For the STS-3 format, there will be three J1 pulses which indicate the start of each of the STS-1 SPEs. The C1 pulse is shown dotted because the C1 pulse may be provided on the DC1 signal lead. If the DC1 signal lead is not used, it must be grounded.

Parameter	Symbol	Min	Typ	Max	Unit
DCLK clock period	t_{CYC}		51.44		ns
DCLK duty cycle, t_{PWH}/t_{CYC}	--	40	50	60	%
DD(7-0) data/DPAR/DC1J1/DC1/DSPE setup time before DCLK↓	t_{SU}	4.0			ns
DD(7-0) data/DPAR/DC1J1/DC1/DSPE hold time after DCLK↓	t_H	4.0			ns

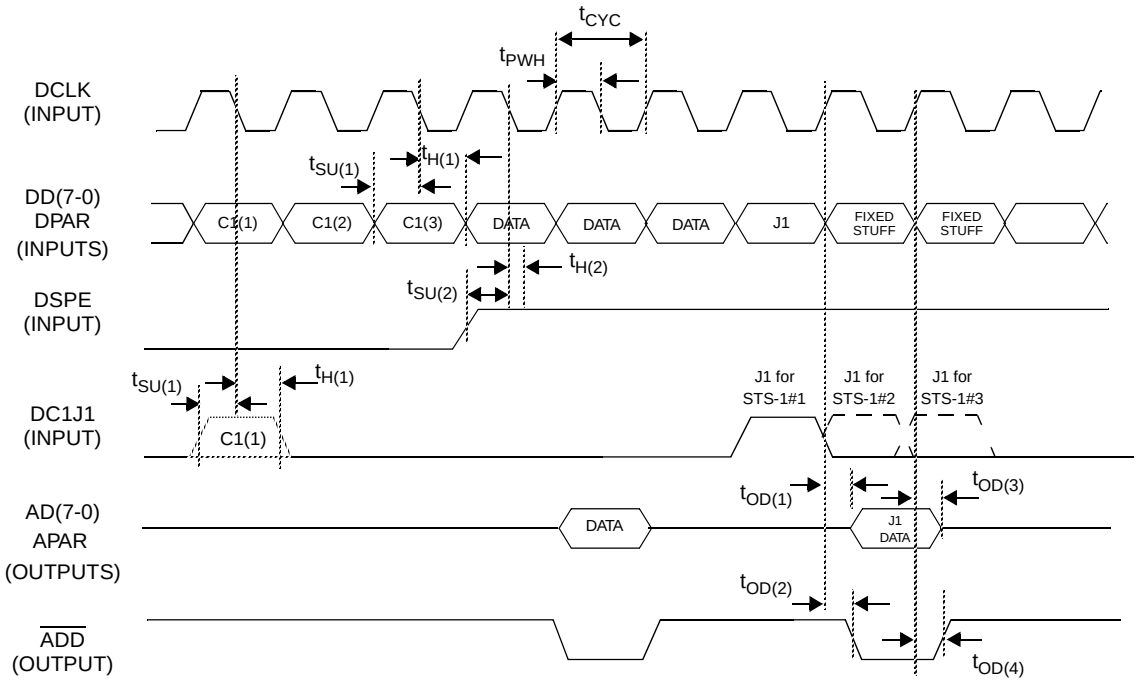
Figure 14. STM-1 Add/Drop Bus Interface Timing



Note: The relationship between J1 and the SPE signals is shown for illustration purposes only, and will be a function of the pointer offset. For the STM-1 format, there will be one J1 pulse which indicates the start of the VC-4 that carries the three TUG-3s. The C1 pulse is shown dotted because the C1 pulse may be provided on the DC1 signal lead. If the DC1 signal lead is not used, it must be grounded. Shown is TUG-3 A being added to the Add bus.

Parameter	Symbol	Min	Typ	Max	Unit
DCLK clock period	t_{CYC}		51.44		ns
DCLK duty cycle, t_{PWH}/t_{CYC}	--	40	50	60	%
DD(7-0) data/DPAR/DC1J1/DC1 setup time before DCLK↓	$t_{SU(1)}$	4.0			ns
DD(7-0) data/DPAR/DC1J1/DC1 hold time after DCLK↓	$t_{H(1)}$	4.0			ns
DSPE setup time before DCLK↓	$t_{SU(2)}$	1.0			ns
DSPE hold time after DCLK↓	$t_{H(2)}$	4.0			ns
AD(7-0) data and APAR delay after DCLK↑	$t_{OD(1)}$	5.0		15.0	ns
$\overline{ADD}$ indicator delay after DCLK↑	$t_{OD(2)}$	7.0		15.0	ns
AD(7-0) and APAR tristate delay after DCLK↑	$t_{OD(3)}$	6.0		15.0	ns
$\overline{ADD}$ high delay after DCLK↑	$t_{OD(4)}$	5.0		12.0	ns

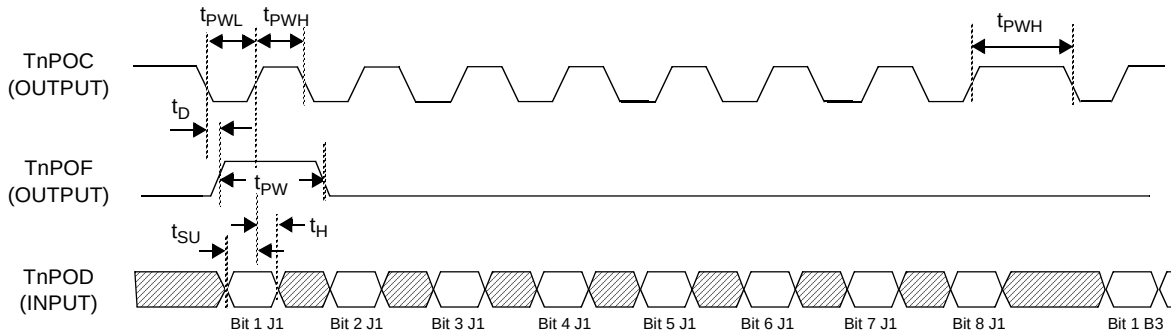
Figure 15. STS-3 Add/Drop Bus Interface Timing



Note: The relationship between J1 and the SPE signals is shown for illustration purposes only, and will be a function of the pointer offset. For the STS-3 format, there will be three J1 pulses with each J1 pulse indicating the start of an STS-1. The C1 pulse is shown dotted because the C1 pulse may be provided on the DC1 signal lead. If the DC1 signal lead is not used, it must be grounded. Shown is STS-1 number 1 being added to the Add bus.

Parameter	Symbol	Min	Typ	Max	Unit
DCLK clock period	t_{CYC}		51.44		ns
DCLK duty cycle, t_{PWH}/t_{CYC}	--	40	50	60	%
DD(7-0)/DPAR/DC1J1/DC1 setup time before DCLK↓	$t_{SU(1)}$	4.0			ns
DD(7-0)/DPAR/DC1J1/DC1 hold time after DCLK↓	$t_{H(1)}$	4.0			ns
DSPE setup time before DCLK↓	$t_{SU(2)}$	1.0			ns
DSPE hold time after DCLK↓	$t_{H(2)}$	4.0			ns
AD(7-0) data and APAR delay after DCLK↑	$t_{OD(1)}$	5.0		15.0	ns
$\overline{ADD}$ indicator delayed after DCLK↑	$t_{OD(2)}$	7.0		15.0	ns
AD(7-0) data and APAR tristate after DCLK↑	$t_{OD(3)}$	6.0		15.0	ns
$\overline{ADD}$ indicator high after DCLK↑	$t_{OD(4)}$	5.0		12.0	ns

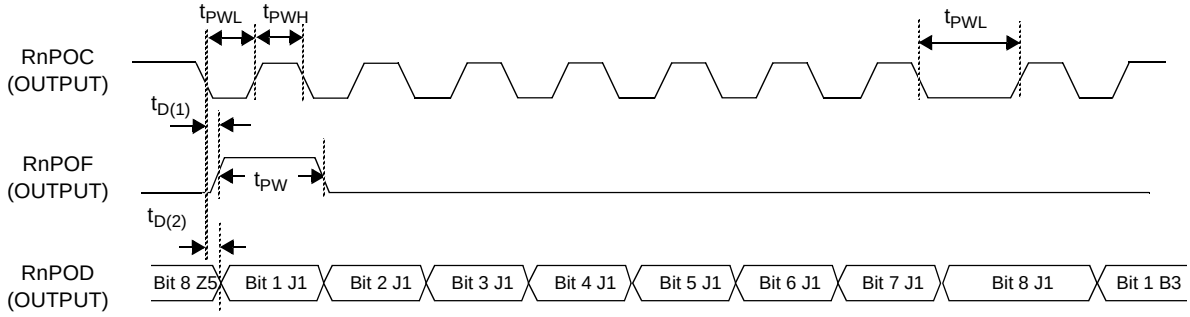
Figure 16. Transmit Path Overhead Timing



Note: The clock cycle that corresponds to bit 8 in each overhead byte is stretched.

Parameter	Symbol	Min	Typ	Max	Unit
TnPOC high time	t_{PWH}	617		3395	ns
TnPOC low time	t_{PWL}		772		ns
TnPOF output delay after TnPOC↓	t_D	-1.0		2.0	ns
TnPOD setup time before TnPOC↑	t_{SU}	15.0			ns
TnPOD data hold time after TnPOC↑	t_H	1.0			ns
TnPOF pulse width	t_{PW}		1389		ns

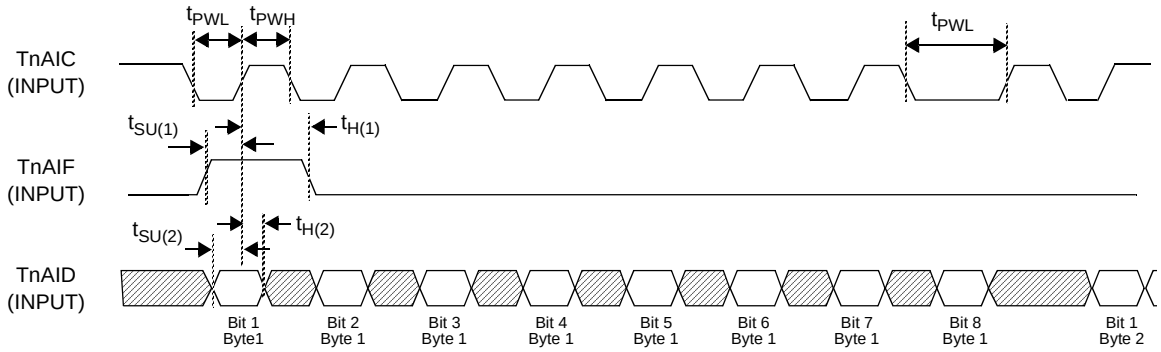
Figure 17. Receive Path Overhead Timing



Note: The clock cycle that corresponds to bit 8 in each overhead byte is stretched.

Parameter	Symbol	Min	Typ	Max	Unit
RnPOC low time	t_{PWL}	617		3395	ns
RnPOC high time	t_{PWH}		772		ns
RnPOF output delay after RnPOC↓	$t_{D(1)}$	0.0		2.0	ns
RnPOD output delay after RnPOC↓	$t_{D(2)}$	0.0		2.0	ns
RnPOF pulse width	t_{PW}		1389		ns

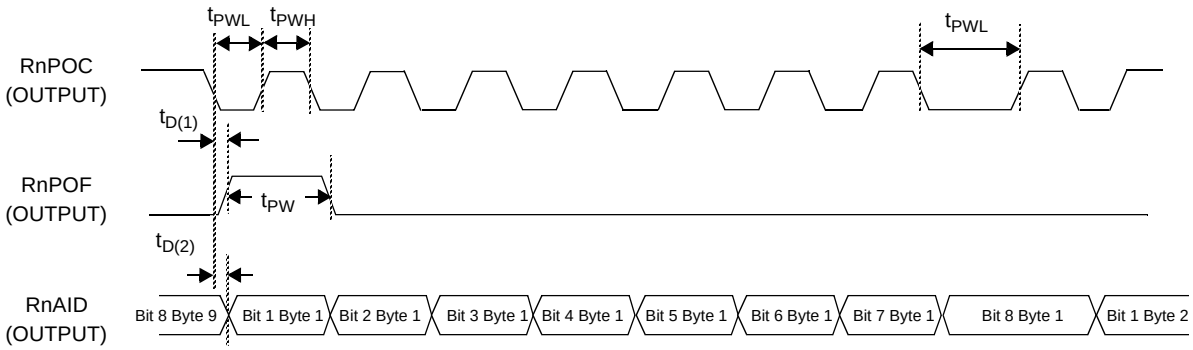
Figure 18. Transmit Alarm Indication Port Timing



Note: The alarm indication byte consists of eight bits and it is repeated nine times. Bit 8 in each byte is stretched. The first four bits correspond to the REI count to be transmitted (bits 1 through 4 in G1), bit 5 is the path RDI value to be transmitted, and bits 6 and 7 are set to 0, while bit 8 is set to 1.

Parameter	Symbol	Min	Typ	Max	Unit
TnAIC low time	t_{PWL}	617		3395	ns
TnAIC high time	t_{PWH}		772		ns
TnAIF setup time before TnAIC↑	$t_{SU(1)}$	2.0			ns
TnAIF hold time after TnAIC↑	$t_{H(1)}$	1.0			ns
TnAID setup time before TnAIC↑	$t_{SU(2)}$	2.0			ns
TnAID hold time after TnAIC↑	$t_{H(2)}$	1.0			ns

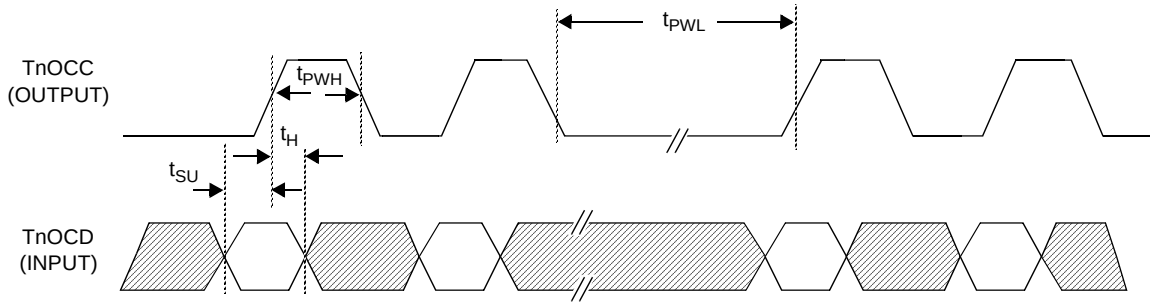
Figure 19. Receive Alarm Indication Port Timing



Note: The alarm indication byte consists of eight bits and it is repeated nine times. Bit 8 in each byte is stretched. The first four bits correspond to the REI count (bits 1 through 4 in G1) based on the received B3 byte errors, bit 5 is the path RDI value to be transmitted based on received alarm indications, and bits 6 and 7 are set to 0, while bit 8 is set to 1.

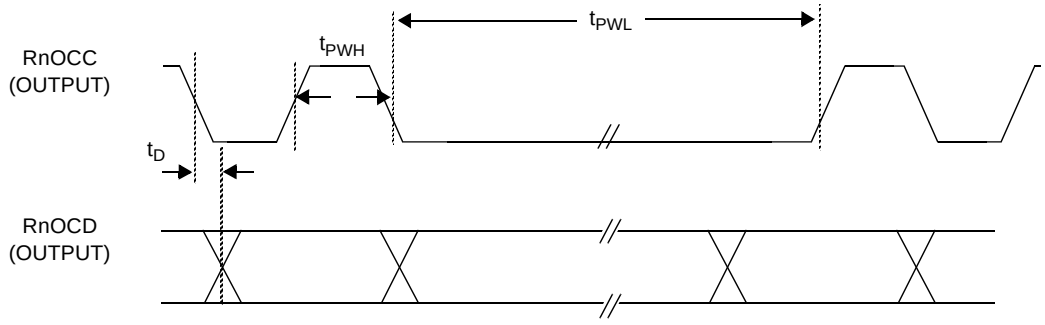
Parameter	Symbol	Min	Typ	Max	Unit
RnPOC low time	t_{PWL}	617		3395	ns
RnPOC high time	t_{PWH}		772		ns
RnPOF output delay after RnPOC↓	$t_{D(1)}$	0.0		2.0	ns
RnAID output delay after RnPOC↓	$t_{D(2)}$	0.0		2.0	ns
RnPOF pulse width	t_{PW}		1389		ns

Figure 20. Transmit Overhead Communications Channel Interface Timing



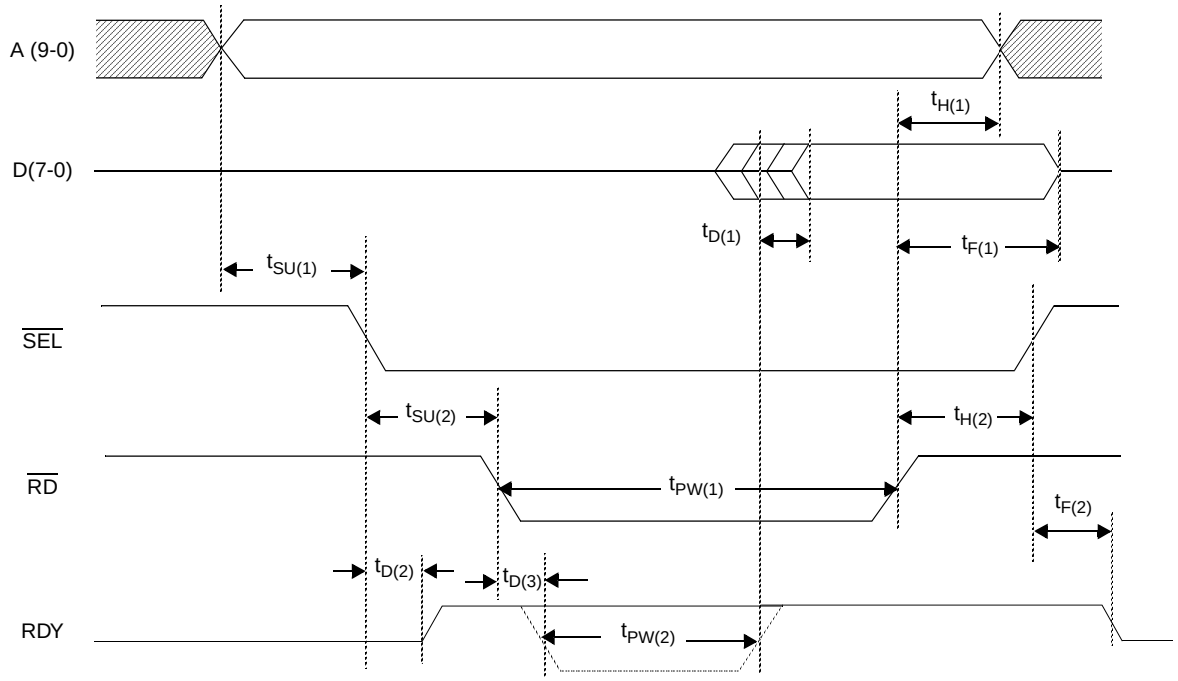
Parameter	Symbol	Min	Typ	Max	Unit
TnOCC high time	t_{PWH}		772		ns
TnOCC low time	t_{PWL}	617		11900	ns
TnOCD setup time before TnOCC↑	t_{SU}	18.0			ns
TnOCD hold time after TnOCC↑	t_H	0.0			ns

Figure 21. Receive Overhead Communications Channel Interface Timing



Parameter	Symbol	Min	Typ	Max	Unit
RnOCC high time	t_{PWH}		772		ns
RnOCC low time	t_{PWL}	4646		7700	ns
RnOCD output delay after RnOCC↓	t_D	0.0		3.5	ns

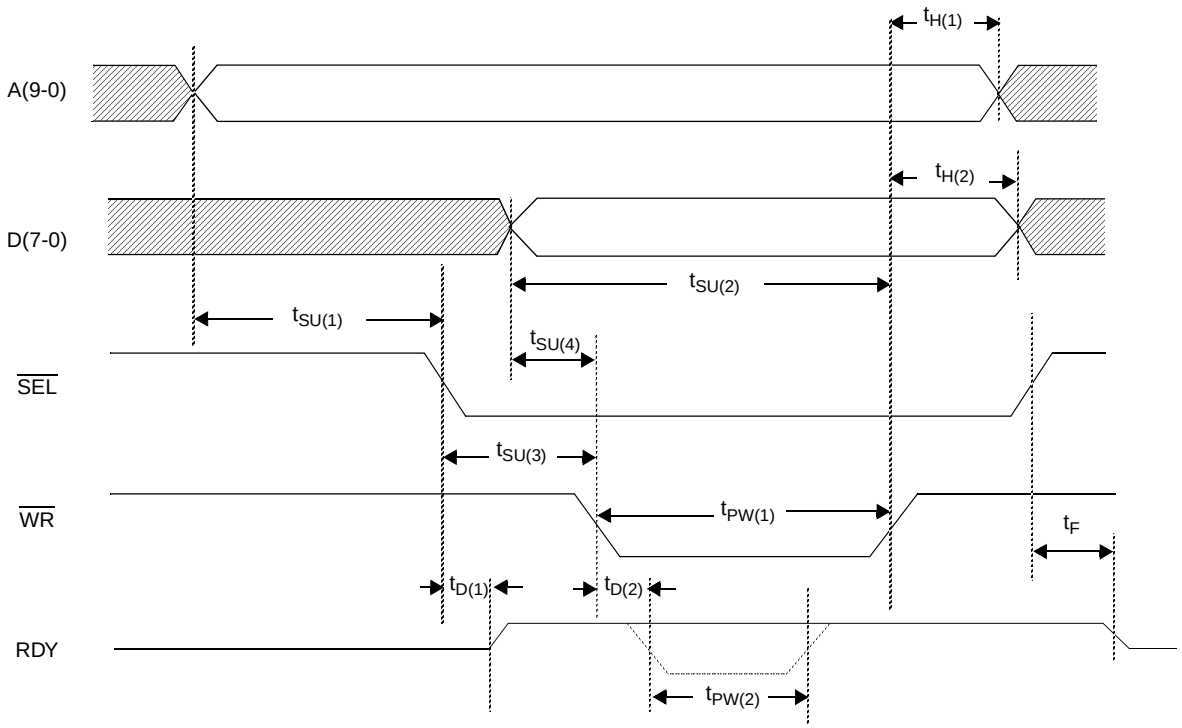
Figure 22. Intel Microprocessor Read Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
A(9-0) address hold time after $\overline{RD}\uparrow$	$t_{H(1)}$	4.0			ns
A(9-0) address setup time before $\overline{SEL}\downarrow$	$t_{SU(1)}$	0.0			ns
D(7-0) data valid delay after RDY$\uparrow$	$t_{D(1)}$			13.0	ns
D(7-0) data float time after $\overline{RD}\uparrow$	$t_{F(1)}$			13.0	ns
$\overline{RD}$ pulse width	$t_{PW(1)}$	40.0			ns
$\overline{SEL}\downarrow$ setup time before $\overline{RD}\downarrow$	$t_{SU(2)}$	10.0			ns
$\overline{SEL}\downarrow$ hold time after $\overline{RD}\uparrow$	$t_{H(2)}$	0.0			ns
RDY$\uparrow$ delay after $\overline{SEL}\downarrow$	$t_{D(2)}$			16.0	ns
RDY$\downarrow$ delay after $\overline{RD}\downarrow$	$t_{D(3)}$			14.0	ns
RDY pulse width (See Note 1)	$t_{PW(2)}$	0.0		48 * Rcyc	µs
RDY float time after $\overline{SEL}\uparrow$	$t_{F(2)}$			12.5	ns

Note 1: RDY goes low when the address being read corresponds to a RAM location but remains high during status or control register access.
R_{CYC} is the period, in nanoseconds, of the RAM clock (RAMCI) (e.g., RAMCI @ 25MHz yields $t_{PW(2)}$ = 1.92 µs max).

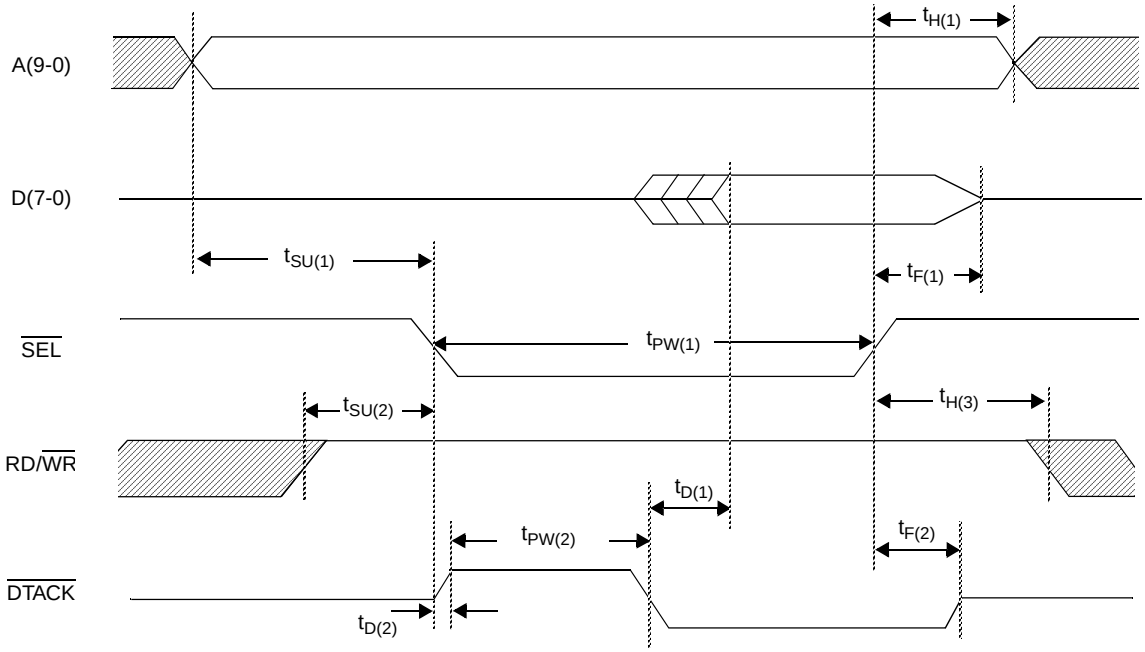
Figure 23. Intel Microprocessor Write Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
A(9-0) address hold time after $\overline{WR}\uparrow$	$t_{H(1)}$	4.0			ns
A(9-0) address setup time before $\overline{SEL}\downarrow$	$t_{SU(1)}$	0.0			ns
D(7-0) data valid setup time before $\overline{WR}\uparrow$	$t_{SU(2)}$	4.0			ns
D(7-0) data hold time after $\overline{WR}\uparrow$	$t_{H(2)}$	3.0			ns
$\overline{SEL}\downarrow$ setup time before $\overline{WR}\downarrow$	$t_{SU(3)}$	10.0			ns
$\overline{WR}$ pulse width	$t_{PW(1)}$	40.0			ns
RDY$\uparrow$ delay after $\overline{SEL}\downarrow$	$t_{D(1)}$			16.0	ns
RDY$\downarrow$ delay after $\overline{WR}\downarrow$	$t_{D(2)}$			15.0	ns
RDY pulse width (See Note 1)	$t_{PW(2)}$	0.0		48 * Rcyc	ns
RDY float time after $\overline{SEL}\uparrow$	t_F			13.0	ns
RAM cycle D(7-0) valid setup time before $\overline{WR}\downarrow$ (See Note 1)	$t_{SU(4)}$	-2 * Rcyc			ns

Note 1: RDY goes low when the address being written to corresponds to a RAM location but remains high during status or control register access.
R_{CYC} is the period, in nanoseconds, of the RAM clock (RAMCI) (e.g., RAMCI @ 25 MHz yields: $t_{SU(4)}$= -80 ns min, $t_{PW(2)}$ = 1.92 µs max).

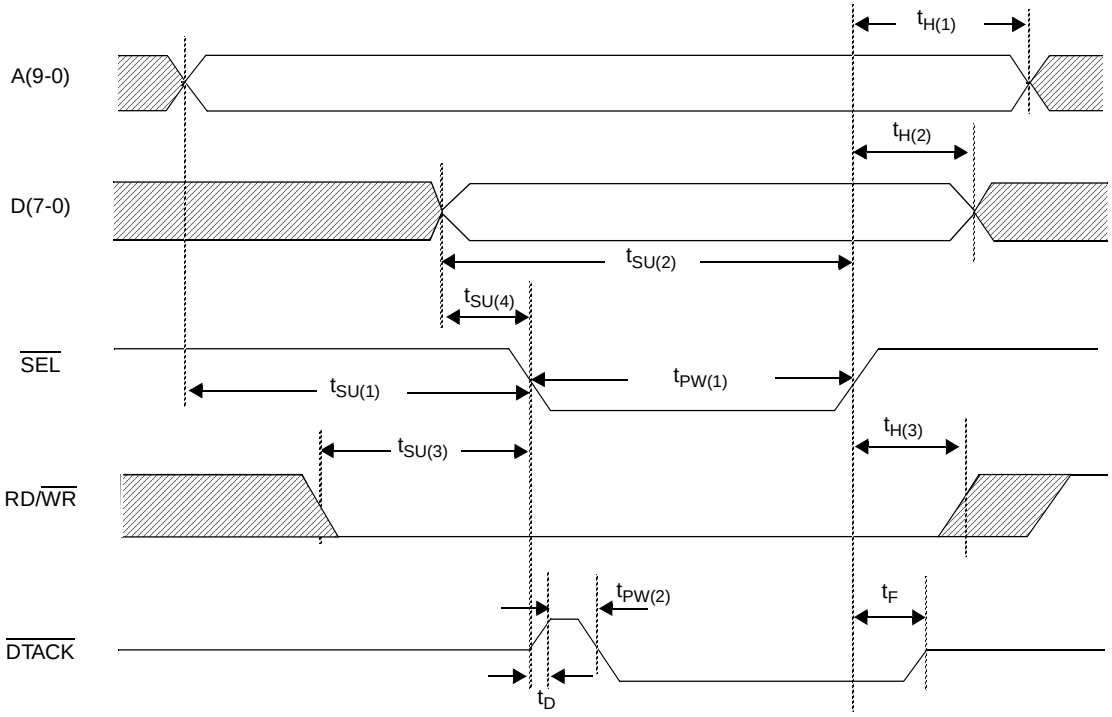
Figure 24. Motorola Microprocessor Read Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
A(9-0) address hold time after $\overline{SEL}\uparrow$	$t_{H(1)}$	5.0			ns
A(9-0) address valid setup time before $\overline{SEL}\downarrow$	$t_{SU(1)}$	2.0			ns
D(7-0) data valid delay after $\overline{DTACK}\downarrow$	$t_{D(1)}$			4.0	ns
D(7-0) data float time after $\overline{SEL}\uparrow$	$t_{F(1)}$			15.0	ns
$\overline{SEL}$ pulse width	$t_{PW(1)}$	40.0			ns
RD/$\overline{WR}\uparrow$ setup time before $\overline{SEL}\downarrow$	$t_{SU(2)}$	5.0			ns
RD/$\overline{WR}\uparrow$ hold time after $\overline{SEL}\uparrow$	$t_{H(3)}$	5.0			ns
$\overline{DTACK}\uparrow$ delay after $\overline{SEL}\downarrow$	$t_{D(2)}$			15.0	ns
$\overline{DTACK}$ pulse width (See Note 1)	$t_{PW(2)}$	0.0		48 * Rcyc	µs
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	$t_{F(2)}$			11.0	ns

Note 1: R_{CYC} is the period, in nanoseconds, of the RAM clock (RAMCI).
(e.g., RAMCI @ 25 MHz yields $t_{PW(2)}$ = 1.92 µs max).

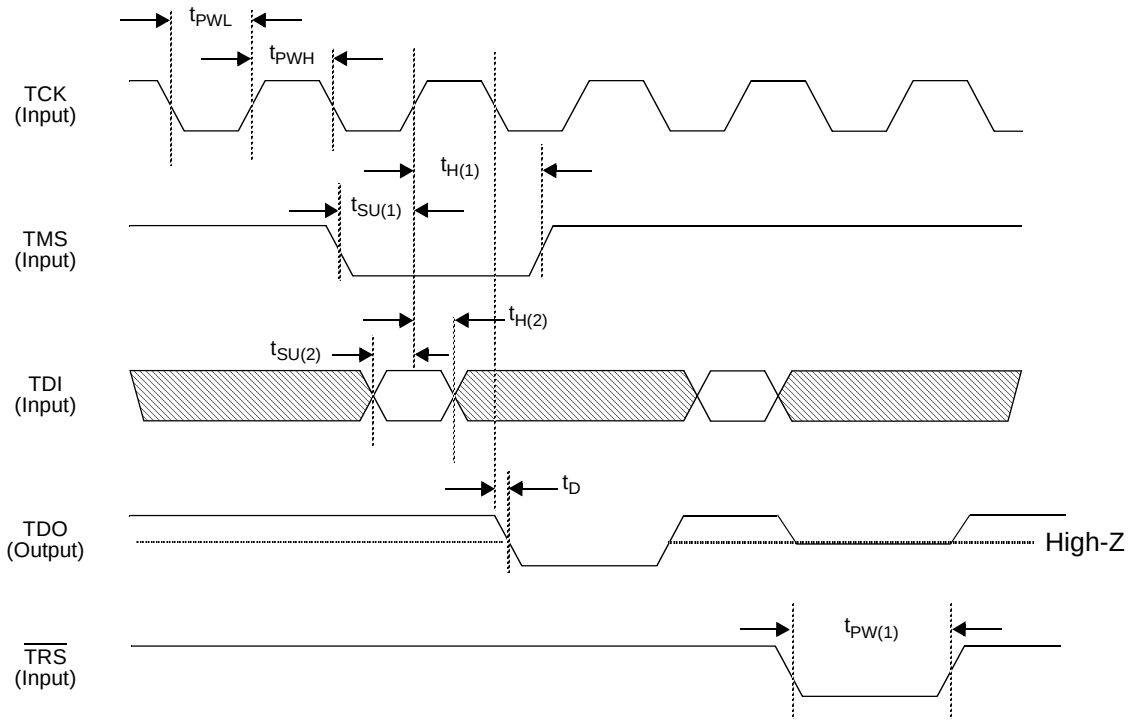
Figure 25. Motorola Microprocessor Write Cycle Timing



Parameter	Symbol	Min	Typ	Max	Unit
A(9-0) address hold time after $\overline{SEL}\uparrow$	$t_{H(1)}$	5.0			ns
A(9-0) address valid setup time before $\overline{SEL}\downarrow$	$t_{SU(1)}$	2.0			ns
D(7-0) data valid setup time before $\overline{SEL}\uparrow$	$t_{SU(2)}$	6.5			ns
D(7-0) data hold time after $\overline{SEL}\uparrow$	$t_{H(2)}$	5.0			ns
$\overline{SEL}$ pulse width	$t_{PW(1)}$	40.0			ns
RD/$\overline{WR}\downarrow$ setup time before $\overline{SEL}\downarrow$	$t_{SU(3)}$	5.0			ns
RD/$\overline{WR}\downarrow$ hold time after $\overline{SEL}\uparrow$	$t_{H(3)}$	5.0			ns
$\overline{DTACK}\uparrow$ delay after $\overline{SEL}\downarrow$	t_D			15.0	ns
$\overline{DTACK}$ pulse width (See Note 1)	$t_{PW(2)}$	0.0		48 * Rcyc	ns
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	t_F			11.0	ns
RAM cycle D(7-0) valid setup time before $\overline{SEL}\downarrow$ (See Note 1)	$t_{SU(4)}$	-2 * Rcyc			ns

Note 1: Rcyc is the period, in nanoseconds, of the RAM clock (RAMCI).
(e.g., RAMCI @ 25 MHz yields: $t_{SU(4)}$= -80 ns min, $t_{PW(2)}$ = 1.92 µs max).

Figure 26. Boundary Scan Timing



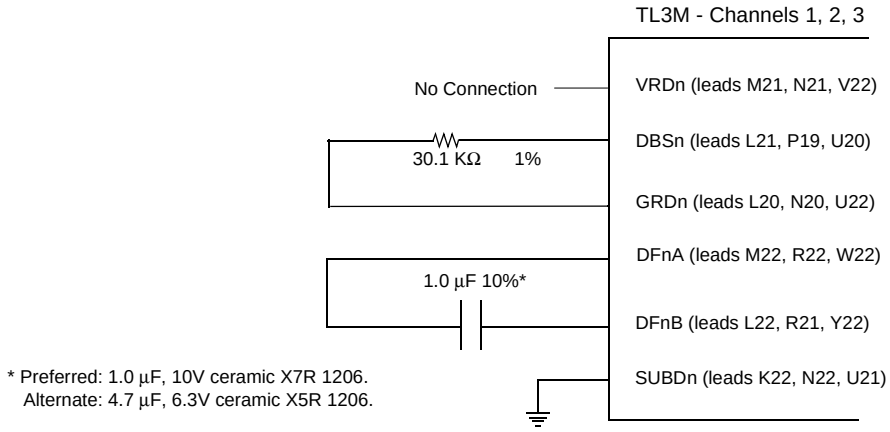
Parameter	Symbol	Min	Max	Unit
TCK clock high time	t_{PWH}	50.0		ns
TCK clock low time	t_{PWL}	50.0		ns
TMS setup time before TCK↑	$t_{SU(1)}$	3.0	-	ns
TMS hold time after TCK↑	$t_{H(1)}$	2.0	-	ns
TDI setup time before TCK↑	$t_{SU(2)}$	3.0	-	ns
TDI hold time after TCK↑	$t_{H(2)}$	4.0	-	ns
TDO output delay after TCK↓	t_D	-	15.0	ns
$\overline{TRS}$ pulse width	$t_{PW(1)}$	250		ns

OPERATION

DIGITAL DESYNCHRONIZER PLL CONNECTIONS

The following diagram shows the external connections required for each of the three digital desynchronizers, where n defines the channels 1 through 3.

Figure 27. Digital Desynchronizer External Component Connections

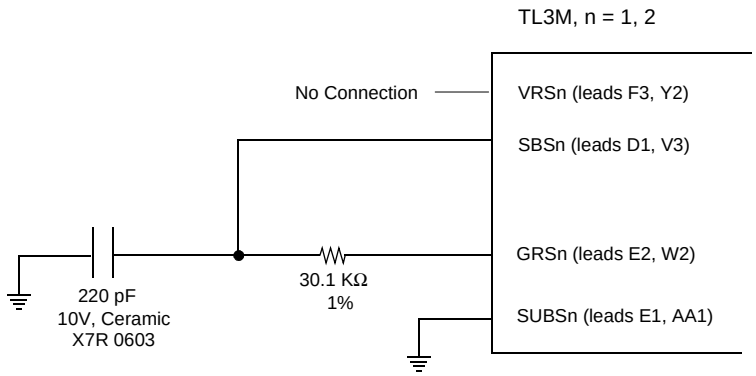


Traces should be kept as short as possible. Place the external components as close as possible to the associated device leads. Please refer to AN-537 (TXC-03453-AN1) for additional recommendations for board layout design. This Application Note is available on the TL3M page of the TranSwitch web site, www.transwitch.com.

TRANSMIT AND RECEIVE SYNTHESIZER CONNECTIONS

The following diagram shows the external connections required for the two synthesizer circuits.

Figure 28. Transmit and Receive Synthesizer External Component Connections



Traces should be kept as short as possible. Place the external components as close as possible to the associated device leads. Please refer to AN-537 (TXC-03453-AN1) for additional recommendations for board layout design. This Application Note is available on the TL3M page of the TranSwitch web site, www.transwitch.com.

TYPICAL TEST RESULTS

Output Jitter

Test Condition	Maximum Measured Jitter (UIpp) at RCLKn output	Jitter Limit Specified by Telcordia GR-253 Ed. 3 Sept. 2000 (UIpp)	
		Required Range See note 3	Objective Range
Mapping Jitter	0.094	0.4	N/A
Single Pointer Adjustment	0.137	0.094 + 0.3	N/A
Pointer Adjustment Burst	0.204	1.3	N/A
Phase Transient Pointer Adjustment Burst	0.170	1.2	N/A
Periodic Pointer Adjustments	0.402 (T = 7.5ms)	N/A	1.0
(87-3 sequence)	0.282 (T = 34ms)	1.0	N/A
	0.117 (T = 6s)[1]	1.0	N/A
Periodic Pointer Adjustments	0.589 (T = 7.5ms)	N/A	1.3
with added or canceled pointer adjustments	0.423 (T = 34ms)	1.3	N/A
(43-44 or 86-4 sequence)	0.128 (T = 6s) [1]	1.3	N/A
Periodic Pointer Adjustments	0.255 (T = 4ms)	N/A	1.5
Continuous Pattern	0.231 (T = 34ms)	1.0	N/A
	0.125 (T = 10s)	1.0	N/A
Periodic Pointer Adjustments	0.380 (T = 18ms) [2]	1.3	N/A
Continuous Pattern with added or canceled	0.275 (T = 34ms)	1.3	N/A
Pointer Adjustments	0.122 (T = 10s)	1.3	N/A

Figure 29. STS3/DS3 Mapping, Measured Jitter

Notes for Figure 29:

1: W&G ANT20 Max. interval = 6.66S

2: W&G ANT20 Min interval = 15mS

3: Valid for DS3 mapped up to +/-45ppm

4: Data errors never occurred during the tests; 5) A low jitter COMBUS reference clock is required

5: Jitter measured with standard filters: HP=10 Hz, LP=400 kHz

Test Condition Fig. 15-3/G.783	Maximum Measured Jitter (UIpp) at RCLKn output		Jitter Limit Specified by ITU-T G.783 ETSI EN 300 417-1-1 V1.1.3 (UIpp) See Note 2	
	HP1/LP	**HP2/LP**	**HP1/LP**	**HP2/LP**
Mapping Jitter	0.063	0.045	0.4	0.075
Sequence A	0.063	0.054	0.4	0.075
Sequence B	0.078	0.050	0.4	0.075
Sequence C	0.099	0.050	0.4	0.075
Sequence D	0.059	0.044	0.75	0.075

Figure 30. STM1/E3 Mapping, Measured Jitter

Notes for Figure 30:

1: Data errors never occurred during the tests

2: Valid for E3 mapped up to +/-55ppm

3: A low jitter COMBUS reference clock is required

4: These measurements represent both AU-4 or TU-3 pointer movements for the SDH mappings

5: HP1=100 Hz, HP2=10 kHz, LP=800 k

MTIE PER GR-253-CORE SEC 5.7

	Observation Time, S							
	0.1 Sec.		1.0 Sec.		10 Sec.		100 Sec.	
Test Condition (GR-253-CORE)	**MTIE (nS)**	**Limit (nS)**	**MTIE (nS)**	**Limit (nS)**	**MTIE (nS)**	**Limit (nS)**	**MTIE (nS)**	**Limit (nS)**
Single STS-1 Pointer Adjustment Phase Variation, Pointer spacing T=100S (GR-253-CORE Fig. 5-38)	(Note 1)	95	9.0	170	50	170	160	170
Maximum Rate Pointer Burst Phase Variation (GR-253-CORE Fig. 5-39)	5.0	182	18	510	53	510	150	510
Phase Transient Pointer Burst Phase Variation (GR-253-CORE Fig. 5-40)	4.0	165	12	1155	60	1155	100	1155
Periodic STS-1 Pointer Adjustment Phase Variation, 87-3 Pattern at T=4mS (beyond objective range, GR-253-CORE Fig. 5-42).	22	183	42	800	43	800	50	800
Periodic STS-1 Pointer Adjustment Phase Variation, 87-3 Pattern at T=100mS (GR-253-CORE Fig. 5-42).	12	183	105	800	210	800	210	800
Periodic STS-1 Pointer Adjustment Phase Variation, Continuous Pattern at T=7.5mS (objective range, GR-253-CORE Fig. 5-42).	9.0	183	22	800	30	800	30	800
Periodic STS-1 Pointer Adjustment Phase Variation, Continuous Pattern at T=34mS (GR-253-CORE Fig. 5-42).	10	183	30	800	50	800	50	800
Periodic STS-1 Pointer Adjustment Phase Variation, Continuous Pattern at T=100mS (GR-253-CORE Fig. 5-42).	7.0	183	43	800	70	800	70	800
Periodic STS-1 Pointer Adjustment Phase Variation, Continuous Pattern at T=1S (GR-253-CORE Fig. 5-42).	4.0	183	12	800	110	800	180	800
Note 1: Minimum observation is 1 Sec. since sample rate was set to 1 Sec.								
General measurement note: Min. MTIE interval is 0.1 Sec., Max 100 Sec. per GR-253-CORE								

	Observation Time, S							
	0.1 Sec.		1.0 Sec.		10 Sec.		100 Sec.	
Test Condition (GR-253-CORE)	**MTIE (nS)**	**Limit (nS)**	**MTIE (nS)**	**Limit (nS)**	**MTIE (nS)**	**Limit (nS)**	**MTIE (nS)**	**Limit (nS)**
Periodic STS-1 Pointer Adjustment Phase Variation, Continuous Pattern at T=10S (GR-253-CORE Fig. 5-42).	11	183	22	800	25	800	90	800
Note 1: Minimum observation is 1 Sec. since sample rate was set to 1 Sec.								
General measurement note: Min. MTIE interval is 0.1 Sec., Max 100 Sec. per GR-253-CORE								

Figure 31. STS-1 Pointer Movements on DS3 Payload

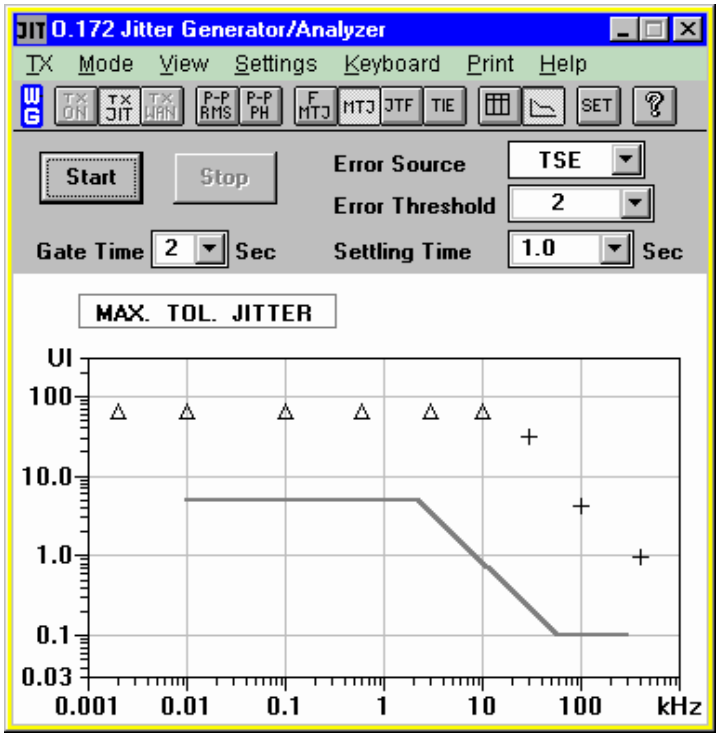


Figure 32. Jitter Tolerance for DS3 (from GR-499)

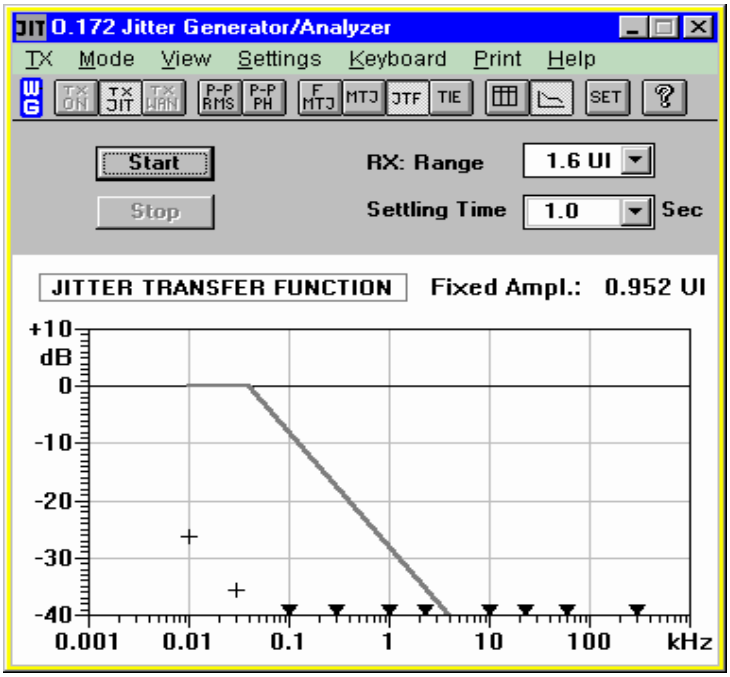


Figure 33. Jitter Transfer for DS3 (GR-253)

Note: At frequencies above 30 KHz, the TL3M exceeds the Jitter Transfer Mask because the applied jitter is attenuated below the generated jitter level. The generated jitter is well within the specification. This result is consistent with limitations of the test equipment and open-ended nature of the specification (-20dB slope with no plateau).

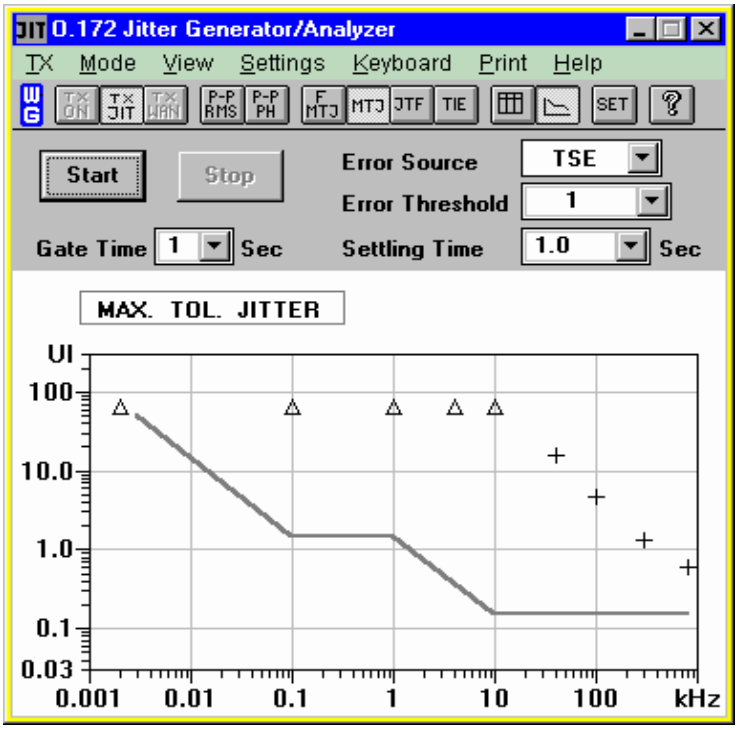


Figure 34. Jitter Tolerance for E3 (ITU G.751 Fig. 2)

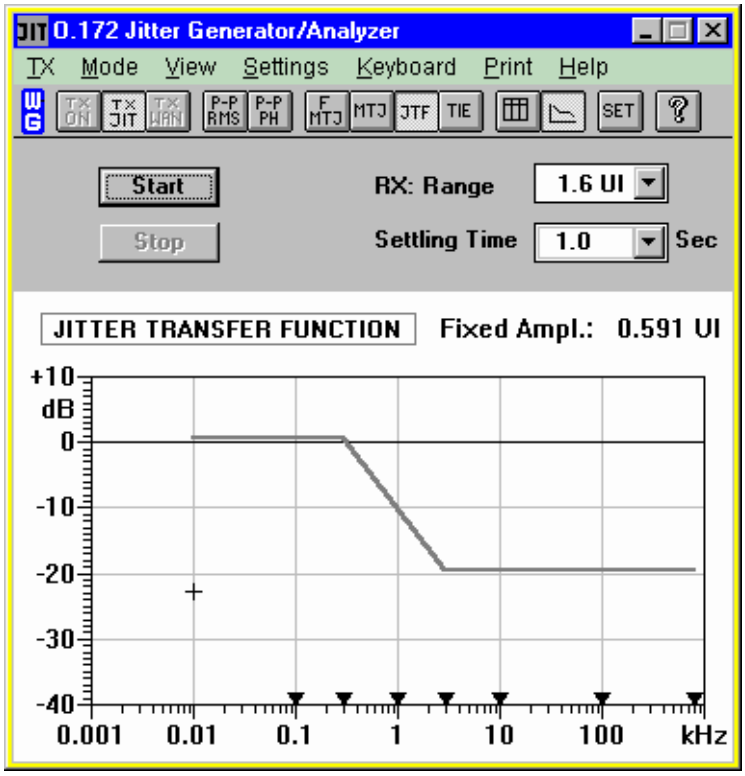


Figure 35. Jitter Transfer for E3 (from ITU G.823 Fig. 15)

TESTING

Loopbacks

Facility and line loopback capabilities are provided for each channel. Their operations are shown in Figure 36. Diagrams illustrating these two loopback modes are provided in the Memory Map section at Address XC1, Bits 2 and 1.

Writing a 1 to control bit FLBK (Bit 2) enables facility loopback. When facility loopback is enabled, the internal DS3/E3 transmit signal becomes the internal receive signal. Either transmit line interface may be used, positive/negative rail or NRZ.

Line loopback is enabled by writing a 1 to control bit L3LBK (Bit 1). The DS3/E3 receive output becomes the transmit line input. The receive line output may be positive/negative rail or NRZ. AIS will be sent as the received data when control bit LLBAIS (bit 0 in register 0C4H) is a 1. When control bit LLBAIS is set to 0, receive data is provided at the rail or NRZ interface.

Test Generators and Analyzers

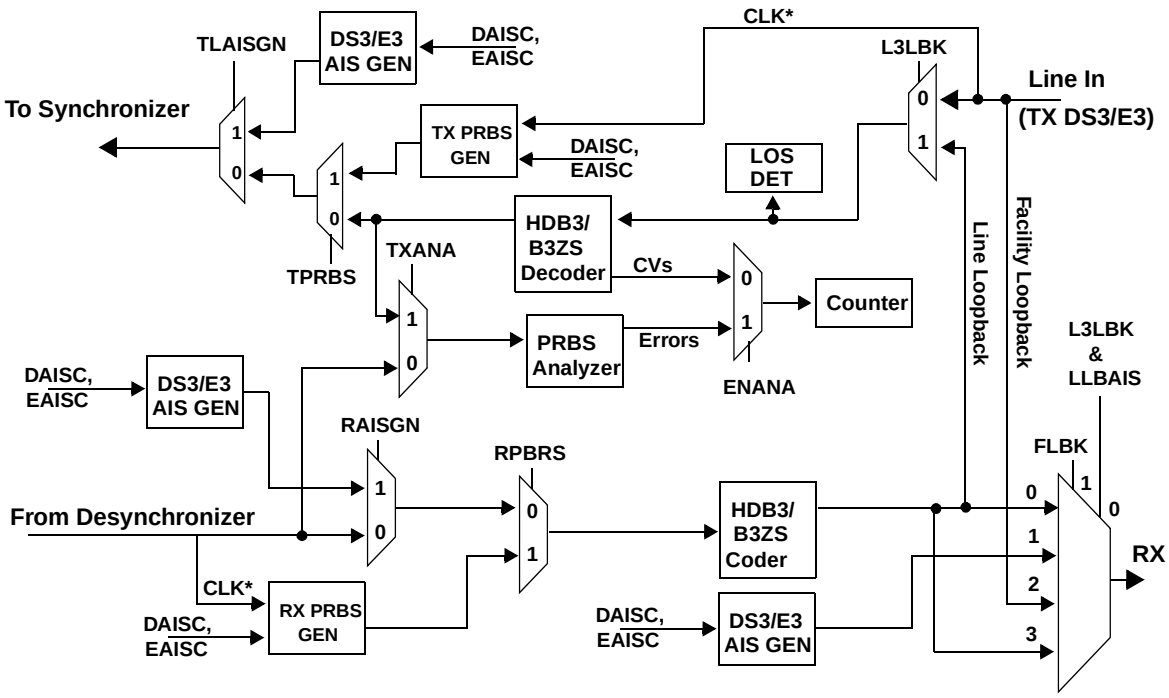
Two pseudo-random binary sequence (PRBS) test generators are provided for each channel, one in the receive direction and the other in the transmit direction, as shown in Figure 36. The generators provide either a 2^{15}-1 or 2^{23}-1 pseudo-random pattern using a common control bit. The selection of the PRBS pattern is also common with the PRBS test analyzer. The test sequence of 2^{23}-1 is selected when a 1 is written into control bit PAT23 (bit 4 in register XC6H). When control bit PAT23 is 0, the pattern is 2^{15}-1.

The transmit test generator is enabled by writing a 1 to control bit TPRBS (bit 1 in register XC6H). When enabled, the transmit test generator inserts the selected pseudo-random pattern in place of the line signal. The transmit test generator uses the clock signal provided at the Transmit Line Clock (TCLK) input lead in order to function.

The receive test generator is enabled by writing a 1 to control bit RPRBS (bit 0 in register XC6H). When enabled, the receive test generator inserts the pseudo-random test pattern in place of the received desynchronized NRZ data.

The test analyzer is enabled by writing a 1 to control bit ENANA (bit 3 in register XC6H). Receive NRZ data is analyzed when a 0 is written to control bit TXANA (bit 2 in register 0C6H). When a 1 is written to control bit TXANA, the transmit NRZ data path is monitored. The selection of the test analyzer disables the decoder coding violation count to the 16-bit CV counter in registers XAEH and XAFH. Instead, this 16-bit counter is configured to count PRBS test analyzer errors when in lock.

Figure 36. Per Channel Loopbacks and PRBS Test Generators/Analyzer



*Note: The Tx and Rx PBRS Generators will normally use their respective clocks for pattern generation. If the normal clock is missing, the AIS clock appropriate to the application will be used to generate the pattern.

Rx Output		
FLBK	L3LBK & LLBAIS	Rx Output
0	0	Rx Data
0	1	DS3/E3 AIS
1	0	Tx Data
1	1	Rx Data

BOUNDARY SCAN

Introduction

The IEEE 1149.1 standard defines the requirements of a boundary scan architecture that has been specified by the IEEE Joint Test Action Group (JTAG). Boundary scan is a specialized scan architecture that provides observability and controllability for the interface leads of the device. As shown in Figure 37, one cell of a boundary scan register is assigned to each input or output lead to be observed or tested (bidirectional leads may have two cells). The boundary scan capability is based on a Test Access Port (TAP) controller, instruction and bypass registers, and a boundary scan register bordering the input and output leads. The boundary scan test bus interface consists of four input signals (Test Clock (TCK), Test Mode Select (TMS), Test Data Input (TDI) and Test Reset ($\overline{\text{TRS}}$)) and a Test Data Output (TDO) output signal. Boundary scan signal timing is shown in Figure 26.

The TAP controller receives external control information via a Test Clock (TCK) signal and a Test Mode Select ($\overline{\text{TMS}}$) signal, and sends control signals to the internal scan paths. The TAP controller is reset by asserting the $\overline{\text{TRS}}$ lead low for a minimum of 250 nanoseconds. Detailed information on the operation of this state machine can be found in the IEEE 1149.1 standard. The serial scan path architecture consists of an instruction register, a boundary scan register and a bypass register. These three serial registers are connected in parallel between the Test Data Input (TDI) and Test Data Output (TDO) signals, as shown in Figure 37.

The boundary scan function will be reset and disabled by holding lead $\overline{\text{TRS}}$ low. When boundary scan testing is not being performed the boundary scan register is transparent, allowing the input and output signals to pass to and from the TL3M device's internal logic. During boundary scan testing, the boundary scan register may disable the normal flow of input and output signals to allow the device to be controlled and observed via scan operations.

Boundary Scan Operation

The maximum frequency the TL3M device will support for boundary scan is 10 MHz. The timing diagrams for the boundary scan interface leads are shown in Figure 26.

The instruction register contains three bits. The TL3M device performs the following six boundary scan test instructions:

The EXTEST test instruction (000) provides the ability to test the connectivity of the TL3M device to external circuitry.

The SAMPLE test instruction (001) provides the ability to examine the boundary scan register contents without interfering with device operation.

The BYPASS test instruction (111) provides the ability to bypass the TL3M boundary scan and instruction registers.

The IDCODE test instruction (110) activates output on lead TDO of the device ID information.

The MEMBIST test instruction (101) provides a means of testing all internal RAMs. This function is intended for TranSwitch manufacturing test only.

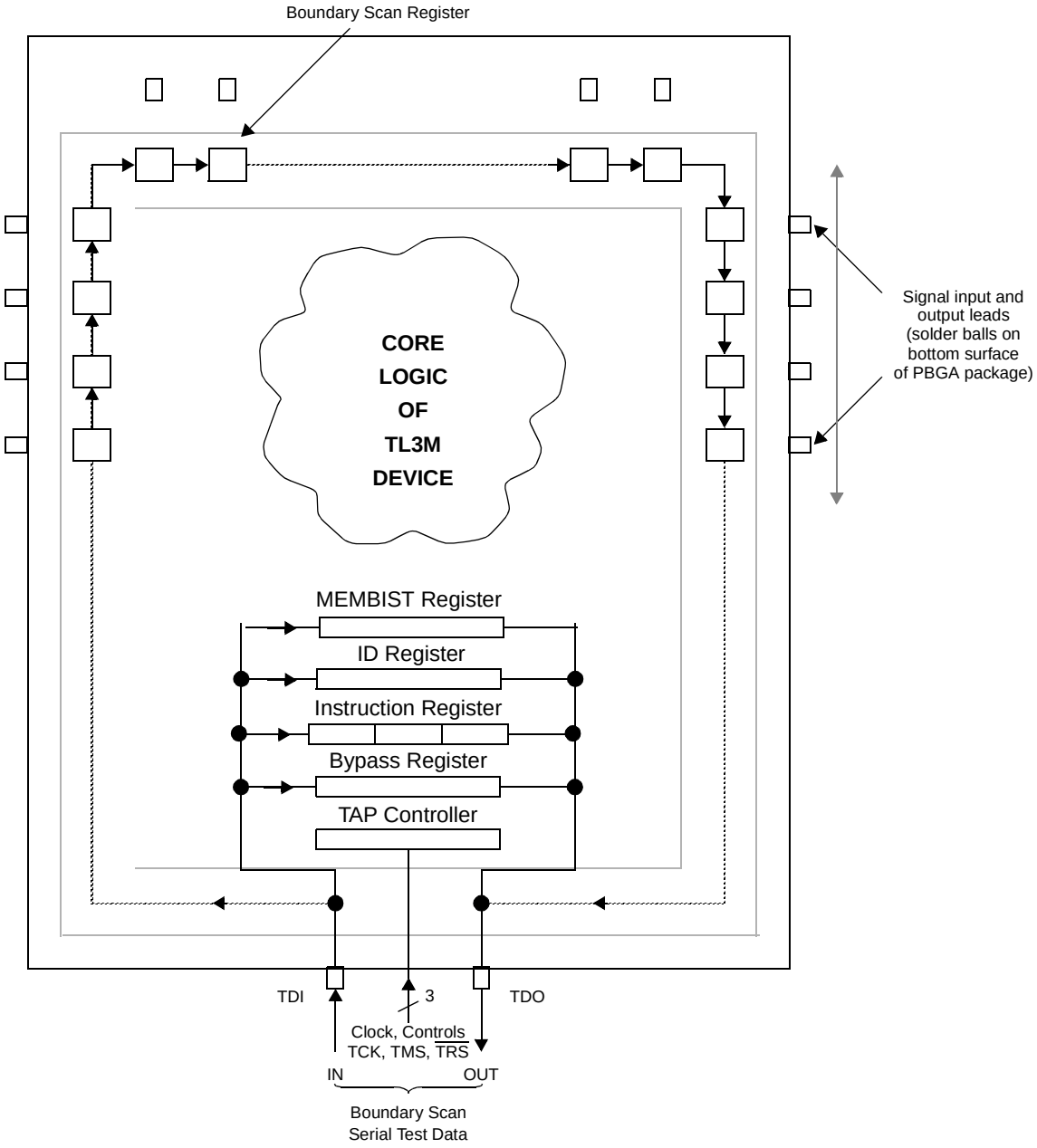
The HI-Z test instruction (011) places all outputs in a high impedance state.

During the *Capture - IR* state, a fixed value (101) is loaded into the instruction register.

Boundary Scan Chain

There are 163 scan cells in the TL3M boundary scan chain. Bidirectional signals require two scan cells. Additional scan cells are used for direction control as needed. A Boundary Scan Description Language (BSDL) source file is available via the Products page of the TranSwitch World Wide Web site (www.transwitch.com).

Figure 37. Boundary Scan Schematic



MEMORY MAP

There are four memory map segments. One, with leading address digit 0, contains registers used for global (common) operation, including device identification (ID). The other three segments have addresses with leading digit X, and their registers correspond to the mapper channel identified by X (where X = 1, 2, 3).

Register status types are: R/W: Read/write; R: Read only; R(L)/W: Read(Latched)/Write.

Read only registers must not be written. Registers that are shown with all bits Reserved must not be accessed, unless otherwise indicated. When writing to a register that contains from one to seven bits that are shown as Reserved or Not Used, these bits should be written as zeros, unless otherwise indicated. Please note that Reserved bits may perform specific test functions and must be set to the specified value when written in order to assure proper device operation, while Not Used bits have no function but should to be set to the specified value when written in case they are assigned functions in future versions of the device, for purposes of backwards compatibility with existing application designs.

Please note that a hardware reset (lead $\overline{\text{RESET}}$), or a software reset via control bit RESETS (bit 0 in register 0C7H), will result in all per channel control bits, Reserved and Not Used bits in used registers (1CXH-3CXH, where X = any listed value in the memory map) being reset to the 1 state, and all common control bits, Reserved and Not Used bits in used registers (0CXH) being reset to the 0 state.

DEVICE IDENTIFICATION REGISTERS (Manufacturer ID plus Triple Level 3 Mapper ID))

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0F0	R	1	1	0	1	0	1	1	1
0F1	R	1	1	0	1	0	0	0	0
0F2	R	1	1	0	1	0	1	1	1
0F3	R	0	0	1	1	0	0	0	0
0F4	R	Set to 0				Set to 0			

Description

The manufacturer and device identifiers are based on the manufacturer ID format given in IEEE standard 1149.1 on Boundary Scan, the ID number assigned by the Solid State Products Engineering Council (JEDEC) to The TranSwitch Corporation, and the part number digits assigned to the TL3M device by TranSwitch. The serial format for this 4-byte ID is shown below, where the MSB is bit 7 in register 0F3H and the LSB (fixed at the value of 1) is bit 0 in register 0F0H:

MSB LSB

Revision	Part Number	Manufacturer Identify	1
4-bits	16 bits	11 bits	

The manufacturer ID for all TranSwitch devices is defined as the binary equivalent of 107, located in bits 3 through 0 in register 0F1H, and bits 7 through 1 of register 0F0H. The part number of the TL3M is 03453, which is expressed as a binary number in bits 3 through 0 in register 0F3H, bits 7 through 0 in register 0F2H, and bits 7 through 4 in register 0F1H. The revision field is in bits 7 through 4 of register 0F3H.

CORE IDENTIFICATION REGISTERS (Manufacturer ID plus Level 3 Mapper Core ID)

Address	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XF0	R	1	1	0	1	0	1	1	1
XF1	R	1	1	0	0	0	0	0	0
XF2	R	1	1	0	1	0	1	1	1
XF3	R	0	0	1	1	0	0	0	0
XF4	R	1	0	0	1	0	0	0	0

Description

A core ID is provided in registers XF0H through XF4H for each of the L3M mapper channel cores. A core ID is indicated by the value of 90 hex in the XF4H register. The core ID is otherwise similar in format to the device ID in registers 0F0H through 0F3H, except that the part number and revision fields correspond to the basic L3M mapper core, part number 03452.

COMMON CONTROL REGISTERS

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0C0		Reserved							
0C1		Reserved							
0C2	R/W	Reserved				INTZN	INTEN	ADDEN	L3EN
0C3		Reserved							
0C4		Reserved							
0C5	R/W	Reserved					TSTCH1	TSTCH0	LLBAIS
0C6		Reserved							
0C7	R/W	Reserved				RESET3	RESET2	RESET1	RESETS

PER CHANNEL CONTROL REGISTERS

Where X=1, 2, or 3, which corresponds to the selected channel:

Address (Hex)	Mode*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XC0	R/W	BFOM1	BFOM0	DPOS1	DPOS0	APOS1	APOS0	Reserved	DS3
XC1	R/W	DECODE	CODE	INVCI	INVCO	RING	FLBK	L3LBK	Reserved
XC2	R/W	ALM2AIS	Reserved	TLAISGN	TPAISGN	TPAIS00	Reserved	ADBEN	L3OEN
XC3	R/W	EXN1	EXK3	EXF3	EXH4	EXF2	EXG1	EXC2	EXJ1
XC4	R/W	EXOO	Reserved	RAMRDI	REIEN	XALM2AIS	Reserved	TLOC2AIS	TLOS2AIS
XC5	R/W	COR	Reserved		POH2RAM	RAISGN	RAISEN	WGDEC	PSL2AIS
XC6	R/W	Reserved			PAT23	ENANA	TXANA	TPRBS	RPRBS
XC7	R/W	TESTB3	FIXPTR	Reserved			TXRST	RXRST	RESETC
XC8	R/W	C2 Compare							
XC9	R/W	Reserved						RDI5	REIBLK
XCA	R/W	Reserved		NOPOH	Reserved				

COMMON STATUS REGISTERS

Address (Hex)	Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0B0	R	Reserved					INT3	INT2	INT1
0B1	R(L)/W	Reserved					INT3	INT2	INT1
0B2-0B5		Not Used							
0B6	R	ADBCN	Reserved						
0B7	R(L)/W	ADBCN	Reserved						

DEVICE COMMON INTERRUPT MASK OR ENABLE REGISTERS

Address (Hex)	Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0BA	R/W	Reserved					INT3	INT2	INT1
0BB		Not Used							
0BC		Not Used							
0BD	R/W	ADBCN	Reserved						

PER CHANNEL STATUS REGISTERS

Where X=1, 2, or 3, which corresponds to the selected channel:

Address (Hex)	Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XB0	R	DLOC	DLOJ1	BUSERR	E1AIS	LOP	PAIS	PSLERR	C2EQ0
XB1	R(L)/W	DLOC	DLOJ1	BUSERR	E1AIS	LOP	PAIS	PSLERR	C2EQ0
XB2	R	RDI	L3LOS	L3LOC	TOVFL	L3AIS	RAMLOC	ALOC	ALOJ1
XB3	R(L)/W	RDI	L3LOS	L3LOC	TOVFL	L3AIS	RAMLOC	ALOC	ALOJ1
XB4	R	SINT	Reserved	J1NEW	TUG3NEW	ROVFL	AISLOC	XISTAT	XPAIS
XB5	R(L)/W	Reserved	Reserved	J1NEW	TUG3NEW	ROVFL	AISLOC	XISTAT	XPAIS
XB6	R	L3ERR	LOVFL	RFRST	TFRST	PLLLOC	TPLOC	RPLOC	OOL
XB7	R(L)/W	L3ERR	LOVFL	RFRST	TFRST	PLLLOC	TPLOC	RPLOC	OOL

PER CHANNEL INTERRUPT MASK OR ENABLE REGISTERS

Where X=1, 2, or 3, which corresponds to the selected channel:

Address (Hex)	Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XBA	R/W	DLOC	DLOJ1	BUSERR	E1AIS	LOP	PAIS	PSLERR	C2EQ0
XBB	R/W	RDI	L3LOS	L3LOC	TOVFL	L3AIS	RAMLOC	ALOC	ALOJ1
XBC	R/W	HINT	Reserved	NEW	TUG3NEW	ROVFL	AISLOC	XISTAT	XPAIS
XBD	R/W	L3ERR	LOVFL	RFRST	TFRST	PLLLOC	TPLOC	RPLOC	OOL

PER CHANNEL TRANSMIT POH BYTE AND O-BIT REGISTERS

Where X=1, 2, or 3, which corresponds to the selected channel:

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X00 to X3F	R/W	Transmit J1 Byte (64 bytes)							
X40	R/W	Transmit B3 Error Mask							
X41	R/W	Transmit C2 Byte							
X42	R/W	Transmit G1 Byte							
X43	R/W	Transmit F2 Byte							
X44	R/W	Transmit H4 Byte							
X45	R/W	Transmit F3 Byte							
X46	R/W	Transmit K3 Byte							
X47	R/W	Transmit N1 Byte							
X48		Not Used							
X49	R/W	Not Used						TOBIT2	TOBIT1

PER CHANNEL RECEIVE POH BYTES, TUG-3 H1/H2 BYTES AND O-BIT REGISTERS

Where X=1, 2, or 3, which corresponds to the selected channel:

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X50 to X8F	R/W	Receive J1 Byte (64 bytes)							
X90	R/W	Receive B3 Byte							
X91	R/W	Receive C2 Byte							
X92	R/W	Receive G1 Byte							
X93	R/W	Receive F2 Byte							
X94	R/W	Receive H4 Byte							
X95	R/W	Receive F3 Byte							
X96	R/W	Receive K3 Byte							
X97	R/W	Receive N1 Byte							
X98	R/W	Receive TUG-3 H1 Byte							
X99	R/W	Receive TUG-3 H2 Byte							
X9A	R/W	Not Used						ROBIT2	ROBIT1

PER CHANNEL PERFORMANCE COUNTERS AND FIFO LEAK RATE REGISTERS

Where X=1, 2, or 3, which corresponds to the selected channel:

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XA0	R	Receive SDH/SONET Frame Counter (8 bits)							
XA1	R	Reserved							
XA2	R/W	FIFO Leak Rate Register (8 bits)							
XA3	R	Positive Justification (Increment) Counter (8 bits)							
XA4	R	Negative Justification (Decrement) Counter (8 bits							
XA5	R	NDF Counter (8 bits)							
XA6	R	TUG-3 Positive Justification (Increment) Counter (8 bits)							
XA7	R	TUG-3 Negative Justification (Decrement) Counter (8 bits)							
XA8	R	TUG-3 NDF Counter (8 bits)							
XA9	R	B3 Block Error Counter (8 bits)							
XAA	R	REI Counter (Low Order Byte)							
XAB	R	REI Counter (High Order Byte)							
XAC	R	B3 Parity Error Counter (Low Order Byte)							
XAD	R	B3 Parity Error Counter (High Order Byte)							
XAE	R	Coding Violations/PRBS Error Counter (Low Order Byte)							
XAF	R	Coding Violations/PRBS Error Counter (High Order Byte)							
XFF	R	Common High Order Byte Counter Snapshot (REI, B3, Coding Violations)							

MEMORY MAP BIT DESCRIPTIONS

Please note that all bits in used registers that are shown as Reserved or Not Used should be set to zero when the register is written, unless otherwise indicated. If the register has not been written, or cannot be written, then the values read from such bits may be arbitrary.

COMMON CONTROL BIT DESCRIPTIONS

Address	Bit	Symbol	Description
0C0	7-0		**Reserved**
0C1	7-0		**Reserved**
0C2	7-4		**Reserved:** Must be set to zero when register is written.
	3	INTZN	**Device Interrupt High Impedance (High-Z) Off State Disable:** This bit works in conjunction with bit INTEN (bit 2) to control the operation of the interrupt output lead INT/IRQ (lead AB8), as described in the table below. A 1 sets the INT/IRQ lead for normal operation if bit INTEN is 1. The lead will be either high when active with the off state low (Intel mode, INT), or low when active with the off state high (Motorola mode, IRQ). A 0 enables the off state to be high impedance instead, for both modes. INTZN / INTEN / Interrupt Lead Action X / 0 / Held in the high impedance state 0 / 1 / Interrupt lead enabled. Held to the high impedance state in the off state, when no interrupts have occurred. 1 / 1 / Normal operation. Driven to high or low in both active and off states, as defined in the lead description.
	2	INTEN	**Device Interrupt Enable:** This bit works in conjunction with bit INTZN (bit 3) as described in the table above.
	1	ADDEN	**Device Add Bus Enable:** A 1 enables the following Add bus output signals for a channel if the per channel control bit ADBEN is also a 1: - AD(7-0) data leads - ADD add indication lead - APAR parity lead. A 0 forces these leads to a high impedance state, or to the off state, regardless of the state of ADBEN. A hardware or software reset forces this bit to the 0 state.
	0	L3EN	**Device Receive Output and Monitor Signals Enable:** A 1 enables the following receive output and monitor signals for a channel if the per channel control bit L3OEN is also a 1: - RCLKn (Receive Clock) - RPOSn (Receive Positive Rail/NRZ) - RNEGn (Receive Negative Rail) - RnNRD (Transmit Monitor NRZ Data) - RnNRC (Transmit Monitor NRZ Clock) A 0 forces these signals to a high impedance state, regardless of the state of L3OEN. A hardware or software reset forces this bit to the 0 state.
0C3	7-0		**Reserved**
0C4	7-0		**Reserved**

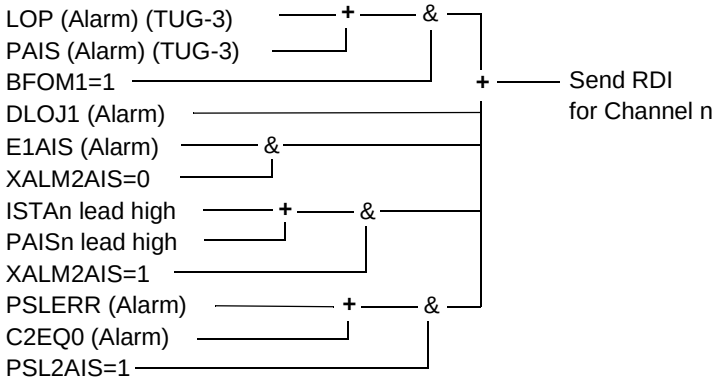
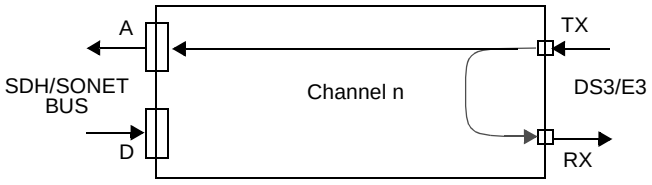
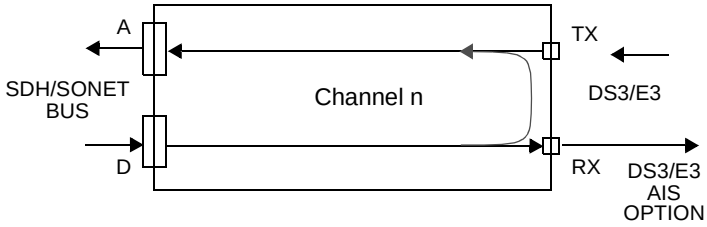
Address	Bit	Symbol	Description
0C5	7-3		**Reserved:** Must be set to zero when register is written.
	2 1	TSTCH1 TSTCH0	**TranSwitch Test Control Bits:** These bits are used for selecting test conditions for each of the three channels. These bits must be set to 00 for normal operation.
	0	LLBAIS	**Line Loopback Receive AIS Output Enable:** This bit works in conjunction with the line loopback control bit (L3LBK, Address XC1H, Bit 1) according to the following table. LLBAIS / L3LBK / Action X / 0 / Normal channel operation 0 / 1 / Line loopback for channel n; output data is the received data 1 / 1 / Line loopback for channel n; output data is a DS3 or E3 AIS signal.
0C6	7-0		**Reserved**
0C7	7-4		**Reserved:** Must be set to zero when register is written.
	3 2 1	RESET3 RESET2 RESET1	**Reset Channel n:** When set to 1, these bits are equivalent to applying a hardware reset to each of the three channels. These bits are not self clearing and must be written with a 0 to resume normal operation.
	0	RESETS	**Device Reset:** When set to 1, this reset bit performs the same functions as the hardware reset lead ($\overline{\text{RESET}}$). This bit is self clearing and will return to 0 after the reset is complete.

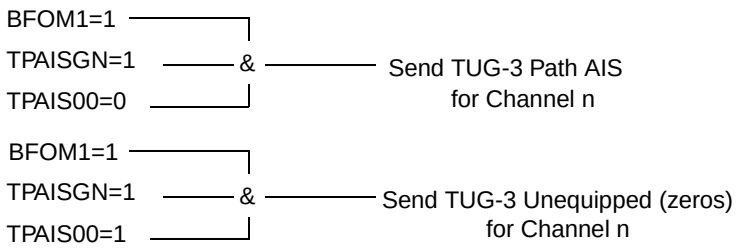
PER CHANNEL CONTROL BIT DESCRIPTIONS

Note: Registers XC0-XCA are set to FFH in the event of a hardware or software reset. The X in the Register addresses, where X = 1, 2, or 3, corresponds to the selected channel:

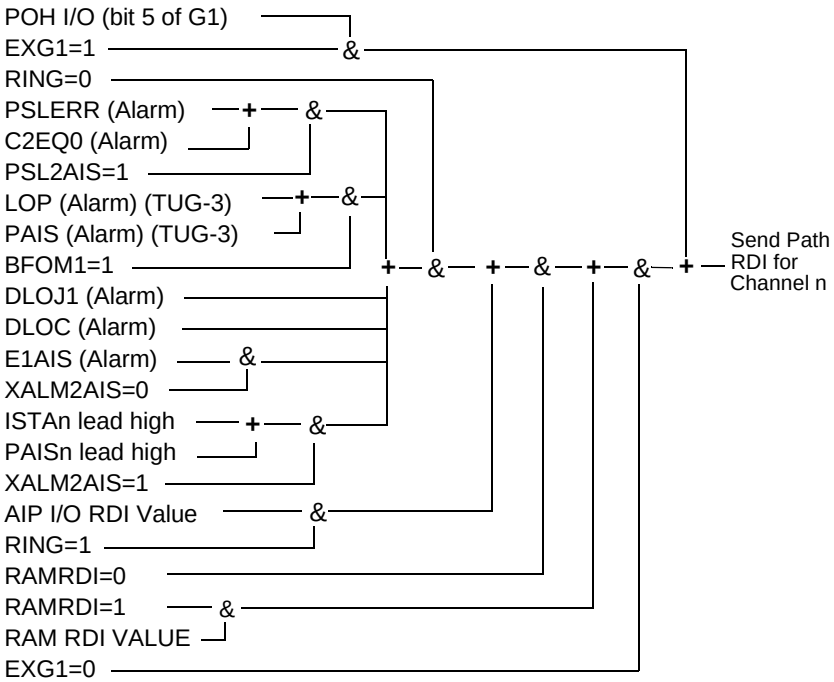
Address	Bit	Symbol	Description
XC0	7 6	BFOM1 BFOM0	**SDH/SONET Bus Operating Format Control Bits:** These bits determine the bus operating format according to the table given below: The SDH/SONET bus operating format control bits must be set to the same value for all three channels. BFOM1 BFOM0 Mapping Format 0 0 Future Use 0 1 STS-3 1 0 Future Use 1 1 STM-1 TUG-3
XC0 (cont.)	5 4	DPOS1 DPOS0	**Dropped TUG-3/STS-1 Selection:** These bits determine which TUG-3 or STS-1 is to be dropped to the channel from the STM-1 or STS-3 according to the table given below. The same TUG-3 or STS-1 may be dropped to one or more channels depending upon the application. Unused channels should be assigned a TUG-3 and, if desired, the Receive Output Enable bit (Bit 0 of Address XC2H, L3OEN) can be set to 0 (High-Z). DPOS1 DPOS0 Mapping 0 0 TUG-3 position A (or STS-1 #1) 0 1 TUG-3 position B (or STS-1 #2) 1 0 TUG-3 position C (or STS-1 #3) 1 1 Do not use
	3 2	APOS1 APOS0	**Add TUG-3/STS-1 Selection:** These bits determine which TUG-3 or STS-1 SPE is to be added from the channel to the STM-1 or STS-3, according to the table given below: Each channel must have a different TUG-3 or STS-1 selection to prevent bus contention. If more than one channel is assigned to the same TUG-3 or STS-1, a common bus contention alarm (ADBCN) will occur. Unused channels should be added to an unassigned TUG-3 position and the Add Bus Enable bit (Bit 1 of Address XC2H, ADBEN) should be set to 0 (High-Z). APOS1 APOS0 Mapping 0 0 TUG-3 position A (or STS-1 #1) 0 1 TUG-3 position B (or STS-1 #2) 1 0 TUG-3 position C (or STS-1 #3) 1 1 Do not use
	1		**Reserved:** Must be set to zero when register is written.
	0	DS3	**DS3 Mode:** Determines the line to SDH/SONET mapping mode according to the table given below: DS3 Mapping Mode 0 E3 (34.368 Mbit/s) 1 DS3 (44.736 Mbit/s)

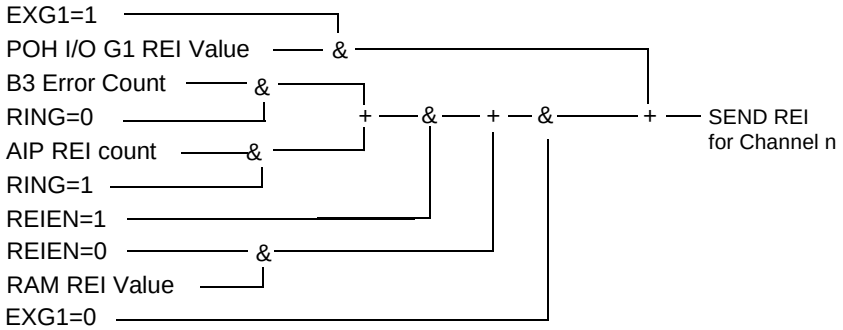
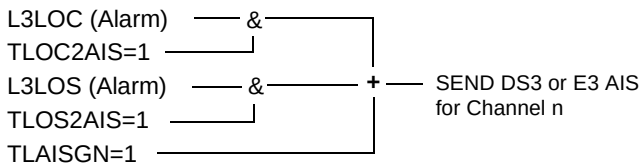
Address	Bit	Symbol	Description
XC1	7	DECODE	**Transmit Line Decoder Enabled:** A 1 enables the transmit HDB3/ B3ZS decoder (for rail operation). A 0 disables the decoder (for NRZ operation). This control bit also selects the transmit line interface to be either positive/ negative rail (decoder enabled) or NRZ.
	6	CODE	**Receive Line Coder Enabled:** A 1 enables the receive HDB3/B3ZS coder (for positive/negative rail operation). A 0 disables the coder (for NRZ operation). This control bit also selects the receive line interface to be either positive/negative rail (coder enabled) or NRZ.
	5	INVCI	**Transmit Invert Line Clock Input:** When set to 0, the DS3 or E3 line signals for the positive/negative rail or NRZ interface are clocked in on rising edges of the line clock (TCLKn). A 1 enables the line signals to be clocked in on falling edges of the clock. This bit has no effect in facility loopback.
	4	INVCO	**Receive Invert Line Clock Output:** When set to 0, the DS3 or E3 line signals for the positive/negative rail or NRZ interface are clocked out on falling edges of the clock (RCLKn). A 1 enables the line signals to be clocked out on rising edges of the clock.

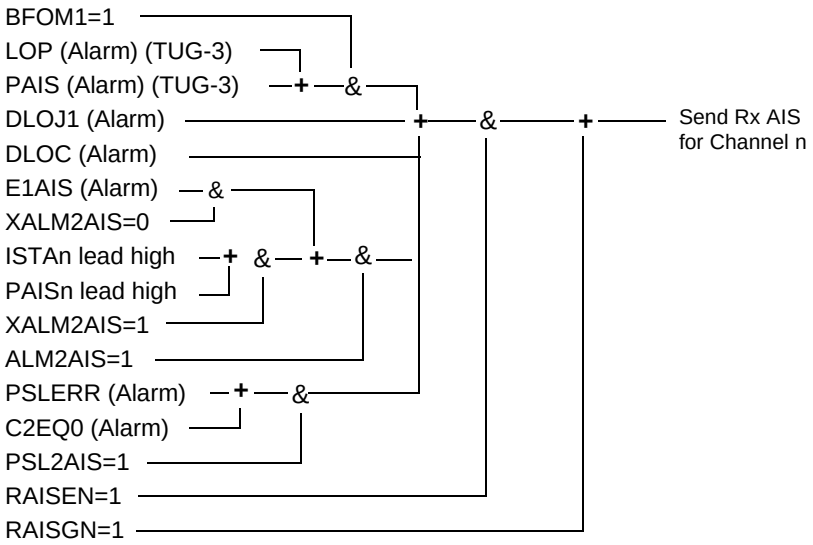
Address	Bit	Symbol	Description
XC1 (cont.)	3	RING	**Ring Operating Mode:** A 1 enables the alarm indication port REI count and RDI indication to be transmitted in the G1 byte. A 0 enables the local RDI generation or path overhead byte interface to control the transmitted RDI state. The alarm conditions that may cause RDI are shown below. The + symbol represents an OR function, while & represents an AND function. Control bit states are given by the = sign. 
	2	FLBK	**Facility Loopback:** A 1 enables the transmit line data and clock input signals to be looped back internally as the receive line data and clock output signals, as illustrated below. The signals from the Drop bus are disabled. 
	1	L3LBK	**DS3/E3 Line Loopback:** A 1 enables the receive line data and clock output signals to be looped back internally as the transmit line data and clock input signals, as illustrated below. The transmit line input signals are disabled. The receive data and clock are provided at the receive line interface. Please note that when control bit LLBAIS (bit 0 in 0C5H) is a 1, DS3 or E3 AIS is sent downstream instead of the received data. 
	0		**Reserved:** Must be set to zero when register is written.

Address	Bit	Symbol	Description
XC2	7	ALM2AIS	**External Alarm Enable AIS:** A 1 enables an AIS detected in the SDH/ SONET E1 byte (when control bit XALM2AIS = 0) or a high on either the ISTAn or PAISn leads (when control bit XALM2AIS = 1) to generate DS3 or E3 line AIS in the receive direction when control bit RAISEN is a 1. See logic diagram for Address XC5H, bit 2.
	6		**Reserved:** Must be set to zero when register is written.
	5	TLAISGN	**Transmit Line AIS:** A 1 written into this position generates and transmits a DS3 or E3 AIS towards the SDH/SONET Add bus, independent of the state of control bit FLBK (bit 2 in register XC1H). DS3 AIS is defined as a valid M-frame with proper subframe structure. The data payload is a 1010... sequence starting with a 1 after each overhead bit. Overhead bits are as follows: F0=0, F1=1, M0=0, M1=1; C-bits are set to 0; X-bits are set to 1; and P-bits are set for valid parity. E3 AIS is defined as an all ones pattern.
	4	TPAISGN	**Transmit TUG-3 Zeros or Path AIS Enable:** A 1 enables TUG-3 unequipped channel generation (SPE with zeros and valid pointer), or a TUG-3 path AIS, towards the SDH/SONET bus, depending on the state of control bit TPAIS00. The logic diagrams for sending TUG-3 path AIS and unequipped are shown below. The + symbol represents an OR function, while & represents an AND function. Control bit states are given by the = sign. 
	3	TPAIS00	**Transmit TUG-3 SPE with Zeros:** When enabled by writing a 1 to control bit TPAISGN, a 1 written into this location causes the TUG-3 (POH bytes and payload) to be transmitted with zeros, but with a valid pointer. A 0 causes a TUG-3 path AIS to be transmitted towards the SDH/SONET bus.
	2		**Reserved:** Must be set to zero when register is written.
	1	ADBEN	**Add Bus Enable:** A 0 forces the Add bus data (AD(7-0)) and Add Parity (APAR) leads to a high impedance state, and ADD high. A 1 enables the Add bus for that channel selection. This bit works in conjunction with bit 1 of Address 0C2H, ADDEN. ADDEN ADBEN 0 0 Add bus high-Z 0 1 Add bus high-Z 1 0 Per channel high-Z 1 1 Add bus enabled Please note: This control bit is forced to 0 on a hardware reset or software reset.

Address	Bit	Symbol	Description
XC2 (cont.)	0	L3OEN	**Receive Output Enable:** A 0 forces the receive interface clock (RCLKn) and data signals (RPOSn and RNEGn), and NRZ outputs (RnNRC and RnNRD) for channel n to a high impedance state. A 1 enables the receive output leads. This bit works in conjunction with bit L3EN (0C2H, bit 0). L3EN L3OEN 0 0 All receive channels high-Z 0 1 All receive channels high-Z 1 0 Per channel high-Z 1 1 Receive outputs enabled Please note: This control bit is forced to 0 on a hardware reset or software reset.
XC3	7	EXN1	**Transmit External Interface N1 byte:** A 1 enables the N1 byte from the POH input/output interface to be transmitted. A 0 enables the corresponding RAM location to be transmitted.
	6	EXK3	**Transmit External Interface K3 byte:** A 1 enables the K3 byte from the POH input/output interface to be transmitted. A 0 enables the corresponding RAM location to be transmitted.
	5	EXF3	**Transmit External Interface F3 byte:** A 1 enables the F3 byte from the POH input/output interface to be transmitted. A 0 enables the corresponding RAM location to be transmitted.
	4	EXH4	**Transmit External Interface H4 byte:** A 1 enables the H4 byte from the POH input/output interface to be transmitted. A 0 enables the corresponding RAM location to be transmitted.
	3	EXF2	**Transmit External Interface F2 byte:** A 1 enables the F2 byte from the POH input/output interface to be transmitted. A 0 enables the corresponding RAM location to be transmitted.
	2	EXG1	**Transmit External Interface G1 Byte:** A 1 enables the G1 byte from the POH input/output interface to be transmitted. A 0 enables the corresponding RAM location or internal logic/alarms to control the transmitted state of REI (FEBE), RDI, and the unassigned bits.
	1	EXC2	**Transmit External Interface C2 Byte:** A 1 enables the C2 byte from the POH input/output interface to be transmitted. A 0 enables the corresponding RAM location to be transmitted.
	0	EXJ1	**Transmit External Interface J1 Bytes:** A 1 enables the J1 bytes from the POH input/output interface to be transmitted. A 0 enables the corresponding RAM segment (64 locations) to be transmitted.

Address	Bit	Symbol	Description
XC4	7	EXOO	**External O-Bit Select:** A 1 selects the two Overhead Communication Bits (O-bits) from the external interface (lead TnOCD) as the two O-bits transmitted in each of the nine subframes of the DS3 format or TranSwitch designated reserved bits in each of the three subframes of the E3 format. A 0 enables the two O-bits from the corresponding RAM location to be transmitted (TOBIT2, TOBIT1 at Address X49H).
	6		**Reserved:** Must be set to zero when register is written.
	5	RAMRDI	**Remote Defect Indication Enabled:** Enable bit for controlling the generation of Path RDI (bit 5 in G1 byte). When control bits RING and EXG1 are 0, and RAMRDI is a 0, RDI is generated when the following alarms or conditions occur: - Drop bus loss of J1 (DLOJ1) - Drop bus loss of clock (DLOC) - Loss of pointer (LOP) (TUG-3 operation) - Path AIS detected (PAIS) (TUG-3 operation) - Received E1 byte has a majority of 1s and control bit XALM2AIS is 0 - Either the ISTAn or PAISn input lead is high and control bit XALM2AIS is a 1 - PSLERR or C2EQ0 alarm, and control bit PSL2AIS is a 1 When control bit RING is a 1, EXG1 is a 0, and RAMRDI is a 0, the RDI state is controlled via the Alarm Indication Port. The microprocessor controls the RDI state when RAMRDI is a 1 and EXG1 is a 0. Note: writing a 1 to the RAMRDI bit will disable the local alarms and the Alarm Indication Port RDI in the ring mode from controlling the state of the transmitted RDI bit. The logic diagram for sending Path RDI is given below. The + symbol represents an OR function, while & represents an AND function. Control bit states are given by the = sign. 

Address	Bit	Symbol	Description
XC4 (cont.)	4	REIEN	**REI Enable:** A 1 enables the local B3 parity error count or the remote B3 parity error count to be inserted as the REI value. A 0 written into this position permits the microprocessor to control the value of the REI count. The logic diagram for sending REI for all conditions is given below. The + symbol represents an OR function, while & represents an AND function. Control bit states are given by the = sign. 
	3	XALM2AIS	**External Alarm AIS Lead Enable:** A 1 enables the external alarm leads (ISTAn and PAISn) to control alarm generation instead of AIS in the E1 byte. A 0 causes alarm generation to be based on E1AIS from the Drop bus.
	2		**Reserved:** Must be set to zero when register is written.
	1	TLOC2AIS	**Transmit Loss Of Clock (TLCK) AIS Enable:** A 1 enables the channel to send SDH/SONET DS3 AIS or E3 AIS automatically when a transmit line clock failure is detected. The logic diagram for transmitting a line AIS is given below. The + symbol represents an OR function, while & represents an AND function. Control bit states are given by the = sign. 
	0	TLOS2AIS	**Transmit Loss Of Signal (TPOSn/TNEGn) AIS Enable:** A 1 enables the channel to send DS3 or E3 AIS automatically when a transmit line signal failure is detected, as shown in the logic diagram above.
XC5	7	COR	**Clear On Read:** A 0 enables all performance counters for that channel to become non- saturating with roll over capability. The contents of the counter are not affected by a read cycle. A 1 causes the performance counters to become saturating counters, which clear on a read cycle.
	6 - 5		**Reserved:** Must be set to zero when register is written.

Address	Bit	Symbol	Description
XC5 (cont.)	4	POH2RAM	**Path Overhead Bytes to RAM:** This bit works in conjunction with the EXnn control bits that select POH bytes (e.g., EXF2). The following table summarizes the action taken by this bit and an EXnn bit: POH2RAM / EXnn (reg. XC3H) / Action 1 / 1 / POH interface byte transmitted and written to RAM location for the selected overhead byte. 0 / 1 / POH interface byte transmitted for the selected byte; the RAM location holds a microprocessor-written overhead byte value. X / 0 / The POH byte written to RAM by the microprocessor is transmitted.
	3	RAISGN	**Generate Receive Line AIS:** A 1 written into this position generates a DS3/E3 AIS towards the line (RPOSn, RNEGn) independent of the state of the receive AIS enable bit (RAISEN).
	2	RAISEN	**Receive AIS Enable:** A 1 enables receive E3 or DS3 Line AIS to be generated when the following alarms/conditions occur: - Loss of Drop bus clock alarm (DLOC) - Loss of Drop bus J1 alarm (DLOJ1) - E1 AIS alarm (E1AIS) and XALM2AIS is 0, and ALM2AIS is a 1 - ISTAn or PAISn lead high and XALM2 is 1, and ALM2AIS is a 1 - Loss of pointer (LOP) (TUG-3) - Path AIS (PAIS) (TUG-3) - PSLERR or C2EQ0 occurs, and Path Signal Label Error Enable AIS control bit (PSL2AIS) is a 1 The logic diagram for generating receive line AIS is given below. The + symbol represents an OR function, while & represents an AND function. Control bit states are given by the = sign. 

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>XC5 (cont.)</td><td>1</td><td>WGDEC</td><td>Test Equipment BPV Selection: A 1 enables the decoder to detect coding violations as found in ‘Type 1’ test equipment. A 0 enables the decoder to detect coding violations as found in ‘Type 0’ test equipment. The following tables summarize the two decoding procedures for coding violations:
BPV For B3ZS
<table>
<tr><th>BPV</th><th>"Type 1” Equipment</th><th>“Type 0” Equipment</th></tr>
<tr><td>++ or --</td><td>000 (preceding bit(s) changed)</td><td>11</td></tr>
<tr><td>0BV or 000V</td><td>0000</td><td>011 or 0001</td></tr>
<tr><td>BB0V after odd</td><td>1000</td><td>1101</td></tr>
<tr><td>B00V after even</td><td>1000</td><td>1001</td></tr>
</table>
BPV For HDB3
<table>
<tr><th>BPV</th><th>"Type 1” Equipment</th><th>“Type 0” Equipment</th></tr>
<tr><td>++ or --</td><td>0000 (preceding bit(s) changed)</td><td>11</td></tr>
<tr><td>0BV or 0000V</td><td>00000</td><td>011 or 00001</td></tr>
<tr><td>BB00V after odd</td><td>10000</td><td>11001</td></tr>
<tr><td>B000V after even</td><td>10000</td><td>10001</td></tr>
</table></td></tr>
<tr><td></td><td>0</td><td>PSL2AIS</td><td>Path Signal Label Error Enable AIS: A 1 enables the channel to send DS3 or E3 line AIS automatically towards the receive line, and path RDI when a PSLERR or C2EQ0 alarm occurs. (See RAMRDI and RAISEN for logic diagrams).</td></tr>
<tr><td>XC6</td><td>7-5</td><td></td><td>Reserved: Must be set to zero when register is written.</td></tr>
<tr><td></td><td>4</td><td>PAT23</td><td>2^{23}-1 Test Pattern Enable: A 0 selects the two PRBS test pattern generators’ and the test pattern analyzer’s pattern to be 2^{15}-1. A 1 selects the pattern generators’ and analyzer’s pattern to be 2^{23}-1.</td></tr>
<tr><td></td><td>3</td><td>ENANA</td><td>Enable Analyzer: A 1 enables the 2^{15}-1 or 2^{23}-1 analyzer. PRBS errors are counted in a 16-bit counter in locations XAEH and XAFH.</td></tr>
<tr><td></td><td>2</td><td>TXANA</td><td>Transmit Analyzer Enable: A 1 connects the analyzer to the transmit NRZ line (DS3/E3) signal after the line decoder. A 0 connects the analyzer to the receive NRZ line data prior to the line coder function. A 1 must be written to control bit ENANA (bit 3) for this bit to function (see Figure 36).</td></tr>
<tr><td></td><td>1</td><td>TPRBS</td><td>Transmit Test Pattern Generator Enable: A 1 enables the transmit test pattern generator and disables the NRZ line decoder output.</td></tr>
<tr><td></td><td>0</td><td>RPRBS</td><td>Receive Test Pattern Generator Enable: A 1 enables the receive test pattern generator and disables the NRZ line coder input from the desynchronizer.</td></tr>
<tr><td>XC7</td><td>7</td><td>TESTB3</td><td>Test B3 Byte: A 1 transmits a B3 value written by the microprocessor in location X40H. A 0 enables the test byte to become a test mask. When configured as a test mask, a 1 in one or more bit positions causes those bits in the transmitted B3 byte to be inverted from their calculated values.</td></tr>
</table>

Address	Bit	Symbol	Description
XC7 (cont.)	6	FIXPTR	**TUG-3 Fixed Pointer Generation:** A 1 forces a fixed pointer of 0 to be generated in the transmitted TUG-3 regardless of any pointer movements (J1 in DC1J1) that may occur on the Drop side when the Drop timing mode is selected, or if a pointer movement (J1 in AC1J1) takes place when Add bus timing is selected. When this bit is written with a 0, a pointer movement on the Add or Drop bus is compensated with an outgoing TUG-3 pointer movement in the opposite direction.
	5-3		**Reserved:** Must be set to zero when register is written.
	2	TXRST	**Transmit Reset:** A 1 written into this position resets the transmit section (Line to SDH/SONET) of the channel. This includes the transmit FIFOs and internal counters. The channel's transmitter will remain reset until the microprocessor writes a 0 into this location.
	1	RXRST	**Receive Reset:** A 1 written into this position resets the receive section (SDH/SONET to Line) of the TL3M device channel. This includes the receive FIFOs and internal counters. The channel's receiver will remain reset until the microprocessor writes a 0 into this location.
	0	RESETC	**Reset Performance Counters:** A 1 written into this position resets the performance counters to 0 for this channel. This bit is self clearing, and does not require the microprocessor to write a 0 into this location.
XC8	7-0	C2 Compare	**Path Signal Label Compare:** The bits in this location are compared against the C2 byte received (register X91H) for a signal label mismatch. The relationship between the bits of this microprocessor-written byte and the received C2 byte is shown below: Rx C2 Byte: 1 2 3 4 5 6 7 8 C2 Compare: 7 6 5 4 3 2 1 0
XC9	7-2		**Reserved:** Must be set to zero when register is written.
	1	RDI5	**RDI 5 Consecutive Enable:** A 1 enables the detection/recovery algorithms of RDI (bit 5 in the G1 byte) to activate on 5 consecutive matches/mismatches. A 0 enables the detection/recovery of RDI to activate on 10 consecutive matches/mismatches.
	0	REIBLK	**REI (FEBE) Counter Block Count Enable:** A 1 configures the REI (FEBE) counter (register locations XAAH and XABH) to count one or more REI errors per received G1 byte as one error (block). A 0 configures the REI counter to count the number of individual errors detected (1 to 8).
XCA	7-6		**Reserved:** Must be set to zero when register is written.
	5	NOPOH	**No Path Overhead Bytes:** When this bit is set to 1, the VC-4 path overhead time slots of the Add bus data signals AD(7-0) are set to a high impedance and the ADD signal is high during these time slots. When this bit is set to 0 the AD(7-0) byte values are set to 00H and the ADD signal is forced low during the time slots that correspond to the POH bytes.
	4-0		**Reserved:** Must be set to zero when register is written.

COMMON STATUS BIT DESCRIPTIONS

Status bits report the condition of alarms as both current status (unlatched) and event record (latched) bit positions. The unlatched bit goes to 1 for only as long as the alarm persists, while a latched bit is set to 1 upon the first occurrence of the alarm and it remains active until its register is read, when it is reset to 0. Only latched bits that are read as 1 are reset, to preserve alarms which occur during the read operation. If a current alarm is present after this reset, the corresponding latched bit will be set to 1 again. The unlatched bits occupy even-numbered registers. Their corresponding latched bits are in the same bit positions of the following odd-numbered register. Latched bits activate an interrupt while set to 1, unless their mask bit is set to 0.

Address	Bit	Symbol	Description
0B0	7-3		**Reserved**
	2 1 0	INT3 INT2 INT1	**Interrupt Indication (INTn) for Channel n:** A 1 indicates that channel n has at least one latched alarm set to 1 that is not masked from causing an interrupt. This bit provides information that enables the microprocessor to read the status bits associated with that channel and determine which alarms have occurred.
0B1	7-0		This register contains latched bits that correspond to the unlatched bits in register 0B0H. These latched bits are reset to 0 when they are read.
0B6	7	ADBCN	**Add Bus Contention Indication:** A 1 indicates that more than one channel is attempting to drive the Add bus at the same time. This is usually due to the fact that more than one channel has been assigned to the same TUG-3 or STS-1 in the add direction.
	6-0		**Reserved**
0B7	7-0		This register contains latched bits that correspond to the unlatched bits in register 0B6H. These latched bits are reset to 0 when they are read.

PER CHANNEL STATUS BIT DESCRIPTIONS

The per channel status bits perform in the same way as described above for common status bits.

Where X=1, 2, or 3, which corresponds to the selected channel:

Address	Bit	Symbol	Description
XB0	7	DLOC	**Drop Bus Loss Of Clock Alarm:** An unlatched loss of clock alarm occurs when the input Telecom Bus Drop bus clock has been stuck high or low for approximately 225 ns. Recovery occurs within 100 ns of the first bus clock transition. ACLK (lead P1), when ABTIM (lead B21) is asserted or DCLK (lead K3), when ABTIM is unasserted, must be present for this alarm to function.
	6	DLOJ1	**Drop Bus Loss of J1:** An unlatched Drop bus loss of J1 alarm occurs when: - 8 consecutive new J1 positions have been detected or - J1 is stuck low for 8 consecutive frames or - J1 is stuck high for 8 consecutive bytes or - 8 J1 pulses are received in one frame. Recovery occurs when the J1 pulse is detected in the same location for 8 consecutive frames.

Address	Bit	Symbol	Description
XB0 (cont.)	5	BUSERR	**Bus Parity Error:** This unlatched alarm indicates that a parity error has been detected on the Drop bus. Odd parity is calculated over the DD(7-0), DSPE, DC1J1, and DC1 leads. Other than providing this alarm, no action is taken by the channel or device.
	4	E1AIS	**E1 Byte AIS Detected:** The E1 byte in the VC-4 and the E1 byte plus the adjoining bytes may be used to carry an upstream in-band SDH/SONET line and path AIS indication. This unlatched alarm indicates that AIS has been detected in the E1 byte corresponding to AU-3/STS-3 STS-1. Please note: For TUG-3 operation, the first E1 byte in the VC-4 is monitored. The alarm occurs when 5 out of 8 ones are detected once. Recovery occurs when fewer than 5 out of 8 bits are equal to 1 once.
	3	LOP	**TUG-3 Loss Of Pointer Alarm:** An unlatched TUG-3 loss of pointer alarm occurs when a New Data Flag (NDF) or an invalid pointer is detected for eight consecutive frames. Recovery occurs when a valid pointer is received for three consecutive frames.
	2	PAIS	**TUG-3 Path AIS Alarm:** An unlatched TUG-3 Path Alarm Indication Signal (PAIS) is activated when all ones are detected in the 16-bit pointer word (H1 and H2) for three consecutive frames. Recovery occurs when a valid NDF is received, or a valid pointer is detected, for three consecutive frames.
	1	PSLERR	**Path Signal Label Error:** This unlatched alarm indicates that the comparison between the received C2 byte and the microprocessor-written C2 byte did not match for 5 consecutive times. Recovery to 0 occurs when the comparison matches five times consecutively.
	0	C2EQ0	**Unequipped Alarm:** This unlatched unequipped alarm is detected when the C2 byte is equal to 00H 5 consecutive times. Recovery occurs when the C2 byte is not equal to 00H five consecutive times.
XB1	7-0		This register contains latched bits that correspond to the unlatched bits in register XB0H. These latched bits are reset to 0 when they are read.
XB2	7	RDI	**Receive RDI Alarm:** When RDI5 is set to 0, an unlatched RDI alarm occurs when bit 5 in the G1 byte is equal to 1 for 10 consecutive frames. Recovery occurs when a 0 has been detected for 10 consecutive frames. When RDI5 is a 1, detection and recovery of the alarm is set to 5 consecutive events instead of 10.
	6	L3LOS	**Transmit Line Loss Of Signal:** For an E3 signal, an unlatched line loss of signal alarm occurs when either the positive or negative rail is stuck low for 256 bit times. Recovery occurs when there are at least 32 transitions (on both positive and negative rails) in a count of 256 clock cycles. For a DS3 signal, a loss of signal alarm occurs when either the positive or negative rail is stuck low for 200 bit times. Recovery occurs on the first line signal transition (both positive and negative rails). When the interface is configured for NRZ operation, an active high on the TNEGn/LOSn lead can be used to provide an external loss of signal indication. Detection and recovery are immediate, following the LOSn transitions.
	5	L3LOC	**Transmit Line Loss of Clock:** This unlatched alarm indicates the incoming line clock (TCLKn) signal has been stuck high or low for approximately 225 ns. Recovery occurs within 100 ns of the first line clock transition. ACLK (lead P1), when ABTIM (lead B21) is asserted or DCLK (lead K3), when ABTIM is unasserted, must be present for this alarm to function.

Address	Bit	Symbol	Description
XB2 (cont.)	4	TOVFL	**Transmit FIFO Overflow/Underflow:** This unlatched alarm indicates that the transmit FIFO has either underflowed or overflowed. The FIFO automatically resets to a preset value on the occurrence of the alarm.
	3	L3AIS	**Transmit Line E3 AIS Detected:** For an E3 signal, this unlatched AIS alarm is detected when four or fewer zeros are detected in 1536 bits, twice in a row. Recovery occurs when there are five or more zeros detected in 1536 bits two consecutive times. Please note: DS3 AIS detection is not supported.
	2	RAMLOC	**RAM Loss Of Clock Detected:** The RAM clock input (RAMCI) is monitored for a stuck high or low state using the internal PLL clock to activate this unlatched alarm when the input has been stuck for approximately 225 ns. Recovery occurs within 100 ns of the first RAM clock transition. ACLK (lead P1), when ABTIM (lead B21) is asserted or DCLK (lead K3), when ABTIM is unasserted, must be present for this alarm to function.
	1	ALOC	**Add Bus Loss Of Clock:** This unlatched alarm is enabled when the Add bus timing is selected (lead ABTIM is high). An Add bus loss of clock alarm occurs when the input add clock (ACLK) is stuck high or low for approximately 225 ns. Recovery occurs within 100 ns of the first bus clock transition. ACLK (lead P1), when ABTIM (lead B21) is asserted or DCLK (lead K3), when ABTIM is unasserted, must be present for this alarm to function.
	0	ALOJ1	**Add Bus Loss of J1:** This unlatched alarm is enabled when the Add bus timing is selected (lead ABTIM is high). An Add bus loss of J1 alarm occurs when: - 8 consecutive new J1 positions have been detected or - J1 is stuck low for 8 consecutive frames or - J1 is stuck high for 8 consecutive bytes or - 8 J1 pulses are received in one frame. Recovery occurs when the J1 pulse is detected in the same location for 8 consecutive frames.
XB3	7-0		This register contains latched bits that correspond to the unlatched bits in register XB2H. These latched bits are reset to 0 when they are read.
XB4	7	SINT	**Software Interrupt:** This unlatched software interrupt indication occurs when one or more bit locations in the interrupt mask locations has been set to 1, and a corresponding latched alarm becomes active. The SINT state is exited when the last latched alarm causing the interrupt is cleared (i.e., when its register is read) or the corresponding bit in the interrupt mask is turned off.
	6		**Reserved**
	5	J1NEW	**J1 New Alarm:** An unlatched indication that a new J1 location, other than those resulting from pointer movements, has been detected in the VC-4 or STS-3 STS-1.
	4	TUG3NEW	**TUG-3 New Alarm:** An unlatched TUG-3 new indication occurs when three consecutive new pointers, or an NDF and a match of the SS bits while the pointer offset value is in range, have been detected.
	3	ROVFL	**Receive FIFO Overflow/Underflow:** This unlatched alarm indicates the pointer leak FIFO has underflowed or overflowed. When this occurs, the FIFO will automatically reset to a preset position and the FIFO Reset Indication output lead (DFnE) will pulse high.

Address	Bit	Symbol	Description
XB4 (cont.)	2	AISLOC	**AIS Loss Of Clock Detected:** The AIS selected (DS3 or E3) is monitored for a stuck high or stuck low condition, An unlatched AIS LOC indication occurs when the EAIS or DAIS clock is stuck high or low for approximately 225 ns. Recovery occurs within 100 ns of the first EAIS or DAIS clock cycle transition. ACLK (lead P1), when ABTIM (lead B21) is asserted or DCLK (lead K3), when ABTIM is unasserted, must be present for this alarm to function.
	1	XISTAT	**External STS-1 Alarm:** This unlatched alarm indicates that the input on the lead labeled ISTAn is high. It may be used to indicate an external alarm condition (e.g., LOP). Detection and recovery follow ISTAn immediately.
	0	XPAIS	**External Path AIS:** This unlatched alarm indicates that the input on the lead labeled PAISn is high. It may be used to indicate an external alarm condition (e.g., path AIS). Detection and recovery follow PAISn immediately.
XB5	7		**Reserved:** Must be set to zero when register is written.
	6		**Reserved:**
	5-0		This register contains latched bits that correspond to the unlatched bits 5-0 in register XB4H. These latched bits are reset to 0 when they are read.
XB6	7	L3ERR	**Analyzer Error Indication:** This unlatched alarm indicates that the 2^{15}-1 or 2^{23}-1 PRBS test analyzer has detected an error when enabled. A 1 written to ENANA (bit 3, in XC6H) enables the analyzer. When control bit ENANA is a 0, the analyzer and alarm are disabled.
	6	LOVFL	**Receive Leak FIFO Overflow/Underflow Alarm:** This unlatched alarm indicates that the receive FIFO has either underflowed or overflowed. The FIFO automatically resets to a preset value on the occurrence of the alarm.
	5	RFRST	**Receive FIFO Reset Indication:** This unlatched alarm indicates that either the leak FIFO or the receive dejitter FIFO has been reset. This may occur because of a FIFO overflow/underflow alarm, or when the receive section has been reset by writing a 1 to control bit RXRST, or upon hardware reset.
	4	TFRST	**Transmit FIFO Reset Indication:** This unlatched alarm indicates that the transmit FIFO has been reset. This may occur because of a FIFO overflow/ underflow alarm, or when the transmitter has been reset by writing a 1 to control bit TXRST, or upon hardware or software reset.
	3	PLLLOC	**Desynchronizer Phase Lock Loop Loss Of Clock:** This unlatched alarm indicates the internal PLL has experienced loss of clock for approximately 225 ns. Recovery occurs within 100 ns of the first PLL clock transition. ACLK (lead P1), when ABTIM (lead B21) is asserted or DCLK (lead K3), when ABTIM is unasserted, must be present for this alarm to function.
	2	TPLOC	**Loss of Transmit PLL Clock:** This unlatched alarm indicates that the internal transmit PLL clock has been stuck high or low for approximately 250 ns. Recovery occurs within 100 ns of the first PLL clock transition. DCLK (lead K3) must be present for this alarm to function.
	1	RPLOC	**Loss of Receive PLL Clock:** This unlatched alarm indicates that the internal receive PLL clock has been stuck high or low for approximately 225 ns. Recovery occurs within 100 ns of the first PLL clock transition. ACLK (lead P1), when ABTIM (lead B21) is asserted or DCLK (lead K3), when ABTIM is unasserted, must be present for this alarm to function.
	0	OOL	**Analyzer Out of Lock:** This unlatched alarm indicates that the PRBS test analyzer, when enabled, is out of lock.
XB7	7-0		This register contains latched bits that correspond to the unlatched bits in register XB6H. These latched bits are reset to 0 when they are read.

COMMON INTERRUPT MASK BIT DESCRIPTIONS

A 1 written to any of the bits in these common interrupt mask registers, and a 1 state for the corresponding latched alarm bit of the same channel in registers 0B1H and 0B7H, causes a hardware interrupt to occur on the INT/IRQ output lead if control bit INTEN (bit 2 in register 0C2H) is set to 1.

Address	Bit	Symbol	Description
0BA	7-3		**Reserved**
	2 1 0	INT3 INT2 INT1	**Mask for Interrupt Indication for Channel n:** A 1 written to a bit enables the corresponding latched status alarm INTn in register 0B1H to cause a hardware interrupt.
0BD	7	ADBCN	**Mask for Add Bus Contention:** A 1 written to this location enables the corresponding status alarm ADBCN in register 0B7H to cause a hardware interrupt.
	6-0		**Reserved**

PER CHANNEL INTERRUPT MASK BIT DESCRIPTIONS

A 1 written to any of the bits in these per channel interrupt mask registers (except HINT), and a 1 state for the corresponding latched alarm bit of the same channel in registers XB1H, XB3H, XB5H (Bits 5-0), and XB7H, causes a software interrupt (SINT) to occur for the channel. If the hardware interrupt bit (HINT) is also written with a 1, and if control bit INTEN (bit 2 in 0C2H) is set to 1, a hardware interrupt will also occur on the INT/IRQ output lead.

Where X=1, 2, or 3, which corresponds to the selected channel:

Address	Bit	Symbol	Description
XBA	7	DLOC	Drop Bus Loss Of Clock
	6	DLOJ1	Drop Bus Loss of J1
	5	BUSERR	Bus Parity Error
	4	E1AIS	E1 Byte AIS detected
	3	LOP	Loss Of Pointer (TUG-3 operation)
	2	PAIS	Path AIS (TUG-3 operation)
	1	PSLERR	Path Signal Label Error
	0	C2EQ0	C2 Equal to 0 alarm (unequipped)
XBB	7	RDI	Receive RDI (yellow) detected.
	6	L3LOS	Transmit Line Loss Of Signal
	5	L3LOC	Transmit Line Loss Of Clock
	4	TOVFL	Transmit FIFO Error (underflowed or overflowed)
	3	L3AIS	E3 Transmit Line AIS Detected
	2	RAMLOC	RAM Loss Of Clock
	1	ALOC	Add Bus Loss Of Clock
	0	ALOJ1	Add Bus Loss of J1

Address	Bit	Symbol	Description
XBC	7	HINT	Hardware Interrupt Enable
	6		**Reserved:** Must be set to zero when register is written.
	5	NEW	New Alarm - NDF and 3x new pointer events (TUG-3 operation)
	4	TUG3NEW	TUG-3 New Alarm - Three new pointer events
	3	ROVFL	Receive FIFO Overflow/Underflow
	2	AISLOC	Alarm Indication Signal Loss Of Clock
	1	XISTAT	External STS-1 Alarm (ISTAn) signal detected as a 1 (if enabled)
	0	XPAIS	External Path AIS (PAISn) signal detected as a 1 (if enabled)
XBD	7	L3ERR	Internal PRBS Test Analyzer bit error detected.
	6	LOVFL	Leak FIFO Overflow/Underflow
	5	RFRST	Receive FIFO Reset Indication
	4	TFRST	Transmit FIFO Reset Indication
	3	PLLLOC	Desynchronizer Phase Lock Loop (PLL) Loss Of Clock
	2	TPLOC	Transmit PLL loss of clock
	1	RPLOC	Receive PLL loss of clock
	0	OOL	PRBS Test Analyzer out of lock.

PER CHANNEL TRANSMIT PATH OVERHEAD BYTES AND O-BIT DESCRIPTIONS

The nine Transmit Path Overhead bytes consist of the J1, B3, C2, G1, F2, H4, F3, K3, and N1 bytes. The POH bytes may be individually transmitted from the POH interface, or from RAM locations written by the microprocessor. When control bit POH2RAM is a 1, the POH interface byte selected for transmission is written into the designated RAM location. For example, if EXC2 is set to 1, the transmit POH interface C2 byte is written into the assigned RAM location, in addition to being transmitted. If EXC2 is set to 0, the transmitted byte is the value written into the corresponding RAM location by the microprocessor. When a 0 is written into the POH2RAM control bit, the capability of writing any of the selected POH interface bytes into their RAM locations is disabled. However, individual bytes may still be transmitted from either the POH interface or the microprocessor-written RAM location. This feature permits switching back and forth between a selected POH interface byte or a RAM location for transmission, without having to re-initialize the RAM location. The following table is a summary of this operation:

POH2RAM XC5H, bit 4	EXnn* XC3H, bits 7-0	Action for associated POH byte
1	1	POH interface byte written into RAM, and also transmitted.
0	1	POH interface byte transmitted, but not written into RAM. Microprocessor writes RAM value as required.
X	0	POH RAM value transmitted.

* e.g., nn = C2.

The relationship between a transmitted path overhead byte and the corresponding RAM location is as follows:

Bits in a RAM Location

7	6	5	4	3	2	1	0

Bits of Transmitted POH Byte

1	2	3	4	5	6	7	8

For example, if a 01 hex (0000 0001) is written into a RAM location, a 01 hex (0000 0001), starting with bit 1 (a 0), is transmitted.

The O-bits consist of two overhead communication bits per subframe, for nine subframes, in the DS3 format, or for 3 designated subframes in the E3 format. Please note that the ETSI and ITU standards do not specify an overhead channel in the E3 mapping format. The selection of the two bits per subframe, either from the O-bit interface or from RAM, operates in the same way as the path overhead bytes, but the O-bits from the transmit O-bit port are not written into the designated RAM location.

Where X=1, 2, or 3, which corresponds to the selected channel:

Address	Bit	Symbol	Description
X00 to X3F	7-0	J1	**Transmit Path Trace:** The bytes written into these 64 registers provide a repetitive 64-byte fixed length message for transmission. The bytes written into these positions are either from the microprocessor or from the external POH input/output interface. The starting address is arbitrary.
X40	7-0	B3 Error Mask	**Transmit B3 Error Mask:** When control bit TESTB3 (bit 7 in XC7H) is a 0, the bits in this register that are written with a one represent the columns in the B3 byte in which errors will be generated. The error is created by inverting the calculated B3 bit position. For example, if a 01 hex is written into this register. Bit 8 in the B3 byte will be transmitted inverted. The B3 errors are sent until this register is rewritten with a 00H. When control bit TESTB3 is a 1, the value written into this register location is the transmitted B3 byte.
X41	7-0	C2	**Transmit Path Signal Label (microprocessor-written value):** The bits of the C2 byte that are written into this position indicate the construction of the AU-3, TUG-3, or SPE (e.g., unequipped).

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>X42</td><td>7-0</td><td>G1</td><td>Transmit G1 Byte: This byte is used for sending the microprocessor-controlled states for REI, RDI, and any unassigned bits, according to the states given in the tables below:

TFEBE
<table><tr><th>EXG1</th><th>REIEN</th><th>Action</th></tr><tr><td>0</td><td>0</td><td>Microprocessor-written value sent</td></tr><tr><td>0</td><td>1</td><td>Internal or mate (ring mode) value sent</td></tr><tr><td>1</td><td>X</td><td>External POH I/O interface value sent</td></tr></table>
TRDI
<table><tr><th>EXG1</th><th>RAMRDI</th><th>Action</th></tr><tr><td>0</td><td>0</td><td>Internal or mate (ring mode) value sent</td></tr><tr><td>0</td><td>1</td><td>Microprocessor-written value sent</td></tr><tr><td>1</td><td>X</td><td>External POH I/O interface value sent</td></tr></table>
Unassigned Bits
<table><tr><th>EXG1</th><th>Action</th></tr><tr><td>0</td><td>Microprocessor-written value sent</td></tr><tr><td>1</td><td>External POH I/O interface value sent</td></tr></table></td></tr>
<tr><td>X43</td><td>7-0</td><td>F2</td><td>Transmit F2 (User) Channel: This location contains either a microprocessor-written value or a POH input/output interface value prior to transmission.</td></tr>
<tr><td>X44</td><td>7-0</td><td>H4</td><td>Transmit H4 Byte: This location contains either a microprocessor-written value or a POH input/output interface value prior to transmission. This byte is not used for E3 or DS-3 to SDH/SONET applications and is normally sent with a value equal to 00H.</td></tr>
<tr><td>X45
X46
X47</td><td>7-0
7-0
7-0</td><td>F3
K3
N1</td><td>Transmit F3, K3, and N1 Bytes: These locations contain either a microprocessor-written value or a POH input/output interface value prior to transmission.</td></tr>
<tr><td>X48</td><td>7-0</td><td></td><td>Not Used</td></tr>
<tr><td rowspan="2">X49</td><td>7-2</td><td></td><td>Not Used</td></tr>
<tr><td>1
0</td><td>TOBIT2
TOBIT1</td><td>Transmit O-Bits: These two bits correspond to the two O-bits found in each of the nine subframes in the DS3 format or the TranSwitch designated reserved bits in the three subframes in the E3 format. The O-bits are read once per frame and inserted into each of the subframes.</td></tr>
</table>

PER CHANNEL RECEIVE PATH OVERHEAD BYTES, TUG-3 H1/H2 BYTES AND O-BIT DESCRIPTIONS

The selected TUG-3 or STS-3 STS-1 received path overhead bytes are written into the locations given below, and are also provided at the receive path overhead byte interface for use by external circuitry, as required. The relationship between a received path overhead byte and the corresponding RAM location is as follows:

Bits of RAM Location:

7	6	5	4	3	2	1	0

Bits of Received POH Byte:

1	2	3	4	5	6	7	8

Where X=1, 2, or 3, which corresponds to the selected channel:

Address	Bit	Symbol	Description
X50 to X8F	7-0	J1	**Receive Path Trace:** The received J1 bytes are written into this 64-byte segment in a rotating fashion. There is no specific starting point.
X90	7-0	B3	**Receive Path B3 Byte:** This register provides the received B3 parity byte.
X91	7-0	C2	**Receive Path Signal Label:** These bits indicate the construction of the AU-3, TUG-3, or SPE (e.g., unequipped).
X92	7-0	G1	**Receive G1 Byte:** This location provides the receive status of the REI bits (bits 7-4), Path RDI (bit 3), and any unassigned bits in the G1 byte (bits 2-0). RAM Bit 7 6 5 4 3 2 1 0 Receive G1 Bit 1 2 3 4 5 6 7 8
X93	7-0	F2	**Receive F2 (User) Channel:** This register provides the F2 path overhead byte.
X94	7-0	H4	**Receive H4 Byte:** This byte is not specified for use in this application. It is provided for future use as required.
X95 X96 X97	7-0 7-0 7-0	F3 K3 N1	**Other Receive Path Overhead Bytes:** These registers provide access to the F3, K3, and N1 bytes, as required.
X98 X99	7-0 7-0	H1 H2	**Received TUG-3 H1 and H2 Pointer Bytes:** The contents of the H1 and H2 pointer bytes for a TUG-3 are provided in the following bit order for microprocessor read access. H1 (X98H) H2 (X99H) Bit 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 N N N N S S I D I D I D I D I D
X9A	7-2		**Not Used**
	1 0	ROBIT2 ROBIT1	**Receive O-Bits:** The received states of the two Overhead Communication channel bits found in the nine subframes in the DS3 format or the three TranSwitch-designated subframes in the E3 format. The two bits are updated once a frame from one of the subframes in the frame.

PER CHANNEL PERFORMANCE COUNTERS AND FIFO LEAK RATE REGISTER DESCRIPTIONS

Some performance counters have 8 bits and some have 16 bits. All 16-bit performance counters allow uninterrupted access, without the danger of one byte changing while the other byte is read. To perform a 16-bit read, the low order byte is read first. This causes a snapshot of the simultaneous value of the high order byte of the counter to be transferred to a common high order byte at location FFH. The common high order byte should be read next to complete the count transfer. If another performance counter low order byte is read first, the contents of the common high order byte will change to reflect the high order byte of the performance counter just read. Counts that occur during the read cycle are held for the counter to be updated afterwards.

All the performance counters can also be configured to be either saturating or non-saturating. When a 1 is written to control bit COR (clear on read), the performance counters are configured to be saturating, with the counters stopping at their maximum count. An 8-bit or 16-bit saturating counter is reset on a microprocessor read cycle. When a 0 is written to control bit COR, the performance counters are configured to be non-saturating, and roll over to zero after the maximum count in the counter is reached. The counters are not cleared on a read cycle.

All the performance counters can be reset simultaneously by writing a 1 to control bit RESETC. This bit is self clearing, and does not require writing a 0 into this location. See exceptions for XA0H and XA2H below.

All drop-bus related performance counters are inhibited (i.e., will not increment) when one or more of the following alarms occurs:

- Loss of Drop bus clock alarm (DLOC)
- Loss of Drop bus J1 alarm (DLOJ1)
- AIS detected in the E1 byte (when XALM2AIS = 0)
- When either ISTAn or PAISn lead is high (when XALM2AIS = 1)
- Loss of pointer alarm (TUG-3)
- Path AIS alarm (TUG-3)

The performance counters can also be written by the microprocessor. However, when writing to a 16-bit counter (at locations n, n+1) it is recommended that the low order byte at location n should be written first. The high order byte can then be written by addressing location n + 1. Since the writes occur in separate cycles, care must be taken to prevent the low byte from passing FFH and incrementing the high byte before the high byte is initialized. Writing a low byte equal to 00H will provide the maximum time for the microprocessor to update the high byte.

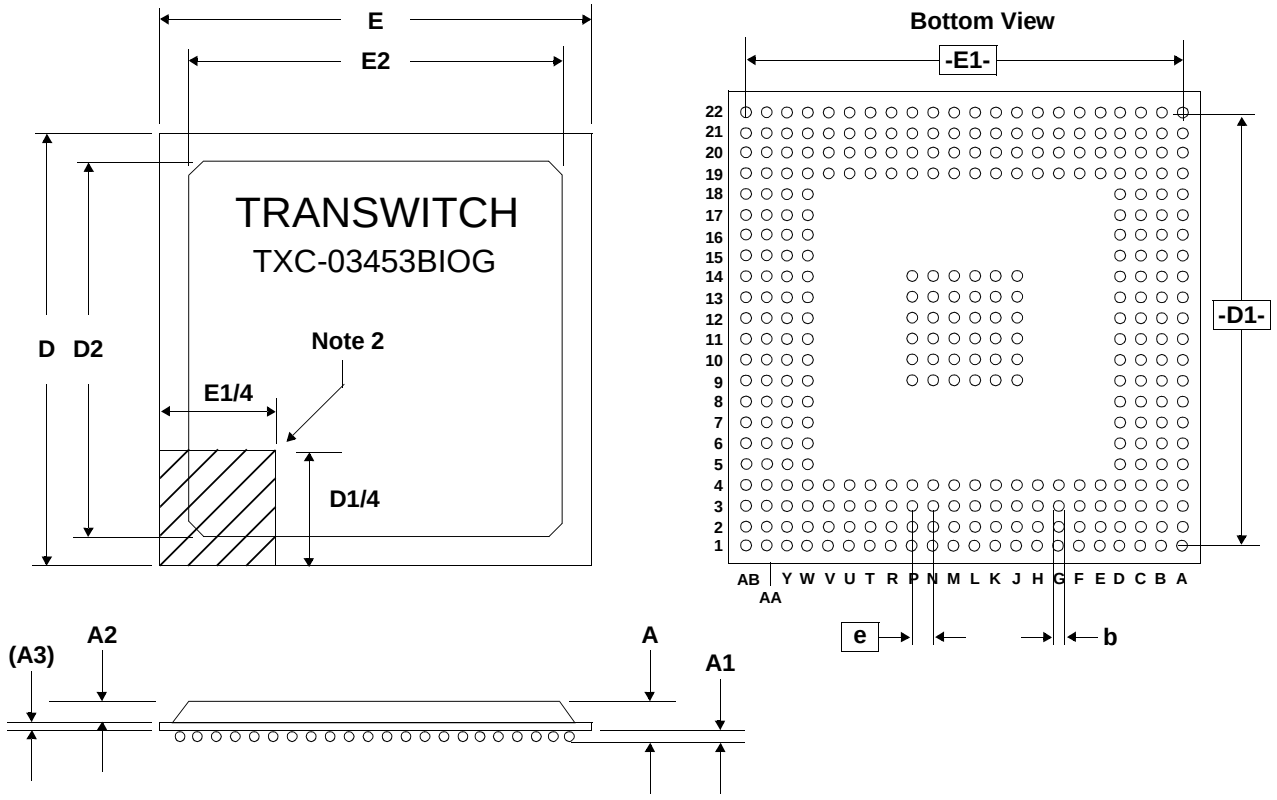
Where X=1, 2, or 3, which corresponds to the selected channel:

Address	Bit	Symbol	Description
XA0	7-0	Rcv Frame Cnt	**Receive SDH/SONET Frame Counter:** Counts the number of received SDH/SONET frames. This register is not cleared by a software reset and must be written to 00H to be cleared.
XA1	7-0		**Reserved**
XA2	7-0	FIFO Leak Rate	**FIFO Leak Rate Register:** When a value greater then 00H is written into this location, this number represents the number of frames between consecutive leaked bits, in multiples of four frames (i.e., a value of x means that there are 4x frames between bit leaks). The value of zero enables an internal TranSwitch pointer leak algorithm. The algorithm is TranSwitch proprietary. This register is not cleared by a software reset and must be written to 00H to be cleared.

Address	Bit	Symbol	Description
XA3	7-0	INC Count	**Positive Justification (Increment) Counter:** Counts the number of positive (increment) pointer movements in the AUG/VC-4 or STS-3/STS-1 based on incoming J1 movements in the C1J1 signal.
XA4	7-0	DEC Count	**Negative Justification (Decrement) Counter:** Counts the number of negative (decrement) pointer movements in the AUG/VC-4 or STS-3/STS-1 based on the incoming J1 movements in the C1J1 signal.
XA5	7-0	NDF Count	**New Data Flag (NDF) Counter:** Counts the number of the incoming J1 movements for the AUG/VC-4 or STS-3/STS-1 in the C1J1 signal.
XA6	7-0	TUG-3 INC Count	**TUG-3 Positive Justification (Increment) Counter:** Counts the number of positive (increment) pointer movements in the TUG-3, based on interpretation of H1 and H2.
XA7	7-0	TUG-3 DEC Count	**TUG-3 Negative Justification (Decrement) Counter:** Counts the number of negative (decrement) pointer movements in the TUG-3, based on interpretation of H1 and H2.
XA8	7-0	TUG-3 NDF Count	**TUG-3 New Data Flag (NDF) Counter:** Counts the number of New Data Flags (NDFs) or new pointers in the TUG-3 pointer (H1/H2).
XA9	7-0	B3 Block Count	**B3 Block Error Counter:** Counts the number of B3 blocks which are received in error. One or more B3 errors per frame is equal to one block error.
XAA, XAB	7-0	REI Counter	**Remote Error Indication (REI) Error Counter:** Counts the REI error count indication received in bits 1 through 4 of the G1 byte when control bit REIBLK is a 0. When control bit REIBLK is a 1, one or more REI errors are counted as one block error. Register location XAAH is defined as the low order byte, while register location XABH is the high order byte of the 16-bit counter. After reading the low order byte from register location XAAH the stored simultaneous value of the corresponding high order byte (XABH) should be read from XFFH.
XAC, XAD	7-0	B3 Counter	**B3 Parity Error Counter:** Counts the number of B3 errors between the incoming received B3 byte and the calculated value. Register location XACH is defined as the low order byte, while register location XADH is the high order byte of the 16-bit counter. After reading the low order byte from register location XACH, the stored simultaneous value of the corresponding high order byte (XADH) should be read from XFFH.
XAE, XAF	7-0	CV/PRBS Error Counter	**HDB3/B3ZS Coding Violations/PRBS Error Counter:** Counts the number of internal coding violation errors detected when the positive/negative rail interface is selected. Register location XAEH is defined as the low order byte while register location XAFH is the high order byte of the 16-bit counter. When control bit ENANA is set to 1, PRBS errors are counted instead when the internal PRBS test analyzer is in lock (i.e., no OOL alarm). After reading the low order byte from XAEH the stored simultaneous value of the corresponding high order byte (XAFH) should be read from XFFH.
XFF	7-0	Common High Byte Snapshot	**Common High Order Byte Counter Snapshot:** This location contains a copy of the high order byte value that existed when the low order byte of a 16-bit counter was last read (i.e., registers XABH, XADH, or XAFH).

PACKAGE INFORMATION

The TL3M device is packaged in a 324-lead plastic ball grid array package suitable for surface mounting, as illustrated in Figure 38.



Notes:
1. All dimensions are in millimeters. Values shown are for reference only.
2. Identification of the solder ball A1 corner is contained within this shaded zone. This package corner may be a 90° angle, or chamfered for A1 identification.
3. Size of array: 22 x 22, JEDEC code MO-151-AAJ-1.

Dimension (Note 1)	Min	Max
A	2.02	2.44
A1	0.40	0.60
A2	1.12	1.22
A3 (Ref.)	0.50	0.62
b (Ref.)	0.63	
D	23.00	
D1 (BSC)	21.00	
D2	19.45	20.20
E	23.00	
E1 (BSC)	21.00	
E2	19.45	20.20
e (BSC)	1.00	

Figure 38. TL3M TXC-03453B Package Diagram

ORDERING INFORMATION

Part Number:	TXC-03453BIOG	324-lead plastic ball grid array package

RELATED PRODUCTS

TXC-02030, DART VLSI Device (Advanced E3/DS3 Receiver/Transmitter). DART performs the transmit and receive line interface functions required for transmission of E3 (34.368 Mbit/s) and DS3 (44.736 Mbit/s) signals across a coaxial interface.

TXC-02302B, SYN155C VLSI Device (155-Mbit/s Synchronizer, Clock and Data Output). Transmits and receives at STS-3/STM-1 rates. Provides the complete STS-3/STM-1 frame synchronization function. Connects directly to optical fiber interface components.

TXC-03001B, SOT-1 VLSI Device (SONET STS-1 Overhead Terminator). This device performs section, line and path overhead processing for STS-1 SONET signals. Has programmable STS-1 or STS-N modes.

TXC-03003B, SOT-3 VLSI Device (STM-1/STS-3/STS-3c Overhead Terminator). This device performs section, line and path overhead processing for STM-1/STS-3/STS-3c signals. Compliant with ANSI and ITU-TSS standards.

TXC-03303, M13E VLSI Device. Single-chip with extended features multiplex/demultiplex device provides the complete interfacing function between a single DS3 signal and 28 independent DS1 signals.

TXC-03305, M13X VLSI Device (DS3/DS1 Mux/Demux). This single-chip device provides the functions needed to multiplex and demultiplex 28 independent DS1 signals to and from a DS3 signal with either an M13 or C-bit frame format. It includes some enhanced features relative to the M13E device.

TXC-03452B, L3M VLSI Device (Level 3 Mapper). Maps a 44.736 Mbit/s DS3 or 34.368 Mbit/s E3 asynchronous line signal into an STM-1/STS-3/STS-1 formatted synchronous signal. Separate Add/Drop bus timing is available for loop multiplexers. The L3M provides the overhead processing for the mapped signal.

TXC-06103, PHAST-3N VLSI Device (SDH/SONET STM-1, STS-3 or STS-3c Overhead Terminator) This PHAST-3N VLSI device provides a Telecom Bus interface for downstream devices and operates from a power supply of 3.3 volts.

TXC-06125, XBERT VLSI Device (Bit Error Rate Generator Receiver). Programmable multi-rate test pattern generator and receiver in a single chip with serial, nibble, or byte interface capability.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute
25 West 43rd Street
New York, New York 10036

Tel: (212) 642-4900
Fax: (212) 398-0023
Web: www.ansi.org

The ATM Forum (U.S.A., Europe, Asia):

404 Balboa Street
San Francisco, CA 94118

Tel: (415) 561-6275
Fax: (415) 561-6120
Web: www.atmforum.com

ATM Forum Europe Office

Kingsland House - 5th Floor
361-373 City Road
London EC1 1PQ, England

Tel: 20 7837 7882
Fax: 20 7417 7500

ATM Forum Asia-Pacific Office

Hamamatsucho Suzuki Building 3F
1-2-11, Hamamatsucho, Minato-ku
Tokyo 105-0013, Japan

Tel: 3 3438 3694
Fax: 3 3438 3698

Bellcore (See Telcordia)

CCITT (See ITU-T)

EIA (U.S.A.):

Electronic Industries Association
Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112

Tel: (800) 854-7179 (within U.S.A.)
Tel: (303) 397-7956 (outside U.S.A.)
Fax: (303) 397-2740
Web: www.global.ihs.com

ETSI (Europe):

European Telecommunications Standards Institute
650 route des Lucioles
06921 Sophia-Antipolis Cedex, France

Tel: 4 92 94 42 00
Fax: 4 93 65 47 16
Web: www.etsi.org

GO-MVIP (U.S.A.):

The Global Organization for Multi-Vendor Integration Protocol (GO-MVIP)
3220 N Street NW, Suite 360
Washington, DC 20007

Tel: (800) 669-6857 (within U.S.A.)
Tel: (903) 769-3717 (outside U.S.A.)
Fax: (903) 769-3818
Web: www.mvip.org

ITU-T (International):

Publication Services of International Telecommunication Union
Telecommunication Standardization Sector
Place des Nations, CH 1211
Geneve 20, Switzerland

Tel: 22 730 5852
Fax: 22 730 5853
Web: www.itu.int

JEDEC (International):

Joint Electron Device Engineering Council
2500 Wilson Boulevard
Arlington, VA 22201-3834

Tel: (703) 907-7559
Fax: (703) 907-7583
Web: www.jedec.org

MIL-STD (U.S.A.):

DODSSP Standardization Documents Ordering Desk
Building 4 / Section D
700 Robbins Avenue
Philadelphia, PA 19111-5094

Tel: (215) 697-2179
Fax: (215) 697-1462
Web: www.dodssp.daps.mil

PCI SIG (U.S.A.):

PCI Special Interest Group
5440 SW Westgate Dr., #217
Portland, OR 97221

Tel: (800) 433-5177 (within U.S.A.)
Tel: (503) 291-2569 (outside U.S.A.)
Fax: (503) 297-1090
Web: www.pcisig.com

Telcordia (U.S.A.):

Telcordia Technologies, Inc.
Attention - Customer Service
8 Corporate Place Rm 3A184
Piscataway, NJ 08854-4157

Tel: (800) 521-2673 (within U.S.A.)
Tel: (732) 699-2000 (outside U.S.A.)
Fax: (732) 336-2559
Web: www.telcordia.com

TTC (Japan):

TTC Standard Publishing Group of the Telecommunication Technology Committee
Hamamatsu-cho Suzuki Building
1-2-11, Hamamatsu-cho, Minato-ku
Tokyo 105-0013, Japan

Tel: 3 3432 1551
Fax: 3 3432 1553
Web: www.ttc.or.jp

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated *PRELIMINARY* TL3M TXC-03453B Edition 3 Data Sheet that have significant differences relative to the previous and now superseded *PRELIMINARY* TL3M TXC-03453B Edition 2 Data Sheet:

Updated TL3M TXC-03453B Data Sheet: *PRELIMINARY* Edition 3, September 2003.

Previous TL3M TXC-03453B Data Sheet: *PRELIMINARY* Edition 2, June 2002.

The page numbers indicated below of this updated TXC-03453B Edition 3 Data Sheet include significant changes relative to the previous TXC-03453B Edition 2 Data Sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed document number, edition number and date.
1	Added Patent number on the bottom left corner.
15	Corrected diagram of Figure 6 at D1 and E1.
26	Changed Name/Function for Symbols VRS1, SBS1, GRS1, VRS2, SBS2 and GRS2
30	Deleted Max value and added Min value for parameter I_{OL} in the "OUTPUT PARAMETERS FOR LVCMOS 4mA" table.
31	Deleted Max values and added Min values for parameter I_{OL} in the "OUTPUT PARAMETERS FOR LVCMOS 8mA" and "INPUT/OUTPUT PARAMETERS FOR LVTTL/LVCMOS 8mA" tables.
51	Changed diagram of Figure 28.
52	Added Note 5 for Figure 29.
53	Added Note 5 for Figure 30.
62	Changed Bits 7-4 at Address 0F3H.
63	Changed Bits 7-4 at Address XF3H. Changed Bit 4 at Address XF4H. Changed second sentence of Description paragraph.
81	Changed Description for Symbol ROVFL.
82	Changed Description for Symbol LOVFL.
92	Changed "Standards Documentation Sources" section.
94	Changed "List of Data Sheet Changes" section.

-NOTES-

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