To our customers,

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April ${ }^{\text {st }}, 2010$
Renesas Electronics Corporation

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## SILICON MMIC HI-IP3 FREQUENCY UP-CONVERTER FOR WIRELESS TRANSCEIVER

## DESCRIPTION

The $\mu$ PC8187TB is a silicon monolithic integrated circuit designed as frequency up-converter for wireless transceiver. This IC is higher operating frequency, lower distortion and higher conversion gain than conventional $\mu$ PC8163TB.

This IC is manufactured using NEC's $30 \mathrm{GHz} \mathrm{f}_{\max }$ UHS0 (Ultra High $\underline{\text { Speed Process) silicon bipolar process. }}$

## FEATURES

- High output frequency : frFout $=0.8$ to 2.5 GHz
- High-density surface mounting: 6-pin super minimold package
- Supply voltage : Vcc = 2.7 to 3.3 V
- Higher $\mathrm{IP}_{3} \quad: \mathrm{OIP}_{3}=+10 \mathrm{dBm} @ \mathrm{fRFout}^{2}=1.9 \mathrm{GHz}$


## APPLICATION

- TDMA, PCS, CDMA etc.


## ORDERING INFORMATION

| Part Number | Package | Marking | Supplying Form |
| :---: | :---: | :---: | :--- |
| $\mu$ PC8187TB-E3 | 6-pin super minimold | C3G | • Embossed tape 8 mm wide. <br> $\bullet$ Pin 1, 2, 3 face the tape perforation side. <br> $\bullet$ Qty 3 kpcs/reel. |

Remark To order evaluation samples, please contact your local NEC sales office.
(Part number for sample order: $\mu$ PC8187TB)

## Caution Electro-static sensitive devices

> The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
> Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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## 1. PIN CONNECTIONS



| Pin No. | Pin Name |
| :---: | :---: |
| 1 | IFinput |
| 2 | GND |
| 3 | LOinput |
| 4 | GND |
| 5 | Vcc |
| 6 | RFoutput |

2. SERIES PRODUCTS $\left(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{cc}}=\mathrm{V}_{\mathrm{PS}}=\mathrm{V}_{\text {RFout }}=3.0 \mathrm{~V}, \mathrm{Z}_{\mathrm{s}}=\mathrm{Z}_{\mathrm{L}}=50 \Omega\right)$

| Part Number | $\begin{gathered} \mathrm{lcc} \\ (\mathrm{~mA}) \end{gathered}$ | $\begin{gathered} \mathrm{f}_{\text {RFout }} \\ (\mathrm{GHz}) \end{gathered}$ | CG (dB) |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | @RF 0.9 GHz ${ }^{\text {Note }}$ | @RF 1.9 GHz | @RF 2.4 GHz |
| $\mu$ PC8187TB | 15 | 0.8 to 2.5 | 11 | 11 | 10 |
| $\mu \mathrm{PC} 8106 \mathrm{~TB}$ | 9 | 0.4 to 2.0 | 9 | 7 | - |
| $\mu \mathrm{PC} 8172 \mathrm{~TB}$ | 9 | 0.8 to 2.5 | 9.5 | 8.5 | 8.0 |
| $\mu$ PC8109TB | 5 | 0.4 to.2.0 | 6 | 4 | - |
| $\mu$ PC8163TB | 16.5 | 0.8 to 2.0 | 9 | 5.5 | - |


| Part Number | $\mathrm{Po}_{\text {(sat) }}(\mathrm{dBm})$ |  |  | $\mathrm{OIP}_{3}(\mathrm{dBm})$ |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | @RF 0.9 GHz ${ }^{\text {Note }}$ | @RF 1.9 GHz | @RF 2.4 GHz | $@$ RF 0.9 GHz ${ }^{\text {Note }}$ | @RF 1.9 GHz | @RF 2.4 GHz |
| $\mu \mathrm{PC} 8187 \mathrm{~TB}$ | +4 | +2.5 | +1 | +10 | +10 | +8.5 |
| $\mu \mathrm{PC8106TB}$ | -2 | -4 | - | +5.5 | +2.0 | - |
| $\mu \mathrm{PC8172TB}$ | +0.5 | 0 | -0.5 | +7.5 | +6.0 | +4.0 |
| $\mu \mathrm{PC8109TB}$ | -5.5 | -7.5 | - | +1.5 | -1.0 | - |
| $\mu$ PC8163TB | +0.5 | -2 | - | +9.5 | +6.0 | - |

Note frfout $=0.83 \mathrm{GHz} @ \mu \mathrm{PC} 8163 \mathrm{~TB}$ and $\mu \mathrm{PC} 8187 \mathrm{~TB}$

Remark Typical performance. Please refer to 8. ELECTRICAL CHARACTERISTICS in detail.
To know the associated product, please refer to each latest data sheet.

## 3. BLOCK DIAGRAM


4. SYSTEM APPLICATION EXAMPLES (SCHEMATICS OF IC LOCATION IN THE SYSTEM)


## 5. PIN EXPLANATION

| Pin <br> No. | Pin <br> Name | Applied <br> Voltage <br> (V) | Pin <br> Voltage $(\mathrm{V})^{\text {Note }}$ | Function and Explanation | Equivalent Circuit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | IFinput | - | 1.2 | This pin is IF input to double balanced mixer (DBM). The input is designed as high impedance. The circuit contributes to suppress spurious signal. Also this symmetrical circuit can keep specified performance insensitive to process-condition distribution. For above reason, double balanced mixer is adopted. |  |
| $\begin{aligned} & 2 \\ & 4 \end{aligned}$ | GND | GND | - | GND pin. Ground pattern on the board should be formed as wide as possible. Track Length should be kept as short as possible to minimize ground impedance. |  |
| 3 | LOinput | - | 2.1 | Local input pin. Recommendable input level is -10 to 0 dBm . |  |
| 5 | Vcc | 2.7 to 3.3 | - | Supply voltage pin. |  |
| 6 | RFoutput | Same bias as Vcc through external inductor | - | This pin is RF output from DBM. This pin is designed as open collector. Due to the high impedance output, this pin should be externally equipped with LC matching circuit to next stage. |  |

Note Each pin voltage is measured at $\mathrm{Vcc}=\mathrm{V}_{\text {RFout }}=2.8 \mathrm{~V}$.

## 6. ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Test Conditions | Rating | Unit |
| :---: | :---: | :---: | :---: | :---: |
| Supply Voltage | Vcc | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | 3.6 | V |
| Power Dissipation | PD | Mounted on double-side copperclad $50 \times 50 \times 1.6 \mathrm{~mm}$ epoxy glass PWB, $\mathrm{T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}$ | 270 | mW |
| Operating Ambient Temperature | $\mathrm{T}_{\text {A }}$ |  | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ |  | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Maximum Input Power | $\mathrm{P}_{\text {in }}$ |  | +10 | dBm |

## 7. RECOMMENDED OPERATING RANGE

| Parameter | Symbol | MIN. | TYP. | MAX. | Unit | Remarks |
| :--- | :---: | :---: | :---: | :---: | :---: | :--- |
| Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 2.7 | 2.8 | 3.3 | V | The same voltage should be <br> applied to pin 5 and 6 |
| Operating Ambient Temperature | $\mathrm{T}_{\mathrm{A}}$ | -40 | +25 | +85 | ${ }^{\circ} \mathrm{C}$ |  |
| Local Input Power | PLoin | -10 | -5 | 0 | dBm | $\mathrm{Zs}_{\mathrm{s}}=50 \Omega$ (without matching) |
| RF Output Frequency | $\mathrm{f}_{\mathrm{RFout}}$ | 0.8 | - | 2.5 | GHz | With external matching circuit |
| IF Input Frequency | $\mathrm{f}_{\text {IFin }}$ | 50 | - | 400 | MHz |  |

## 8. ELECTRICAL CHARACTERISTICS

$\left(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, \mathrm{Vcc}=\mathrm{V}_{\mathrm{rFout}}=\mathbf{2 . 8} \mathrm{V}, \mathrm{fiFin}_{\mathrm{I}}=\mathbf{1 5 0} \mathrm{MHz}, \mathrm{P}_{\text {Loin }}=\mathbf{- 5} \mathrm{dBm}\right)$

| Parameter | Symbol | Test Conditions ${ }^{\text {Note }}$ | MIN. | TYP. | MAX. | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Circuit Current | Icc | No signal | 11 | 15 | 19 | mA |
| Conversion Gain | CG1 | $\mathrm{frFout}^{\text {a }}$ 0.83 GHz, PIFin $=-20 \mathrm{dBm}$ | 8 | 11 | 14 | dB |
|  | CG2 |  | 8 | 11 | 14 | dB |
|  | CG3 | $\mathrm{ffFout}=2.4 \mathrm{GHz}, \mathrm{P}_{\text {IFin }}=-20 \mathrm{dBm}$ | 7 | 10 | 13 | dB |
| Saturated Output Power | $\mathrm{Po}($ (sat) 1 | $\mathrm{frFout}=0.83 \mathrm{GHz}, \mathrm{PIFFin}=0 \mathrm{dBm}$ | +1.5 | +4 | - | dBm |
|  | $\mathrm{Po}($ (sat)2 | $\mathrm{ffFout}=1.9 \mathrm{GHz}, \mathrm{P}_{\text {IFin }}=0 \mathrm{dBm}$ | 0 | +2.5 | - | dBm |
|  | Po (sat) 3 | $\mathrm{frFout}=2.4 \mathrm{GHz}, \mathrm{P}_{\text {IFin }}=0 \mathrm{dBm}$ | -1.5 | +1 | - | dBm |

Note $\mathrm{frFout}^{<} \mathrm{f}$ LOin @ frFout $=0.83 \mathrm{GHz}$
$f_{\text {Loin }}<$ frFout @fRFout $=1.9 \mathrm{GHz} / 2.4 \mathrm{GHz}$
9. OTHER CHARACTERISTICS, FOR REFERENCE PURPOSES ONLY
$\left(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{cc}}=\mathrm{V}_{\text {RFout }}=2.8 \mathrm{~V}, \mathrm{P}_{\text {Loin }}=-5 \mathrm{dBm}\right)$

| Parameter | Symbol | Test Conditions ${ }^{\text {Note }}$ |  | Value | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output 3rd Order Distortion Intercept Point | $\mathrm{OIP}_{3} 1$ | $\mathrm{ffFout}^{\text {a }}$ 0.83 GHz | $\begin{aligned} & f_{\text {flin } 1}=150 \mathrm{MHz} \\ & f_{\text {flin } 2}=151 \mathrm{MHz} \end{aligned}$ | +10 | dBm |
|  | $\mathrm{OIP}_{3} 2$ | $\mathrm{frFout}=1.9 \mathrm{GHz}$ |  | +10 | dBm |
|  | $\mathrm{OIP}_{3} 3$ | $\mathrm{fRFout}=2.4 \mathrm{GHz}$ |  | +8.5 | dBm |
| Input 3rd Order Distortion Intercept Point | IIP31 | $\mathrm{f}_{\text {fFout }}=0.83 \mathrm{GHz}$ | $\begin{aligned} & \mathrm{f}_{\text {fiFin } 1}=150 \mathrm{MHz} \\ & \mathrm{f}_{\mathrm{IF} \text { Fin2 }}=151 \mathrm{MHz} \end{aligned}$ | -1.0 | dBm |
|  | IIP32 | $\mathrm{frFout}=1.9 \mathrm{GHz}$ |  | -1.0 | dBm |
|  | IIP33 | $\mathrm{ffFout}^{\text {a }} 2.4 \mathrm{GHz}$ |  | -1.5 | dBm |
| SSB Noise Figure | SSB•NF1 | $\mathrm{f}_{\text {frout }}=0.83 \mathrm{GHz}$ | $\mathrm{fiFin}=150 \mathrm{MHz}$ | 11 | dB |
|  | SSB•NF2 | $\mathrm{frFout}^{\text {a }} 1.9 \mathrm{GHz}$ |  | 12 | dB |
|  | SSB•NF3 | $\mathrm{ffFout}^{\text {a }}$ 2.4 GHz |  | 12.5 | dB |

Note frFout < fLoin @ frFout $=0.83 \mathrm{GHz}$
$\mathrm{f}_{\mathrm{LO} \text { in }}<\mathrm{ff}_{\mathrm{fFout}}$ @ frFout $=1.9 \mathrm{GHz} / 2.4 \mathrm{GHz}$

## ^ 10. TEST CIRCUITS

10.1 TEST CIRCUIT 1 (frfout $=0.83 \mathrm{GHz}$ )


EXAMPLE OF TEST CIRCUIT 1 ASSEMBLED ON EVALUATION BOARD


## COMPONENT LIST

| Form | Symbol | Value |
| :--- | :---: | :---: |
| Chip capacitor | $\mathrm{C}_{1}, \mathrm{C}_{5}, \mathrm{C}_{7}$ | 1000 pF |
|  | $\mathrm{C}_{2}, \mathrm{C}_{4}$ | 100 pF |
|  | $\mathrm{C}_{6}$ | 10 pF |
|  | $\mathrm{C}_{3}$ | 4 pF |
| Chip inductor | L | $2.2 \mathrm{nH}^{\text {Note }}$ |

(*1) $35 \times 42 \times 0.4 \mathrm{~mm}$ polyimide board, double-sided copper clad
$(* 2) \quad$ Ground pattern on rear of the board
$(* 3) \quad$ Solder plated patterns
(*4) ○○○: Through holes
$(* 5) \quad$ : Join patterns with electrical tape

Note 2.2 nH: LL1608-FH2N25 (TOKO Co., Ltd.)

### 10.2 TEST CIRCUIT 2 (frfout $=1.9 \mathrm{GHz}$ )



## EXAMPLE OF TEST CIRCUIT 2 ASSEMBLED ON EVALUATION BOARD



COMPONENT LIST

| Form | Symbol | Value |
| :--- | :---: | :---: |
| Chip capacitor | $\mathrm{C}_{1}, \mathrm{C}_{6}, \mathrm{C}_{8}$ | 1000 pF |
|  | $\mathrm{C}_{2}, \mathrm{C}_{3}$ | 100 pF |
|  | $\mathrm{C}_{7}$ | 10 pF |
|  | $\mathrm{C}_{4}$ | 3 pF |
|  | $\mathrm{C}_{5}$ | 0.5 pF |
| Chip inductor | L | $470 \mathrm{nH}^{\text {Note }}$ |

(*1) $35 \times 42 \times 0.4 \mathrm{~mm}$ polyimide board, double-sided copper clad
(*2) Ground pattern on rear of the board
$(* 3) \quad$ Solder plated patterns
(*4) $\circ \bigcirc \bigcirc$ : Through holes

Note $470 \mathrm{nH}:$ LL2012-FR47 (TOKO Co., Ltd.)
10.3 TEST CIRCUIT 3 (frfout $=2.4 \mathrm{GHz}$ )


## EXAMPLE OF TEST CIRCUIT 3 ASSEMBLED ON EVALUATION BOARD



COMPONENT LIST

| Form | Symbol | Value |
| :---: | :---: | :---: |
| Chip capacitor | $\mathrm{C}_{1}, \mathrm{C}_{6}, \mathrm{C}_{8}$ | 1000 pF |
|  | $\mathrm{C}_{2}, \mathrm{C}_{5}$ | 100 pF |
|  | $\mathrm{C}_{7}$ | 10 pF |
|  | $\mathrm{C}_{3}$ | 1 pF |
|  | $\mathrm{C}_{4}$ | 0.75 pF |
| Chip inductor | L | $470 \mathrm{nH}^{\text {Note }}$ |

(*1) $35 \times 42 \times 0.4 \mathrm{~mm}$ polyimide board, double-sided copper clad
(*2) Ground pattern on rear of the board
(*3) Solder plated patterns
$(* 4) \quad \circ \bigcirc$ : Through holes

Note 470 nH : LL2012-FR47 (TOKO Co., Ltd.)

Caution The test circuits and board pattern on data sheet are for performance evaluation use only (They are not recommended circuits). In the case of actual design-in, matching circuit should be determined using S-parameter of desired frequency in accordance to actual mounting pattern.
$\star$ 11. TYPICAL CHARACTERISTICS (Unless otherwise specified, $\mathrm{T}_{\mathrm{A}}=+\mathbf{2 5}{ }^{\circ} \mathrm{C}, \mathrm{Vcc}=\mathrm{V}_{\mathrm{RFout}}$ )

CIRCUIT CURRENT vs.
SUPPLY VOLTAGE


CIRCUIT CURRENT vs. OPERATING AMBIENT TEMPERATURE


CONVERSION GAIN vs. LOCAL INPUT POWER


CONVERSION GAIN vs. LOCAL INPUT POWER


RF OUTPUT POWER vs. IF INPUT POWER


RF OUTPUT POWER vs.
IF INPUT POWER



RF OUTPUT POWER OF EACH


RF OUTPUT POWER OF EACH $\hat{E}_{\bar{E}} \quad$ TONE, IM vs. IF INPUT POWER


RF OUTPUT POWER OF EACH


RF OUTPUT POWER OF EACH


RF OUTPUT POWER OF EACH


RF OUTPUT POWER OF EACH


LOCAL LEAKAGE AT RF PIN vs.
LOCAL INPUT FREQUENCY


LOCAL LEAKAGE AT IF PIN vs.
LOCAL INPUT FREQUENCY


IF LEAKAGE AT RF PIN vs. IF INPUT FREQUENCY


LOCAL LEAKAGE AT RF PIN vs.
LOCAL INPUT POWER


LOCAL LEAKAGE AT IF PIN vs. LOCAL INPUT POWER


IF LEAKAGE AT RF PIN vs. IF INPUT POWER

$11.2 \mathrm{fRFout}^{\mathbf{~}} \mathbf{1 . 9 \mathrm { GHz }}$

CONVERSION GAIN vs.
LOCAL INPUT POWER


CONVERSION GAIN vs.
LOCAL INPUT POWER


RF OUTPUT POWER vs. IF INPUT POWER


RF OUTPUT POWER vs.
IF INPUT POWER



RF OUTPUT POWER OF EACH


RF OUTPUT POWER OF EACH $\hat{E}_{\bar{E}} \quad$ TONE, IM vs. IF INPUT POWER


RF OUTPUT POWER OF EACH




RF OUTPUT POWER OF EACH



LOCAL LEAKAGE AT RF PIN vs.
LOCAL INPUT FREQUENCY


LOCAL LEAKAGE AT IF PIN vs. LOCAL INPUT FREQUENCY


IF LEAKAGE AT RF PIN vs. IF INPUT FREQUENCY


LOCAL LEAKAGE AT RF PIN vs. LOCAL INPUT POWER


LOCAL LEAKAGE AT IF PIN vs. LOCAL INPUT POWER


IF LEAKAGE AT RF PIN vs. IF INPUT POWER


## 11.3 fRFout $=2.4 \mathrm{GHz}$

CONVERSION GAIN vs.
LOCAL INPUT POWER


CONVERSION GAIN vs.
LOCAL INPUT POWER


RF OUTPUT POWER vs. IF INPUT POWER


RF OUTPUT POWER vs.
IF INPUT POWER



RF OUTPUT POWER OF EACH



RF OUTPUT POWER OF EACH
TONE, IM 3 vs. IF INPUT POWER


RF OUTPUT POWER OF EACH TONE, IM 3 vs. IF INPUT POWER



RF OUTPUT POWER OF EACH



LOCAL LEAKAGE AT RF PIN vs.
LOCAL INPUT FREQUENCY


LOCAL LEAKAGE AT IF PIN vs. LOCAL INPUT FREQUENCY


IF LEAKAGE AT RF PIN vs. IF INPUT FREQUENCY


LOCAL LEAKAGE AT RF PIN vs.
LOCAL INPUT POWER


LOCAL LEAKAGE AT IF PIN vs. LOCAL INPUT POWER


IF LEAKAGE AT RF PIN vs. IF INPUT POWER

12. S-PARAMETERS FOR EACH PORT (Vcc $=\mathrm{V}_{\mathrm{RFout}}=2.8 \mathrm{~V}$ ) (The parameters are monitored at DUT pins)

LO port

| $S_{11}$ | $Z$ |  |
| :--- | :---: | :--- |
| REF | 1.0 Units |  |
| 1 | 200.0 mUnits/ |  |
| $\nabla_{h p}$ | $22.762 \Omega$ | $-104.25 \Omega$ |



START $\quad 0.100000000 \mathrm{GHz}$ STOP $\quad 3.100000000 \mathrm{GHz}$

RF port (without matching)


IF port


* 13. S-PARAMETERS FOR MATCHED RF OUTPUT (Vcc = Vrfout $=2.8 \mathrm{~V}$ )
- ON EVALUATION BOARD - (S22 data are monitored at RF connector on board)
0.83 GHz (matched in test circuit 1 )

| S22 | Z |
| :--- | :--- |
| REF | 1.0 Units |
| 1 | $200.0 \mathrm{mUnits} /$ |
| $\nabla_{h p}$ | $62.424 \Omega$ |
|  | $-9.7871 \Omega$ |




### 1.9 GHz (matched in test circuit 2)

$\mathrm{S}_{22} \mathrm{Z}$
REF 1.0 Units
$\begin{array}{ll}\nabla & 200.0 \text { mUnits/ }\end{array}$
$51.719 \Omega \quad 5.6523 \Omega$
C


14. PACKAGE DIMENSIONS

6-PIN SUPER MINIMOLD (UNIT: mm)


## 15. NOTE ON CORRECT USE

(1) Observe precautions for handling because of electrostatic sensitive devices.
(2) Form a ground pattern as wide as possible to minimize ground impedance (to prevent undesired oscillation).
(3) Connect a bypass capacitor to the Vcc pin.
(4) Connect a matching circuit to the RF output pin.
(5) The DC cut capacitor must be each attached to the input and output pins.

## 16. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

| Soldering Method | Soldering Conditions | Recommended Condition Symbol |
| :--- | :--- | :---: |
| Infrared Reflow | Package peak temperature: $235^{\circ} \mathrm{C}$ or below <br> Time: 30 seconds or less (at $210^{\circ} \mathrm{C}$ ) <br> Count: 3, Exposure limit: None ${ }^{\text {Note }}$ | IR35-00-3 |
| VPS | Package peak temperature: $215^{\circ} \mathrm{C}$ or below <br> Time: 40 seconds or less (at $\left.200^{\circ} \mathrm{C}\right)$ <br> Count: 3, Exposure limit: None ${ }^{\text {Note }}$ | VP15-00-3 |
| Wave Soldering | Soldering bath temperature: $260^{\circ} \mathrm{C}$ or below <br> Time: 10 seconds or less <br> Count: 1, Exposure limit: None ${ }^{\text {Note }}$ |  |
| Partial Heating | Pin temperature: $300^{\circ} \mathrm{C}$ <br> Time: 3 seconds or less (per side of device) <br> Exposure limit: None ${ }^{\text {Note }}$ | WS60-00-1 |

Note After opening the dry pack, keep it in a place below $25^{\circ} \mathrm{C}$ and $65 \%$ RH for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).
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