TEMx28® Device
28 Channel Dual Bus High Density Mapper
TXC-04222

DATA SHEET

FEATURES

- Add/drop up to 28 E1, DS1, or VT/TU payloads from two add and two drop STM-1/VC4, STS-3 buses
- Add bus and drop bus timing modes
- Cross mapping applications (DS1 mapped to/from VT2/TU-12s)
- Selectable HDB3/B8ZS/AMI positive/negative rail, NRZ, or VT/TU interfaces per channel
- H4 multiframe option in place of Telecom Bus V1 pulse
- Digital desynchronizer
- Drop buses are monitored for parity, loss of clock, and upstream AIS
- Performance counters for pointer movements, BIP-2 errors, REI and coding violations
- Single-bit or three-bit RDI operation per channel
- Tandem connection capability per ETSI standards
- J2 trail trace comparison option
- Processor access to H1/H2, H4 overhead bytes, and V1/V2 and V4 bytes
- Selectable positive, negative or positive/negative alarm transition interrupt options
- Line and facility loopbacks, generation of BIP-2 and REI errors, PRBS generator and analyzer per channel
- Polling registers and global summary alarm status
- One second measurements: counters and alarms
- Software device driver is provided
- IEEE 1149.1 standard boundary scan
- +3.3 V and 1.8 V power supplies, 5 V tolerant I/O leads
- 376-lead plastic ball grid array (PBGA) package (23 mm x 23 mm)

DESCRIPTION

The TEMx28® device is designed for add/drop multiplexer, terminal multiplexer, and dual and single unidirectional ring applications. Up to 28 E1, DS1, or VT/TU payloads are mapped to and from VT1.5/TU-11s and VT2/TU-12s carried in an STM-1 VC-4 or STS-3 format. The device interfaces to a multiple-segment, byte-parallel SDH/SONET-formatted bus at the 19.44 Mbyte/s byte rate. The E1 and DS1 signals can be HDB3 or B8ZS/AMI rail signals, or NRZ signals. The VT/TU interface can be provided with or without the overhead bytes for virtual concatenation applications. The TEMx28 performs pointer tracking and overhead byte processing, including single-bit or three-bit RDI operation, and optional tandem connection capability. All overhead bytes, including the V1/V2/V4 bytes, are provided for microprocessor access.

The TEMx28 can generate receive and transmit line AIS, transmit unequipped and supervisory unequipped channels, and transmit VT/TU AIS, in addition to standards-compliant overhead byte monitoring. It also provides test features and a microprocessor interface.

APPLICATIONS

- 3 STS-3/STM-1 to 1.544 Mbit/s and 2.048 Mbit/s add/drop mux/demux
- Unidirectional or bidirectional ring applications
- STS-3/STM-1 termination terminal mode multiplexer
- STS-3/STM-1 test equipment

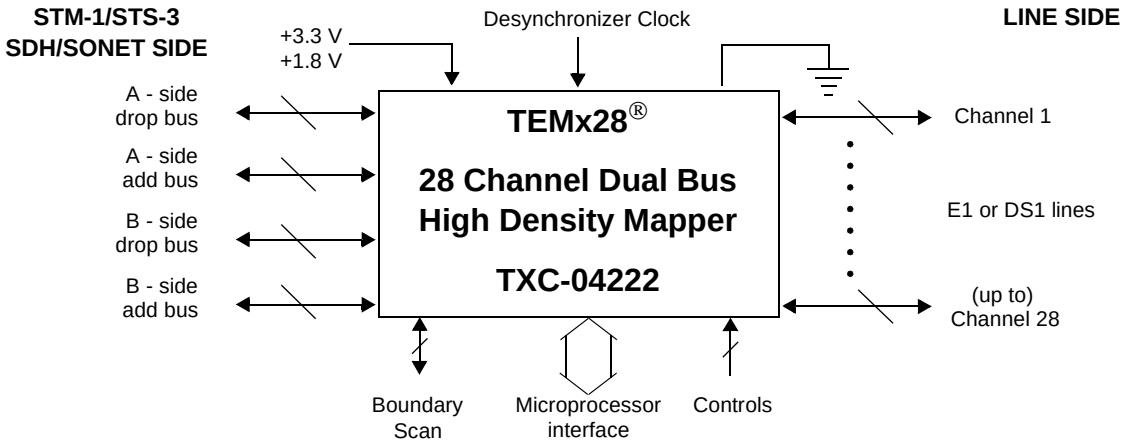

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TABLE OF CONTENTS

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LIST OF FIGURES

OVERVIEW

The TEMx28 device is designed for add/drop multiplexer, terminal multiplexer, and dual and single unidirectional ring applications. Up to 28 E1, DS1, or VT/TU payloads are mapped to and from VT1.5/TU-11s and VT2/TU-12s carried in an STM-1 VC-4 or STS-3 format. The device interfaces to a multiple-segment, byte-parallel SDH/SONET-formatted bus at the 19.44 Mbyte/s byte rate. The E1 and DS1 signals can be HDB3 or B8ZS/AMI positive/negative rail (dual unipolar) signals, or NRZ signals. The VT/TU interface can be provided with or without the overhead bytes for virtual concatenation applications. The TEMx28 performs pointer tracking and overhead byte processing, including single-bit or three-bit RDI operation, and optional tandem connection capability. All overhead bytes, including the V1/V2/V4 bytes, are provided for microprocessor access.

The TEMx28 can generate receive and transmit line AIS, transmit unequipped and supervisory unequipped channels, and transmit VT/TU AIS, in addition to standards-compliant overhead byte monitoring.

For testing, the device provides IEEE 1149.1 boundary scan, a PRBS generator and analyzer, and both line and facility loopbacks. The TEMx28 supports split bus access for either Intel or Motorola microprocessors. Its performance counters can be configured to be either saturating or roll over. Interrupts can be generated by alarms that latch on positive, negative, or both positive and negative status transitions, and they can be disabled via mask bits. A software polling register and summary alarm bit status are also provided. One second measurements are performed for alarms and counters.

FEATURES

The following is a detailed list of features supported by the TEMx28:

- Bus Modes of operation (Each Channel)
  - Drop Mode Only
    - Drop from A or B
  - Add Mode only
    - Add to A or B
    - Add to A and B
  - Single Unidirectional Ring
    - Drop from A, Add to A
    - Drop from B, Add to B
  - Multiplexer
    - Drop from A, Add to B
    - Drop from B, Add to A
  - Dual Protection Ring
    - Drop from A, Add to A and B
    - Drop from B, Add to B and A

- Bus Timing
  - Drop Bus Timing
    - Add Bus Timing Derived from the same named Drop Bus
  - Add Bus Timing
    - Add Bus Timing is independent of the Drop Bus
  - Lead Selectable

- SONET/SDH COMBUS Interface
  - Drop Bus Timing Enabled
    - Drop Bus: C1J1V1, SPE, Byte Wide Data, Clock, Parity
    - Add Bus: Byte Wide Data, Parity, Add Indicator
      - Option: Clock, C1J1V1, and SPE are Outputs
  - Add Bus Timing Enabled
    - Drop Bus: C1J1V1, SPE, Byte Wide Data, Clock, Parity
    - Add Bus: Clock, C1J1V1, SPE are inputs; Byte Wide Data, Parity, Add Indicator are Outputs.

- Mappings
  - Maximum of up to 28 Channels
    - DS1/E1 Line Asynchronous Formats, or VC-11/VC-12s
    - Independent VT1.5/TU-11 or VT2/TU12 Selection per Channel for both Drop and Add Buses
    - Cross Mapping: DS1 mapped into VT1.5/TU-12

- SONET/SDH Operating Formats
  - STS-3 STS-1 (19.44 Mbyte/s)
  - STM-1 VC-4/TUG-3/TUG-2 (19.44 Mbyte/s)
  - STM-1 AU-3s (19.44 Mbyte/s)

- Other Bus Features
  - Drop Buses
    - Input Parity Check with Alarm Indication
      - Odd, or Even
      - Data Only, or Bus Signals
    - Input Loss Of Clock Detection
      - Stuck High or Low
  - Add Buses
    - Output Parity Generation
      - Odd, or Even
      - Data Only, or Bus Signals
    - Add to Bus Indicator
    - High Z Output Bus Signals Control
    - Individual Channel High Z VT/TU Time Slots

- SONET/SDH Features
  - In-band upstream AIS Detection
    - H1/H2 Pointer Bytes
    - E1 Bytes using Majority Voting
  - H4 Byte Multiframe Detectors or V1 pulse (C1J1V1) reference input
    - Determines Location of V1/V2 Pointer Bytes
  - Pointer Tracking
    - ETSI/ITU/ANSI State Machine
    - Wrong Size Bits Detection
    - Positive/Negative Justification 8-bit Counters
  - Microprocessor Access to
    - V1/V2 Pointer Bytes (Each Channel)
    - H4 POH Bytes (Both Buses, VC-4 or Three STS-1s)
    - E1 (used for Upstream AIS Indication) Bytes (Both Buses, VC-4 or Three STS-1s)
    - H1/H2 Pointer Bytes (Both Buses, VC-4 or Three STS-1s)

- VT/TU Overhead Byte Processing
  - J2 Byte
    - 64 Byte Read Segment with Optional CR/LF Alignment
    - 16 Byte Read Segment with Optional Trail Trace Message Comparison
  - V5/K4 Byte
    - Three Bit or Single Bit RDI (Programmable for Each Channel)
      - Detection/Recovery Selection: 5 or 10 event Option
    - REI Error Counter
    - RFI Detector
    - BIP-2 Bit/Block Error Counter Option
    - Signal Label Mismatch, Unequipped, and VC AIS detection
      - Detection/Recovery: 5 events
  - N2 Byte
    - Tandem Connection Option
    - Trail Trace Message Comparison against Microprocessor Written Message

- Overhead Byte Access
  - Both A and B Buses

- Desynchronizer
  - Meets ANSI/ETSI/ITU Requirements
    - Pointer Test Sequences
    - Jitter/MTIE
  - External Clock (Common to Both Rates)
  - Leak Rate Control
    - Microprocessor Control - 10 Bits

- Line AIS (DS1/E1) Generation
  - Mask Bits for Individual Alarms
  - Global Mask Bit for all Alarms
  - Microprocessor Control

- VT/TU Overhead Byte Insertion (per Channel)
  - J2 Byte
    - 64 or 16 byte Microprocessor Written Message
    - J2 Forced to 0 Option
  - V5/K4 Byte
    - REI Insertion (from Drop Side VT/TU)
    - RFI Value from Microprocessor
    - BIP-2 Calculation and Insertion
    - RDI Insertion
      - Single or Three Bit
    - RDI Generated for a Minimum of 20 Multiframes
      - Mask bits for Alarms
      - Global Mask Bit for all Alarms
      - Microprocessor Control
  - K4 Byte
    - Input Bits 1 and 2 from External VT/TU interface
  - N2 Byte
    - Tandem Connection Option
      - 16 byte Message Insertion
      - Mask Alarm Bits or Microprocessor for TC ODI and RDI Generation
      - Internal Multiframe Generation
      - TC AIS Generation
      - TC Unequipped Generation

- Overhead Single Byte Insertion
  - All Bytes
  - Test purpose

- Unequipped Generation (per Channel)
  - Supervisory Unequipped Generation Option
- Transmit AIS Generation

- TU/VT AIS
  - Microprocessor Control
- DS1 or E1 AIS
  - Alarms with mask Bits
  - Microprocessor Control

- O-bit Access
  - Drop and Add both A and B Buses

- Line Interface
  - NRZ
    - External Loss Of Signal or Coding Violation Input
  - Rail
    - CODEC
      - AMI/B8ZS/HDB3
      - Coding Violation Counter
    - Loss Of Signal Detector
  - VT/TU Interface
    - Add Bus Timing Mode Only
    - Fixed C1J1 Locations in Add Direction
    - Two Modes: With or Without (Gapped Clock) Overhead Bytes
    - Transmit Direction: Fixed Framing References and Clock Outputs, Data in
      - Bits 1 and 2 in K4 byte clocked in with data for symmetrical clock

- Microprocessor Interface
  - Intel or Motorola Split Bus
    - LDS lead Option (683XX Processors)
    - READY/$\overline{\text{DTACK}}$ Leads
    - Interrupt Structure
  - Positive, Negative, Positive/Negative Alarm Transitions
  - Polling Registers with Mask Bits
    - Alarm Summary Bits with Mask Bits
    - One Second Measurements
  - Counters
    - Roll Over or Saturating
    - One Second Measurements
- Test features
  - Boundary Scan
  - DS-1/E1 loopbacks
    - Facility
    - Line
  - COMBUS loopback
- High Z all Leads (except Boundary Scan Output)
- PRBS Generator and Analyzer
  - 2^{15}-1 as defined in O.151 and T1M1.3/92-006R3 or QRSS (2^{20}-1) as defined in ANSI T1.403-1195)
  - Drop or Add Direction Placement
- Single Bit Error Generation for Transmit REI and BIP-2

BLOCK DIAGRAM

A block diagram of the TEMx28 device is shown in Figure 1. Further information on device operation and the interfaces to external circuits is provided in the following paragraphs.

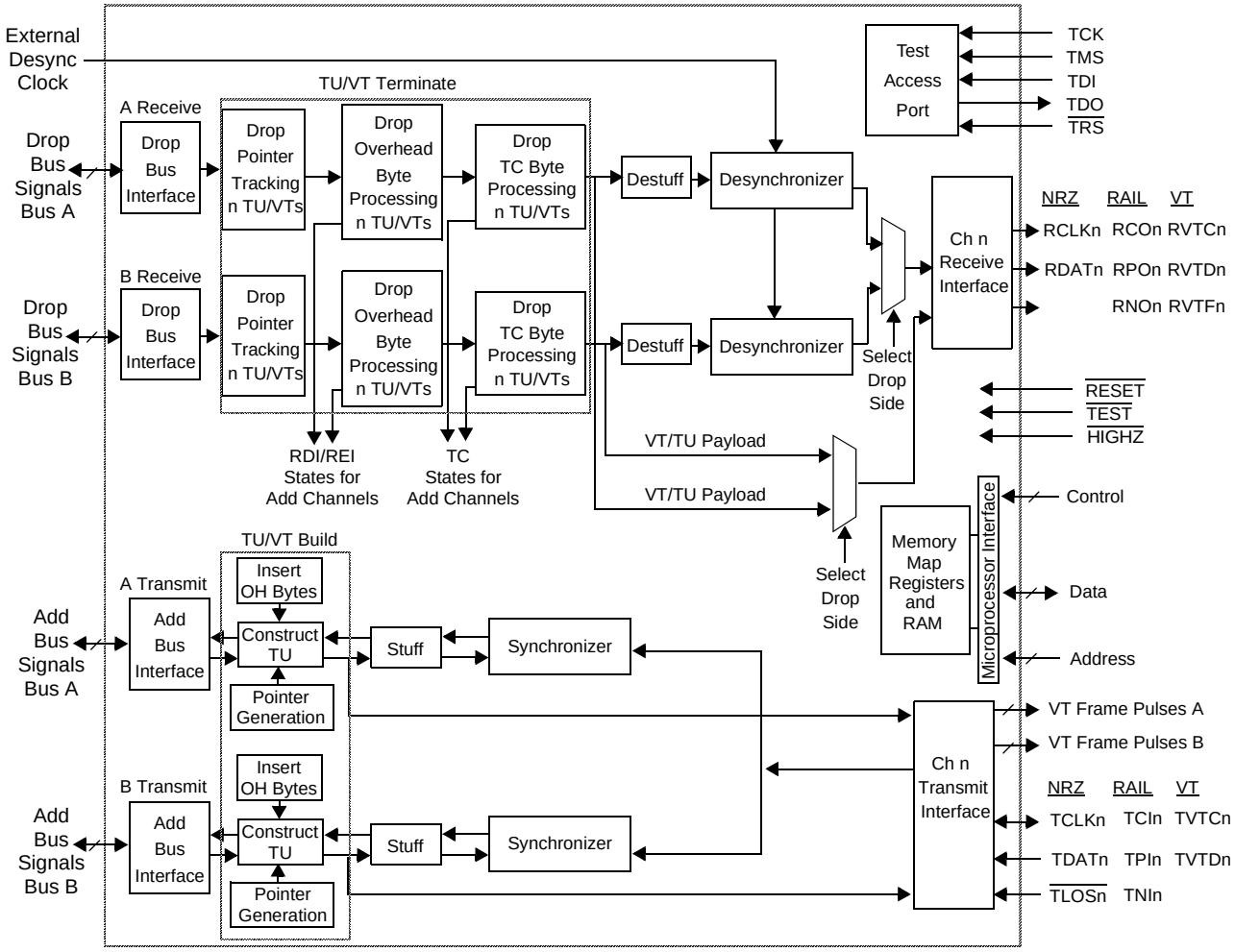


Figure 1. TEMx28 TXC-04222 Block Diagram

BLOCK DIAGRAM DESCRIPTION

As illustrated in Figure 1, the TEMx28 interfaces to four buses, designated as A Drop, B Drop, A Add, and B Add. The four buses run at the STM-1/STS-3 rate of 19.44 Mbyte/s. For North American applications, asynchronous DS1 signals are carried in a floating Virtual Tributary 1.5 (VT1.5) format, while E1 signals are carried in a floating Virtual Tributary 2 (VT2) format. A maximum of 28 VT1.5 and 21 VT2 signals are carried in a Synchronous Transport Signal - 1 (STS-1) format. Three STS-1s are in turn carried in a STS-3 signal. For ITU-T applications, asynchronous E1 signals are carried in floating mode Tributary Unit - 12 (TU-12) format and DS1 signals are carried in floating mode Tributary Unit - 11 (TU-11) format. The TU-12s and TU-11s are carried in an STM-1 Virtual Container - 4 (VC-4) structure using Tributary Unit Group - 3 (TUG-3), or in the STM-1 Virtual Container - 3 (VC-3) structure using Tributary Unit Group - 2 (TUG-2) mapping schemes. Up to 28 DS1 or E1 signals, or a combination of DS1 and E1 signals, can be dropped from one bus (A Drop or B Drop) to the DS1 or E1 lines. A maximum of 28 asynchronous DS1 or E1 signals are converted into TU-11/TU-12 or VT1.5/VT2 format and are added to either of the add buses, or both, depending upon the mode of operation.

The TEMx28 can provide, on a per channel basis, the Virtual Container - 11 (VC-11), or the E1 Virtual Container - 12 (VC-12) formats in place of the DS1 or E1 signals for Virtual Concatenation applications. The VC format contains the payload and overhead bytes associated with the TU-11 and TU-12 formats.

The TEMx28 also supports the cross mapping feature specified in ITU Recommendation G707. This feature enables a DS1 asynchronous line signal to be carried in a TU-12/VT2 payload. This feature is supported in the TEMx28 on a per channel basis.

When the TEMx28 is configured for drop bus timing, the add buses are, by definition, byte- and multiframe-synchronous with their like-named drop buses, but are delayed by one or two byte times because of internal processing. For example, if a byte in the STM-1 Virtual Container - 4 (VC-4) structure using Tributary Unit Group - 3 (TUG-3), TU-12/VT2 is to be added to the A Add bus, the time of its placement on the bus is derived from the A Drop bus timing, and from software instructions specifying which TU/VT number is being added. Note that the TU/VT A drop bus selection can be different from the A add bus selection. An option is provided which enables the dropped timing signals to be sent as outputs on the add bus. When the device is configured for add bus timing, the add bus, parity, and add indicator signals are derived from the input add bus clock, C1J1V1 and SPE signals.

In the drop (receive) direction, the A Receive Drop Bus Interface block is identical to the B Receive block. The TU/VT Terminate block, Destuff block and Desychronizer block are repeated 56 times, 28 for each side (A and B sides). The Channel n Receive Interface blocks are repeated 28 times, one for each channel. The interface between a drop bus and the receive block consists of 12 input leads: a 19.44 MHz byte clock, byte-wide data, a C1J1 indicator which may be also carrying a V1 indication making the signal a C1J1V1 indicator, an SPE indicator, and an odd/even parity bit. The Drop C1J1V1 signal is used in conjunction with the Drop SPE signal to determine the location of the various bytes in the SONET/SDH format. A single J1 pulse identifies the starting location of the J1 byte in the VC-4 format, when the SPE signal is high. Three J1 pulses are provided for the STS-3 format, each identifying the starting location of the J1 byte in each of the three STS-1 signals.

The TEMx28 can function with either a V1 pulse in the C1J1V1 signal, or it can use an internal H4 detector, for determining the location of the V1 byte. The V1 pulse location is used to determine the location of the pointer bytes V1 and V2. For STM-1 VC-4 operation, if the C1J1V1 signal is used, a one add or drop bus clock cycle wide pulse must occur every four frames and three drop bus clock cycles after the J1 pulse while the SPE is high. The J1 pulse identifies the J1 byte location (defined as the starting location for the VC-4) in the POH bytes. In the next column (first clock cycle) all the rows are assigned as fixed stuff. Similarly, in the next column (second clock cycle) all the rows are assigned as fixed stuff. The next column (third clock cycle) defines the start of TUG-3 A. This column is where the V1 pulse occurs every four frames. However, the actual V1 byte location is six clock cycles after the V1 pulse. For STS-3 operation, three V1 pulses must be present every four frames. Each of the three V1 pulses must be present three clock cycles after the corresponding J1 pulse, when the SPE signal is high.

Each drop bus (A and B) is monitored for parity errors, loss of clock, H4 multiframe alignment if selected, and an upstream SDH/SONET AIS indication. The TEMx28 can monitor either the TOH E1 order wire bytes or the H1/H2 bytes for an upstream AIS indication.

Each TU/VT Terminate block (A and B side) performs pointer processing using the V1 and V2 bytes. The pointer bytes are monitored for loss of pointer, Alarm Indication Signal (AIS), and a New Data Flag (NDF). The pointer tracking process is based on ETSI/ITU-T standards, which also meets ANSI requirements. Pointer increments and decrements are also counted, and the size bits are monitored for the correct value. This block also processes and monitors the various alarms found in the four overhead bytes. These operations including signal label mismatch detection, unequipped status detection, BIP-2 parity error detection and error counter, REI error counting, and single-bit or three-bit Remote Defect Indications (RDI). The TEMx28 performs a 16-byte J2 trail trace comparison on the channels selected. For 64-byte messages, the bytes are stored in a memory map segment for a microprocessor read cycle. The device also provides the TU tandem connection feature and performs the 16-byte message comparison for the N2 (formerly known as Z6) byte message.

All VT/TU overhead bytes, eight overhead communications channel bits (O-bits), the V1/V2 pointer bytes, and the V4 byte for each channel are available for a microprocessor read cycle. Also, the E1 order wire bytes, the H1/H2 pointer bytes, and the H4 bytes from the upstream circuitry are also available for a microprocessor read cycle.

A control bit for each port selects the TU/VT from either the A Drop or B Drop bus. The TU/VT is destuffed in the Destuff block using majority logic rules for the three sets of three justification control bits to determine if the two S-bits are data bits or frequency justification bits.

The Desynchronizer block removes the effects on the DS1 or E1 output of systemic jitter that might occur because of signal mappings and pointer movements in the network. The Desynchronizer block is comprised of a pointer leak buffer and a loop buffer. The pointer leak buffer spaces bursts of pointer movements more gradually over time and can accept up to five consecutive pointer movements. The loop buffer consists of a digital loop filter, which is designed to track the frequency of the received signal and to remove both transmission and stuffing jitter.

The Channel n Receive Interface block of each channel provides either NRZ data, positive and negative rail signal, or a VT/TU interface. Receive data (towards the line), for each of the channels, can be clocked out on either rising or falling edges of the clock. In addition, a control bit is provided for forcing the data and clock signals to a high impedance state (tristate), or to the zero state.

In the add (transmit) direction, the TEMx28 accepts a clock and either NRZ data or positive and negative rail signals. Data, for each of the channels, can be clocked in on either the falling or rising edge of the clock. In the NRZ mode, an external loss of clock indication or external coding violations can be provided. For the rail signal, coding violations are counted, and there is a loss of signal detector. A DS1/E1 AIS detector is also provided.

Each channel can also be configured for VT/TU interface for Virtual Concatenation data applications. When this interface is selected, a clock signal is provided for strobing in data for either the A or B bus. Four framing pulses are also provided which define the starting location of the VT1.5/TU-11 and VT2/TU-12. An option is provided for including the four overhead bytes. However, except for bits 1 and 2 in the K4 bytes, the other bits are ignored. Bits 1 and 2 in the K4 byte carry an extended signal label and information pertaining to the payload position within the Virtual Concatenation channel. The Virtual Concatenation channel will be assigned to n VT/TUs based on the data bandwidth required for the application.

For a NRZ or positive/negative rail transmit interface, the line signal is written into two FIFOs, one for add A side and the other for the B side, in one of the two Stuff/Synchronizer block pairs. Threshold modulation is used for the frequency justification process. Timing information from the A and B drop buses or from the A and B add buses is used to read the FIFO and perform the TU/VT justification process. The Synchronizer block permits tracking of an incoming signal having an average frequency offset as high as 120 ppm, and up to 1.5 UI of peak-to-peak jitter. Since the TEMx28 supports two different network architectures (DS1 and E1), two sets of blocks are provided for each channel. The TU/VT A and B add bus selection can be different. The VT/TU add bus selection can be different from the drop VT/TU selection. A control bit, and transmit line alarms, can also generate DS1/E1 AIS.

The TU/VT Build blocks format the TU/VT into an STS-3 or STM-1 structure for the asynchronous DS1 or E1 signals. The pointer value carried in the V1 and V2 bytes is transmitted with a fixed value of 78 for the VT1.5/TU-11 and 105 for the VT2/TU-12. Transmit access is provided for the eight overhead communications channel bits (O-bits) via the microprocessor. The microprocessor also writes the signal label, and the value of the J2 message, either as a 16-byte or a 64-byte message. The TEMx28 provides the TU tandem connection feature for the TU-11 or TU-12, including the transmission of the 16-byte message and the various alarms associated with the tandem connection feature. The device provides either single-bit or three-bit RDI using the V5 and K4 bytes. Local alarms, or the microprocessor, can generate the remote payload, server, or connectivity defect indications. The Remote Error Indication (REI) is inserted from the BIP-2 errors detected on the receive side, and BIP-2 parity is generated for the V5 byte. Control bits are provided for generating unequipped status, generating TU/VT AIS, and inserting REI and BIP-2 errors in the V5 byte. Control bits are also provided that enable the microprocessor to insert overhead byte test values, including the V1/V2 pointer bytes and the V4 byte.

The A Transmit block is identical to the B Transmit block. The interface between an add bus and a Transmit block consists of three input leads and ten output leads, when the add bus timing mode is selected. The input leads are a byte clock, a C1J1V1 indicator, and an SPE indicator. The output leads are byte-wide data, and a parity indicator, and an add-to-bus indicator signal. The Add C1J1V1 signal is used in conjunction with the Add SPE signal to determine the location of the various bytes in the SONET/SDH format.

When drop bus timing is selected, the output leads are byte-wide data, a parity indicator, and an add-to-bus indicator. The add bus clock, SPE and C1J1V1 signals, which are derived from the drop bus, can disabled or provided. The selection is performed by a lead.

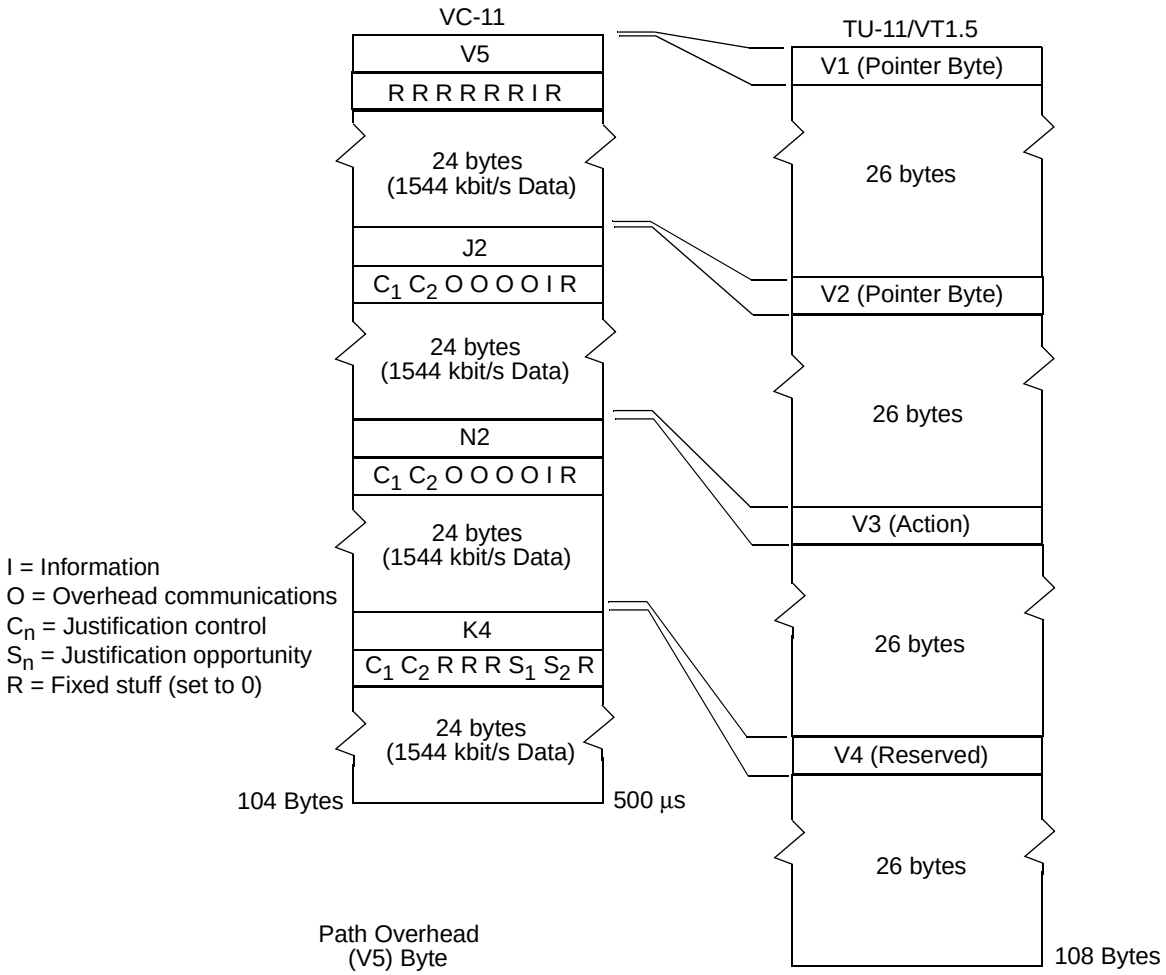
The Microprocessor Input/Output Interface block consists of an Intel- or Motorola-compatible split address/data bus interface that provides access to assigned TEMx28 memory map addresses. Interrupt capability, interrupt mask bits, alarm summary bits, and software polling bits are also provided. The alarms that cause the interrupt can be set on positive, negative, or both positive and negative transitions.

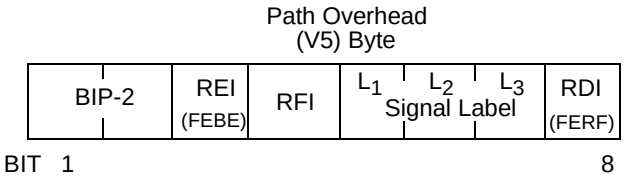
Control bits are provided which enable a facility or a line loopback. In addition, a PRBS analyzer and generator are provided. A 2^{15}-1 or 2^{20}-1 PRBS pattern is supported. The analyzer and generator can be used in the drop or add line direction for additional testing flexibility.

The Test Access Port (TAP) block provides a five-lead Boundary Scan capability that conforms to the IEEE 1149.1 standard. This standard provides external boundary scan functions to read and write the external Input/Output leads from the TAP for board and component test.

The TEMx28 software driver has the same architecture of the other TranSwitch device drivers such as the ML3M software, and is meant to be easily integrated with them. The application software calls the driver functions to configure, control and manage the TEMx28 device. The device driver insulates the application from the internal details of the device register usage and provides a higher level of abstraction. Particularly powerful are the default configurations provided within the driver that allow one single command to bring the device to operational mode.

Figure 2. 1544 kbit/s Asynchronous Mapping





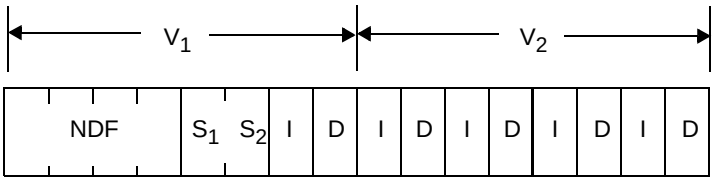
BIP-2 = Bit Interleaved Parity (2 bits)

REI = Remote Error Indication
(formerly FEBE, Far End
Block Error Indication)

RFI = Remote Failure Indication

$L_1L_2L_3$ = Signal Label

RDI = Remote Defect Indication
(formerly FERF, Far End
Receive Failure Indication)



New Data Flag
Normal = 0110, 1110, 0010, 0100 or 0111
New = 1001, 0001, 1101, 1011 or 1000

Size
S_1S_2 = 11

Positive Justification = Invert five I-bits
Negative Justification = Invert five D-bits

Pointer Range = 0 - 103 decimal

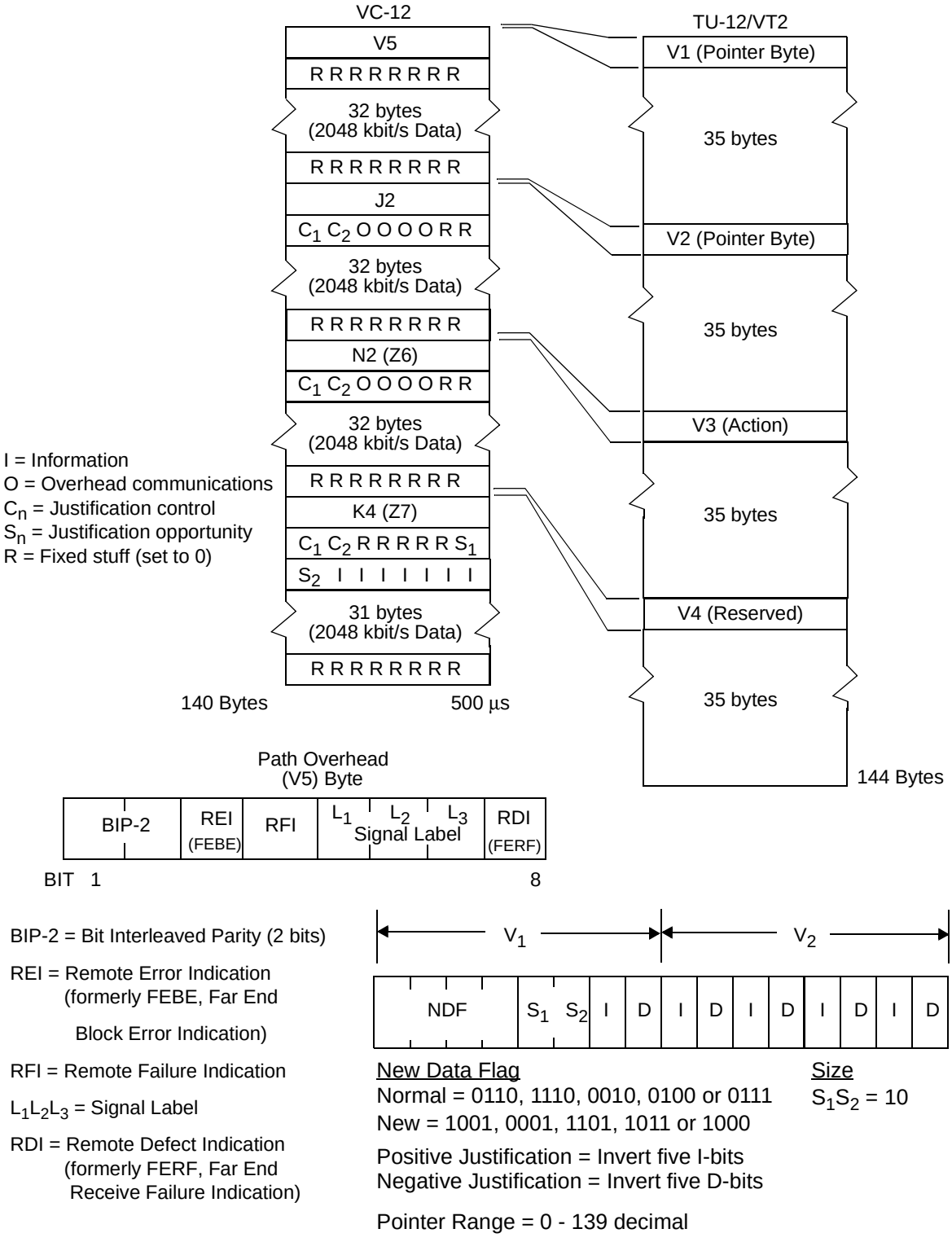
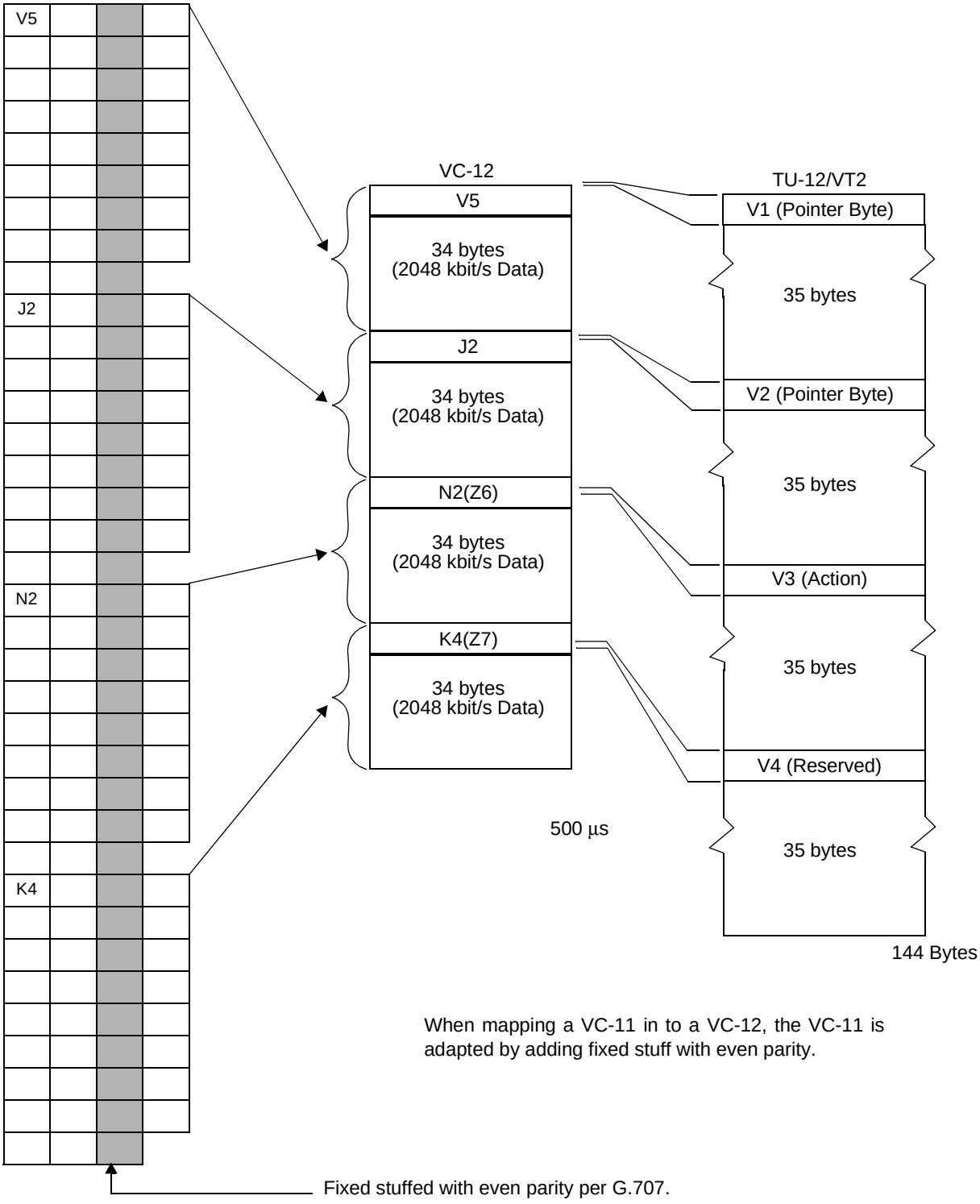


Figure 3. 2048 kbit/s Asynchronous Mapping

Figure 4. VC-11 to VC-12 Cross Mapping



APPLICATION EXAMPLE

The application diagram in Figure 5 below shows a fully configured bidirectional add/drop fiber multiplexer. Using the four-bus capability of the TEMx28, channels may be dropped from either direction with full time slot reuse in both directions. Using only the B Drop and the A Add buses provides add/drop service back to the network source only, and eliminates the block marked “East Terminal” for a terminal configuration.

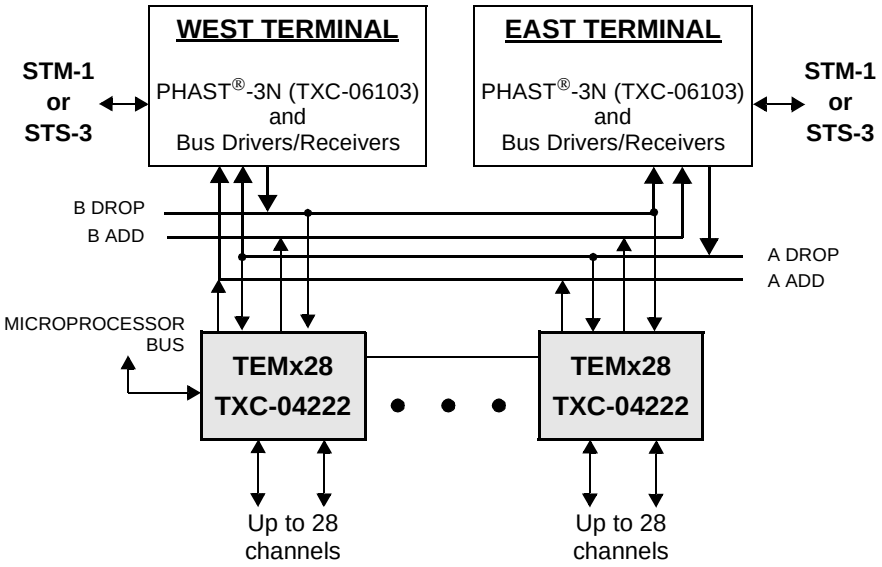


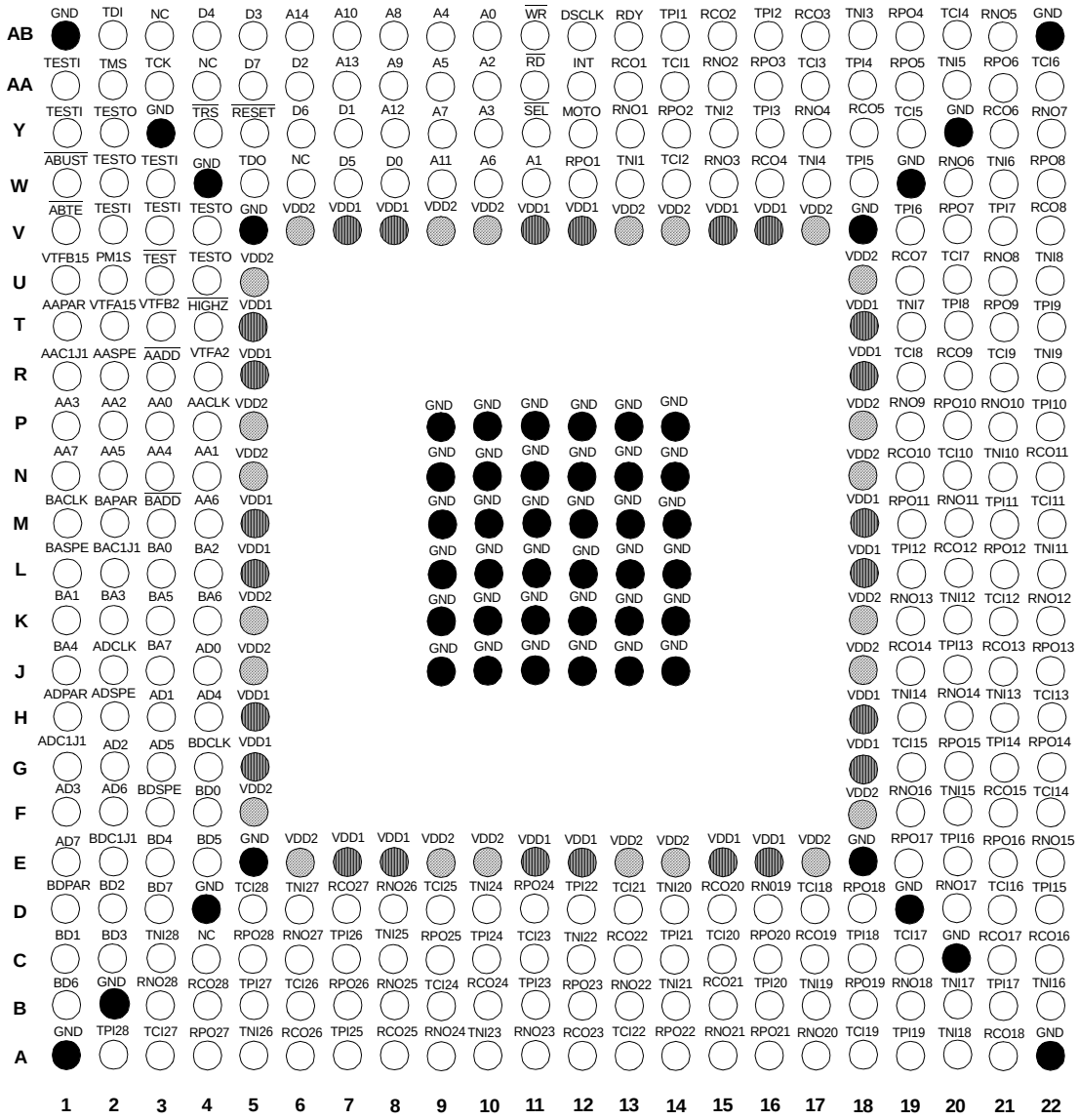
Figure 5. Application Using the TEMx28 TXC-04222

INTEROPERABILITY

The TEMx28 works directly with the following TranSwitch devices:

- QT1F-*Plus* (TXC-03103)
- T1Fx8 (TXC-03108)
- E1Fx8 (TXC-03109)
- QE1F-*Plus* (TXC-03114)
- PHAST®-3N (TXC-06103)
- T3BwP (TXC-06826)

LEAD DIAGRAM



Note: This is the bottom view. The leads are solder balls. See Figure 42 for package information. Some signal Symbols have been abbreviated to fit the space available. The Symbols are shown in full in the Lead Descriptions section.

Figure 6. TEMx28 TXC-04222 376-Lead Plastic Ball Grid Array Package Lead Diagram

LEAD DESCRIPTIONS

POWER SUPPLY, GROUND AND NO CONNECTS

Symbol	Lead No.	I/O/P *	Name/Function
VDD1	E7, E8, E11, E12, E15, E16, G5, G18, H5, H18, L5, L18, M5, M18, R5, R18, T5, T18, V7, V8, V11, V12, V15, V16	P	**VDD1:** +1.8 volt supply voltage, ±5%.
VDD2	E6, E9, E10, E13, E14, E17, F5, F18, J5, J18, K5, K18, N5, N18, P5, P18, U5, U18, V6, V9, V10, V13, V14, V17	P	**VDD2:** +3.3 volt supply voltage, ±5%. This supply voltage should be powered up prior to the 1.8 V (VDD1) supply voltage or at the same time. This supply voltage must not go below VDD1 by more than 0.5 V at any time including power down.
GND	A1, A22, B2, C20, D4, D19, E5, E18, J9 - J14, K9 - K14, L9 - L14, M9 -M14, N9 - N14, P9 - P14, V5, V18, W4, W19, Y3, Y20, AB1, AB22	P	**Ground:** 0 volt reference.
NC	C4, W6, AA4, AB3		**No Connect:** NC leads are not to be connected, not even to another NC lead, but must be left floating. Connection of these leads may impair performance or cause damage to the device.

*Note: I = Input; O = Output; P = Power; T=Tristate

A DROP AND A ADD BUS I/O

Symbol	Lead No.	I/O/P	Type *	Name/Function
ADCLK	J2	I	TTL3V	**A Drop Bus Clock:** This clock operates at 19.44 MHz for STM-1/STS-3 operation. A Drop bus byte-wide data (AD7-AD0), the parity bit (ADPAR), SPE indication (ADSPE), and the C1J1V1 indication (ADC1J1V1) are clocked in on falling edges of this clock. This clock may also be used for add bus timing and deriving the like-named add bus byte-wide data, add and TU/VT indications, and parity bits.
ADPAR	H1	I	TTL3V	**A Drop Bus Parity Bit:** A parity bit input signal representing the odd or even parity calculation for each data byte, SPE, and C1J1V1 signal from the drop bus, or the data byte only.
AD(7-0)	E1, F2, G3, H4, F1, G2, H3, J4	I	TTL3V	**A Drop Bus Data Byte:** Byte-wide data that corresponds to the STM-1/STS-3 signal on the drop bus. The first bit received (dropped) corresponds to bit 7 which is lead E1.

*See Input, Output and Input/Output Parameters section below for Type definitions.

Symbol	Lead No.	I/O/P	Type *	Name/Function
ADSPE	H2	I	TTL3V	**A Drop Bus SPE Indicator:** A signal that is active high for each byte of the STM-1 VC-4 and STS-3/STS-1 SPEs, and low for overhead byte times.
ADC1J1(V1)	G1	I	TTL3V	**A Drop Bus C1J1V1 Indications:** An active high timing signal that carries STM-1/STS-3 frame and SPE information. This signal works in conjunction with the ADSPE signal. The C1 pulse identifies the location of the first C1 byte in the STM-1 and STS-3 signals, when ADSPE signal is low. The J1 pulse identifies the starting location of the J1 byte in the STM-1 VC-4 signal when ADSPE is high. Three J1 pulses identify the starting location for each of the three STS-1 signals in the STS-3 signal. A single V1 pulse identifies the location for the V1/V2 bytes in the TUG-3 within the VC-4. Three V1 pulses identify the location of the V1/V2 bytes within each of the three STS-1s. The V1 pulses may be absent. In which case the mapper will detect the starting location of the multiframe within the H4 byte.
AACLK	P4	I/O(T)	TTL3V/ CMOS3V 8mA	**A Add Bus Clock:** When the add bus timing mode is selected (lead ABUST is low), this input must be provided for add bus timing. This clock operates at 19.44 MHz for STM-1/STS-3 operation. The add bus SPE indication (AASPE), and the C1J1V1 indication (AAC1J1V1) are clocked in on falling edges of this clock. Add bus byte-wide data (AA7-AA0), add indicator (AADD), and the parity bit (AAPAR) are clocked out on rising edges of the clock during the time slots that correspond to the selected TU/VT. When drop bus timing is selected (lead ABUST is high), and lead ABTE is low, this clock, which is derived from the like-named drop bus is an output. When lead ABTE is high in the drop bus timing mode, this lead is disabled.
AAPAR	T1	O(T)	CMOS3V 8mA	**A Add Bus Parity Bit:** An odd or even parity output signal that is calculated over the byte-wide add data. When drop bus timing is selected (lead ABUST is high), and lead ABTE is low, parity may be also calculated for the C1J1V1 and SPE signals. This lead is only active when there is data being added to the add bus.
AA(7-0)	N1, M4, N2, N3, P1, P2, N4, P3	O(T)	CMOS3V 8mA	**A Add Bus Data Byte:** Byte-wide data that corresponds to the selected TU/VT. The first bit transmitted (added) corresponds to bit 7 which is lead N1.
AASPE	R2	I/O(T)	TTL3V/ CMOS3V 8mA	**A Add Bus SPE Indicator:** When the add bus timing mode is selected, this signal must be provided for add bus timing. This signal must be high during each byte of the STM-1/STS-3 payload, and low during Transport Overhead byte times. When drop bus timing is selected (lead ABUST is high), and lead ABTE is low, this signal, which is derived from the like-named drop bus is an output. When lead ABTE is high in the drop bus timing mode, this lead is disabled.

Symbol	Lead No.	I/O/P	Type *	Name/Function
AAC1J1(V1)	R1	I/O(T)	TTL3V/ CMOS3V 8mA	**A Add Bus C1J1V1 Indications:** An active high timing signal that carries STM-1/STS-3 frame and SPE information. This signal works in conjunction with the AASPE signal. The C1 pulse identifies the location of the first C1 byte in the STM-1 and STS-3 signals, when AASPE signal is low. The J1 pulse identifies the starting location of the J1 byte in the STM-1 VC-4 signal when ADSPE is high. Three J1 pulses identify the starting location for each of the three STS-1 signals in the STS-3 signal. A single V1 pulse identifies the starting location for the V1/V2 bytes in the TUG-3 within the VC-4. Three V1 pulses identify the starting location of the V1/V2 bytes within each of the three STS-1s. When drop bus timing is selected (lead ABUST is high), and lead ABTE is low, this signal, which is derived from the like-named drop bus is an output. When lead ABTE is high in the A drop bus timing mode, this lead is disabled.
AADD	R3	O	CMOS3V 8mA	**A Add Bus Add Data Present Indicator:** This normally active low signal is present when output data to the A Add bus is valid. It identifies the location of all of the TU/VT time slots being selected. When control bit ADDI (bit 0, register 03AH) is 1, the indicator is active high instead of active low.

B DROP AND B ADD BUS I/O

Symbol	Lead No.	I/O/P	Type	Name/Function
BDCLK	G4	I	TTL3V	**B Drop Bus Clock:** This clock operates at 19.44 MHz for STM-1/STS-3 operation. A Drop bus byte-wide data (BD7-BD0), the parity bit (BDPAR), SPE indication (BDSPE), and the C1J1V1 indication (BADC1J1V1) are clocked in on falling edges of this clock. This clock may also be used for add bus timing and deriving the like-named add bus byte-wide data, add and TU/VT indications, and parity bits.
BDPAR	D1	I	TTL3V	**B Drop Bus Parity Bit:** A parity bit input signal representing the odd or even parity calculation for each data byte, SPE, and C1J1V1 signal from the drop bus, or the data byte only.
BD(7-0)	D3, B1, E4, E3, C2, D2, C1, F4	I	TTL3V	**B Drop Bus Data Byte:** Byte-wide data that corresponds to the STM-1/STS-3 signal on the drop bus. The first bit received (dropped) corresponds to bit 7 which is lead D3.
BDSPE	F3	I	TTL3V	**B Drop Bus SPE Indicator:** A signal that is active high for each byte of the STM-1 VC-4 and STS-3/STS-1 SPEs, and low for overhead byte times.

Symbol	Lead No.	I/O/P	Type	Name/Function
BDC1J1(V1)	E2	I	TTL3V	**B Drop Bus C1J1V1 Indications:** An active high timing signal that carries STM-1/STS-3 frame and SPE information. This signal works in conjunction with the BDSPE signal. The C1 pulse identifies the location of the first C1 byte in the STM-1 and STS-3 signals, when BDSPE signal is low. The J1 pulse identifies the starting location of the J1 byte in the STM-1 VC-4 signal when BDSPE is high. Three J1 pulses identify the starting location for each of the three STS-1 signals in the STS-3 signal. A single V1 pulse identifies the location for the V1/V2 bytes in the TUG-3 within the VC-4. Three V1 pulses identify the location of the V1/V2 bytes within each of the three STS-1s. The V1 pulses may be absent. In which case the mapper will detect the starting location of the multiframe within the H4 byte.
BACLK	M1	I/O(T)	TTL3V/ CMOS3V 8mA	**B Add Bus Clock:** When the add bus timing mode is selected (lead ABUST is low), this input must be provided for add bus timing. This clock operates at 19.44 MHz for STM-1/STS-3 operation. The add bus SPE indication (BASPE), and the C1J1V1 indication (BAC1J1V1) are clocked in on falling edges of this clock. Add bus byte-wide data (BA7-BA0), add indicator (BADD), and the parity bit (BAPAR) are clocked out on rising edges of the clock during the time slots that correspond to the selected TU/VT. When drop bus timing is selected (lead ABUST is high), and lead ABTE is low, this clock, which is derived from the like-named drop bus is an output. When lead ABTE is high in the drop bus timing mode, this lead is disabled and forced to the high impedance state.
BAPAR	M2	O(T)	CMOS3V 8mA	**B Add Bus Parity Bit:** An odd or even parity output signal that is calculated over the byte-wide add data. When drop bus timing is selected (lead ABUST is high), and lead ABTE is low, parity may be also calculated for the C1J1V1 and SPE signals. This lead is only active when there is data being added to the add bus.
BA(7-0)	J3, K4, K3, J1, K2, L4, K1, L3	O(T)	CMOS3V 8mA	**B Add Bus Data Byte:** Byte-wide data that corresponds to the selected TU/VT. The first bit transmitted (added) corresponds to bit 7 which is lead J3.
BASPE	L1	I/O(T)	TTL3V/ CMOS3V 8mA	**B Add Bus SPE Indicator:** When the add bus timing mode is selected, this signal must be provided for add bus timing. This signal must be high during each byte of the STM-1/STS-3 payload, and low during Transport Overhead byte times. When drop bus timing is selected (lead ABUST is high), and lead ABTE is low, this signal, which is derived from the like-named drop bus is an output. When lead ABTE is high in the drop bus timing mode, this lead is disabled and forced to the high impedance state.

Symbol	Lead No.	I/O/P	Type	Name/Function
BAC1J1(V1)	L2	I/O(T)	TTL3V/ CMOS3V 8mA	**B Add Bus C1J1V1 Indications:** An active high timing signal that carries STM-1/STS-3 frame and SPE information. This signal works in conjunction with the AASPE signal. The C1 pulse identifies the location of the first C1 byte in the STM-1 and STS-3 signals, when AASPE signal is low. The J1 pulse identifies the starting location of the J1 byte in the STM-1 VC-4 signal when ADSPE is high. Three J1 pulses identify the starting location for each of the three STS-1 signals in the STS-3 signal. A single V1 pulse identifies the starting location for the V1/V2 bytes in the TUG-3 within the VC-4. Three V1 pulses identify the starting location of the V1/V2 bytes within each of the three STS-1s. When drop bus timing is selected (lead $\overline{\text{ABUST}}$ is high), and lead $\overline{\text{ABTE}}$ is low, this signal, which is derived from the like-named drop bus is an output. When lead $\overline{\text{ABTE}}$ is high in the B drop bus timing mode, this lead is disabled and forced to the high impedance state.
$\overline{\text{BADD}}$	M3	O	CMOS3V 8mA	**B Add Bus Add Data Present Indicator:** This normally active low signal is present when output data to the A Add bus is valid. It identifies the location of all of the TU/VT time slots being selected. When control bit ADDI (bit 0, register 03AH) is 1, the indicator is active high instead of active low.

CHANNEL n LINE INTERFACE (n = 1, up to 28)

Symbol	Lead No.	I/O/P	Type	Name/Function
RCOn RCLKn RVTCn (n=1-28)	AA13, AB15, AB17, W16, Y18, Y21, U19, V22, R20, N19, N22, L20, J21, J19, F21, C22, C21, A21, C17, D15, B15, C13, A12, B10, A8, A6, D7, B4	O(T)	CMOS3V 4mA	**Receive Channel n Rail, NRZ, TU/VT Output Clock:** A DS1, E1, or VT/TU clock output. Data (Rail or NRZ) is clocked out on positive transitions of this clock when control bit RnCLKI (bit 3, register X+000H) is a 1. When control bit RnCLKI is a 0, data is clocked out on negative transitions of this clock. RCOn is the E1/T1 rail clock (control bits RnLINT1/0 (bits 7/6, register X+006H) are 10). RCLKn is the NRZ clock (control bits RnLINT1/0 are 01). RVTCn is the TU/VT NRZ clock (control bits RnLINT1/0 are 11). This lead is disabled when control bits RnLINT1/0 are 00. When disabled, this lead can be forced to ether a high impedance state (control bit RnOUTL (bit 5, register 006H) is a 0), or to zeros (control bit RnOUTL is a 1). Lead AA13 is RCO1/RCLK1/RVTC1 (Channel 1). **Note:** See Description for control bit RnOUTL for detailed operation.
RPOn RDATn RVTDn (n=1-28)	W12, Y14, AA16, AB19, AA19, AA21, V20, W22, T21, P20, M19, L21, J22, G22, G20, E21, E19, D18, B18, C16, A16, A14, B12, D11, C9, B7, A4, C5	O(T)	CMOS3V 4mA	**Receive Channel n Data Positive Rail, NRZ, TU/VT:** When control bits RnLINT1/0 are set to 10, positive rail E1/T1 data (RPOn) is provided on this lead. When control bit RnLINT1/0 is set to 01, NRZ E1/T1 data (RDATn) is provided on this lead. When control bits RnLINT1/0 are set to 11, VT/TU NRZ data (RVTDn) is provided on this lead. This lead is disabled when control bits RnLINT1/0 are 00. When disabled, this lead can be forced to ether a high impedance state (control bit RnOUTL is a 0), or to zeros (control bit RnOUTL is a 1). Lead W12 is RPO1/RDAT1/RVTD1 (Channel 1). **Note:** See Description for control bit RnOUTL for detailed operation.

Symbol	Lead No.	I/O/P	Type	Name/Function
RNOn RVTFn (n=1-28)	Y13, AA15, W15, Y17, AB21, W20, Y22, U21, P19, P21, M20, K22, K19, H20, E22, F19, D20, B19, D16, A17, A15, B13, A11, A9, B8, D8, C6, B3	O(T)	CMOS3V 4mA	**Receive Channel n Data Negative Rail, TU/VT Framing Pulse:** When control bits RnLINT1/0 are set to 10, negative rail E1/T1 data (RNOn) is provided on this lead. When control bits RnLINT1/0 are set to 11, a VT/TU framing pulse (RVTFn) is provided on this lead. This lead is disabled when control bits RnLINT1/0 are 00. When disabled, this lead can be forced to ether a high impedance state (control bit RnOUTL is a 0), or to zeros (control bit RnOUTL is a 1). Lead Y13 is RNO1/RVTF1 (Channel 1). **Note:** See Description for control bit RnOUTL for detailed operation. Output will be forced low during normal operation while in NRZ mode.
TCIn TCLKn TVTCn (n=1-28)	AA14, W14, AA17, AB20, Y19, AA22, U20, R19, R21, N20, M22, K21, H22, F22, G19, D21, C19, D17, A18, C15, D13, A13, C11, B9, D9, B6, A3, D5	I/O(T)	TTL3V/ CMOS3V 4mA	**Transmit Channel n Rail, NRZ Input Clock, VT/TU Output Clock:** A DS1 or E1 clock input when the Rail or NRZ interface is selected or a VT/TU clock output when the VT/TU interface is selected. TCIn is the E1/T1 rail clock (control bits TnLINT1/0 (bits 7/6, register X+002H) are 10). TCLKn is the E1/T1 NRZ clock (control bits TnLINT1/0 are 01). TVTCn is the VT/TU NRZ clock output (control bits TnLINT1/0 are 11). Rail (TPIn/TNIn), NRZ (TDATn/$\overline{\text{TLOS}}$n) or VT/TU NRZ data (TVTDn) is clocked in on negative transitions of this clock when control bit TnCLKI (bit 3, register X+002H) is a 0. When control bit TnCLKI is a 1, data is clocked in on positive transitions of this clock. Lead AA14 is TCI1/TCLK1/TVTC1 (Channel 1).
TPIn TDATn TVTDn (n=1-28)	AB14, AB16, Y16, AA18, W18, V19, V21, T20, T22, P22, M21, L19, J20, G21, D22, E20, B21, C18, A19, B16, C14, D12, B11, C10, A7, C7, B5, A2	I	TTL3V	**Transmit Channel n Data Positive Rail, NRZ, or VT/TU:** When control bits TnLINT1/0 are set to 10, positive rail E1/T1 data (TPIn) is clocked in this lead. When control bit TnLINT1/0 are set to 01, NRZ E1/T1 data (TDATn) is clocked in on this lead. When control bits TnLINT1/0 are set to 11, VT/TU NRZ data (TVTDn) is clocked in on this lead. Lead AB14 is TPI1/TDAT1/TVTD1 (Channel 1).
TNIn/ $\overline{\text{TLOS}}$n (n=1-28)	W13, Y15, AB18, W17, AA20, W21, T19, U22, R22, N21, L22, K20, H21, H19, F20, B22, B20, A20, B17, D14, B14, C12, A10, D10, C8, A5, D6, C3	I	TTL3V	**Transmit Channel n Data Negative Rail, External Loss Of Signal, Coding Violations:** When control bits TnLINT1/0 are set to 10, negative rail E1/T1 data (TNIn) is clocked in on this lead. When control bits TnLINT1/0 are set to 01, an external loss of signal (when control bit EXnLOS (bit 1, register X+003H) is a 1) is clocked in on this lead. When control bit EXnLOS is a 0, external coding violations can be clocked in on this lead. Lead W13 is TNI1/$\overline{\text{TLOS1}}$.

CONTROLS, EXTERNAL CLOCK, FRAMING PULSES AND TEST LEADS

Symbol	Lead No.	I/O/P	Type	Name/Function
$\overline{\text{TEST}}$	U3	I	TTL3Vp	**TranSwitch Test Lead:** This lead is used for TranSwitch testing and must remain an active high for the mapper to function. This lead is pulled high by an internal pull-up to VDD2. It must be left floating or held high.
DSCLK	AB12	I	TTL3V	**Desynchronizer Reference Clock:** This clock is used for desynchronizer operation and for other internal functions, such as generating a receive AIS signal. The clock frequency must be 68.68 MHz (+/- 30 ppm over life) and the clock duty cycle must be (50 +/- 10)%.
$\overline{\text{RESET}}$	Y5	I	TTL3Vp	**Hardware Reset:** When an active low pulse is applied to this lead for a minimum duration of 150 nanoseconds after power is applied, this pulse clears all performance counters and alarms, resets the control bits, and initializes the internal FIFOs. This action takes approximately 4 microseconds. Status bit RESETD (bit 0, register 059H) is set to 1 when the reset is complete. This lead is pulled high by an internal pull-up to VDD2.
$\overline{\text{HIGHZ}}$	T4	I	TTL3Vp	**High Impedance Select:** A low forces all output leads, except the boundary scan lead TDO, to the high impedance state for testing purposes. This lead is pulled high by an internal pull-up to VDD2.
PM1S	U2	I	TTL3V	**One Second Performance Clock Input.** This clock input is used for the one second shadow counters, and PM (Performance Monitoring)/FM (Fault Monitoring) alarm registers. This clock should be a 1.0 Hz +/- 32 ppm clock, with a minimum 30 ns high and low time. When this lead is held low, the PM/FM alarm and shadow counter features are disabled. This clock is required to write to the Bit Leak Registers in X+017H and X+018H.
$\overline{\text{ABTE}}$	V1	I	TTL3Vp	**Add Bus Timing Output Signals enable:** An active low enables the like-named drop bus clock, C1J1V1 and SPE signals to be provided as output signals on the add bus when the drop bus timing mode is selected (lead $\overline{\text{ABUST}}$ is high). When high, the clock, C1J1V1, and SPE signals are disabled as outputs on the add buses when the drop bus timing mode is selected. This lead is pulled high by an internal pull-up to VDD2.
VTFA15	T2	O	CMOS3V 4 mA	**Transmit VT1.5 Framing Pulse.** Positive one clock cycle pulse that is used when the VT/TU line interface is selected for a channel. The pulse determines the start of the VT1.5/TU-11 multiframe in the transmit direction for Add Bus A. The pulse occurs even when no VT/TU line interface is selected (as long as Add Bus A is active). The pulse is clocked out on the rising edge of the TVTCn clock when control bit TnCLKI (bit 3, register X+002H) is a 0.
VTFA2	R4	O	CMOS3V 4 mA	**Transmit VT2 Framing Pulse.** Positive one clock cycle pulse that is used when the VT/TU line interface is selected for a channel. The pulse determines the start of the VT2/TU-12 multiframe in the transmit direction for Add Bus A. The pulse occurs even when no VT/TU line interface is selected (as long as Add Bus A is active). The pulse is clocked out on the rising edge of the TVTCn clock when control bit TnCLKI (bit 3, register X+002H) is a 0.

Symbol	Lead No.	I/O/P	Type	Name/Function
VTFB15	U1	O	CMOS3V 4 mA	**Transmit VT1.5 Framing Pulse.** Positive one clock cycle pulse that is used when the VT/TU line interface is selected for a channel. The pulse determines the start of the VT1.5/TU-11 multiframe in the transmit direction for Add Bus B. The pulse occurs even when no VT/TU line interface is selected (as long as Add Bus B is active). The pulse is clocked out on the rising edge of the TVTCn clock when control bit TnCLKI (bit 3, register X+002H) is a 0.
VTFB2	T3	O	CMOS3V 4 mA	**Transmit VT2 Framing Pulse.** Positive one clock cycle pulse that is used when the VT/TU line interface is selected for a channel. The pulse determines the start of the VT2/TU-12 multiframes in the transmit direction for Add Bus B. The pulse occurs even when no VT/TU line interface is selected (as long as Add Bus B is active). The pulse is clocked out on the rising edge of the TVTCn clock when control bit TnCLKI (bit 3, register X+002H) is a 0.
$\overline{\text{ABUST}}$	W1	I	TTL3Vp	**Add Bus Timing Select:** A low selects the add bus timing mode. In this timing mode, the drop and add bus timing signals are independent of each other. A high selects the drop bus timing mode. In this timing mode, the add signals (Add bus clock, SPE and C1J1V1 signals) are derived from the like-named drop bus. Note: The add bus timing mode must be selected when any of the channels are assigned to a VT/TU interface. In addition, the J1 and V1 pulses must be fixed regarding their locations. This restriction is required, because the TEMx28 provides the downstream circuitry with timing information. This lead is pulled high by an internal pull-up to VDD2.

MICROPROCESSOR BUS INTERFACE SELECTION

Symbol	Lead No.	I/O/P	Type	Name/Function
MOTO	Y12	I	TTL3V	**Motorola Mode**: The following table lists the bus selection options. MOTO — Action L — Intel bus interface H — Motorola bus interface

MICROPROCESSOR BUS INTERFACE - SPLIT BUS FOR MOTOROLA (M) OR INTEL (I)

Symbol	Lead No.	I/O/P	Type	Name/Function
A(14-0)	AB6, AA7, Y8, W9, AB7, AA8, AB8, Y9, W10, AA9, AB9, Y10, AA10, W11, AB10	I	TTL3V	**Address Bus (Motorola/Intel Buses):** These address line inputs are used for accessing memory map locations for a read/write cycle. A14 (lead AB6) is the most significant bit.

Symbol	Lead No.	I/O/P	Type	Name/Function
D(7-0)	AA5, Y6, W7, AB4, AB5, AA6, Y7, W8	I/O(T)	TTL3V/ CMOS3V 8mA	**Data Bus (Motorola/Intel Buses):** Bidirectional data lines used for transferring data to or from a memory map location. D7 (lead AA5) is the most significant bit.
$\overline{SEL}$	Y11	I	TTL3V	**Select:** An active low enables data transfers between the microprocessor and the memory map location during a read/write cycle.
$\overline{RD}$ / RD/$\overline{WR}$	AA11	I	TTL3V	**Read (I mode) or Read/Write (M mode):** Intel Mode - An active low signal generated by the microprocessor for reading memory map locations. Motorola Mode - An active high signal generated by the microprocessor for reading the memory map locations. An active low signal is used to write to memory map locations.
$\overline{WR}$ / $\overline{LDS}$	AB11	I	TTL3V	**Write (I mode) or Device Select (M mode):** Intel Mode - An active low signal generated by the microprocessor for writing to memory map locations. Motorola Mode - The $\overline{SEL}$ and $\overline{LDS}$ inputs are logically OR-gated inside the device, generating an internal active low select signal ($\overline{CS}$) that is similar to $\overline{SEL}$. This internal signal is used to enable data transfer. This lead can be used for the interface with the Motorola 68302 microprocessor. If this lead is not used, it should be tied to ground.
RDY / $\overline{DTACK}$	AB13	O(T)	CMOS3V 8mA	**Ready (I mode) or Data Transfer Acknowledge (M mode):** Intel Mode - A high is an acknowledgment from the addressed memory map location that the transfer can be completed. A low indicates that the Mapper cannot complete the transfer cycle, and that microprocessor wait states must be generated. Motorola Mode - During a read bus cycle, a low signal indicates that the information on the data bus is valid. During a write bus cycle, a low signal acknowledges the acceptance of data.
INT/ $\overline{IRQ}$	AA12	O	CMOS3V 8mA	**Interrupt:** A high on this output lead signals an interrupt request INT to the microprocessor, as required for Intel compatibility microprocessors. For Motorola operation, a low signals an interrupt request $\overline{IRQ}$ to the microprocessor. Please note: it will take approximately 4 microseconds before the interrupt is asserted after the last enabling mask bit is set to 1. The interrupt is asserted immediately when the gating event is the latched alarm.

BOUNDARY SCAN INTERFACE

Symbol	Lead No.	I/O/P	Type	Name/Function
TCK	AA3	I	TTL3V	**IEEE 1149.1 Test Port Serial Scan Clock:** This signal is used to shift data into TDI on the rising edge, and out of TDO on the falling edge. The maximum clock frequency is 10 MHz.

Symbol	Lead No.	I/O/P	Type	Name/Function
TMS	AA2	I	TTL3Vp	**IEEE 1149.1 Test Port Mode Select:** TMS is sampled on the rising edge of TCK, and is used to place the Test Access Port controller into various states as defined in IEEE 1149.1. This lead is set high internally by an internal pull-up to VDD2 for normal operation.
TDI	AB2	I	TTL3Vp	**IEEE 1149.1 Test Port Serial Scan Data In:** Serial test instructions and data are clocked into this lead on the rising edge of TCK. This input has an internal pull-up to VDD2.
TDO	W5	O(T)	CMOS3V 4mA	**IEEE 1149.1 Test Port Serial Scan Data Out:** Serial test instructions and data are clocked out of this lead on the falling edge of TCK. When inactive, this 3-state output will be put into its high impedance state.
$\overline{\text{TRS}}$	Y4	I	TTL3Vp	**IEEE 1149.1 Test Port Reset Lead:** This lead will asynchronously reset the Test Access Port (TAP) controller. This lead must be held low, asserted low or pulsed low (for a minimum duration of 20 ns) to reset the TAP controller on TEMx28 power-up. This input has an internal pull-up to VDD2. Failure to perform a TAP controller reset may cause the TAP controller to take control of some of the TEMx28 output leads.

TRANSWITCH TEST LEADS

Symbol	Lead No.	I/O/P	Type	Name/Function
TESTI	V2, V3, W3, Y1, AA1	I	TTL3Vd	**TranSwitch Test Input Leads:** For TranSwitch testing purposes only. These leads have an internal pull down to GND and should be held low.
TESTO	U4, V4, W2, Y2	O(T)	CMOS3V 4 mA	**TranSwitch Test Output Leads:** For TranSwitch testing purposes only. These leads should be left open (floating).

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Core Supply Voltage, +1.8V nominal	V_{DD1}	-0.3	2.1	V	Notes 1, 4
I/O Supply Voltage, +3.3V nominal	V_{DD2}	-0.3	3.9	V	Notes 1, 4
DC input voltage	VIN	-0.5	5.5	V	Notes 1, 4
Storage temperature range	T_S	-55	150	°C	Note 1
Ambient operating temperature	T_A	-40	85	°C	0 ft/min. linear airflow
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative humidity, during assembly	RH	30	60	%	Note 2
Relative humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD	absolute value 2000		V	Note 3
Latch-up	LU				Meets JEDEC STD-78

Notes:

1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.
3. Test method for ESD per MIL-STD-883E, Method 3015.7.
4. Device core is 1.8V only.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance - junction to ambient		22		^{o}C/W	0 ft/min linear airflow

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD2}	3.15	3.3	3.45	V	
I_{DD2}		36	48	mA	See Notes 1 and 2
P_{DD2}		119	166	mW	See Notes 1 and 2
V_{DD1}	1.71	1.8	1.89	V	
I_{DD1}		262	336	mA	See Notes 1 and 2
P_{DD1}		472	635	mW	See Notes 1 and 2

Notes:

1. Typical values are based on measurements made with nominal voltages at 25° C. Maximum values are based on measurements made at maximum voltages at 85° C.
2. All 28 channels are configured as E1 and are being added and dropped in Dual Protection Ring Mode.

INPUT, OUTPUT AND INPUT/OUTPUT PARAMETERS

INPUT PARAMETERS FOR TTL3V (5 VOLT TOLERANT)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.3		5.5	V	$3.15 \leq V_{DD2} \leq 3.45$
V_{IL}			1.0	V	$3.15 \leq V_{DD2} \leq 3.45$
Input leakage current		±10 nA	±1 µA	µA	$V_{DD2} = 3.45$
Input capacitance		3.1		pF	

INPUT PARAMETERS FOR TTL3Vp (5 VOLT TOLERANT, PULL-UP RESISTOR)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.3			V	$3.15 \leq V_{DD2} \leq 3.45$
V_{IL}			1.0	V	$3.15 \leq V_{DD2} \leq 3.45$
Input current		±10 nA	±1 µA		$V_I = V_{DD2}$
Input leakage current	25		100	µA	V_{DD2} =3.45; Input = 0 volts
Input capacitance		3.1		pF	

INPUT PARAMETERS FOR TTL3Vd (5 VOLT TOLERANT, PULL-DOWN RESISTOR)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.3			V	$3.15 \leq V_{DD2} \leq 3.45$
V_{IL}			1.0	V	$3.15 \leq V_{DD2} \leq 3.45$
Input current		-10 nA	-1 µA		$V_I = 0V$
Input leakage current	28		100	µA	V_{DD2} = 3.45; Input = 3.45 volts
Input capacitance		3.1		pF	

OUTPUT PARAMETERS FOR CMOS3V 4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	V_{DD2} = 3.15; I_{OH} = -4.0
V_{OL}			0.4	V	V_{DD2} = 3.15; I_{OL} = 4.0
I_{OL}	4.4		8.5	mA	V_{OL}=0.4 V
I_{OH}	-6.4		-20	mA	V_{OH}=2.4 V
t_{RISE}			10	ns	C_{LOAD} = 15 pF
t_{FALL}			10	ns	C_{LOAD} = 15 pF
Leakage tristate		±10 nA	±1 µA		0 to 3 V input
Output capacitance		3.1		pF	

OUTPUT PARAMETERS FOR CMOS3V 8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
Output capacitance		7.5		pF	
V_{OH}	2.4			V	V_{DD2} = 3.15; I_{OH} = -8.0
V_{OL}			0.4	V	V_{DD2} = 3.15; I_{OL} = 8.0
I_{OL}	8.8		17	mA	
I_{OH}	-12.8		-40	mA	
t_{RISE}					
t_{FALL}					
Leakage tristate		±10 nA	±1 µA		0 to 3 V input

INPUT/OUTPUT PARAMETERS FOR TTL3VP INPUT AND CMOS3V OUTPUT 4mA (5 VOLT TOLERANT Input)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.3		5.5	V	$3.15 \leq V_{DD2} \leq 3.45$
V_{IL}	-0.5		1.0	V	$3.15 \leq V_{DD2} \leq 3.45$
Input leakage current		±10 nA	±1 µA		0 to 3.3 V input
Input capacitance		3.1		pF	
V_{OH}	2.4			V	V_{DD2} = 3.15; I_{OH} = -4.0
V_{OL}			0.4	V	V_{DD2} = 3.15; I_{OL} = 4.0
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}			10	ns	C_{LOAD} = 25 pF
t_{FALL}			5	ns	C_{LOAD} = 25 pF

INPUT/OUTPUT PARAMETERS FOR TTL3V INPUT AND CMOS3V OUTPUT 8mA (5 VOLT TOLERANT Input)

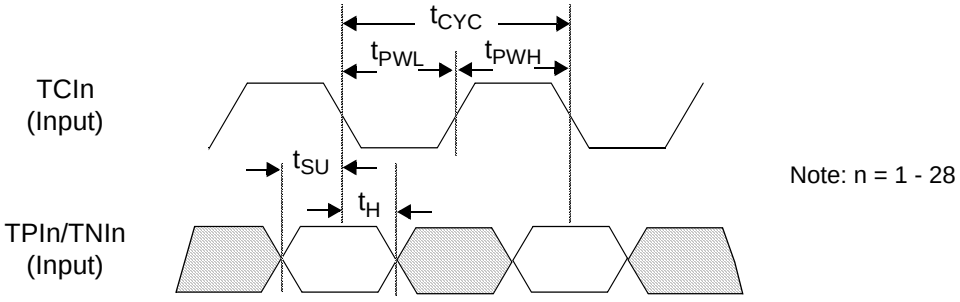
Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.3			V	$3.15 \leq V_{DD2} \leq 3.45$
V_{IL}			1.0	V	$3.15 \leq V_{DD2} \leq 3.45$
Input leakage current		±10 nA	±1 µA		0 to 3.3 V input; see Note 1.
Input capacitance		3.1		pF	
V_{OH}	2.4			V	V_{DD2} = 3.15; I_{OH} = -8.0
V_{OL}			0.4	V	V_{DD2} = 3.15; I_{OL} = 8.0
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	
t_{RISE}			10	ns	C_{LOAD} = 25 pF
t_{FALL}			5	ns	C_{LOAD} = 25 pF

Note: 1. The leakage current is from V_{DD2}. It is most pronounced at -40 ^{O}C.

TIMING CHARACTERISTICS

Detailed timing diagrams for the TEMx28 device are illustrated in the following Figures with values of the timing intervals tabulated below the waveform diagrams. The tristate condition of a signal waveform is shown as mid-way between high and low. The timing parameters are measured at voltage levels of $(V_{IH} + V_{IL})/2$ for input signals or $(V_{OH} + V_{OL})/2$ for output signals, unless otherwise indicated. Where a waveform diagram describes both A and B bus signals, their symbols are combined in labeling the waveform (e.g., A/BADD for AADD and BADD).

Figure 7. Channels 1 - 28 DS1/E1 Transmit Rail Interface Timing



Notes:

1. TCIn is shown for TnCLKI = 0, where data is clocked in on falling edges for channel n. Data is clocked in on rising edges when TnCLKI =1.

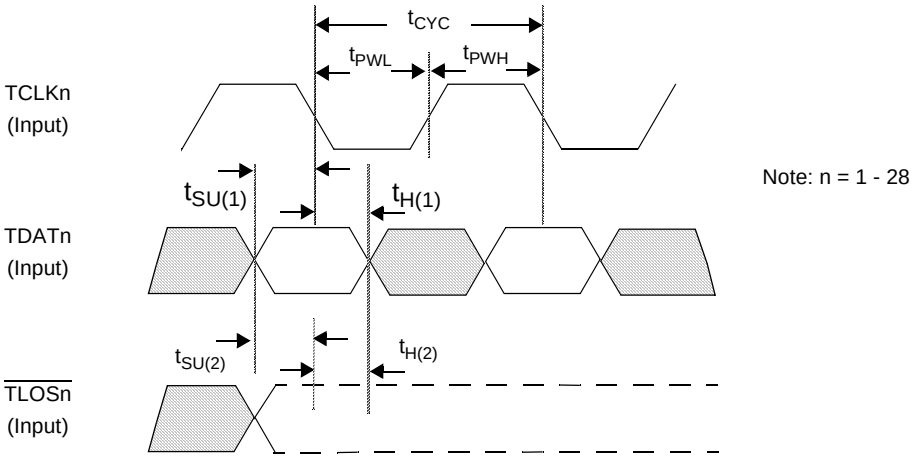
DS1 Interface

Parameter	Symbol	Min	Typ	Max	Unit
TCIn Clock period	t_{CYC}	580.0	647.7		ns
TCIn clock low time	t_{PWL}	280			ns
TCIn clock high time	t_{PWH}	280			ns
TPIn/TNIn data setup time before TCIn↓	t_{SU}	15			ns
TPIn/TNIn data hold time after TCIn↓	t_H	2.0			ns

E1 Interface

Parameter	Symbol	Min	Typ	Max	Unit
TCIn Clock period	t_{CYC}	435.0	488.28		ns
TCIn clock low time	t_{PWL}	150			ns
TCIn clock high time	t_{PWH}	150			ns
TPIn/TNIn data setup time before TCIn↓	t_{SU}	15			ns
TPIn/TNIn data hold time after TCIn↓	t_H	2.0			ns

Figure 8. Channels 1 - 28 DS1/E1 Transmit NRZ Interface Timing



Notes:

1. TCLKn is shown for TnCLKI = 0, where data is clocked in on falling edges for channel n. Data is clocked in on rising edges when TnCLKI =1.
2. The Negative Rail lead may be used to input an external loss of signal indication when control bit EXnLOS = 1. The loss-of-signal indication must be present for a minimum of 8 TCLKn cycles. When control bit EXnLOS = 0, external coding violations may be clocked in. When control bit EXnLOSP = 0, the external loss-of-signal. Code violations are counted when $\overline{\text{TLOSn}}$ is high and the TCLKn edge occurs per the TnCLKI selection (see Note 1 above).

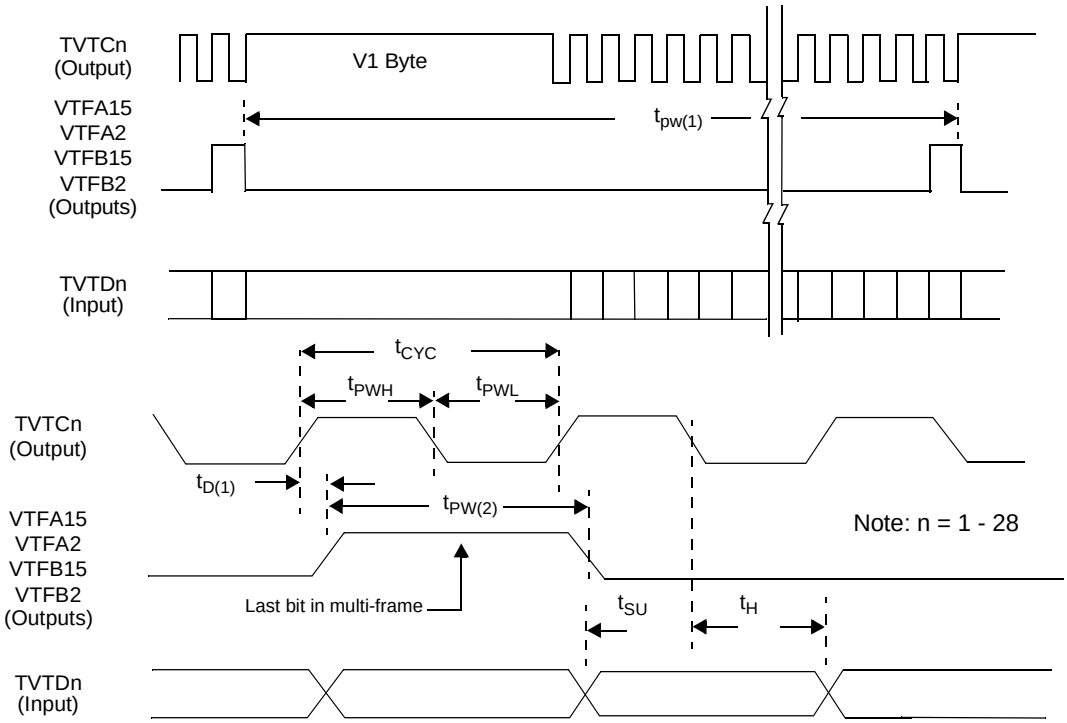
DS1 Interface

Parameter	Symbol	Min	Typ	Max	Unit
TCLKn clock period	t_{CYC}	580.0	647.7		ns
TCLKn clock low time	t_{PWL}	280			ns
TCLKn clock high time	t_{PWH}	280			ns
TDATn data setup time before TCLKn↓	$t_{SU(1)}$	15			ns
TDATn data hold time after TCLKn↓	$t_{H(1)}$	2.0			ns
$\overline{\text{TLOSn}}$ data setup time before TCLKn↓	$t_{SU(2)}$	15			ns
$\overline{\text{TLOSn}}$ data hold time after TCLKn↓	$t_{H(2)}$	2.0			ns

E1 Interface

Parameter	Symbol	Min	Typ	Max	Unit
TCLKn clock period	t_{CYC}	435.0	488.28		ns
TCLkn clock low time	t_{PWL}	150			ns
TCLKn clock high time	t_{PWH}	150			ns
TDATn data setup time before TCLKn↓	$t_{SU(1)}$	15			ns
TDATn data hold time after TCLKn↓	$t_{H(1)}$	2.0			ns
$\overline{\text{TLOSn}}$ data setup time before TCLKn↓	$t_{SU(2)}$	15			ns
$\overline{\text{TLOSn}}$ data hold time after TCLKn↓	$t_{H(2)}$	2.0			ns

Figure 9. Channels 1 - 28 Transmit VT/TU Interface Timing -Gapped Pointer Bytes



Notes:- TVTCn is shown for TnCLKI =0, data with falling edge & Frame pulse with rising edge.
- Clock gaps are present during the time of pointer bytes V1-V4. When TnCLKI = 1, timing is similar to Figure 10.

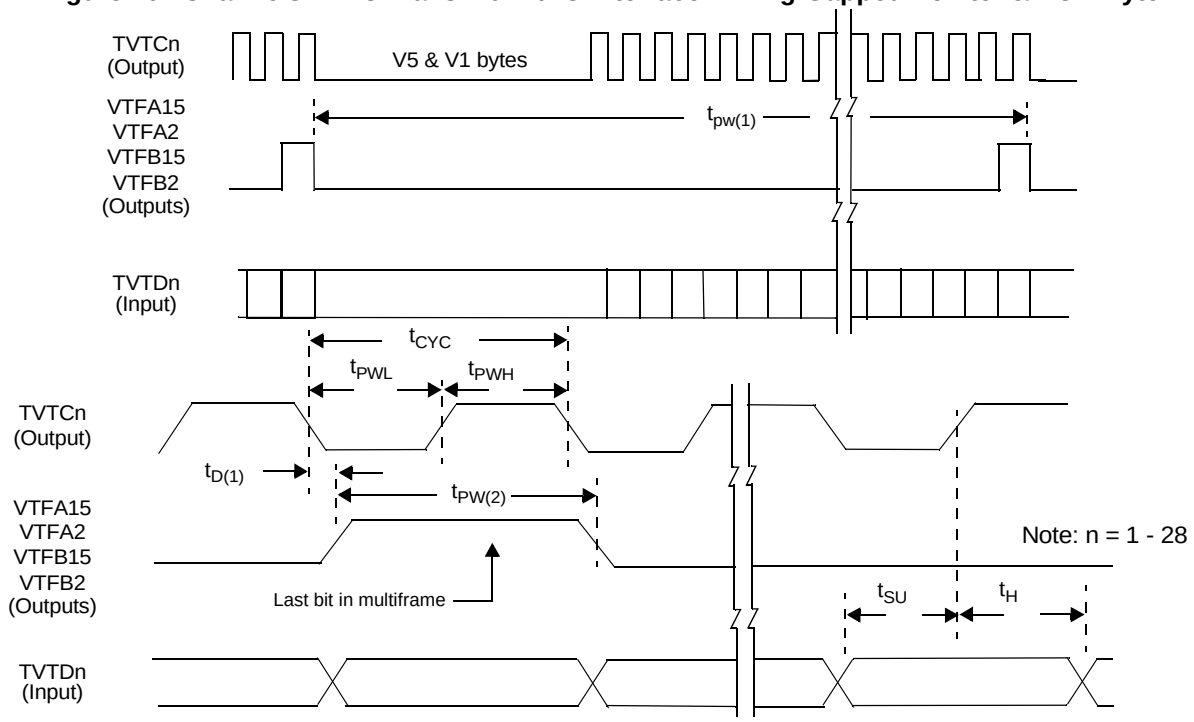
VT 1.5 INTERFACE

Parameter	Symbol	Min	Typ	Max	Unit
TVTCn clock period	t_{CYC}	565.84		5401.20	ns
TVTCn clock low time	t_{PWL}	257.20		5144.0	ns
TVTCn clock high time	t_{PWH}	257.20		5144.0	ns
TVTCn Clock frequency (nominal)			1.664		MHz
TVTDn data setup time before TVTCn↓	t_{SU}	30			ns
TVTDn data hold time after TVTCn↓	t_H	2.0			ns
VTFA/B15 delay from TVTCn↑	$t_{D(1)}$	45		51	ns
Multiframe Time	$t_{PW(1)}$	500		500	µs
VTFA/B15 pulse width	$t_{PW(2)}$	565.84		875.0	ns

VT 2 INTERFACE

Parameter	Symbol	Min	Typ	Max	Unit
TVTCn clock period	t_{CYC}	411.52		4166.64	ns
TVTCn clock low time	t_{PWL}	205.76		3960.88	ns
TVTCn clock high time	t_{PWH}	205.76		3960.88	ns
TVTCn clock frequency (nominal)			2.240		MHz
TVTDn data setup time before TVTCn↓	t_{SU}	30			ns
TVTDn data hold time after TVTCn↓	t_H	2.0			ns
VTFA/B2 delay from TVTCn↑	$t_{D(1)}$	45		51	ns
Multiframe Time	$t_{PW(1)}$	500		500	µs
VTFA/B2 pulse width	$t_{PW(2)}$	462.96		772	ns

Figure 10. Channels 1 - 28 Transmit VT/TU Interface Timing-Gapped Pointer & POH Byte



Notes: - TVTCn is shown for TnCLKI = 1, data with rising edge & Frame pulse with falling edge.
- Clock gaps are present during the time of pointer bytes (V1-V4) and the overhead bytes (V5, J2, N2/Z6, K4/Z7), and may not be contiguous. When TnCLKI = 0, timing is similar to Figure 9.

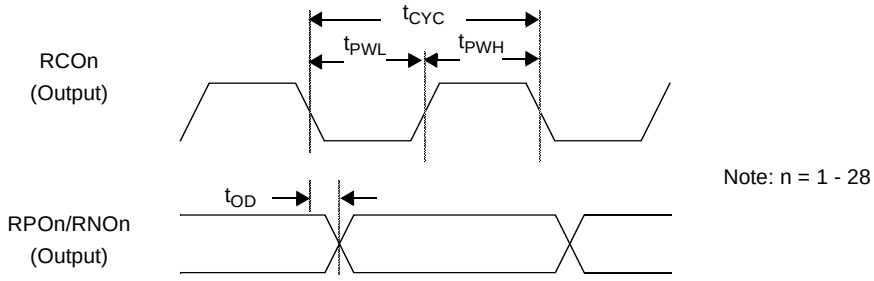
VT 1.5 INTERFACE

Parameter	Symbol	Min	Typ	Max	Unit
TVTCn clock period	t_{CYC}	565.84		9927.92	ns
TVTCn clock low time	t_{PWL}	257.20		9670.72	ns
TVTCn clock high time	t_{PWH}	257.20		9670.72	ns
TVTCn clock frequency (nominal)			1.600		MHz
TVTDn data setup time before TVTCn↑	t_{SU}	30			ns
TVTDn data hold time after TVTCn↑	t_{H}	2.0			ns
VTFA/B15 delay from TVTCn↓	$t_{SU(2)}$	45		51	ns
Multiframe Time	$t_{PW(1)}$	500		500	µs
VTFA/B15 pulse width	$t_{PW(2)}$	565.84		875.0	ns

VT 2 INTERFACE

Parameter	Symbol	Min	Typ	Max	Unit
TVTCn clock period	t_{CYC}	411.52		7561.68	ns
TVTCn clock low time	t_{PWL}	205.76		7355.92	ns
TVTCn clock high time	t_{PWH}	205.76		7355.92	ns
TVTCn clock frequency (nominal)			2.176		MHz
TVTDn data setup time before TVTCn↑	t_{SU}	30			ns
TVTDn data hold time after TVTCn↑	t_{H}	2.0			ns
VTFA/B2 delay from TVTCn↓	$t_{SU(2)}$	45		51	ns
Multiframe Time	$t_{PW(1)}$	500		500	µs
VTFA/B2 pulse width	$t_{PW(2)}$	462.96		772	ns

Figure 11. Channels 1 - 28 DS1/E1 Receive Rail Timing



Note: RCOn is shown for RnCLKI=0, where data is clocked out on falling edges. Data is clocked out on rising edges when RnCLKI=1.

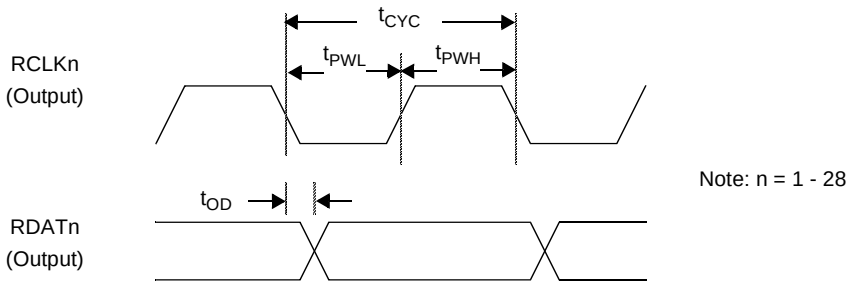
DS1 Interface

Parameter	Symbol	Min	Typ	Max	Unit
RCOn clock period	t_{CYC}	640		656	ns
RCOn clock low time	t_{PWL}	320		335	ns
RCOn clock high time	t_{PWH}	320		321	ns
RPOn/RNOn data delay after RCOn↓	t_{OD}	-5.0		5.0	ns

E1 Interface

Parameter	Symbol	Min	Typ	Max	Unit
RCOn clock period	t_{CYC}	480		498	ns
RCOn clock low time	t_{PWL}	233		248	ns
RCOn clock high time	t_{PWH}	247		248	ns
RPOn/RNOn data delay after RCOn↓	t_{OD}	-5.0		5.0	ns

Figure 12. Channels 1 - 28 DS1/E1 Receive NRZ Timing



Note: RCOn is shown for RnCLKI=0, where data is clocked out on falling edges. Data is clocked out on rising edges when RnCLKI=1.

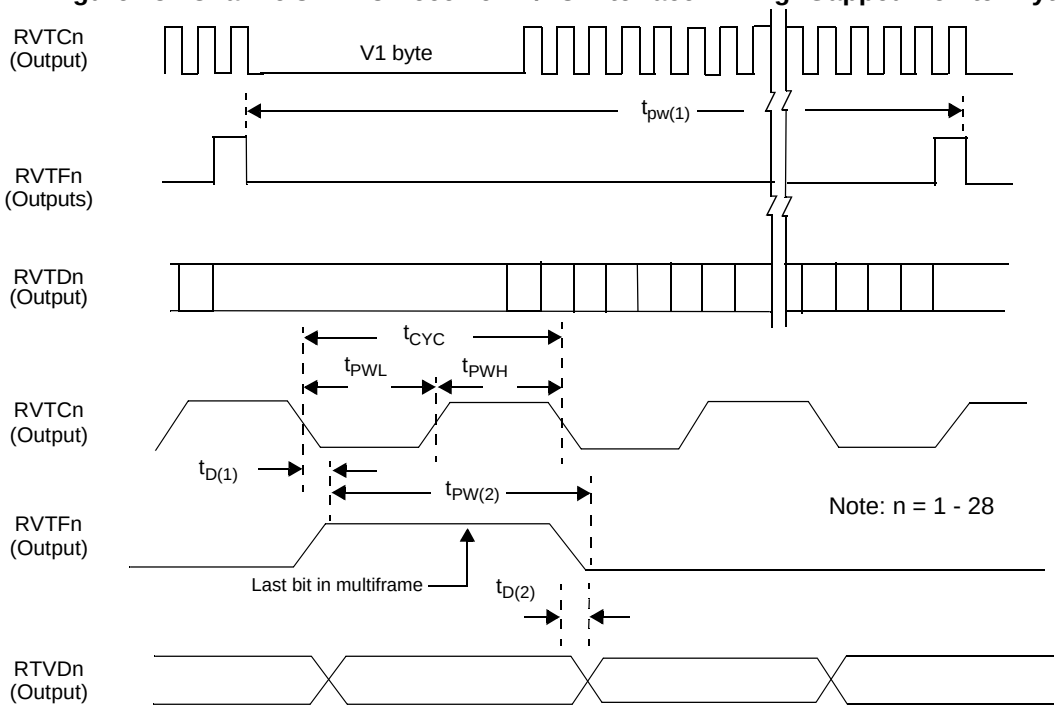
DS1 Interface

Parameter	Symbol	Min	Typ	Max	Unit
RCLKn clock period	t_{CYC}	637		658	ns
RCLKn clock low time	t_{PWL}	320		335	ns
RCLKn clock high time	t_{PWH}	318		321	ns
RDATn data delay after RCLKn↓	t_{OD}	-5.0		5.0	ns

E1 Interface

Parameter	Symbol	Min	Typ	Max	Unit
RCLKn clock period	t_{CYC}	480		498	ns
RCLKn clock low time	t_{PWL}	233		248	ns
RCLKn clock high time	t_{PWH}	247		248	ns
RDATn data delay after RCLKn↓	t_{OD}	-5.0		5.0	ns

Figure 13. Channels 1 - 28 Receive VT/TU Interface Timing -Gapped Pointer Bytes



Notes: - RVTCn is shown for RnCLKI = 0, data & Frame pulse with falling edge.
- Clock gaps are present during the time of pointer bytes V1-V4. When RnCLKI = 1, timing is similar to Figure 14.

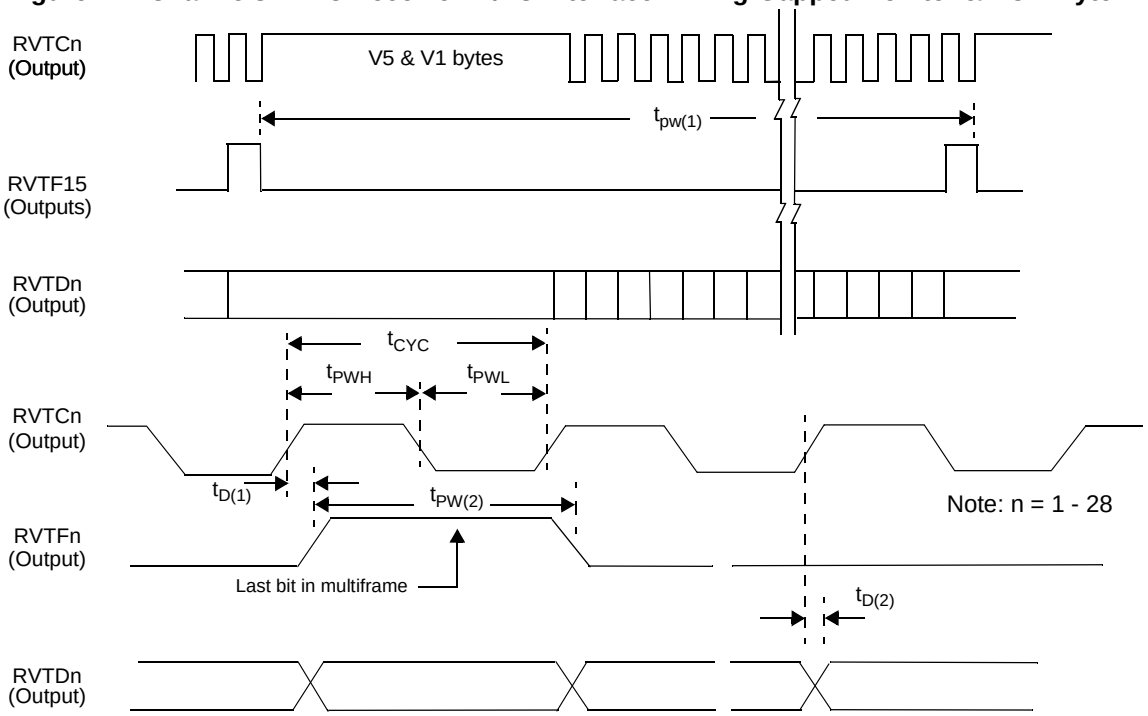
VT 1.5 INTERFACE

Parameter	Symbol	Min	Typ	Max	Unit
RVTCn clock period	t_{CYC}	553.3		5080.0	ns
RVTCn clock low time	t_{PWL}	291.2		4804.0	ns
RVTCn clock high time	t_{PWH}	262.1		276.6	ns
RVTCn clock frequency (nominal)			1.664		MHz
RVTFn delay after RVTCn↓	$t_{D(1)}$	13.1		14.5	ns
RVTDn delay after RVTCn↓	$t_{D(2)}$	14.0		14.5	ns
Multiframe Time	$t_{PW(1)}$	500		500	µs
RVTFn pulse width	$t_{PW(2)}$	567.8		873	ns

VT 2 INTERFACE

Parameter	Symbol	Min	Typ	Max	Unit
RVTCn clock period	t_{CYC}	422.2		4000.0	ns
RVTCn clock low time	t_{PWL}	233.0		3811.0	ns
RVTCn clock high time	t_{PWH}	189.3		189.3	ns
RVTCn clock frequency (nominal)			2.240		MHz
RVTFn delay after RVTCn↓	$t_{D(1)}$	13.1		14.5	ns
RVTDn delay after RVTCn↓	$t_{D(2)}$	14.0		14.5	ns
Multiframe Time	$t_{PW(1)}$	500		500	µs
RVTFn pulse width	$t_{PW(2)}$	422.2		770	ns

Figure 14. Channels 1 - 28 Receive VT/TU Interface Timing-Gapped Pointer & POH Byte



Notes: - RVTCn is shown for RnCLKI = 1, data & Frame pulse with Rising Edge.
- Clock gaps are present during the time of pointer bytes (V1-V4) and the overhead bytes (V5, J2, N2/Z6, K4/Z7), and may not be contiguous. When RnCLKI = 0, timing is similar to Figure 13.

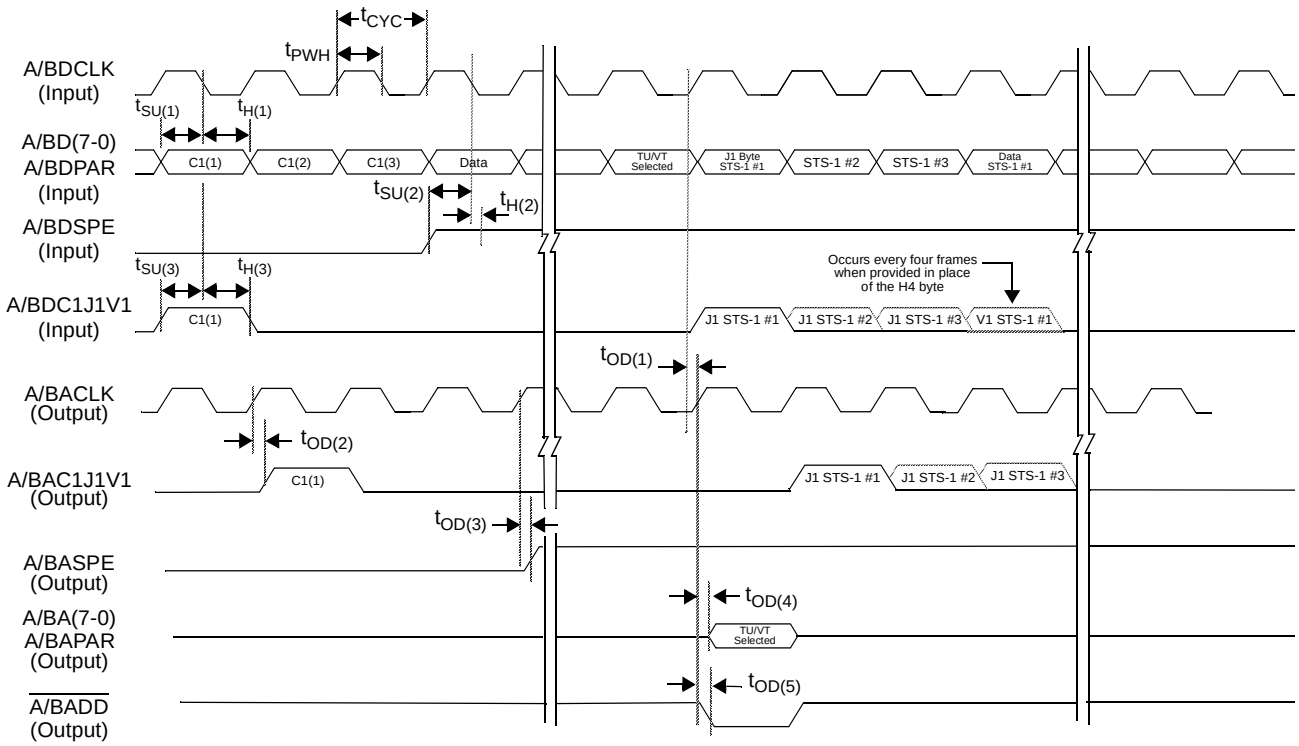
VT 1.5 INTERFACE

Parameter	Symbol	Min	Typ	Max	Unit
RVTCn clock period	t_{CYC}	553.3		9930.1	ns
RVTCn clock low time	t_{PWL}	291.2		9668.0	ns
RVTCn clock high time	t_{PWH}	262.1		276.6	ns
RVTCn clock frequency (nominal)			1.600		MHz
RVTFn delay after RVTCn↑	$t_{D(1)}$	13.1		14.5	ns
RVTDn delay after RVTCn↑	$t_{D(2)}$	14.0		14.5	ns
Multiframe Time	$t_{PW(1)}$	500		500	µs
RVTFn pulse width	$t_{PW(2)}$	567.8		873	ns

VT 2 INTERFACE

Parameter	Symbol	Min	Typ	Max	Unit
RVTCn clock period	t_{CYC}	422.2		7425.7	ns
RVTCn clock low time	t_{PWL}	233.0		7236.4	ns
RVTCn clock high time	t_{PWH}	189.3		189.3	ns
RVTCn clock frequency (nominal)			2.176		MHz
RVTFn delay after RVTCn↑	$t_{D(1)}$	13.1		14.5	ns
RVTDn delay after RVTCn↑	$t_{D(2)}$	14.0		14.5	ns
Multiframe Time	$t_{PW(1)}$	500		500	µs
RVTFn pulse width	$t_{PW(2)}$	422.2		770	ns

Figure 15. STS-3 A/B Drop and Add Bus Signals, Timing Derived from Drop Bus (lead $\overline{\text{ABTE}}$ low)

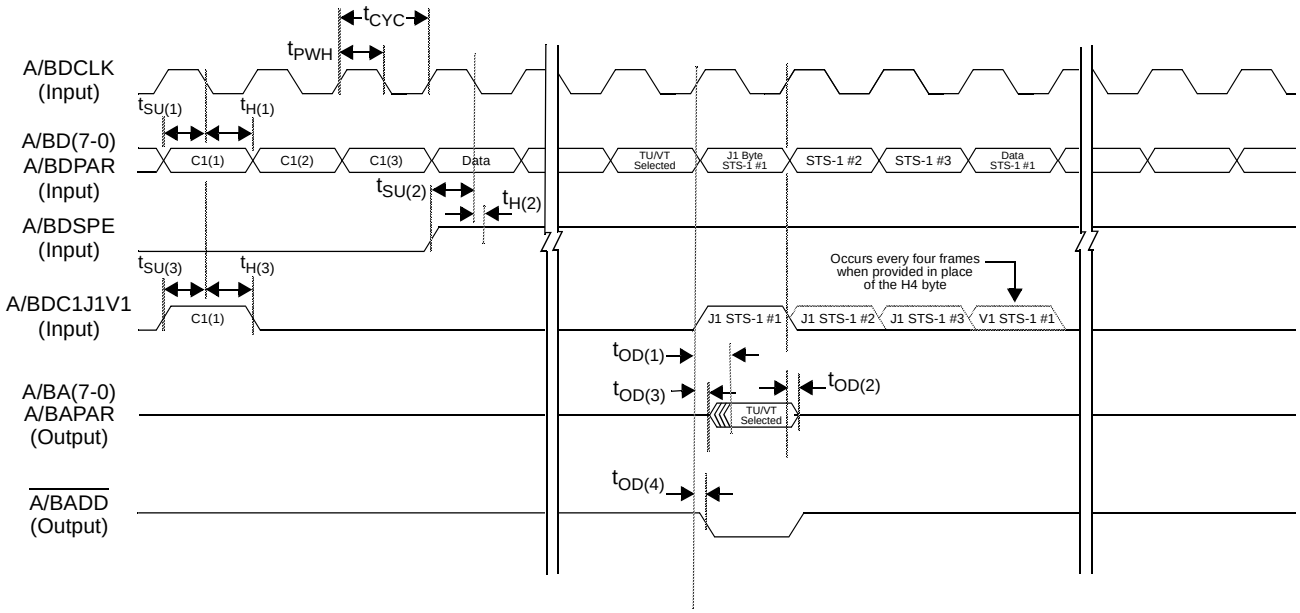


Note: A single TU/VT (number 21/28 in STS-1 number 3) is shown for illustration purposes. The A and B add bus outputs are delayed an additional clock cycle from their respective drop bus timing inputs when control bit ABOD (bit 1, 03BH) is written with a 1.

Parameter	Symbol	Min	Typ	Max	Unit
A/BDCLK clock period	t_{CYC}		51.44		ns
A/BDCLK duty cycle t_{PWH}/t_{CYC}		40	50	60	%
A/BD(7-0)/A/BDPAR data /parity setup time before A/BDCLK↓	$t_{SU(1)}$	5.0			ns
A/BD(7-0)/A/BDPAR data /parity hold time after A/BDCLK↓	$t_{H(1)}$	2.0			ns
A/BDSPE setup time before A/BDCLK↓	$t_{SU(2)}$	5.0			ns
A/BDSPE hold time after A/BDCLK↓	$t_{H(2)}$	3.0			ns
A/BDC1J1V1 setup time before A/BDCLK↓	$t_{SU(3)}$	5.0			ns
A/BDC1J1V1 hold time after A/BDCLK↓	$t_{H(3)}$	3.0			ns
A/BACLK ↑delay from A/BDCLK↑	$t_{OD(1)}$	4.0		12.0	ns
A/BAC1J1V1 delay from A/BACLK↑	$t_{OD(2)}$	-2.0		2.5	ns
A/BASPE delay from A/BCLK↑	$t_{OD(3)}$	-2.0		2.5	ns
A/B(7-0) and A/BAPAR data /parity out valid delay from A/BACLK↑	$t_{OD(4)}$	-2.0		10.0	
$\overline{\text{A/BADD}}$ delay from A/BACLK↑	$t_{OD(5)}$	-2.0		7.0	ns

Note: All output times are measured with the 50 pf load capacitance.

Figure 16. STS-3 A/B Drop and Add Bus Signals, Timing Derived from Drop Bus (lead $\overline{\text{ABTE}}$ high)

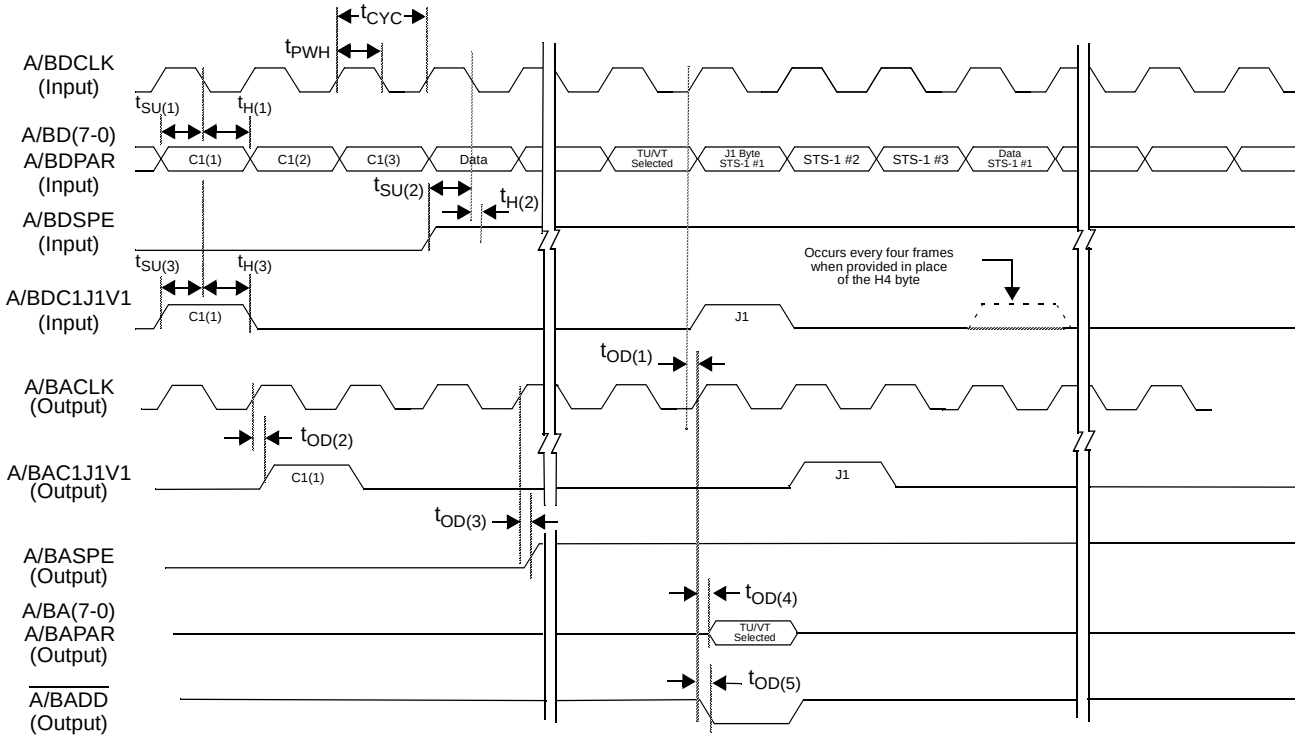


Note: A single TU/VT (number 21/28 in STS-1 number 3) is shown for illustration purposes. The A and B add bus outputs are delayed an additional clock cycle from their respective drop bus timing inputs when control bit ABOD (bit 1, 03BH) is written with a 1.

Parameter	Symbol	Min	Typ	Max	Unit
A/BDCLK clock period	t_{CYC}		51.44		ns
A/BDCLK duty cycle t_{PWH}/t_{CYC}		40	50	60	%
A/BD(7-0)/A/BDPAR data /parity setup time before A/BDCLK↓	$t_{SU(1)}$	5.0			ns
A/BD(7-0)/A/BDPAR data /parity hold time after A/BDCLK↓	$t_{H(1)}$	2.0			ns
A/BDSPE setup time before A/BDCLK↓	$t_{SU(2)}$	5.0			ns
A/BDSPE hold time after A/BDCLK↓	$t_{H(2)}$	3.0			ns
A/BDC1J1V1 setup time before A/BDCLK↓	$t_{SU(3)}$	5.0			ns
A/BDC1J1V1 hold time after A/BDCLK↓	$t_{H(3)}$	3.0			ns
A/BA(7-0)/A/BAPAR data /parity out valid delay from A/BDCLK↑	$t_{OD(1)}$	4.0		21.0	ns
A/BA(7-0)/A/BAPAR data /parity to tristate delay from A/BDCLK↑	$t_{OD(2)}$	4.0		15.0	ns
$\overline{\text{A/BADD}}$ add indicator delay from A/BDCLK↑	$t_{OD(4)}$	4.0		18.0	ns
A/BA(7-0)/A/BAPAR data /parity out tristate to driven delay from A/BDCLK↑	$t_{OD(3)}$	4.0		15.0	ns

Note: All output times are measured with the 50 pf load capacitance.

Figure 17. STM-1 VC-4 A/B Drop and Add Bus Signals, Timing Derived from Drop Bus (lead $\overline{\text{ABTE}}$ low)

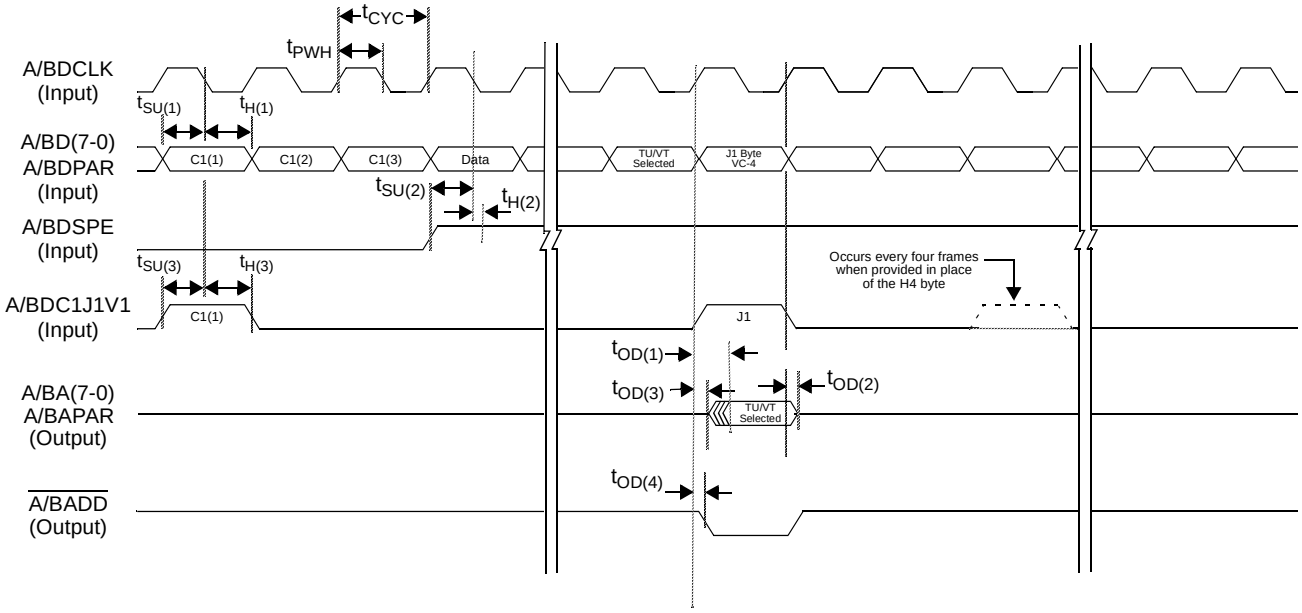


Note: A single TU/VT (number 21/28 in STS-1 number 3) is shown for illustration purposes. The A and B add bus outputs are delayed an additional clock cycle from their respective drop bus timing inputs when control bit ABOD (bit 1, 03BH) is written with a 1.

Parameter	Symbol	Min	Typ	Max	Unit
A/BDCLK clock period	t_{CYC}		51.44		ns
A/BDCLK duty cycle t_{PWH}/t_{CYC}		40	50	60	%
A/BD(7-0)/A/BDPAR data /parity setup time before A/BDCLK↓	$t_{SU(1)}$	5.0			ns
A/BD(7-0)/A/BDPAR data /parity hold time after A/BDCLK↓	$t_{H(1)}$	2.0			ns
A/BDSPE setup time before A/BDCLK↓	$t_{SU(2)}$	5.0			ns
A/BDSPE hold time after A/BDCLK↓	$t_{H(2)}$	3.0			ns
A/BDC1J1V1 setup time before A/BDCLK↓	$t_{SU(3)}$	5.0			ns
A/BDC1J1V1 hold time after A/BDCLK↓	$t_{H(3)}$	3.0			ns
A/BACLK ↑delay from A/BDCLK↑	$t_{OD(1)}$	4.0		12.0	ns
A/BAC1J1V1 delay from A/BACLK↑	$t_{OD(2)}$	-2.0		2.5	ns
A/BASPE delay from A/BCLK↑	$t_{OD(3)}$	-2.0		2.5	ns
A/B(7-0) and A/BAPAR data /parity out valid delay from A/BACLK↑	$t_{OD(4)}$	-2.0		10.0	
$\overline{\text{A/BADD}}$ delay from A/BACLK↑	$t_{OD(5)}$	-2.0		7.0	ns

Note: All output times are measured with the 50 pf load capacitance.

Figure 18. STM-1 VC-4 A/B Drop and Add Bus Signals, Timing Derived from Drop Bus (lead $\overline{\text{ABTE}}$ high)

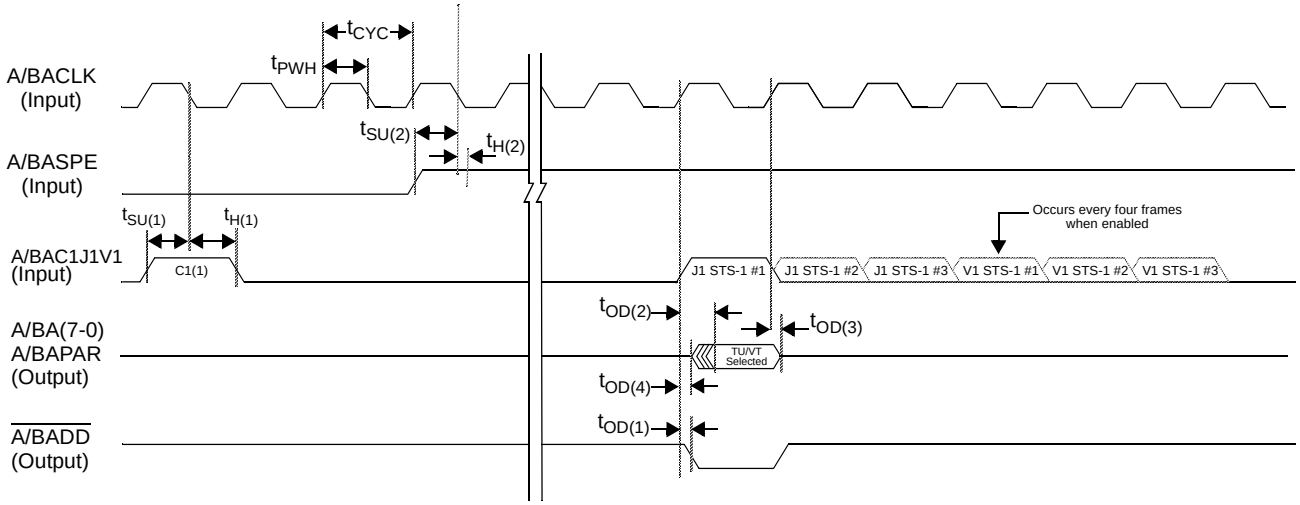


Note: A single TU/VT (number 21/28 in STS-1 number 3) is shown for illustration purposes. The A and B add bus outputs are delayed an additional clock cycle from their respective drop bus timing inputs when control bit ABOD (bit 1, 03BH) is written with a 1.

Parameter	Symbol	Min	Typ	Max	Unit
A/BDCLK clock period	t_{CYC}		51.44		ns
A/BDCLK duty cycle t_{PWH}/t_{CYC}		40	50	60	%
A/BD(7-0)/A/BDPAR data /parity setup time before A/BDCLK↓	$t_{SU(1)}$	5.0			ns
A/BD(7-0)/A/BDPAR data /parity hold time after A/BDCLK↓	$t_{H(1)}$	2.0			ns
A/BDSPE setup time before A/BDCLK↓	$t_{SU(2)}$	5.0			ns
A/BDSPE hold time after A/BDCLK↓	$t_{H(2)}$	3.0			ns
A/BDC1J1V1 setup time before A/BDCLK↓	$t_{SU(3)}$	5.0			ns
A/BDC1J1V1 hold time after A/BDCLK↓	$t_{H(3)}$	3.0			ns
A/BA(7-0)/A/BAPAR data /parity out valid delay from A/BDCLK↑	$t_{OD(1)}$	4.0		21.0	ns
A/BA(7-0)/A/BAPAR data /parity to tristate delay from A/BDCLK↑	$t_{OD(2)}$	4.0		15	ns
$\overline{\text{A/BADD}}$ add indicator delay from A/BDCLK↑	$t_{OD(4)}$	4.0		18.0	ns
A/BA(7-0)/A/BAPAR data /parity out tristate to driven delay from A/BDCLK↑	$t_{OD(3)}$	4.0		15.0	ns

Note: All output times are measured with the 50 pf load capacitance.

Figure 19. STS-3 A/B Add Bus Signals, Timing Derived from Add Bus

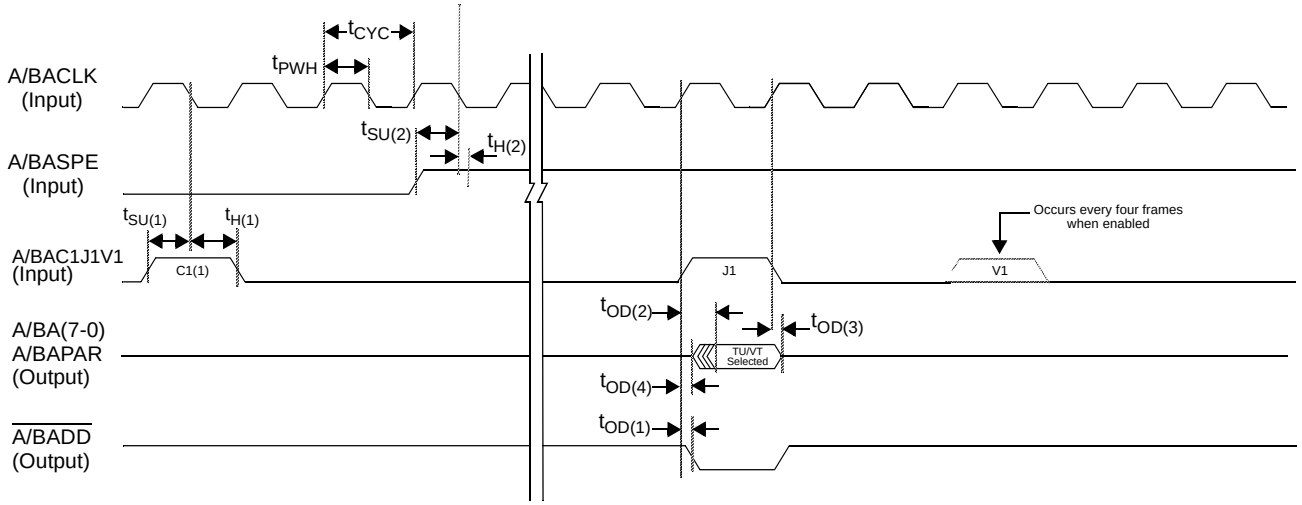


Note: A single TU/VT (number 21/28 in STS-1 number 3) is shown for illustration purposes. The A and B add bus outputs are delayed an additional clock cycle from their respective add bus timing inputs when control bit ABOD (bit 1, 03BH) is written with a 1.

Parameter	Symbol	Load	Min	Typ	Max	Unit
ACLK clock period	t_{CYC}			51.44		ns
ACLK duty cycle, t_{PWH}/t_{CYC}			40	50	60	%
AC1J1V1 setup time before ACLK↓	$t_{SU(1)}$		5.0			ns
AC1J1V1 hold time after ACLK↓	$t_{H(1)}$		5.0			ns
ASPE setup time before ACLK↓	$t_{SU(2)}$		5.0			ns
ASPE hold time after ACLK↓	$t_{H(2)}$		5.0			ns
A(7-0)/APAR data /parity out valid delay from ACLK↑	$t_{OD(2)}$	50pF	4.0		21.0	ns
A(7-0)/APAR data /parity to tristate delay from ACLK↑	$t_{OD(3)}$		4.0		15	ns
$\overline{ADD}$ add indicator delayed from ACLK↑	$t_{OD(1)}$	50pF	4.0		17.0	ns
A(7-0)/APAR data /parity out tristate to driven delay from ACLK↑	$t_{OD(4)}$	50pF	4.0		15	ns

Note: All output times are measured with the specified load capacitance.

Figure 20. STM-1 VC-4 A/B Add Bus Signals, Timing Derived from Add Bus

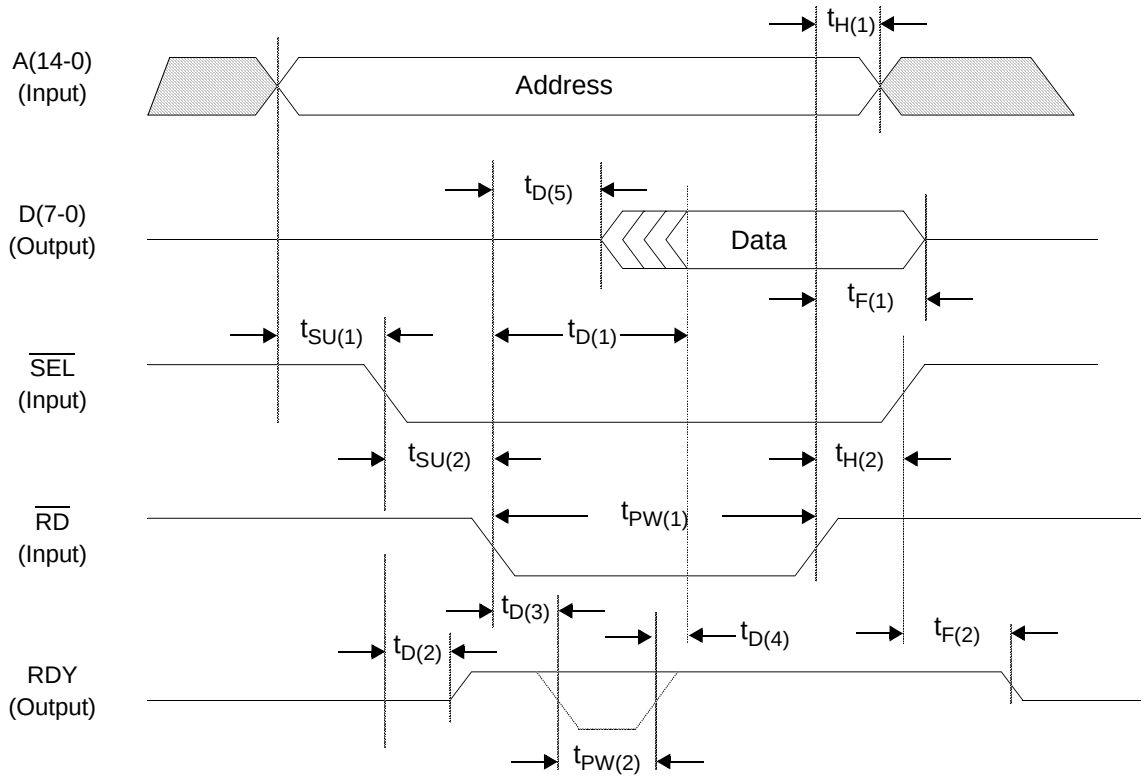


Note: A single TU/VT (number 21/28 in STS-1 number 3) is shown for illustration purposes. The A and B add bus outputs are delayed an additional clock cycle from their respective add bus timing inputs when control bit ABOD (bit 1, 03BH) is written with a 1.

Parameter	Symbol	Load	Min	Typ	Max	Unit
ACLK clock period	t_{CYC}			51.44		ns
ACLK duty cycle, t_{PWH}/t_{CYC}			40	50	60	%
AC1J1V1 setup time before ACLK↓	$t_{SU(1)}$		5.0			ns
AC1J1V1 hold time after ACLK↓	$t_{H(1)}$		5.0			ns
ASPE setup time before ACLK↓	$t_{SU(2)}$		5.0			ns
ASPE hold time after ACLK↓	$t_{H(2)}$		5.0			ns
A(7-0)/APAR data /parity out valid delay from ACLK↑	$t_{OD(2)}$	50pF	4.0		21	ns
A(7-0)/APAR data /parity to tristate delay from ACLK↑	$t_{OD(3)}$		4.0		15	ns
$\overline{\text{ADD}}$ add indicator delayed from ACLK↑	$t_{OD(1)}$	50pF	4.0		17	ns
A(7-0)/APAR data /parity out tristate to driven delay from ACLK↑	$t_{OD(4)}$	50pF	4.0		15	ns

Note: All output times are measured with the specified load capacitance.

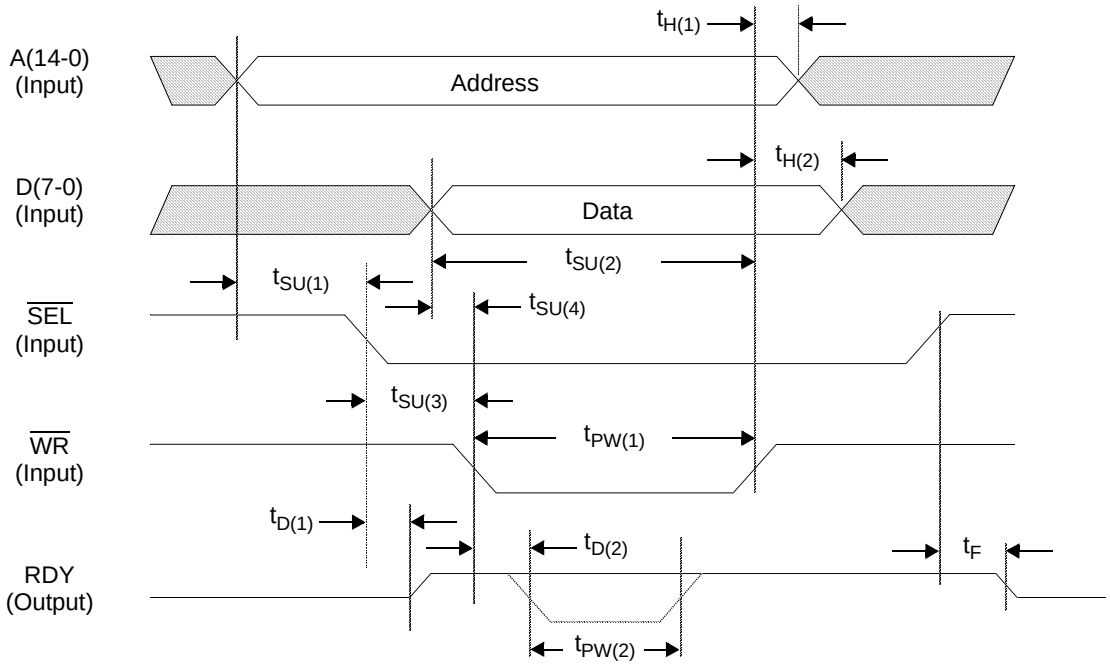
Figure 21. Microprocessor Read Cycle Timing - Intel



Parameter	Symbol	Min	Typ	Max	Unit
A(14-0) address setup time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	3.0			ns
A(14-0) address hold time after $\overline{RD}\uparrow$	$t_{H(1)}$	3.0			ns
D(7-0) data output float time after $\overline{RD}\uparrow$	$t_{F(1)}$			15	ns
$\overline{SEL}\downarrow$ setup time to $\overline{RD}\downarrow$	$t_{SU(2)}$	3.0			ns
$\overline{RD}$ pulse width	$t_{PW(1)}$	20			ns
$\overline{SEL}\downarrow$ hold time after $\overline{RD}\uparrow$	$t_{H(2)}$	3.0			ns
RDY$\uparrow$ delay after $\overline{SEL}\downarrow$	$t_{D(2)}$	8.0		15.0	ns
RDY$\downarrow$ delay after $\overline{RD}\downarrow$	$t_{D(3)}$			14.0	ns
RDY float time after $\overline{SEL}\uparrow$	$t_{F(2)}$			12.0	ns
RDY pulse width	$t_{PW(2)}$			1.2	µs
Data output valid delay after $\overline{RD}\downarrow$	$t_{D(1)}$			12.0	ns
Data output valid delay after RDY$\uparrow$	$t_{D(4)}$			5.0	ns
Data output tristate to driven delay after $\overline{RD}\downarrow$	$t_{D(5)}$			9.0	ns

Note: All output times are measured with a maximum 25 pF load capacitance.

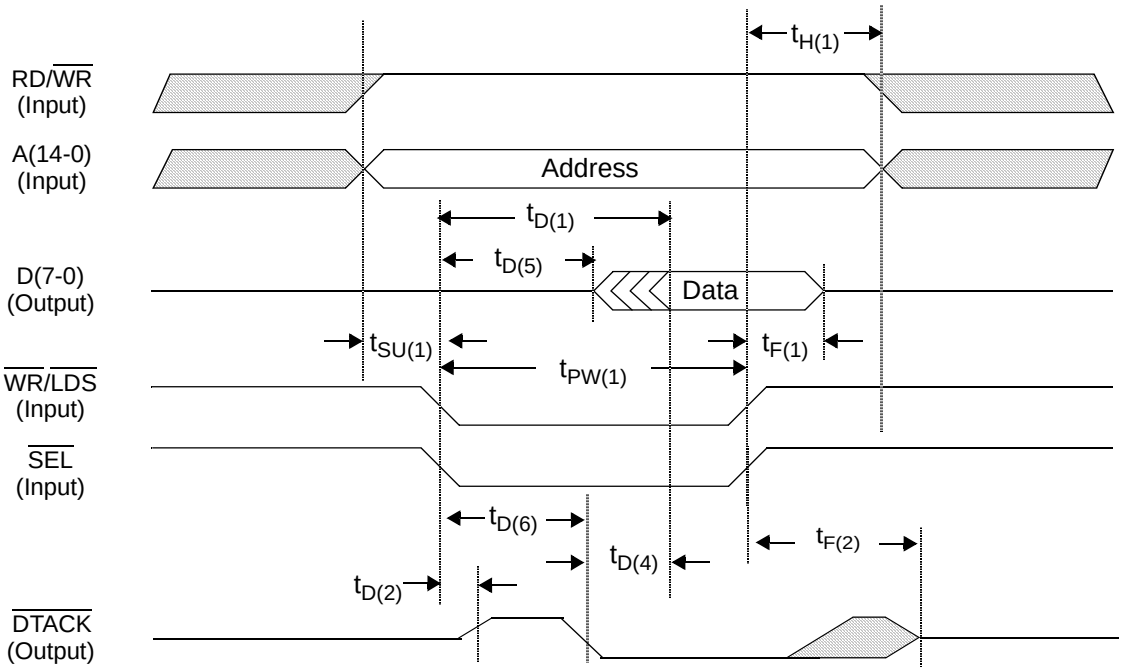
Figure 22. Microprocessor Write Cycle Timing - Intel



Parameter	Symbol	Min	Typ	Max	Unit
A(14-0) address setup time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	3.0			ns
A(14-0) address hold time after $\overline{WR}\uparrow$	$t_{H(1)}$	7			ns
D(7-0) data input valid setup time to $\overline{WR}\uparrow$	$t_{SU(2)}$	5			ns
D(7-0) data input hold time after $\overline{WR}\uparrow$	$t_{H(2)}$	7			ns
$\overline{SEL}$ setup time to $\overline{WR}\downarrow$	$t_{SU(3)}$	3			ns
$\overline{WR}$ pulse width	$t_{PW(1)}$	20			ns
RDY$\uparrow$ delay after $\overline{SEL}\downarrow$	$t_{D(1)}$	8		15	ns
RDY$\downarrow$ delay after $\overline{WR}\downarrow$	$t_{D(2)}$			14	ns
RDY float time after $\overline{SEL}\uparrow$	t_F			12	ns
RDY pulse width	$t_{PW(2)}$			1.2	µs
D(7-0) data valid setup time to $\overline{WR}\downarrow$	$t_{SU(4)}$	3			ns

Note: All output times are measured with a maximum 25 pF load capacitance.

Figure 23. Microprocessor Read Cycle Timing - Motorola

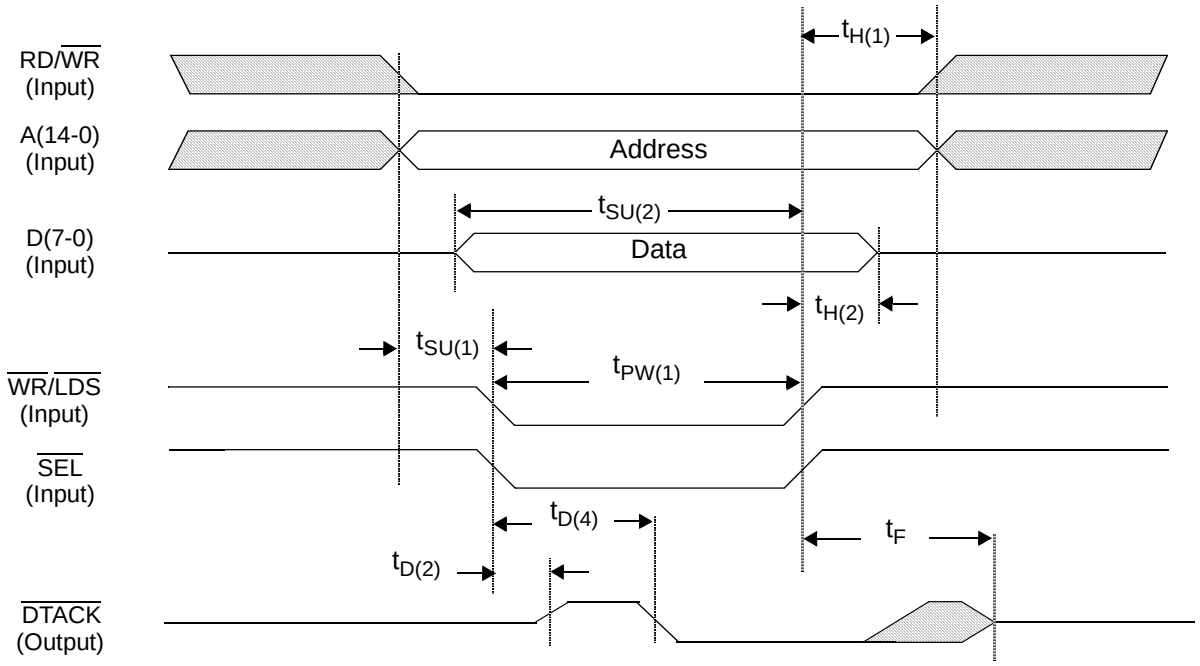


Parameter	Symbol	Min	Typ	Max	Unit
A(14-0) address setup time and RD/WR↑ setup time before SEL↓, WR/LDS ↓ (See Note 2)	$t_{SU(1)}$	3.0			ns
A(14-0) address hold time and RD/WR delay time after SEL↑, WR/LDS↑ (See Note 3)	$t_{H(1)}$	3			ns
D(7-0) data output float time after SEL↑, WR/LDS ↑ (See Note 3)	$t_{F(1)}$			15	ns
SEL or WR/LDS pulse width	$t_{PW(1)}$	20			ns
DTACK driven delay after SEL↓, WR/LDS ↓ (See Note 2)	$t_{D(2)}$	7		15	ns
DTACK float time after SEL↑, WR/LDS ↑ (See Note 3)	$t_{F(2)}$			12	ns
DTACK ↓ delay after SEL↓, WR/LDS ↓ (See Note 2)	$t_{D(6)}$			1.2	µs
D(7-0) data output delay after SEL↓, WR/LDS ↓ (See Note 2)	$t_{D(1)}$			1.2	µs
D(7-0) data output delay after DTACK↓	$t_{D(4)}$			5	ns
D(7-0) data output tristate to drive delay after SEL ↓, WR/LDS ↓ (See Note 2)	$t_{D(5)}$	4		10	ns

Notes:

1. All output times are measured with a maximum 25 pF load capacitance.
2. Measured with respect to the later of SEL or WR/LDS falling edge.
3. Measured with respect to the earlier of SEL or WR/LDS rising edge.

Figure 24. Microprocessor Write Cycle Timing - Motorola

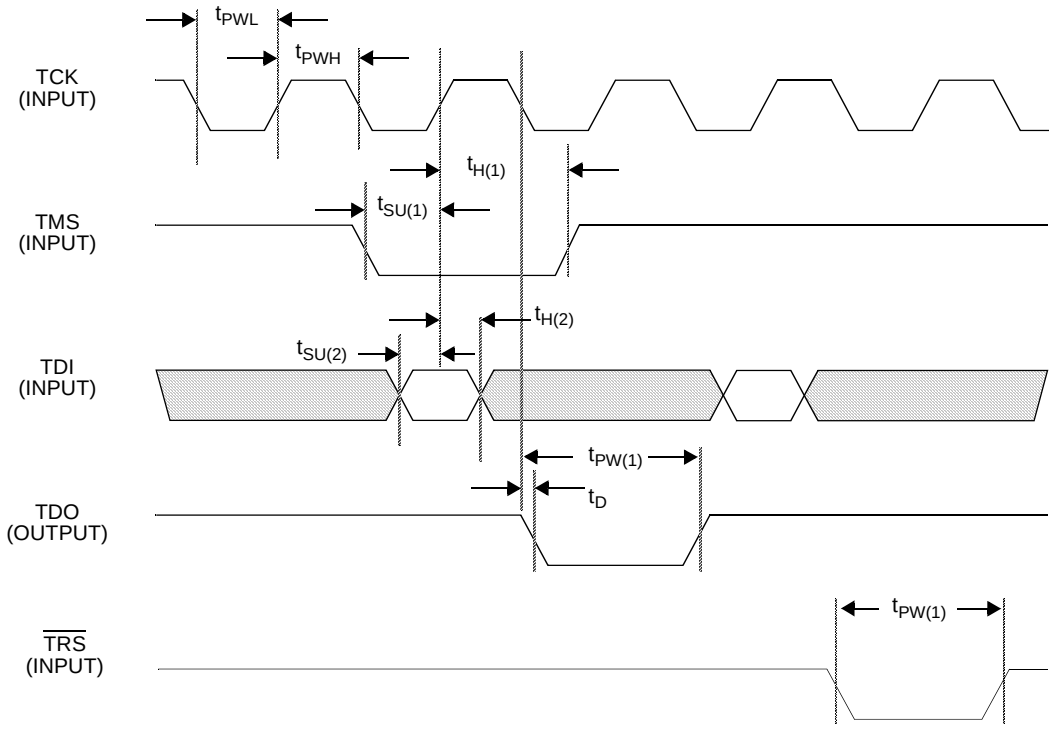


Parameter	Symbol	Min	Typ	Max	Unit
A(14-0) address setup time and RD/$\overline{WR}$ setup time before $\overline{SEL}\downarrow$, $\overline{WR}/\overline{LDS}\downarrow$ (See Note 2)	$t_{SU(1)}$	3			ns
A(14-0) address hold time and RD/$\overline{WR}$ delay time after $\overline{SEL}\uparrow$, $\overline{WR}/\overline{LDS}\uparrow$ (See Note 3)	$t_{H(1)}$	8			ns
D(7-0) data input setup time before $\overline{SEL}\uparrow$, $\overline{WR}/\overline{LDS}\uparrow$ (See Note 3)	$t_{SU(2)}$	8			ns
D(7-0) data input hold time after $\overline{SEL}\uparrow$, $\overline{WR}/\overline{LDS}\uparrow$ (See Note 3)	$t_{H(2)}$	8			ns
$\overline{SEL}$ or $\overline{WR}/\overline{LDS}$ pulse width	$t_{PW(1)}$	20			ns
$\overline{DTACK}$ driven delay after $\overline{SEL}\downarrow$, $\overline{WR}/\overline{LDS}\downarrow$ (See Note 2)	$t_{D(2)}$			15	ns
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$, $\overline{WR}/\overline{LDS}\uparrow$ (See Note 3)	t_F			15	ns
$\overline{DTACK}\downarrow$ delay after $\overline{SEL}\downarrow$, $\overline{WR}/\overline{LDS}\downarrow$ (See Note 2)	$t_{D(4)}$			1.2	us

Notes:

1. All output times are measured with a maximum 25 pF load capacitance.
2. Measured with respect to the later of $\overline{SEL}$ or $\overline{WR}/\overline{LDS}$ falling edge.
3. Measured with respect to the earlier of $\overline{SEL}$ or $\overline{WR}/\overline{LDS}$ rising edge.

Figure 25. Boundary Scan Timing



Parameter	Symbol	Min	Max	Unit
TCK clock high time	t_{PWH}	50		ns
TCK clock low time	t_{PWL}	50		ns
TMS setup time before TCK↑	$t_{SU(1)}$	3.0	-	ns
TMS hold time after TCK↑	$t_{H(1)}$	2.0	-	ns
TDI setup time before TCK↑	$t_{SU(2)}$	3.0	-	ns
TDI hold time after TCK↑	$t_{H(2)}$	4.0	-	ns
TDO delay from TCK↓ (see Note)	t_D	-	25	ns
$\overline{TRS}$ Pulse Width	$t_{PW(1)}$	20	-	ns

Note: The output time (TDO) is measured with a maximum of 25 pF load capacitance.

OPERATION

The following sections detail the operation of the TEMx28 Mapper.

BUS INTERFACE MODES

Each channel in the TEMx28 Mapper supports the following SONET/SDH bus modes of operation:

- Drop Mode
- Add Mode
- Single Unidirectional Ring Mode
- Multiplexer Mode
- Dual Unidirectional Ring Mode

Drop Mode

In the drop mode of operation, TU/VTs from both the A and B buses are monitored, and a TU/VT is terminated from either the A or B Drop bus to the receive output, without a return path in the transmit direction to the A and B add buses.

Add Mode

In the add mode of operation, TU/VTs are monitored from the A or B Drop buses without a receive output, but a path in the transmit direction for either A or B add buses is provided.

Single Unidirectional Ring Mode

In the single unidirectional ring mode of operation, a TU/VT is dropped from the A (or B) Drop bus, with the return path the A (or B) Add bus. The other drop bus monitors the VT/TU. Timing for the TU/VT to be added to the A (or B) Add bus is derived from either the A (or B) Drop bus, or from the A (or B) Add bus.

Multiplexer Mode

In the multiplexer mode of operation, a TU/VT is dropped from the A (or B) Drop bus, with the return path the B (or A) Add bus. The other drop bus monitors the VT/TU. Timing for the TU/VT to be added to the A (or B) Add bus is derived from either the A (or B) Drop bus, or from the A (or B) Add bus.

Dual Unidirectional Ring Mode

In the dual unidirectional ring mode of operation, a TU/VT is dropped from the A (or B) Drop bus, with the return path both the A and B Add buses. The other drop bus monitors the VT/TU. Timing for the TU/VT to be added to the A (or B) Add bus is derived from either the A (or B) Drop bus, or from the A (or B) Add bus.

BUS MODE SELECTION

The TU/VT bus mode selection is performed by the control bits defined in the table shown below. The n represents the channel number (1-28). Note: Both the A and B Add buses upon power up and reset are in the high impedance state. A 0 must be written to control bits AAHZE (bit 1, 03AH) and BAHZE (bit 2, 03AH) for normal add bus operation.

Mode Type	TnSEL1 (bit 1, X+006H)	TnSEL0 (bit 0, X+006H)	RnSEL (bit 2, X+006H)	DROP from Bus	ADD to Bus
Dropping only, from A	0	0	0	A	Drop-only (1)
Dropping only, from B	0	0	1	B	Drop-only (1)
Single unidirectional ring [2]	0	1	0	A	A
Single unidirectional ring [2]	0	1	1	B	B
Multiplexer, A in, B out	1	0	0	A	B
Multiplexer, B in, A out	1	0	1	B	A
Dual unidirectional ring	1	1	0	A	A and B
Dual unidirectional ring	1	1	1	B	B and A

Notes:

1. When the drop-only mode is selected, the ability to add a TU/VT is disabled, and the add bus is tristated.
2. Writing a 1 to control bit FnRDIS (bit 3, X+006H) causes the REI value to always be transmitted as zero. In addition, receive side alarms are disabled from generating RDI and RDI is transmitted as zero. However, the microprocessor can send an RDI, if required.

Bus Mode Selection for Channel n

SDH/SONET ADD/DROP MULTIPLEXING FORMAT SELECTIONS

The control bit settings for the SONET/SDH mapping format selection are given in the table shown below. This selection is valid for both the A and B Drop and Add buses. A Drop Bus Reset operation should be performed after modifying the STS-3 bit. See DRESET bit at address 039H in the Memory Map Description.

Format	STS3 (bit 1, 01AH)
STS-3 Format or STM-1 AU-3 Format	1
STM-1 VC4 Format	0

STS-3 STS-1/STM-1 VC-4 Format Selection

DROP AND ADD TU/VT SELECTION

There are four VT/TU selection registers per channel. Two registers are used for selecting the VT1.5/TU-11 or VT2/TU-12 (VT2) for the A and B drop buses, and the other two registers are used for selecting the VT1.5/TU-11 or VT2/TU-12 (VT2) for the A and B Add buses. Thus, two different VT/TUs can be assigned to the A and B drop buses, and two different VT/TUs can be assigned to the A and B add buses for channel n. In addition, broadcast capability is supported in the drop direction. This feature permits the same VT/TU to be dropped to more than one channel. In the add direction only one channel can be used for the broadcast mode. Each selection register consists of eight bits, which is programmed according to the following table. A 00H forces a high impedance state at the receive interface for channel n. In addition, the REI and RDI states will be transmitted as zeros. Any unlatched Drop Bus channel alarms that are set in a channel will remain set when 00 is written into that channel's Drop VT selection register regardless of a change in the alarm condition. In the add direction, a 00H or invalid value forces a high impedance state for that channel. The register assignment for the A side drop bus is: X+012H, A side add bus is: X+01AH, B side drop bus is: X+082H, and the B add bus is: X+08AHB, where X is the channel number (1 to 28) in hex. When changing the value of an Add Bus per channel VT selection register, 00H should be written into the register first, followed by the new channel assignment value. When changing the value of a Drop Bus per channel VT Selection Register, 00H should be written into the register, followed by the new channel assignment value. If another channel has been assigned the same value, then nothing else needs to be done. If no other channel has been assigned the same value, then a Drop Bus A or B per channel reset (control bit DACHnR or DBCHnR) operation should be performed for the channel whose VT selection register has been modified.

7	6	5	4	3	2	1	0	
TU/VT Type	AU-3/TUG-3 or STS-1		TU/VT Group Number			TU/VT Number		Meaning
0	0	0	0	0	0	0	0	No TU/VT Selected
0								VT1.5/TU-11 Format
1								VT2/TU-12 Format
	0	0						Not used
	0	1						AU-3/TUG-3 A, STS-1 #1
	1	0						AU-3/TUG-3 B, STS-1 #2
	1	1						AU-3/TUG-3 C, STS-1 #3
			0	0	1			TU/VT Group Number 1
			0	1	0			TU/VT Group Number 2
			0	1	1			TU/VT Group Number 3
			1	0	0			TU/VT Group Number 4
			1	0	1			TU/VT Group Number 5
			1	1	0			TU/VT Group Number 6
			1	1	1			TU/VT Group Number 7
						0	1	TU/VT Number 1
						1	0	TU/VT Number 2
						1	1	TU/VT Number 3
						0	0	TU/VT Number 4 (VT1.5/TU-11 format)

A and B Drop and Add VT/TU Selection

BUS TIMING

Timing for adding a TU/VT to the add bus is derived from the like-named drop bus, or from the like-named add bus. The add bus timing-source selection is determined by lead ABUST, as shown in the table below. For the drop bus timing mode, the add bus timing is derived from the drop bus clock, C1J1(V1), and SPE signals. The V1 pulse may be present in the C1J signal or may be derived from internal H4 multiframe detectors. An option is also provided in which the internal clock, C1J1V1, and SPE signals may be provided as outputs on the A and B Add buses in the drop bus timing mode. For Add bus timing, an input clock, C1J1V1, and SPE signal must be provided as input signals.

ABUST lead	Action
Low	Add bus timing selected.
High	Drop bus timing selected.

Bus Timing Selection

PERFORMANCE COUNTERS

There are three types of performance counters provided: saturating/rollover, current one second, and previous one-second counters.

All counters, other than the one-second counters, can be configured as saturating (when control bit CROV (bit 0, 01AH) is a 0), or rollover (when control bit CROV is a 1). When a counter is configured to be saturating, it stops at its maximum count. A rollover counter rolls over to zero after maximum count is reached.

A saturating counter is reset to 0 by a hardware reset (RESET lead), the software reset (RESETH control bit), when it is read by the microprocessor, or by any of the following resets as they apply: RESETC (resets all performance counters), DRESET (resets all drop side performance counters), DACHnR/DBCHnR (resets all A/B drop side performance counters for a selected channel), TRESET (resets all add side performance counters), and TnRESET (resets all add side performance counters for a selected channel).

A rollover counter is reset to FFFEH/FEH by a software reset. A hardware reset sets the CROV bit to 0 (saturating) and all performance counters to 0. Rollover counters do not reset when read by the microprocessor. The software resets must be held high for a minimum of one DSCLK clock cycle (excluding RESETH which is self clearing). Since these resets are not self-clearing they must be brought low before another reset operation can take place.

Reset action of the Current one-second and previous one-second counters is not dependent upon the CROV control bit. These counters always reset to 0 (never FFFEH/FEH) by a hardware or software reset. For a 16-bit counter, the low order byte must be read first, followed by a read of the high order byte, before any other low order byte is read. During a microprocessor read cycle of any performance counter, counts are held and updated afterwards to ensure that no counts are lost.

ALARM STRUCTURE

All alarm indications are reported as unlatched and latched status bits. The latched bit of an alarm can be set on the positive transitions, negative transitions, or both positive and negative transitions. Reading a latched alarm bit clears the bit to 0. Control bits INTR1 and INTR0 (bits 7 and 6, 01BH) should be programmed to select the transition(s) on which the latched bits are set (see table below).

INTR1 (bit 7, 01BH)	INTR0 (bit 6, 01BH)	Action on an Alarm
0	0	Not used. No latched alarm event indication, or interrupt indication.
1	0	Alarm sets latched alarm on positive transitions of the alarm.
0	1	Alarm sets latched alarm on negative transitions of the alarm.
1	1	Alarm sets latched alarm on positive or negative transitions of the alarm.

The alarm bits latch according to the various states shown in Figure 26 below.

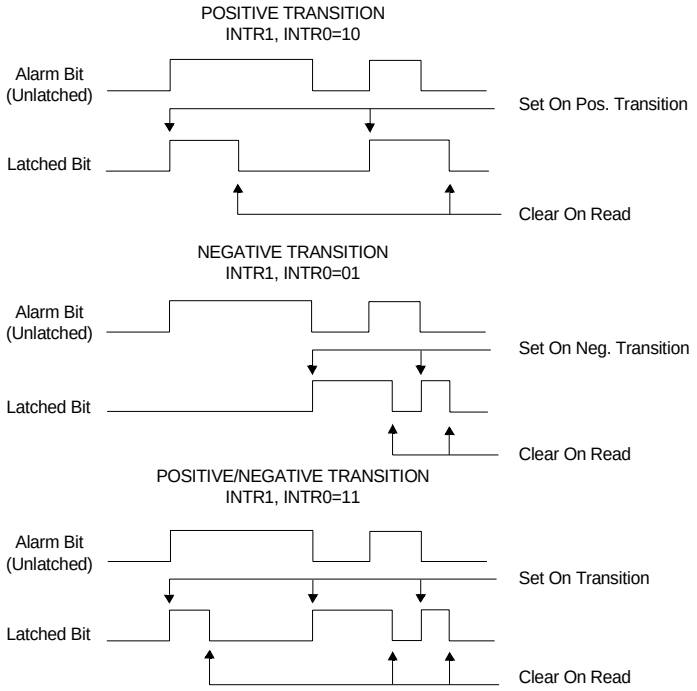
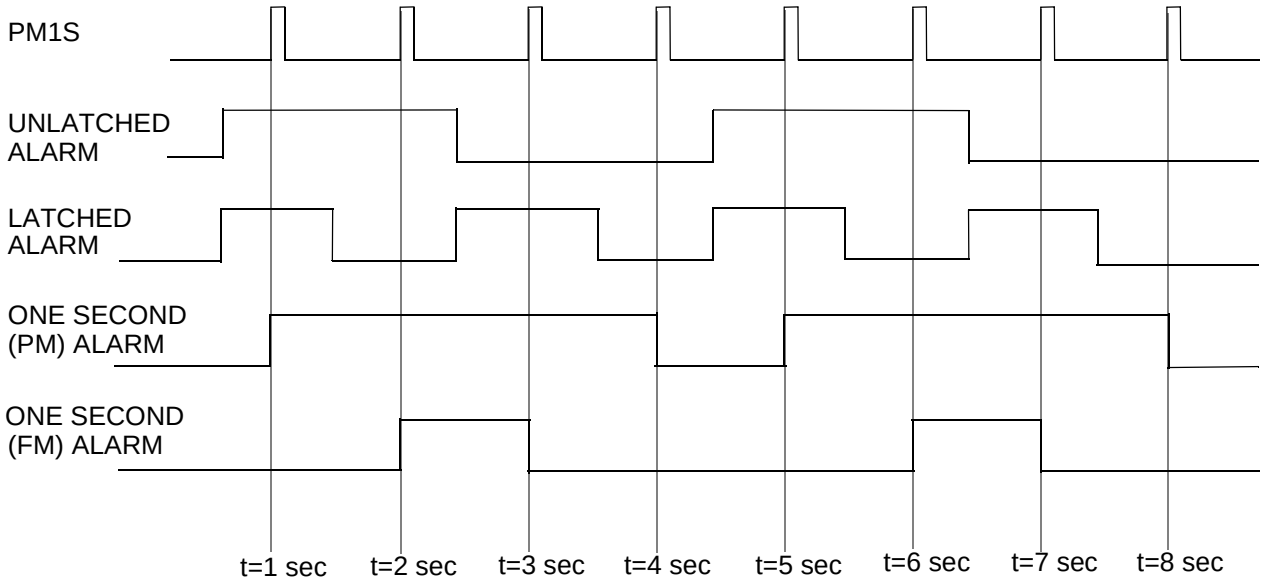


Figure 26. Alarm Latching Configurations

As shown in the above diagram there are three possible alarm latching configurations: positive transition, negative transition, or positive/negative transition. The positive level latching configuration is not supported in this device. For example, assume that control bits INTR1 and INTR0 are equal to 10. This configures the latched alarm circuits to set on positive transitions (0 to 1) of an alarm. The positive transition of an alarm causes the corresponding latched bit to set to 1. The latched bit will remain set until the register containing the latched bit position is read by the microprocessor, at which time the latched bit positions in the register will be reset to 0. Even though the alarm (unlatched) remains active, it will not cause a latched state to recur. The latched bit will remain reset to 0 until another positive alarm (unlatched) transition occurs to set it to 1.

ONE SECOND (SHADOW) REGISTERS

The TEMx28 also provides One Second registers for the alarms. The One Second register feature in the TEMx28 is enabled by applying a positive pulse at one-second intervals to lead PM1S. Figure 27 illustrates the operation of the One Second (Shadow) registers for any alarm. This figure assumes that interrupt control bits INTR1 and INTR0 (bits 7 and 6, 01BH) are set to a value of 11. The One Second (PM) status bit is a 1 whenever there is an alarm transition during the last one-second interval or the alarm is present at the end of the last one-second interval. The Persistent (FM) status bit is a 1 if the alarm is active but did not become active during the previous one-second interval.



Note 1: For this example, latched events are set only on positive and negative event transitions.

Figure 27. One Second (Shadow) Register Operation

INTERRUPT STRUCTURE

The interrupt indication structure contains both global alarm indication and polling registers, along with mask bits at various levels in the interrupt structure. The following figures illustrate the interrupt structure. As shown in Figure 30, the hardware interrupt is controlled by control bit HINT (bit 7, 005H). When this control bit is written with a 0, the hardware interrupt to the microprocessor is disabled. When written with a 1, the hardware interrupt lead is enabled. Status bits GDA, GDB, GAB, PCDA, PCDB, and PCAB (050H) are global status bits, and will set provided their corresponding mask bits are set to 1 (MGDA, MGDB, MGA, MPCDA, MPCDB, and MPCAB (005H)), and the mask bits that correspond to the alarms are also set to 1. Status bit GDA (bit 5 - 050H) is set to 1 when an alarm occurs on the A drop bus (e.g., loss of B bus clock). Status bit GDB (bit 4 - 050H) is set to 1 when an alarm occurs on the B drop bus (e.g., loss of B bus clock). Status bit GAB (bit 3 - 050H) is set to 1 when an alarm occurs on either of the two add buses (e.g., loss of clock). Status bit PCDA (bit 2 - 050H) is set to 1 when an alarm occurs in one the 28 channels that is dropping a VT/TU from the A drop bus (e.g., channel 1 has detected a loss of pointer alarm). Status bit PCDB (bit 1 - 050H) is set to 1 when an alarm occurs in one the 28 channels that is dropping a VT/TU from the B drop bus (e.g., channel 1 has detected a loss of pointer alarm). Status bit PCAB (bit 0 - 050H) is set to 1 when an alarm occurs in one the 28 channels that is adding a VT/TU from the A and/or B add bus (e.g., channel 10 has detected a transmit loss of signal alarm).

As shown in Figure 29, for each channel there are polling bits (1 through 28) for the A drop side, B drop side, and the add side, with each bit setting to 1, when there is a corresponding alarm, and the mask bits that correspond to the polling bit and the alarms are also set to 1. A polling bit in the add polling registers (055H - 058H) sets to 1 when a channel detects an add side alarm (e.g., channel 3 detects a transmit loss of clock). A polling bit in the A drop polling registers (074H - 077H) sets to 1 when a channel detects a A drop side alarm for the VT/TU selected (e.g., channel 5 detects a signal label mismatch alarm). A polling bit in the B drop polling registers (094H - 097H) sets to 1 when a channel detects a B drop side alarm for the VT/TU selected (e.g., channel 8 detects a unequipped alarm). Associated with each one the three polling bits per channel are corresponding

mask bits when set to 1, enable the global polling indication bits. Also shown in Figure 29 are the drop and add bus alarm locations and their corresponding mask bits for setting the three global bus indication bits. For example, if an upstream AIS indication is detected in A drop bus for STS-3 STS-1 No. 1, and the corresponding mask bit is set, a global indication is also set.

As shown in Figure 28, each of the alarms has a corresponding mask bit in each channel. These correspond to the add side alarms (e.g., line AIS detected), A drop VT/TU alarms (e.g., NDF alarm detected), and B drop VT/TU alarms (e.g., LOP alarm detected). When the corresponding mask bit is set to 1, the alarm sets a bit in one of the three polling registers corresponding to the channel. In addition, there is a set of mask bits which can inhibit an alarm type from setting one or more channel bits in a polling register. For example, an unequipped alarm that occurs in any channel can be masked from setting that channels polling bit register location.

The interrupt is cleared by reading the latched alarm bit position, or by setting the appropriate mask bits to 0. Please note: it will take approximately 4 microseconds before the interrupt will change states when an alarm mask bit is enabled (turned off).

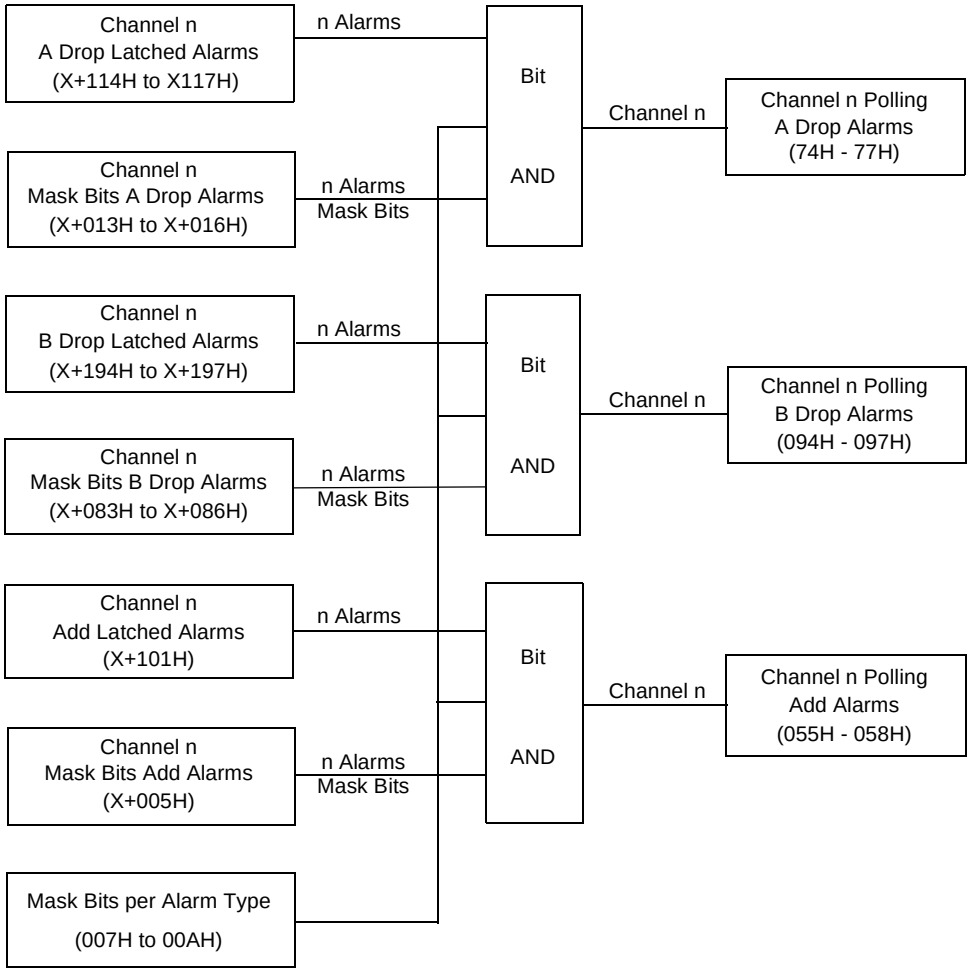


Figure 28. Channel Polling Alarms

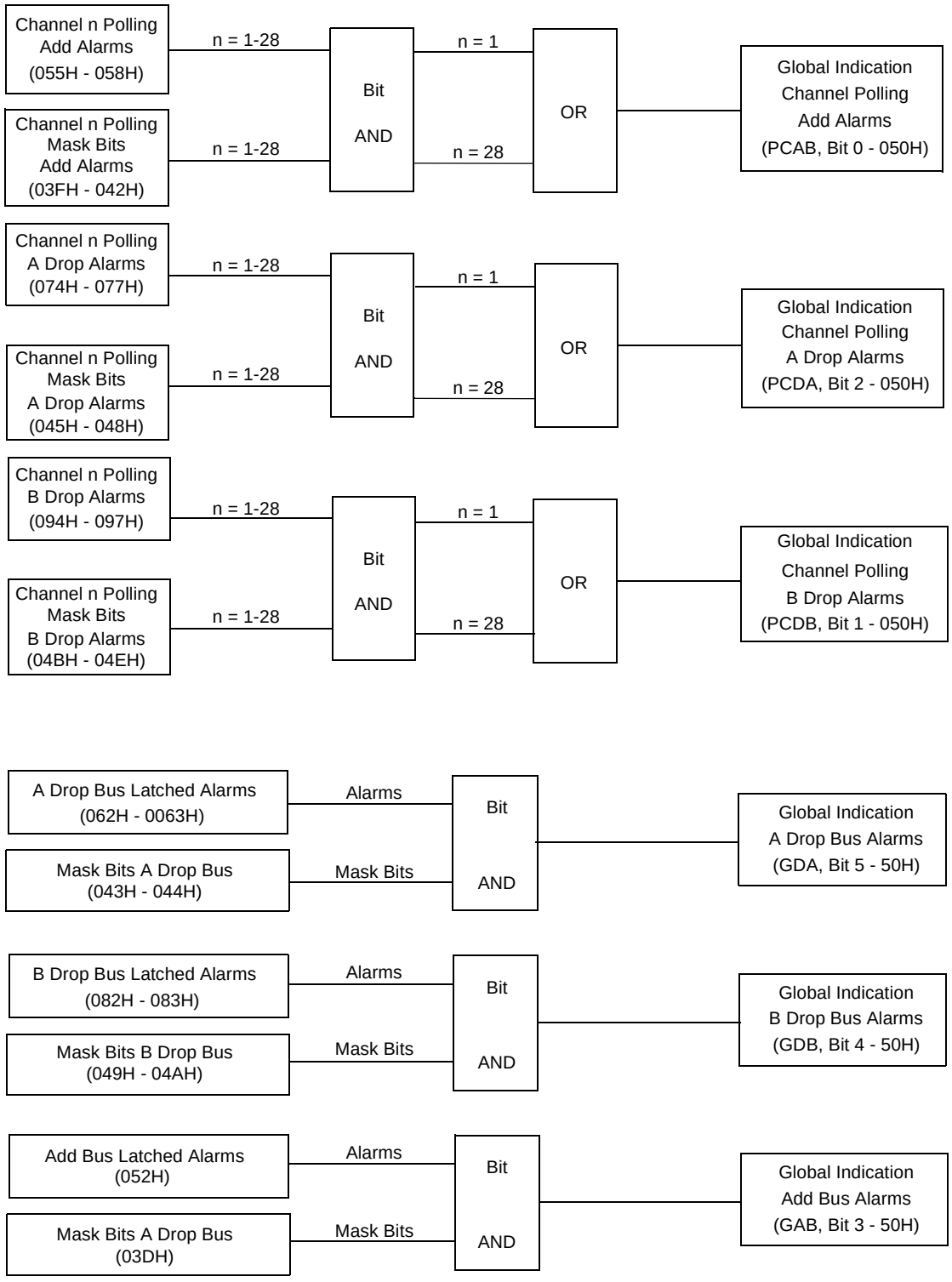


Figure 29. Global Indication Alarms

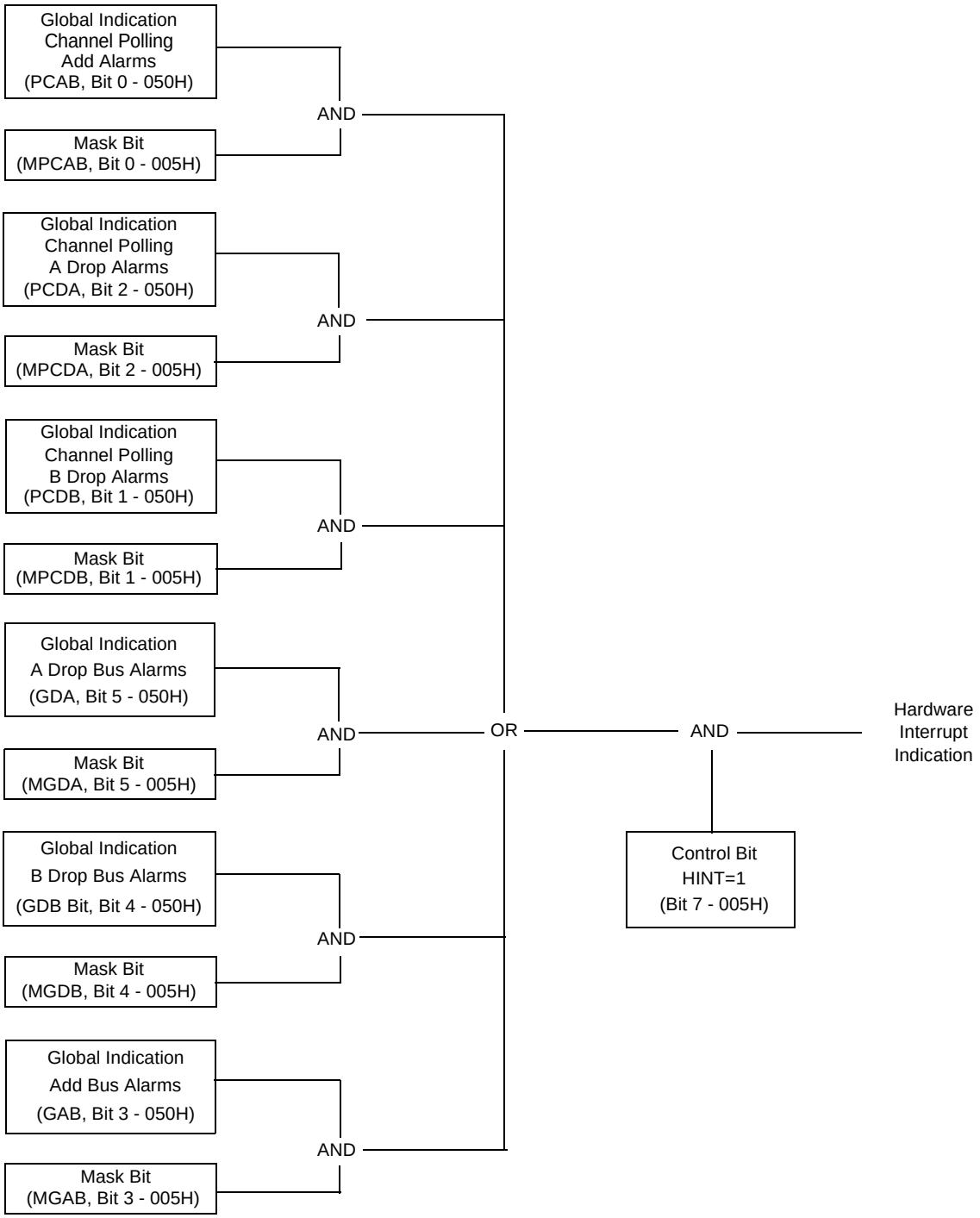


Figure 30. Hardware Interrupt Indication

DROP BUS INTERFACE

Two SONET/SDH Drop buses are provided, and are labeled A side Drop, and B side Drop. The two drop buses consist of the following leads:

- Input data (A/BD(7-0)),
- Input parity, (A/BDPAR),
- Input C1, J1, and optional V1 marker pulses (A/BDC1J1V1),
- Input payload indication (A/BDSPE).

The Most Significant Bit (MSB) is assigned to AD7 and BD7 in the AD(7-0) and BD(7-0) signals. The MSB is defined as the first bit received in a SONET/SDH byte (i.e., bit 1 in the SONET/SDH byte). The bus rate is 19.44 kbit/s for STS-3 and STM-1 operation. The STS-1 rate is not supported. The two drop buses are monitored for loss of clock. The alarms are ADLOC (bit 0, 060H) for the A side drop bus and BDLOC (bit 0, 080H) for the B side.

DROP BUS PARITY SELECTION

The parity selection for two drop buses, A and B Drop, is according to the following table. A parity error for the A side drop bus is indicated by alarm ADPAR (bit 1, 060H), and for the B side drop bus is indicated by alarm BDPAR (bit 1, 080H). Other than an alarm indication, no action is taken within the TEMx28.

DBPE (bit 0, 019H)	PDDO (bit 1, 019H)	Drop Bus Parity Selection
0	0	Odd parity is calculated for the input leads consisting of data (A/BD(7-0)), clock (A/BDCLK), C1, J1, and V1 marker pulses (A/BDC1J1V1), and the payload indication (A/BDSPE).
0	1	Odd parity is calculated for the data input leads (A/BD(7-0)).
1	0	Even parity is calculated for the input leads consisting of data (A/BD(7-0)), clock (A/BDCLK), C1, J1, and V1 marker pulses (A/BDC1J1V1), and the payload indication (A/BDSPE).
1	1	Even parity is calculated for the data Input leads (A/BD(7-0)).

DROP BUS MULTIFRAME ALIGNMENT

Pointer byte alignment (V1 and V2 bytes) for the VT/TUs in the receive direction (from the drop bus) is established by detecting the multiframe pattern in the H4 byte or the V1 reference pulse in the ADC1J1V1 and BDC1J1V1 signal. Depending on the format, one or three V1 pulses will be present in this signal. When the H4 byte is used to establish V1 byte alignment, the V1 pulse does not have to be present in the ADC1J1V1 or BDC1J1V1 signal. Writing a 1 to control bit DV1SEL (bit 2, 019H) selects the V1 pulse in the ADC1J1V1 and BDC1J1V1 signal to be used to establish the V1 byte location reference, while a 0 selects the H4 byte as the multiframe detector for establishing the V1 reference. The H4 multiframe detection circuits are disabled when the V1 pulse is selected in place of the H4 byte. A Drop Bus Reset operation should be performed after modifying the DV1SEL bit. See DRESET bit at address 039 in the Memory Map Description.

For STM-1 VC-4 operation, a single V1 pulse must occur three drop bus clock cycles every four frames following the J1 pulse. For STM-1 AU3/STS-3 operation, three V1 pulses must be present every four frames. Each V1 pulse must be present for one clock cycle, three clock cycles after the corresponding J1 pulse, when the SPE signal is high. For example, in a VC-4 signal, the J1 pulse identifies the J1 byte location (defined as the starting location for the VC-4) in the POH bytes. In the next column (first clock cycle) all the rows are assigned as fixed stuff. Similarly, in the next column (second clock cycle) all the rows are assigned as fixed stuff. The next column (third clock cycle) defines the start of TUG-3 A. This column is where the V1 pulse occurs every four frames. However, the actual V1 byte occurs six clock cycles after the V1 pulse.

For STS-1 operation, one V1 pulse must be present. The V1 pulse must occur on the next clock cycle after J1, and when the SPE signal is high. The J1 pulse identifies the J1 byte location (defined as the starting location for the STS-1) in the POH bytes. The next column (first clock cycle) defines the VTs starting location. Thus, the V1 pulse identifies the starting location of the first V1 byte in the signal. The rest of the V1 bytes for the 21 VT2s are also aligned with respect to the V1 pulse. The timing relationships between J1, V1, and other signals are shown in the Timing Characteristics section.

The H4 byte is used to identify the location of the V1 byte as shown in Figure 31 below:

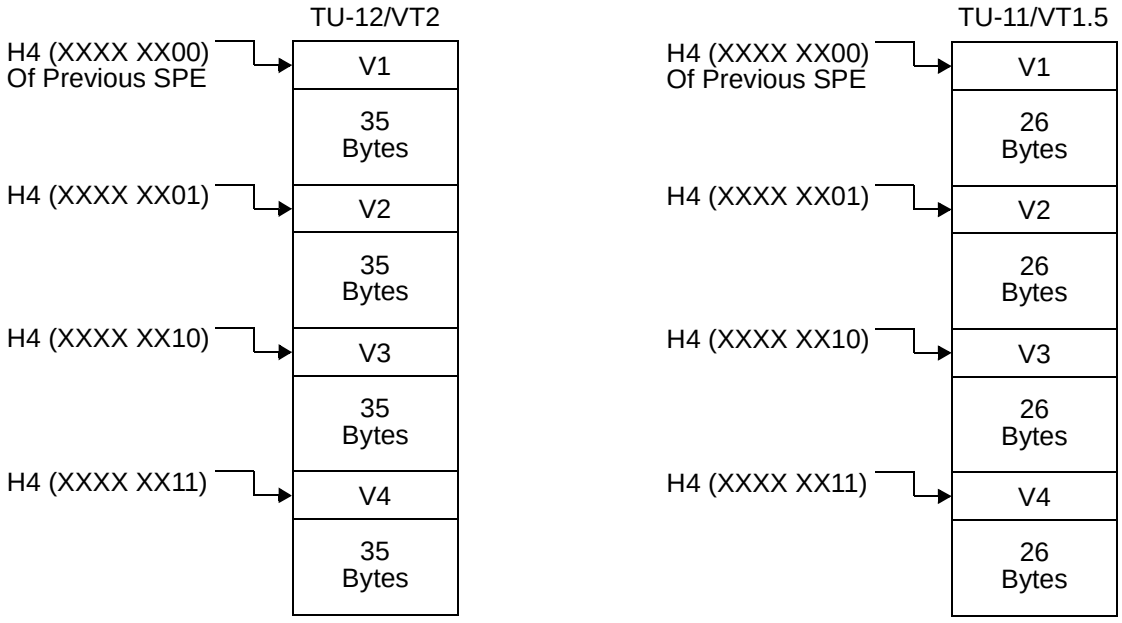


Figure 31. H4 Byte Floating VT Mode Bit Allocation

The H4 byte is monitored for multiframe alignment when enabled. For STM-1 operation, there is only one H4 detector per A and B drop buses. For STS-3 operation, there are three H4 byte detectors, one for each STS-1 for the A side and for the B side drop buses. Each STS-1 may have its own phase regarding the H4 multiframe sequence.

When the H4 multiframe detector is enabled, an Out-Of-Multiframe alarm (AxHOOM and BxHOOM) is declared when an error is detected in bits 7 and 8 of the H4 byte (where x is 1, 2, or 3 for each of the STS-1 signals in an STS-3 or 1 for the STM-1 VC-4 format). Recovery occurs when an error free H4 byte sequence is detected in four consecutive frames (beginning with the detection of the 00 code).

Once in the OOM state, if recovery does not take place within 1 ms, an Out-Of-Multiframe alarm (AxHLOM and BxHLOM) is declared (where x is 1, 2, or 3 for each of the STS-1 signals in an STS-3 or 1 for the STM-1 VC-4 format). Recovery occurs upon recovering of the AxHOOM or BxHOOM alarm.

SDH/SONET AIS DETECTION

The TEMx28 can detect an upstream SONET/SDH AIS condition using either the H1/H2 pointer bytes or the E1 order wire byte. The selection is according to the following table.

HEAISE (bit 0, 01DH)	SE1AIS (bit 1, 01DH)	Action
0	X	No upstream AIS monitoring performed.
1	0	The H1/H2 bytes are monitored for upstream AIS.
1	1	The E1 byte is monitored for upstream AIS.

Note: VT/TU AIS is detected by each of the pointer tracking state machines independently of the SONET/SDH H1/H2 or E1 byte AIS detection circuitry.

When the control bit STS3 (bit1, 01AH) selects the VC-4/TUG-3 format, the H1 and H2 bytes or the E1 byte per A and B drop buses are monitored for AIS. When the STS3 control bit selects the STS-3 or AU-3 format, each set of the three H1/H2 bytes or the E1n bytes per A Drop and B Drop buses are monitored for an AIS indication. Each of the three H1/H2 pointer bytes or E1n bytes corresponds to the like-numbered AU-3/STS-1 signal (n=1-3).

When the H1/H2 bytes are selected and if all ones are detected in the H1/H2 bytes in the A drop bus for three consecutive frames, the alarm bits AxUAIS will set, where x is equal to 1, 2, or 3, which corresponds to the like numbered STS-1. For a VC-4 format, x is equal to 1 only. If all ones are detected in the H1/H2 bytes in the B drop bus for three consecutive frames, the alarm bits BxUAIS will set. Recovery occurs when a normal NDF (bits 1 through 4) in H1 is detected for three consecutive frames.

When the E1n bytes are monitored for an upstream AIS condition majority logic is used to determine if an E1n byte is carrying an upstream AIS indication. If five or more ones are detected in an A/B Drop bus E1n byte, the alarm bit AxUAIS or BxUAIS is set. Recovery occurs when four or less ones are detected in the byte.

TU/VT POINTER TRACKING

The starting location of the V1 byte is determined by either the V1 pulses in the A/BC1J1V1 signals or the H4 multiframe detection circuits, as described in an earlier section. The TU/VT pointer bit assignment for the V1 and V2 bytes is shown below. The alignment is necessary to determine the starting locations of the V5 byte and the other bytes that are carrying the DS1 or E1 format.

	V1 Byte							V2 Byte							
1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
N	N	N	N	SS-bits		I	D	I	D	I	D	I	D	I	D

I = Increment Bit
D = Decrement Bit
N = New Data Flag Bit
(enabled = 1001 or 0001/1101/1011/1000, normal or disabled = 0110 or 1110/0010/0100/0111)
SS-bits (VT Size) = 11 for DS1 (1544 kbit/s) and 10 for E1 (2048 kbit/s)

Pointer Bytes Bit Assignment

The pointer value is a binary number with a range of 0 to 103 for the DS1 (1544 kbit/s) and 0 to 139 for the E1 (2048 kbit/s) format. The pointer offset indicates the offset from the V2 byte to the V5 byte in the VT1.5/TU-11 or TU-12/VT2 mapping. The pointer bytes are not counted in the offset calculation. The pointer offset arrangement for this format is shown below.

VT1.5/TU-11
V1
78
79-102
103
V2
0
1-24
25
V3
26
27-50
51
V4
52
53-76
77

VT2/TU-12
V1
105
106-138
139
V2
0
1-33
34
V3
35
36-68
69
V4
70
71-103
104

TU/VT Pointer Offset Locations

Fifty-six independent pointer-tracking state machines are used in the TEMx28, one for each channel in the A and B drop buses. The values of the V1/V2 pointer bytes in each multiframe are provided in registers X+183H and X+184H for the A side, and registers X+203H and X+204H for the B side. The pointer tracking algorithm is illustrated in the following Figure 32. The pointer tracking state machine is based on the pointer tracking state machine defined in the ETSI and ANSI requirements. When control bit PTALTE (bit 1, 01BH) is 0, the transition from AIS to LOP is disabled (shown dotted).

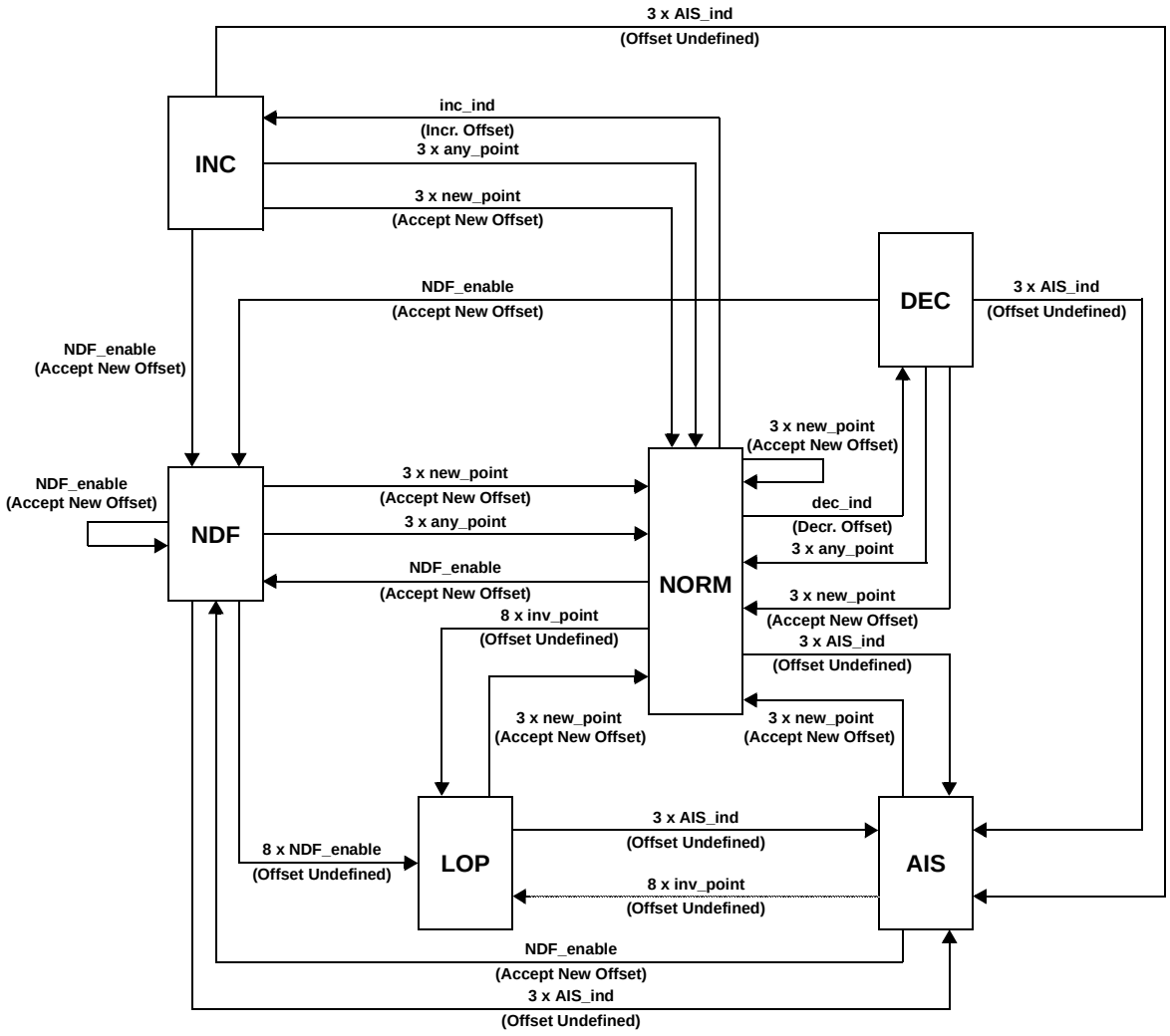


Figure 32. VT/TU Pointer Tracking State Machine

The AIS Indication (A/BnAIS) is provided in bit 3 of registers X+111/X+191H.
The LOP Indication (A/BnLOP) is provided in bit 2 of registers X+111/X+191H.
The NDF Indication (A/BnNDF) is provided in bit 1 of registers X+111/X+191H.
The Wrong Size Indication (A/BnSIZE) is provided by bit 0 of registers X+111/X+191H.
The Positive Justification Counter is located in registers X+120H for the A side and X+1A0H for the B side.
The Negative Justification Counter is located in registers X+121H for the A side and X+1A1H for the B side.

Pointer Tracking State Machine States Definition

Event	Definition
norm_point	Disabled NDF (0110, 1110, 0010, 0100, 0111) AND match of SS-bits AND receive pointer offset value equal to active offset value.
NDF_enable	NDF enabled (1001, 0001, 1101, 1011, 1000) AND match of SS-bits AND received pointer offset value in range.
AIS_ind	pointer = 11111111 11111111 (FF Hex, FF Hex)
inc_ind	NDF disabled (0110, 1110, 0010, 0100, 0111) AND match of SS-bits AND a match of 8 or more of the 10 I and D bits. Please note that this requirement differs from the majority of I bits inverted and no majority of D bits received.
dec_ind	NDF disabled (0110, 1110, 0010, 0100, 0111) AND match of SS-bits AND a match of 8 or more of the 10 I and D bits. Please note that this requirement differs from the majority of D bits inverted and no majority of I bits received.
inv_point	Not norm_point AND NOT NDF_enable AND NOT AIS_ind AND NOT {(inc_ind or dec_ind) AND norm_state}.
8 x NDF_enable	8 consecutive NDF_ enable.
3 x AIS_ind	3 consecutive AIS_ind.
3 x any_point	3 x NOT NDF_enable AND NOT 3 x AIS_ind AND NOT 3 x new_point.
new_point	Disabled NDF (0110, 1110, 0010, 0100, 0111) AND match of SS-bits AND receive pointer offset value in range but not equal to the active offset value.
3 x new_point	3 consecutive new_point received.

Notes:

1. The active offset value is defined as the accepted current phase of the VT1.5/VT2 in the state norm_state and is undefined in other states.
2. NDF Enabled is defined as one of the following bit patterns: 1001, 0001, 1101, 1011, 1000.
3. NDF Disabled is defined as one of the following bit patterns: 0110, 1110, 0010, 0100, 0111.
4. The remaining six NDF codes (0000, 0011, 0101, 1010, 1100 and 1111) result in an inv_point indication. The NDF code 1111 does not result in an inv_point indication if it is part of an AIS_ind.
5. Note that the new_point is also an inv_point.
6. 3 x new_point takes precedence over other events.
7. The second and third offset value received in 3 x new_point must be identical with the first.
8. The consecutive new_point counter is reset to 0 on a change of state, except for transitions occurring among the INC, DEC, NDF and NORM states.
9. The consecutive inv_point counter can be incremented in all states. The consecutive inv_point counter is not reset on a change of state.
10. The consecutive AIS_ind counter is not reset on a change of state.
11. The consecutive NDF_enable counter is reset to zero on a change of AIS to NDF state. Otherwise the counter is not reset.
12. Inc_ind/dec_ind causes the active offset value to be incremented/decremented, respectively. The subsequent detection of a 3 x new_point with an offset value equal to the offset value caused by inc_ind/dec_ind will not cause the new pointer flag to assert.
13. SS-bits match for DS1 is 11 and 10 for E1.

OVERHEAD BYTE PROCESSING

In addition to overhead byte (V5, J2, N2, and K4 bytes) processing, all four overhead bytes for both the A and B drop buses are written into single byte locations for the channel selected, every 500 microseconds.

V5 Byte Processing

The placement of bits within the V5 byte is shown below.

Bit	1	2	3	4	5	6	7	8
	BIP-2		REI	RFI	Signal Label			RDI
	MSB							LSB

BIP-2

Bits 1 and 2 are used for error performance monitoring. A Bit Interleaved Parity scheme is used. One or two errors may be detected in the BIP-2 comparison, and they are counted individually in an 8-bit counter when control bit BLOCK (bit 4, 01AH) is written with a 0. When control bit BLOCK is written with a 1, one or two parity errors are counted as a single block error.

Remote Error Indication (REI)

A Remote Error Indications (REI) is sent by the distant end when one or two errors are detected in the BIP-2. Otherwise it is set to 0. A Remote Error Indication (REI) is counted in an 8-bit counter.

Remote Failure Indication (RFI)

The Remote Failure Indication (RFI) is normally used for byte synchronous applications and is normally set to 0. If the received value is equal to 1 five times consecutively, an RFI alarm indication (AnRFI (bit 0, X+110H) for A drop or BnRFI (bit 0, X+190H) for B drop) is asserted. Recovery occurs when bit 4 of the V5 byte is equal to 0 five times consecutively.

Signal Label

Bits 5, 6, and 7 in the V5 byte provide a signal label. The TEMx28 provides the following monitoring circuits for the signal label:

- Signal label Mismatch Detection
- Unequipped Detection
- VC AIS Detection

Remote Defect Indication Detection

There are two Remote Defect Indication schemes defined: single bit RDI and three bit RDI. A common circuit per channel is used to detect both the three bit RDI states, and the single bit RDI state. The single bit RDI scheme is defined for SDH applications, while three bit RDI is defined for SONET applications. Single bit RDI uses bit 8 in the V5 byte, while three bit RDI uses bits 5, 6 and 7 in the K4 byte, in conjunction with bit 8 in the V5 byte. Three bit RDI (or enhanced RDI) allows the user to differentiate between server, connectivity, and payload defects. Bit 8 in V5 is set equal to bit 5 in the K4 byte. Bit 7 in the K4 byte is set to the inverse of bit 6 in the K4 byte in order to distinguish the enhanced version of RDI from single bit RDI. It should be noted that when bits 6 and 7 in the K4 byte are either 01 or 10, the RDI indication is also influenced by bit 8 in the V5 byte, as shown in the table below. When bits 6 and 7 are either 00 or 11, then RDI is determined solely by bit 8 in the

V5 byte. This allows detection of an RDI originating from equipment that generates single bit RDI in the V5 byte. The following table lists the RDI defect indications that may be carried in the V5 and K4 bytes.

Bit 8 V5	Bit 5 K4	Bit 6 K4	Bit 7 K4	Definition
0	0	0	0	No defect indications
0	0	0	1	No defect indications
0	0	1	0	Remote Payload Defect, indicates a: - Path Label Mismatch
0	0	1	1	No defect indications
0	1	0	0	No defect indications
0	1	0	1	No defect indications
0	1	1	0	No defect indications
0	1	1	1	No defect indications
1	0	0	0	Remote defect indication (single bit RDI)
1	0	0	1	Remote defect indication (single bit RDI)
1	0	1	0	Remote defect indication (single bit RDI)
1	0	1	1	Remote defect indication (single bit RDI)
1	1	0	0	Remote defect indication (single bit RDI)
1	1	0	1	Remote Server Defect; indicates a: - VT Loss of Pointer - VT AIS detected - Upstream AIS detected (E1 or H1/H2 Bytes).
1	1	1	0	Remote Connectivity Defect - Unequipped Signal Label - J2 Mismatch - J2 Loss of Lock
1	1	1	1	Remote defect indication (single bit RDI)

Three Bit RDI and Single Bit RDI Detection

Receive RDI Detection and Recovery

The RDI alarm indications are defined in the table below. The number of consecutive events for detection and recovery is controlled by control bit V5AL10 (bit 0, 01BH). The value of five is selected when the V5AL10 control bit is 0, and the value of ten is selected when the V5AL10 control bit is 1. The number of detection and recovery events is valid for both three bit RDI and single bit RDI.

AnRDIC BnRDIC	AnRDIP BnRDIP	AnRDIS BnRDIS	Action
0	0	1	Remote Server Defect Indication, and a single bit RDI indication (Bit 8 in the V5 byte).
0	1	0	Remote Payload Defect Indication.
1	0	0	Remote Connectivity Indication.

RDI Alarm Definitions

J2 Byte Processing

There are two possible received J2 message sizes, 16 bytes (ITU-T), or 64 bytes (ANSI). The TEMx28 is capable of dimensioning the transmit RAM memory segment to the two sizes (16-Byte or 64-Byte). In addition, two modes of operation are provided for the 16-byte (ITU-T) format: a microprocessor read mode, and a compare read mode. The following table lists the various control states associated with J2 processing. Please note: The 64 byte RAM is used on a shared basis with the J2 and N2 bytes. When the 64 byte RAM is configured for a 64 byte J2 message, the N2 tandem connection feature is disabled. When the RAM segment is configured for a 16 byte J2 byte message, two 16 byte segment are provided for the Tandem Connection feature when enabled, and for the J2 byte processing feature.

ARnJ2S1 (bit 1, X+010H) BRnJ2S1 (bit 1, X+080H)	ARnJ2S0 (bit 0, X+010H) BRnJ2S0 (bit 0, X+080H	Action
0	0	Receive J2 segment for channel n is configured for the 16-byte J2 message size. The bytes are written into the segment on a rotating basis, starting with an arbitrary address. The J2 alarms are disabled.
0	1	Receive J2 segment for channel n is configured for the 16-byte J2 message size, and comparison. The received 16-byte message is compared against a 16 byte microprocessor written message, that must be aligned to the starting address of the segment. The J2 alarms are enabled.
1	0	Receive J2 segment for channel n is configured for the 64-byte J2 message size. The bytes are written into the segment on a rotating basis, starting with an arbitrary address. The J2 alarms are disabled.

ARnJ2S1 (bit 1, X+010H) BRnJ2S1 (bit 1, X+080H)	ARnJ2S0 (bit 0, X+010H) BRnJ2S0 (bit 0, X+080H	Action
1	1	Receive J2 segment for channel n is configured for the 64-byte J2 message size with alignment only. Receiving an ASCII CR/LF will synchronize an internal counter so that the next character after the last LF character will be written into the starting address of the 64 byte segment. The J2 alarms are disabled.

The ITU-T defined 16-byte message consists of an alignment signal of (10000000 00000000) in the most significant bit (bit 1) of the message. The remaining 7 bits in each byte carry a data message, as illustrated below.

Bit	1	2	3	4	5	6	7	8
	1	16-Byte J2 Message						
	0							
	0							
	0							
	0							
	0							
	0							
	0							
	0							
	0							
	0							
	0							
	0							
	0							
	0							

ITU-T 16-Byte J2 Message Format

The J2 16-byte message comparison works according to the following steps:

1. The microprocessor-written J2 byte segment should be initialized with a 16-byte message before enabling the J2 message comparison function.
2. The J2 message comparison function is then enabled (A/BRnJ2S0 = 1; A/BRnJ2S1 = 0) and immediately the J2 Loss of Lock alarm will be active (A/BnJ2LOL = 1) and the J2 Trace Identifier Mismatch alarm will be inactive (A/BnJ2TIM = 0). This is the first step in the sequence - to initialize these alarms.
3. The incoming trace message is received, and the J2 comparison circuit searches for the J2 alignment pattern (Bit 1: 1000...0 pattern).
4. J2 alignment pattern is found and the Received stable trace message locations are updated with this incoming trace message.
5. The incoming trace message is then checked for three consecutive 16-byte message repeats.
6. If an error occurs before step 5 is completed, the sequence repeats, starting at step 3 (searching for the alignment pattern).
7. If the incoming trace message repeats three times in a row (after the alignment pattern is detected) without an error then this is an in-lock condition, and the J2 Loss of Lock alarm is reset (A/BnJ2LOL = 0). Note that at this time the J2 mismatch alarm is still inactive (A/BnJ2TIM =0).

8. Once the incoming trace message is in-lock, the stable message, is compared against the microprocessor-written reference message, byte for byte, for 16 bytes (the length of the multiframe message). If they compare, a match is declared, with no mismatch alarm (A/BnJ2TIM = 0). If they do not compare, a trace mismatch alarm is declared (A/BnJ2TIM = 1). There is no Loss of Lock alarm (A/BnJ2LOL = 0) because the incoming trace message is stable.
10. If the incoming message changes for three consecutive 16-byte messages, a loss of lock alarm (A/BnJ2LOL = 1) occurs and the sequence starts again from the beginning (step 2).

N2 Byte (Tandem Connection)

The Tandem Connection feature is enabled by writing a 1 to control bit ARnTCEN (bit 5, X+010H) for the A drop side or BRnTCEN (bit 5, X+080H) for the B drop side, when control bit ARnJ2S1 (bit 1, X+010H) and BRnJ2S1 (bit 1, X+080H) is a 0. When control bit ARnJ2S1 (BRnJ2S1) is written with a 1, the Tandem Connection feature for the A Drop (B Drop) VT/TU is disabled. When control bit ARnTCEN or BRnTCEN is written with a 0, the tandem connection feature is disabled. The bit placement in a received N2 byte configured for Tandem Connection operation is shown below:

Bit	1	2	3	4	5	6	7	8
	BIP-2		1	AIS Indication	TC REI	TC OEI	Trace ID TC RDI/ODI	
	MSB							LSB

TC BIP-2 Processing

One or two errors may be detected in the TC BIP-2 comparison, and they are counted individually in an 8-bit counter when control bit BLOCK (bit 4, 01AH) is written with a 0. When control bit BLOCK is written with a 1, one or two parity errors are counted as a single block error.

TC AIS Indication

A tandem connection AIS alarm (AnTCAIS, BnTCAIS) is declared when bit 4 is equal to 1 for five consecutive frames. Recovery occurs when bit 4 is equal to 0 for five consecutive frames.

TC REI Processing

An 8-bit counter (An TC REI Counter, Bn TC REI Counter) is provided for counting the number of REI bits received as equal to 1 in bit 5 (TC REI) in the N2 byte. An REI indication indicates that the distant end has detected one or two errors when the BIP-2 calculated for frame f-1 (all the bytes) is compared against the BIP-2 value carried in the N2 byte in frame f.

TC OEI Processing

An 8-bit counter (An TC OEI Counter, Bn TC OEI Counter) is provided for counting the number of OEI bits received as equal to 1 in bit 6 (TC OEI) in the N2 (Z6) byte. An OEI indication (a 1) indicates that the distant end has detected one or two errors when the BIP-2 calculated for frame f-1 is compared against the BIP-2 value carried in the V5 byte in frame f.

BITS 7 and 8

A multiframe alignment pattern, trace identifier message, TC RDI and TC ODI indications are assigned to bits 7 and 8 in the frames of a 76-frame structure, as shown below:

Frame No.	N2 Byte Definition
1 - 8	Frame Alignment, 1111 1111 1111 1110
9 - 12	TC Trace ID Byte No. 0 (1 CRC-7)
13 - 16	TC Trace ID Byte No. 1 (0 X X X X X X X)
17 - 20	TC Trace ID Byte No. 2 (0 X X X X X X X)
21 thru 64	TC Trace ID Bytes No. 3 thru 13
65 - 68	TC Trace ID Byte No. 14 (0 X X X X X X X)
69 - 72	TC Trace ID Byte No. 15 (0 X X X X X X X)
73	Bit 7 = 0, Bit 8 = TC RDI
74	Bit 7 = TC ODI, Bit 8 = 0
75	Bit 7 = 0, Bit 8 = 0
76	Bit 7 = 0, Bit 8 = 0

Loss of multiframe (status bits AnTCLM, BnTCLM) occurs when two consecutive Frame Alignment Signals (1111 1111 1111 1110) are detected in error (i.e., one or more error in each FAS). Multiframe alignment is recovered when one consecutive non-errored FAS are found.

The TC trace identifier message comparison is based on the same state machine as that used for the 16-byte J2 message. The TC lock is removed when 3 messages are received in error and the AnTCLL or BnTCLL alarm is declared. The TC lock is established when 3 valid, identical messages are received. A comparison is performed between the microprocessor-written TC and the contents of the incoming message. The message consists of TC Trace ID bytes 0 to 15. A TC Trace Identifier Mismatch (AnTCTM, BnTCTM) alarm is declared when any byte does not match. Recovery occurs when there is a match between the microprocessor message and the accepted message.

Bit 8 in frame 73 is defined as a Tandem Connection Remote Defect Indication (TC RDI). A TC RDI alarm occurs when a 1 has been detected in bit 8 in frame 73 for five consecutive multiframes (where each multiframe is 38 ms). The TC RDI alarm state is exited when bit 8 is equal to 0 for five consecutive multiframes. An alarm indication is reported as AnTCRDI or BnTCRDI.

Bit 7 in frame 74 is defined as a Tandem Connection Outgoing Defect Indication (TC ODI). A TC ODI alarm occurs when a 1 has been detected in bit 7 in frame 74 for five consecutive multiframes (where each multiframe is 38 ms). The TC ODI alarm state is exited when bit 7 is equal to 0 for five consecutive multiframes. An alarm indication is reported as AnTCODI or BnTCODI.

Tandem Connection Unequipped Status

Unequipped Tandem Connection detection is provided. Five or more consecutive received tandem connection N2 bytes equal to XX00 0000 result in a TC unequipped indication (AnTCUQ, BnTCUQ). The alarm state is exited when five or more consecutive received tandem connection N2 (Z6) bytes are not equal to XX00 0000. Note that bits 1 and 2 of the N2 (Z6) byte are masked (shown as X) and do not affect the detection. The XX represents a don't care value and may be equal to a BIP-2 value.

OVERHEAD COMMUNICATIONS BIT ACCESS

Microprocessor access is provided for the eight overhead communications bits (O-bits) carried in the two justification control (JC) bytes in the multiframe format, e.g., in a 1544 kbit/s Tributary, shown partially below. The bits in the justification control byte are numbered 1 through 8, starting with C1 as bit 1.

	Other Bytes							
	J2 Byte							
JC Byte 1	C1	C2	O(1)	O(2)	O(3)	O(4)	D	R
	24 Bytes - Information							
	N2 Byte							
JC Byte 2	C1	C2	O(5)	O(6)	O(7)	O(8)	D	R
	Other Bytes							

O-bit Placement in a 1544 kbit/s Tributary

In the receive direction, the eight O-bits are stored in 8-bit registers for each channel assigned for the A and B drop buses. The A side register location is X+18AH, and B side register location is X+20AH. The O-bit registers are updated each multiframe with the two O-bit nibbles from the same multiframe. Bits 7 through 4 in an O-bit register correspond to bits 3 through 6 (C1C2 OOOO DR) in the first justification control byte, and bits 3 through 0 in an O-bit register correspond to bits 3 through 6 in the second justification control byte, as shown below.

Register	7	6	5	4	3	2	1	0
O-bits	O(1)	O(2)	O(3)	O(4)	O(5)	O(6)	O(7)	O(8)

O-bit Assignment Memory Map

VT/TU RECEIVE INTERFACE

The VT/TU interface provides user access to the 104 byte VC-11 or the 140 byte VC-12 with or without the overhead bytes. The VT/TU interface is enabled when control bits RnLINT1 (bit 7, X+006H) and RnLINT0 (bit 6, X+006H) are set to 11. The options associated with this interface are given in the following table.

RnSEL (bit 2, X+006H)	RnVTVC (bit 4, X+008H)	Interface Selected
0	0	A side payload bytes provided. The V5, J2, N2, and K4 overhead bytes are not provided. The clock is gapped during the overhead byte times. A positive frame pulse determines the last bit of the frame.
0	1	A side payload bytes provided. The V5, J2, N2, and K4 overhead bytes are provided. A positive frame pulse determines the last bit of the frame.
1	0	B side payload bytes provided. The V5, J2, N2, and K4 overhead bytes are not provided. The clock is gapped during the overhead byte times. A positive frame pulse determines the last bit of the frame.
1	1	B side payload bytes provided. The V5, J2, N2, and K4 overhead bytes are provided. A positive frame pulse determines the last bit of the frame.

RECEIVE CROSS MAPPING APPLICATIONS

The TEMx28 supports cross mapping applications in which a DS1 format is carried in a VC-12 for transport by a VT2/TU-12. The options associated with this feature are given in the following table. The cross mapping feature control in the drop direction is independent of the add direction. Please note: the cross connect feature will not be supported when the VT/TU interface for channel n is selected.

Bit 7, X+012H/082H VT/TU Select Register A/B Drop	RnE1SL, Bit 4, X+006H	Operation
0	0	DS1 Asynchronous format demapped from a VT1.5/TU-11.
0	1	Not used.
1	0	Cross Mapping. DS1 Asynchronous format demapped from a VT2/TU-12.
1	1	E1 Asynchronous format demapped from a VT2/TU-12.

LINE AIS INSERTION

An Alarm Indication Signal (AIS) is defined as an unframed all ones signal for both the DS1 (1544 kbit/s) and E1 (2048 kbit/s) line rates. Line AIS will be inserted into the interface data lead (including the VT/TU) interface for channel n for the drop bus alarms when enabled. In addition, the microprocessor can also force the AIS state independent of the drop side alarms. When control bit RnSEL is a 0, the A side Drop bus VT/TU is selected. When RnSEL is a 1, the B side drop bus VT/TU is selected. The following is a list of alarms and enable bits for controlling the insertion of receive line AIS.

- When control bit RnAISE is a 1 and the side that is active (RnSEL bit state):
  - Drop Bus Loss Of Clock (ADLOC, BDLOC) when DLCAE is a 1
  - Drop Bus AIS alarm (AxUAIS, BxUAIS) when HEAISE and UAISE are 1
  - Loss of pointer alarm (AnLOP, BnLOP)
  - VT/TU AIS detected (AnAIS, BnAIS)
  - Unequipped signal label (AnUNEQ, BnUNEQ) when UQAISE is a 1
  - Mismatch signal label (AnSLER) when PLSAISE is a 1
  - J2 Loss Of Lock Alarm (AnJ2LOL, BnJ2LOL) when J2AISEN is a 1
  - J2 Mismatch Alarm (AnJ2TIM, BnJ2TIM) when J2AISEN is a 1
  - VT AIS detected (AnVCAIS, BnVCAIS) when VCAISE is a 1
  - TC Loss Of Multiframe (AnTCLM, BnTCLM), TC enabled and TCTAE is a 1
  - TC Loss Of Lock Alarm (AnTCLL, BnTCLL), TC enabled and TCTAE is a 1
  - TC Mismatch Alarm (AnTCTM, BnTCTM), TC enabled and TCTAE is a 1
  - TC Unequipped Alarm (AnTCUQ, BnTCUQ), TC enabled and TCUAE is a 1
  - TC AIS Detected (AnTCAIS, BnTCAIS), TC enabled and TCAISE is a 1
  - Control bit RnSAIS is a 1)
  - FIFO alarm (AnRFFE, BnRFFE)

- When control bit RnAISE is a 0:
  - Control bit RnSAIS is a 1)

Note: The AIS will be sent for two to three multiframes when a receive FIFO error occurs.

RECEIVE INTERFACE

The TEMx28 provides the user with three interface choices per channel. The options associated with this interface are given in the following table. The receive interface selection is independent of the transmit interface selection.

RnLINT1 (bit 7, X+006H)	RnLINT0 (bit 6, X+006H)	RnOUTL (bit 5, X+006H)	Interface Selected
0	0	0	All interface leads forced to the high impedance state.
0	0	1	All interface leads forced to the 0 state.
0	1	X	NRZ Interface selected.
1	0	X	Rail Interface selected.
1	1	X	VT/TU Interface selected.

The line interface rate is selected according to the following table:

RnE1SL (bit 4, X+006H)	Interface Rate Selected
0	DS1 rate (1.544 Mbit/s)
1	E1 rate (2.048 Mbit/s)

TRANSMIT INTERFACE

The TEMx28 provides the user with three interface choices per channel. The options associated with this interface are given in the following table. The transmit interface selection is independent of the receive interface selection.

TnLINT1 (bit 7, X+002H)	TnLINT0 (bit 6, X+002H	Interface Selected
0	0	Not used.
0	1	NRZ Interface selected.
1	0	Rail Interface selected.
1	1	VT/TU Interface selected.

Interface Rate Selection

The line interface rate is selected according to the following table:

TnE1SL (bit 4, X+002H)	Interface Rate Selected
0	DS1 rate (1.544 Mbit/s)
1	E1 rate (2.048 Mbit/s)

VT/TU Interface

The VT/TU interface is selected when control bits TnLINT1/0 (bits 7 and 6, X+002H) are set to 11. The TnSEL1/0 (bits 1 and 0, X+006H) and RnSEL (bit 2, X+006H) control bits determine the drop buses and add buses from which a VT/TU is dropped and added. The VT/TU interface is not valid for dual unidirectional ring mode of operation (TnSEL1/0 are 11). Four framing pulse lead references are provided: VTA1.5 (VT1.5s for A add bus), VTA2 (VT2s for A add bus, VTB1.5 (VT1.5s for B add bus) and VT2 (VTs for B add bus). The overhead byte option associated with this interface is selected according to the following table:

TnVTVC (bit 1, X+007H)	Overhead Byte Access
0	Gapped output clock. The overhead bytes V5, J2, N2, and K4, in the data stream are not clocked in. The clock is gapped during the overhead byte times.
1	Symmetrical output clock. The overhead bytes in the data stream are not clocked in except for bits 1 and 2 in the K4 byte. Bits 3 through 8 in the K4 byte are ignored. Bits 1 and 2 are inserted and transmitted from the VT/TU interface. Bits 1 and 2 define an extended signal label and virtual concatenation information pertaining to the payload.

CODEC

When the rail interface is selected, the CODEC may be configured for the AMI code, or B8ZS/HDB3. When control bit TnB8ZS (bit 2, X+002H) is set to 0, the CODEC is configured for the AMI line code for both the DS1 and E1 line rates. When this control bit is set to 1, the B8ZS line code is selected for the DS1 line rate, and the HDB3 line code is selected for the E1 rate. A coding error is processed in the following way:

- A string of 16 or more zeros is counted as a coding violation when the line code is AMI (DS1 or E1).
- A string of more than 4 zeros is counted as a coding violation when the line code is HDB3 (E1).
- A string of more than 8 zeros is counted as a coding violation when the line rate is B8Zs (DS1).

Coding violation are counted in a 16 bit counter in addition to one second counters. When the interface for channel n is selected for a NRZ interface, the negative Rail lead may be used to input either an external loss of signal indication or external coding violations. When control bit EXnLOS (bit 1, X+003H) is set to 0, external coding may be counted. When set to 1, an external loss of signal may be inputted. An external loss of signal indication must be present for a minimum of 8 clock cycles (DS1 or E1). The active sense associated with the external loss of signal indication is controlled by control bit EXnLOSP (bit 0, X+003H). When control bit EXnLOSP is a 1, the sense is active high. External violations are counted when $\overline{\text{TLOSn}}$ is high and the selected TCLKn edge occurs. TCLKn edge selection is done with control bit TnCLKI.

Loss Of Signal Detection

The rail interface only is monitored for a loss of signal. A loss of signal alarm (TnLOS) for the DS1 line rate is declared when no transitions are detected on the positive and negative rail leads for 175 +/- 75 consecutive pulse positions. Recovery occurs when the average pulse density of at least 12.5% occurs over 175 +/- 75 pulse positions.

A loss of signal alarm for the E1 line rate is declared when no transitions are detected on the positive and negative rail leads for 256 consecutive pulse periods. Recovery occurs when there are at least 32 transitions counted on the positive and negative rail leads for 256 consecutive clock cycles.

Clock Inversion

The transmit data for each of the Rail and NRZ interfaces can be clocked in on either negative or positive transitions of the input clock for each channel. When control bit TnCLKI (bit 3, X+002H) is a 0, transmit data is clocked in negative transitions of the input clock. When a 1 is written to this control bit, data is clocked in on positive transitions of the clock.

For the VT/TU interface selection, when control bit TnCLKI is set to 0, the framing pulses are clocked out positive transitions of the output clock, while data is clocked in on negative transitions of the clock. When control bit TnCLKI is set to 1, the framing pulses are clocked out negative transitions of the output clock, while data is clocked in on positive transitions of the clock.

NRZ Data Inversion

An option is provided which enables the data stream to be inverted when the NRZ interface only is selected independently in both the receive and transmit directions. When control bit TnNRZP (bit 5, X+002H) is set to 1, the NRZ data stream will be inverted.

LINE AIS DETECTION

The transmit NRZ and Rail line signals are monitored for line AIS. A line AIS condition is defined as an all ones unframed signal for both the DS1 and E1 line rates. A line AIS alarm (TnAIS) for the DS1 line rate is declared when 99.9% or more ones are detected in the received signal for a period of 48 ms. Recovery occurs when the receive signal has fewer than 99.9% of ones in a 48 ms period.

An AIS alarm for the E1 rate is declared when the signal has two or less zeros in each of two consecutive double frame period (four frames). Recovery occurs when each of two consecutive double frame periods contain three or more zeros.

LINE AIS GENERATION

The TEMx28 provides the ability to generate a line AIS signal on a per channel basis. Line AIS for the DS1 (1544 kbit/s) and for the E1 (2048 kbit/s) line rate is defined as an unframed all ones signal. The following is a list of alarms and enable bits for controlling the insertion of transmit line AIS.

- When control bit TnAISE is a 1 and any of the following alarms occur:
  - Transmit Loss Of Clock (TnLOC)
  - Transmit Loss Of Signal (TnLOS) when the Rail interface is selected
  - External Loss Of Signal (TnLOS) when the NRZ interface is selected and control bit EXnLOS is a 1
  - When control bit TnSAIS is a 1

- When control bit TnAISE is a 0:
  - When control bit TnSAIS is a 1

Note: When control bit TnAISE is a 0 and the Transmit Loss of Clock (TnLOC) alarm occurs, transmit line AIS may be generated regardless of the state of control bit TnSAIS.

TRANSMIT CROSS MAPPING APPLICATIONS

The TEMx28 supports cross mapping applications in which a DS1 format is carried in a VC-12 for transport by a VT2/TU-12. The options associated with this feature are given in the following table. The cross mapping feature control in the add direction is independent of the drop direction. Please note: the cross connect feature will not be supported when the VT/TU interface for channel n is selected.

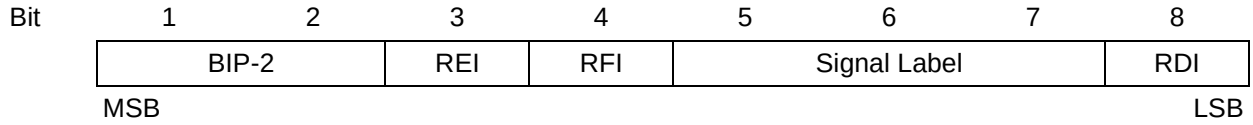
Bit 7 X+01AH, 08AH VT/TU Select Register A/B Add	TnE1SL (bit 4, X+002H)	Operation
0	0	DS1 Asynchronous format mapped to a VT1.5/TU-11.
0	1	Not used.
1	0	Cross Mapping. DS1 Asynchronous format mapped to a VT2/TU-12.
1	1	E1 Asynchronous format mapped to a VT2/TU-12.

OVERHEAD BYTE INSERTION

In general, the transmitted overhead byte states (V5, J2, N2, and K4 bytes) for each channel may be controlled by internal alarm states, or by the microprocessor.

V5 Byte

The placement of bits with in the V5 byte is shown below.



BIP-2

Bits 1 and 2 in the V5 byte carry a Bit Interleaved Parity - 2 (BIP-2). Bit 1 is set so that the parity of all odd numbered bits (1, 3, 5, and 7) in all the bytes in the previous VC-11/VC-12 is even, while bit 2 is set similarly for all even numbered bits.

The calculation includes all of the payload and overhead bytes, but excludes the V1, V2, V3 and the V4 bytes. BIP-2 errors can be transmitted by setting control bit ATnFB2 (bit 3, register X+064H) or BTnFB2 (bit 3, register X+0D4H) for the A and B side add buses respectively.

Remote Error Indication Bit

Bit 3 carries a remote error indication (REI). This bit carries the block error indication from the incoming BIP-2 comparison performed in the drop direction for the VT/TU selected for channel n. The TEMx28 provides a synchronization circuit between the dropped TU/VT and the added TU/VT to prevent lost counts due to differences in clock phases between the drop and add sides. Single REI can be transmitted by setting control bit ATnFFB (bit 6, register X+065H) or BTnFFB (bit 6, register X+0D5H) for the A and B side add buses respectively.

Remote Failure Indication

The transmit remote failure indication for the VT/TU selected is controlled by control bit ATnRFI (bit 7, X+064H) or BTnRFI (bit 7, X+0D4H) for the A and B side add buses respectively. When control ATnRFI or BTnRFI is set to 1, bit 4 in the V5 byte is transmitted as a 1.

Signal Label

Bits 5, 6, and 7 provide a signal label for the distant end. There are eight possible states. Any value other then 000 represents an equipped VT/TU. The values written into ATnSL1-3 (bits 5-3, register X+065H) and BTnSL1-3 (bits 5-3, register X+0D5H0, for the A and B side add buses respectively, are transmitted in the V5 byte bits 5-7.

Remote Defect Indication

The TEMx28 supports both single bit and three bit RDI operation. The selection of single bit or three bit RDI is determined by the value written to control bit TnDISB (bit 0, X+007H). When control bit TnDISB is set to 0, three bit RDI operation is selected. When this control bit is set to 1, single bit RDI is selected.

Single Bit RDI

Bit 8 in the V5 byte provides a single bit RDI state, as indicated in the following table. ITU Recommendation G.707 recommends that bits 5, 6, and 7 in the K4 byte be transmitted as 000 or 111.

Bit 8 V5	Definition
0	No defect indications.
1	Remote Defect Indication

A single bit RDI state is sent for the following unlatched alarm conditions in the V5 overhead byte of the VT/TU selected for the A or B Add bus, depending on the states of the RnSEL (active bus selected), TnSEL1 and TnSEL0 (bus enabled) control bits. RDI is sent for a minimum of 20 multiframes (500 microseconds per multi-frame).

- When control bit RDI enable (RnDIEN) is 1:
    - Drop bus loss of clock (ADLOC, BDLOC) when DLCRE is a 1
    - Upstream AIS in H1/H2 or the E1 byte (AxUAIS, BxUAIS), when HEAISE and URDIE are a 1
    - VT/TU AIS (AnAIS, BnAIS)
    - VT/TU Loss of Pointer (AnLOP, BnLOP)
    - VC AIS (AnVCAIS, BnVCAIS) when VCRDIE is a 1
    - Unequipped (AnUNEQ, BnUNEQ), when UQRDIE is 1
    - J2 Loss of Lock (AnJ2LOL, BnJ2LOL), when J2RDIE is a 1
    - J2 Mismatch (AnJ2TIM, BnJ2TIM), when J2RDIE is 1
    - Microprocessor writes a 1 to ATnRDIS, BTnRDIS
- When RDI enable (RnDIEN) is 0:
    - Microprocessor writes a 1 to ATnRDIS, BTnRDIS

Three Bit RDI

In addition to using bit 8 in the V5 byte, bits 5, 6, and 7 in the K4 byte are also used. Bit 8 in the V5 byte works in conjunction with bits, 5, 6, and 7 in the K4 byte to provide the following possible RDI states. Three bit RDI is recommended for ANSI North American applications:

Bit 8 V5 Bit 5 K4	Bit 6 K4	Bit 7 K4	Definition
0	0	0	No defect indications.
0	0	1	No defect indications.
0	1	0	Remote Payload Defect - Path Label Mismatch
0	1	1	No defect indications.
1	0	0	Single bit Remote Defect Indication
1	0	1	Remote Server Defect - VT Loss of Pointer - VT AIS detected - Upstream AIS detected (E1 or H1/H2 Bytes).
1	1	0	Remote Connectivity Defect - Unequipped Signal Label - J2 Mismatch - J2 Loss of Lock.
1	1	1	Single bit Remote Defect Indication.

Three bit RDI permits the user to differentiate between the SONET alarms at the distant end. The three RDI alarms are defined as: Remote Server Defect Indication, Remote Connectivity Defect Indication, and Remote Connectivity Defect Indication. The Remote Server Defect Indication has the highest priority, followed by the Remote Connectivity Defect Indication and the lowest priority, Remote Payload Defect Indication. A remote defect indication is sent for the following unlatched alarm conditions in the V5 and K4 overhead bytes of the VT/TU selected for the A or B Add bus, depending on the states of the RnSEL (active bus selected), TnSEL1 and TnSEL0 (bus enabled) control bits. A remote defect indication is sent for a minimum of 20 multiframes (500 microseconds per multiframe).

- When control bit RDI enable (RnDIEN) is 1, a Remote Server Defect Indication is sent for:
    - Drop bus loss of clock (ADLOC, BDLOC) when DLCRE is a 1
    - Upstream AIS in H1/H2 or the E1 byte (AxUAIS, BxUAIS), when HEAISE and URDIE are a 1
    - VT/TU AIS (AnAIS, BnAIS)
    - VT/TU Loss of Pointer (AnLOP, BnLOP)
    - VC AIS (AnVCAIS, BnVCAIS) when VCRDIE is a 1
    - Microprocessor writes a 1 to ATnRDIS, BTnRDIS
- When control bit RDI enable (RnDIEN) is 1, a Remote Connectivity Defect Indication is sent for:
    - Unequipped (AnUNEQ, BnUNEQ), when UQRDIE is 1
    - J2 Loss of Lock (AnJ2LOL, BnJ2LOL), when J2RDIE is a 1
    - J2 Mismatch (AnJ2TIM, BnJ2TIM), when J2RDIE is 1
    - Microprocessor writes a 1 to ATnRDIC, BTnRDIC
- When control bit RDI enable (RnDIEN) is 1, a Remote Payload Defect Indication is sent for:
    - Mismatch Signal Label (AnSLER, BnSLER) when PSRDIE is a 1

- Microprocessor writes a 1 to ATnRDIP, BTnRDIP

- When control bit RDI enable (RnDIEN) is 0:
  - Remote Server Defect Indication is sent when control bit ATnRDIS, BTnRDIS is a 1
  - Remote Connectivity Defect Indication is sent when control bit ATnRDIC, BTnRDIC is a 1
  - Remote Payload Defect Indication is sent when control bit ATnRDIP, BTnRDIP is a 1

J2 Byte

The J2 byte may be used to send a trail trace message. The Trail trace message may be 16 bytes or 64 bytes in length. The 64 byte RAM segment allocated for the J2 message will be used on a shared basis with the N2 byte according to the following table.

ATnJ2TEN (bit 1, X+063H) BTnJ2TEN (bit 1, X+0D3H)	ATnJ2TSZ (bit 0, X+063H) BTnJ2TSZ (bit 0, X+0D3H)	Operation
0	0	Transmit J2 RAM segment is configured for a 16 byte message. The bytes will be transmitted starting with an arbitrary address. Please note the TEMx28 does not calculate the CRC-7 for the message, nor does it insert the 1000... pattern transmitted the message.
0	1	Transmit J2 RAM segment is configured for a 64 byte message. The bytes will be transmitted starting with an arbitrary address.
1	X	The J2 byte is transmitted as 00H. The 16 byte message written into the J2 RAM segment is ignored.

N2 Byte

The N2 byte may be used for a Tandem Connection application. The Tandem Connection feature works in conjunction with control bits ATnJ2TSZ/BTnJ2TSZ (bit 0, X+063H, X+0D3H) according to the following table.

ATnJ2TSZ (bit 0, X+063H) BTnJ2TSZ (bit 0, X+0D3H)	ATnTCEN (bit 2, X+063H) BTnTCEN (bit 2, X+0D3H)	Operation
0	0	Tandem Connection feature is disabled. The value written to registers X+061H (A side N2 byte) for the A side, and X+0D1H (B side N2 byte) for the B side are transmitted.
0	1	Tandem Connection feature is enabled. The 16 byte trail trace message is written to registers X+03CH to X+04BH for the A side, and X+0ACH to X+0BBH for the B side.
1	0	Tandem Connection feature disabled. The value written to registers X+061H (A side N2 byte) for the A side, and X+0D1H (B side N2 byte) for the B side are transmitted.
1	1	Tandem Connection feature is enabled. However, the value written to registers X+061H (A side N2 byte) for the A side, and X+0D1H (B side N2 byte) for the B side is repeated 16 times as the trail trace message.

The bit placement of the transmitted N2 (Z6) byte is as shown below:

Bit	1	2	3	4	5	6	7	8
	BIP-2		1	AIS Indication	TC REI	TC OEI (FEBE)	Trace ID TC RDI/ODI	
	MSB							LSB

TC AIS Generation

Bit 4 in the N2 byte is defined as an AIS indication. When control bit AnTCAIS (bit 4, X+113H) or BnTCAIS (bit 4, X+193H) is a 1, bit 4 is transmitted as a 1.

Bits 7 and 8

The TEMx28 will construct and transmit the 76 frame sequence in bits 7, and 8. A multiframe alignment pattern, trace identifier message, TC RDI and TC ODI indications are assigned to bits 7 and 8 in the frames of a 76-frame structure, as shown below. The TEMx28 will generate the multiframe pattern specified for frames 1 through 8. This will followed by inserting the 16 byte message written to the 16 byte N2 RAM segment by the microprocessor, which is followed by the insertion of TC RDI and TCODI. Please note the TEMx28 does not calculate the CRC-7 for the message, nor does it insert the 1000... pattern transmitted the message.

Frame No.	N2 Byte Definition
1 - 8	Multiframe Alignment, 1111 1111 1111 1110
9 - 12	TC Trace ID Byte No. 0 (1 C1 thru C7)
13 - 16	TC Trace ID Byte No. 1 (0 X X X X X X X)
17 - 20	TC Trace ID Byte No. 2 (0 X X X X X X X)
21 - 24 thru 61 - 64	TC Trace ID Bytes No. 3 thru 13
65 - 68	TC Trace ID Byte No. 14 (0 X X X X X X X)
69 - 72	TC Trace ID Byte No. 15 (0 X X X X X X X)
73	Bit 7 = 0, Bit 8 = TC RDI
74	Bit 7 = TC ODI, Bit 8 = 0
75	Bit 7 = 0, Bit 8 = 0
76	Bit 7 = 0, Bit 8 = 0

TC RDI Generation

Bit 8 in frame 73 is defined as a Tandem Connection Remote Defect Indication (TC RDI). A TC RDI alarm is generated for the following unlatched alarm indications. TC RDI is sent for a minimum of 10 times.

- When TC enable (TCnRE) is a 1 and the RnJ2S1 of the corresponding drop bus is 0.
  - Drop Bus Loss Of Clock (ADLOC, BDLOC) when DLCTE is a 1
  - Drop Bus AIS alarm (AxUAIS, BxUAIS) when HEAISE and USTCE are 1
  - Loss of pointer alarm (AnLOP, BnLOP)
  - VT/TU AIS detected (AnAIS, BnAIS)
  - Unequipped signal label (AnUNEQ, BnUNEQ) when UQTCE is a 1
  - Mismatch signal label (AnSLER) when PLSTCE is a 1
  - J2 Loss Of Lock Alarm (AnJ2LOL, BnJ2LOL) when J2TCE is a 1
  - J2 Mismatch Alarm (AnJ2TIM, BnJ2TIM) when J2TCE is a 1
  - VT AIS detected (AnVCAIS, BnVCAIS) when VCTCE is a 1
  - TC Loss Of Multiframe (AnTCLM, BnTCLM)
  - TC Loss Of Lock Alarm (AnTCLL, BnTCLL)
  - TC Mismatch Alarm (AnTCTM, BnTCTM)
  - TC Unequipped Alarm (AnTCUQ, BnTCUQ)
  - A 1 written to ATnTCSR, BTnTCSR
- When TC enable (TCnRE) is a 0
  - A 1 written to ATnTCSR, BTnTCSR

TC ODI Generation

Bit 7 in frame 74 is defined as a Tandem Connection Outgoing Defect Indication (TC ODI). An TC ODI alarm indication is generated for the following unlatched alarm indications. TC ODI is sent for a minimum of 10 times.

- When TC enable (TCnRE) is a 1 and the RnJ2S1 of the corresponding drop bus is 0.
  - Drop Bus Loss Of Clock (ADLOC, BDLOC) when DLCTE is a 1
  - Drop Bus AIS alarm (AxUAIS, BxUAIS) when HEAISE and USTCE are 1
  - Loss of pointer alarm (AnLOP, BnLOP)
  - VT/TU AIS detected (AnAIS, BnAIS)
  - Unequipped signal label (AnUNEQ, BnUNEQ) when UQTCE is a 1
  - Mismatch signal label (AnSLER) when PLSTCE is a 1
  - J2 Loss Of Lock Alarm (AnJ2LOL, BnJ2LOL) when J2TCE is a 1
  - J2 Mismatch Alarm (AnJ2TIM, BnJ2TIM) when J2TCE is a 1
  - VT AIS detected (AnVCAIS, BnVCAIS) when VCTCE is a 1
  - TC Loss Of Multiframe (AnTCLM, BnTCLM)
  - TC Loss Of Lock Alarm (AnTCLL, BnTCLL)
  - TC Mismatch Alarm (AnTCTM, BnTCTM)
  - TC Unequipped Alarm (AnTCUQ, BnTCUQ)
  - TC AIS Detected (AnTCAIS, BnTCAIS), TC enabled and TCAISE is a 1
  - A 1 written to ATnTCSO, BTnTCSO
- When TC enable (TCnRE) is a 0
  - A 1 written to ATnTCSO, BTnTCSO

TC Unequipped Generation

The TEMx28 provides the ability to generate a VT/TU Tandem Connection Unequipped signal on a per channel basis when the TC feature is enabled for a channel. When control bit AnTCUQ (bit 2, X+064H) or BnTCUQ (bit 2, X+0D4H) is a 1, a TC unequipped status is transmitted. The TEMx28 can generate a unequipped status byte with a valid BIP-2 (bits 1 and 2, and the remaining bits in the byte equal to 0 (XX00 0000), or all bits in the N2 byte equal to 0 (0000 0000). When control bit TB2DIS (bit 2, register 03BH) is a 0, a valid BIP-2 is transmitted.

Overhead Bytes - Microprocessor Written

In addition to the J2 byte, the overhead bytes may also be transmitted with a microprocessor written value. The microprocessor written value has priority over any other source except Unequipped or VT/TU AIS. When control bit ATnV5BS (bit 0, X+064H) or BTnV5BS (bit 0, X+0D4H) is written with a 1, the value written to register X+060H for the A side and register X+0D0H for the B side is transmitted in the V5 byte.

When control bit ATnK4PC (bit 1, X+065H) or BTnK4PC (bit 1, X+0D5H) is written with a 1, the value written to register X+062H for the A side and register X+0D2H for the B side is transmitted in the K4 byte.

When control bit ATnTCEN (bit 2, X+063H) or BTnTCEN (bit 2, X+0D3H) is written with a 0 (TC feature disabled), the value written to register X+061H for the A side and register X+0D1H for the B side is transmitted in the N2 byte.

VT/TU AIS GENERATION

The TEMx28 provides the ability to generate a VT/TU AIS signal on a per channel basis. When a 1 is written to control bit ATnGAIS (bit 6, X+063H) or BTnGAIS (bit 6, X+0D3H) for channel n, a TU/VT AIS is generated for corresponding bus. A TU/VT AIS consists of all ones in the entire tributary signal, including bytes V1 through V4. A TU/VT AIS will override a unequipped channel when set.

UNEQUIPPED GENERATION

The TEMx28 Mapper is capable of generating and sending an unequipped channel or unequipped supervisory channel over either the A or B buses or both buses for channel n. An unequipped VT/TU format consists of:

- Normal NDF (0110) in the V1/V2 pointer bytes
- Size bits equal to 11 in the V1/V2 pointer bytes for VC-11 and 10 for VC-12
- Pointer value equal to 78 (decimal) for VC-11 and 105 (decimal) for VC-12
- V4 byte equal to 0 or the microprocessor written value
- Payload bytes equal to 0
- Valid BIP-2 value in the V5 byte
- All other bits in the overhead bytes equal to 0.

An unequipped supervisory VT/TU format consists of:

- Normal NDF (0110) in the V1/V2 pointer bytes
- Size bits equal to 11 in the V1/V2 pointer bytes for VC-11 and 10 for VC-12
- Fixed pointer value equal to 78 (decimal) for VC-11 and 105 (decimal) for VC-12
- V4 byte equal to 0 or the microprocessor written value
- Valid J2 byte
- Valid REI in the V5 byte
- Valid BIP-2 value in the V5 byte
- Valid RDI value (single bit or three bit)
- K4 byte equal to 0 for single bit RDI mode; Bits 1-4, 8 equal 0 for three bit RDI mode
- Signal label equal to 0 in the V5 byte
- RFI bit in the V5 byte set to 0
- N2 byte can be enabled for TC operation, otherwise it is set to 0
- Payload bytes equal to 0.

The various states associated with an unequipped channel selection are shown in the table below. Where n is equal to 1-28.

AnUQGE (bit 4, X+063H) BnUQGE (bit 4, X+0D3H)	AnUQSU (bit 3, X+063H) BnUQSU (bit 3, X+0D3H)	Action
0	X	Normal Operation.
1	0	Unequipped TU/VT Generated
1	1	Unequipped Supervisory TU/VT Generated

Note: Control bits ATnTPTV (bit 5, X+063H) and BTnTPTV (bit 5, X+0D3H) must be set to 0 when generating unequipped or supervisory unequipped.

POINTER GENERATION

The VT/TUs that are added to the A and B add buses have fixed pointers references to the V1 pulse derived from either the drop side for drop bus timing or from the add side for add bus timing. The VT1.5/TU-11 is fixed with a pointer value equal 78, and for a VT2/TU-12 the pointer is fixed to a value of 105.

V4 Byte

Normally the V4 byte is transmitted with a value equal to 00H. When control bit ATnV4BS (bit 0, X+066H) or BTnV4BS (bit 0, X+0D6H) is written with a 1, the value written to register X+05EH for the A side and register X+0CEH for the B side is transmitted instead.

V1 and V2 Bytes

Normally the V1/V2 bytes and the VT/TU payloads and overhead bytes are transmitted with a fixed pointer. When control bit ATnTPTV (bit 5, X+063H) or BTnTPTV (bit 5, X+0D3H) is written with a 1, the value written to registers X+05CH and 05DH for the A side and registers X+0CCH and X+0CDH for the B side are transmitted instead for the V1/V2 bytes. The payload and overhead bytes are still transmitted with fixed the equivalent fixed pointer values of 78 and 105. This permits a test pointer to be transmitted.

ADD BUSES

The two add buses, A and B, consists of leads supporting the COMBUS interface. The possible interface selections, including bus timing, are according to the following table.

$\overline{\text{ABUST}}$	$\overline{\text{ABTE}}$	Add Bus Interfaces
Low	X	Add Bus Timing Mode. The output leads consists of data (A/BA(7-0)), parity, (A/BAPAR), and Add indicator (A/BADD). The input leads consists of clock (A/BACLK), C1, J1, and V1 marker pulses (A/BAC1J1V1), and payload indication (A/BASPE).
High	Low	Drop Bus Timing Mode. The output leads consists of data (A/BA(7-0)), parity, (A/BAPAR), Add indicator (A/BADD), clock (A/BACLK), C1, J1, and V1 marker pulses (A/BAC1J1V1), and payload indication (A/BASPE). The clock, C1J1V1, and SPE signals are derived from their liked name drop bus. The V1 pulse is derived from either the V1 pulse present in the C1J1V1 signal, or from the H4 byte detectors.
High	High	Drop Bus Timing Mode. The output leads consists of data (A/BA(7-0)), parity, (A/BAPAR), and Add indicator (A/BADD). The clock (A/BACLK), C1, J1, and V1 marker pulses (A/BAC1J1V1), and payload indication (A/BASPE) leads are tristated.

Add Bus Parity Selection

The parity selection for two add buses, A and B Add, is according to the following table:

ABPE (bit 5, 03AH)	PADO (bit 6, 03AH)	Add Bus Parity Selection
0	0	Odd parity is calculated for the output leads consisting of data (A/BA(7-0)) in the drop bus timing mode, and also the output leads: clock (A/BACLK), C1, J1, and V1 marker pulses (A/BAC1J1V1), and payload indication (A/BASPE) when they are provided as outputs in the drop bus timing mode.
0	1	Odd parity is calculated for the data output leads (A/BA(7-0)).
1	0	Even parity is calculated for the output leads consisting of data (A/BA(7-0)) in the drop bus timing mode, and also the output leads: clock (A/BACLK), C1, J1, and V1 marker pulses (A/BAC1J1V1), and payload indication (A/BASPE) when they are provided as outputs in the drop bus timing mode.
1	1	Even parity is calculated for the data output leads (A/BA(7-0)).

ADD Indicator Invert

An option is provided that inverts the add indicator ($\overline{\text{AADD}}$ and $\overline{\text{BADD}}$) leads. When a 1 is written to control bit ADDIV (bit 0, 03AH), the output sense of the two leads is active high when a time slot for channel n is being added to a bus. When set to 0, the output sense of the two leads is active low when a time slot for channel n is being added to a bus.

Force Bus to a High Impedance State

An option is provided that can force either of the output add bus signals to a high impedance state, independent of the channel selections. When control bit BAHZE (bit 2, 03AH) for the B side or AAHZE (bit 1, 03AH) for the A side is written with a 1, the following add bus signals are forced to a high impedance state: data (A/BD(7-0), parity, (A/BPAR), and Add indicator ($\overline{\text{A/BADD}}$). If enabled as output signals, the following leads are also forced to a high impedance state: clock (A/BCLK), C1, J1, and V1 marker pulses (A/BC1J1V1), and the payload indication (A/BSPE).

Force Channel N to a High Impedance State

The data and add indication corresponding to a channel can be forced to a high impedance state in two way. The A and B Add Bus VT/TU selection register is written to 00H, or control bit AnHIGHZ (bit 0, X+065H) or BnHIGHZ (bit 0, 0D5H) is written with a 1.

ADD Bus Delay

Normally there is one clock cycle of delay between the add bus data (A/BD(7-0)) and the timing signals such as A/BSPE (add bus timing), or timing signals from the corresponding drop bus in the drop bus timing mode. The delay may be increased to two clock cycles when control bit ABOD (bit 1, 03BH) is written with a 1.

TEST FUNCTIONS

PRBS PATTERN GENERATOR AND ANALYZER

Each DS1 or E1 channel has a PRBS generator and analyzer. The PRBS pattern is selectable, either a 2^{15}-1 or 2^{20}-1 pattern. The 2^{15}-1 pattern is unframed and is defined in Recommendation O.151, and T1M1.3/92-006R3. The 2^{20}-1s pattern, referred to as a QRS pattern, is unframed and is defined in T1.403-1995 and T1M1.3/92-006R3. When control bit TnPRN (bit 2, X+004H) is a 0, the PRBS pattern is defined as 2^{15}-1.

The test pattern generator is enabled when control bit TnPTG (bit 5, X+004H) is a 1. The analyzer is enabled when control bit TnANZ (bit 4, X+004H) is a 1. In addition, on a global basis, when control bit PRBSG (bit 1, 018H) is a 0, the generators are configured for the transmit direction and when set to 1, are configured for the receive direction. When control bit PRBSA (bit 3, 018H) is 0, all analyzers are in the receive direction and when set to 1 are configured for the transmit direction. Note that when the generators are replaced in the receive path, a channel must have a VT/TU selected for the generator to operate.

An out of lock alarm (CnOOL (bit 2, X+100H)) is provided when the PRBS analyzer is enabled. An out of lock alarm occurs when there is a bit mismatch in the analyzed PRBS pattern. Recovery occurs when:

- The analyzed data is in lock for the 2^{15}-1 pattern for more then 25 clock cycles.
- The analyzed data is in lock for the 2^{20}-1 pattern for more then 32 clock cycles.

Figure 33 shows the placement of the PRBS generator and analyzer.

BIP-2 Error Generation

For each channel, a BIP-2 error may be transmitted in the V5 byte. When control bit ATnFB2 (bit 3, X+064H) or BTnFB2 (bit 3, X+0D4H) is set to a 1, the transmitted BIP-2 is transmitted inverted from its calculated value for one frame. In order to send another error, the control bit must be first written with a 0.

REI Error Generation

For each channel, an REI error may be transmitted in the V5 byte. When control bit ATnFFB (bit 6, X+065H) or BTnFFB (bit 6, X+0D5H) is set to a 1, the REI value will be transmitted as a 1 once in the next available V5 byte. A pending REI error as a result of a BIP-2 error, shall be queue, until completion of sending the error is complete. In order to send another error, the control bit must be first written with a 0.

Loopbacks

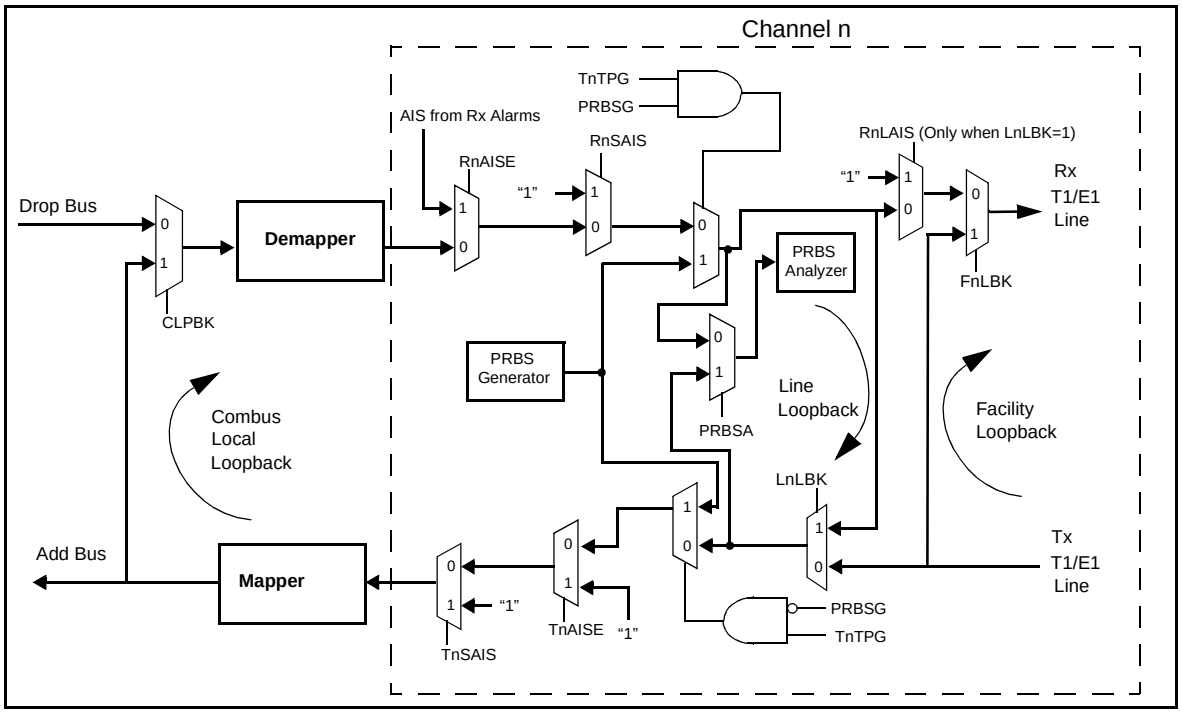
The TEMx28 supports two loopbacks on the DS1/E1 line side: facility and line loopback on a per channel basis. Bidirectional loopback occurs when facility and line loopback are simultaneously enabled. It also supports a COMBUS SONET/SDH loopback. The three loopbacks are illustrated in Figure 33. Note that the facility and line loopbacks are not supported when the VT/TU line interface is selected.

The selection of the loopbacks is according to the following table:

LnLBK (bit 1, X+004H)	FnLBK (bit 0, X+004H)	Loopback Selection
0	0	Off
0	1	Facility Loopback enabled.
1	0	Line loopback enabled.
1	1	Bidirectional loopback enabled.

Facility loopback enables the transmit DS1 or E1 data and clock signals to be looped back as the receive Data and Clock signals. The transmit data is sent for the VT/TU selected.

Figure 33. Loopback, Line AIS and PRBS Generator/Analyzer



Line loopback enables the received DS1 or E1 data and clock signals to be looped back as transmit signals. The DS1 or E1 line signals at the input are disabled. The VT/TU are demapped and mapped according to the VT/TU selection registers. When control bit RnLAIS (bit 0, X+000H) is a 1, line AIS is outputted for the receive rail or NRZ interface while the receive data for the VT/TU is simultaneously looped back. When RnLAIS is set to 0, the receive data for the VT/TU is outputted in addition to being looped back. RnLAIS is enabled only when line loopback is enabled. The RnCLKI (bit 3, register X+000H) and TnCLKI (bit 3, register X+002H) control bits must be programmed for opposite edges for this loopback.

Bidirectional loopback enables the transmit side clock and data to be looped back as the output at the receive interface. The output of the demapper is looped back as transmit data (as with Line Loopback, the RnCLKI and TnCLKI control bits must be programmed for opposite edges).

COMBUS SDH/SONET Local Loopback is enabled when control bit CLPBK (bit 4, 019H) is written with a 1. This mode is valid in either the add bus or drop bus timing modes. Timing is derived from the selected mode. The VT/TU are mapped and demapped according to the VT/TU selection registers. No VT/TU are passed to the demapper from either of the drop buses during COMBUS loopback. COMBUS loopback is valid only when control bit DV1SEL (bit 2, register 019H) is a 1. COMBUS loopback is valid from A Add to A Drop and B Add to B Drop.

RESETS

The TEMx28 has several reset options. These include the following:

- Hardware Reset ($\overline{\text{RESET}}$ lead)
- Software Reset (RESETH), Bit 0 - 006H
- A and B Drop Reset (DRESET), Bit 0 - 039H
- A and B Add Reset (TRESET), Bit 0 - 03CH
- Per Channel A Drop Reset (DACHnR), Bit 0 - X+011H
- Per Channel B Drop Reset (DBCHnR), Bit 0 - X+081H
- Per Channel Add Reset (TnRESET), Bit 0 - X+009
- Reset all Channel Counters (RESETC), bit 5 - 01AH

All of the software reset bits except for RESETH, are not self-clearing. A 0 must be written to these bits before another reset can take place.

Hardware Reset

When an active low pulse is applied to the $\overline{\text{RESET}}$ lead for a minimum duration of 150 nanoseconds after power is applied, this pulse clears all performance counters and latched alarms, resets the control bits, and initializes the internal FIFOs, and state machines. The microprocessor must wait at least 4 microseconds before the memory map states are written to. This enables an internal state machine to cycle through and clear all internal RAM locations.

Software Reset

The software reset bit RESETH (bit 0, 006H) is equivalent to the hardware reset bit. When a 1 is written to this control bit, it clears all performance counters and latched alarms, resets the control bits, and initializes the internal FIFOs and state machines. The microprocessor must wait at least 4 microseconds before the memory map states are written to. This enables an internal state machine to cycle through and clear all internal RAM locations.

A and B Drop Reset

Writing a 1 to control bit DRESET (bit 0, 039H) clears all performance counters and alarms, and initializes the internal FIFOs and state machines for all channels for the A and B drop buses. It does not clear the control bit settings. A DRESET operation may cause the following latched alarms to be set if the latched alarms are enabled (See INTR0, INTR1 control bit description in memory map) while the operation is performed: LAnLOP, LBnLOP, LAxHOOM, LBxHOOM (x =1,2 or 3), LADPAR, and LBDPAR.

A and B Add Reset

Writing a 1 to the control bit TRESET (bit 0, 03CH) clears all performance counters and alarms, and initializes the internal FIFOs and state machines for all channels for the A and B add buses. It does not clear the control bit settings.

Per Channel A Drop Reset

Writing a 1 to control bit DACHnR (bit 0, X+011H) clears all performance counters, and initializes the internal FIFOs and state machines for the A drop bus VT/TU channel selected. It does not clear the control bit settings, or latched alarms for the channel selected.

Per Channel B Drop Reset

Writing a 1 to control bit DBCHnR (bit 0, X+081H) clears all performance counters, and initializes the internal FIFOs and state machines for the B drop bus VT/TU channel selected. It does not clear the control bit settings, or latched alarms for the channel selected.

Per Channel A and B Add Reset

Writing a 1 to control bit TnRESET (bit 0, X+009H) clears all performance counters, and initializes the internal FIFOs and state machines for the A and B add bus VT/TU channel selected. It does not clear the control bit settings, or latched alarms for the channel selected.

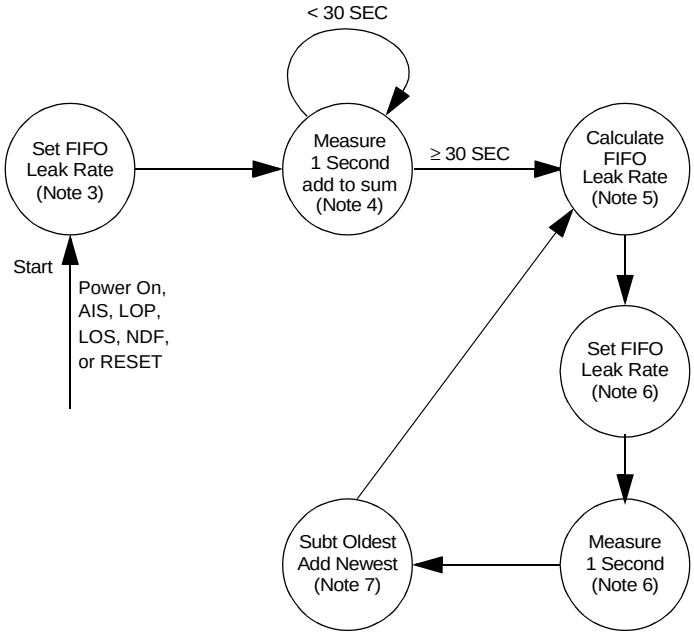
DATA THROUGHPUT DELAY

On the receive side (SONET/SDH to T1/E1) the nominal delay for T1 is approximately 62 µs and for E1 is approximately 49 µs. Nominal conditions are no pointer movements, nominal T1/E1 clock frequency, and either no line coding (NRZ) or AMI line coding. B8ZS line coding adds 5 µs of delay, and HDB3 adds 2.5 µs delay.

On the transmit side (T1/E1 to SONET/SDH) the nominal delay for T1 is approximately 64 µs and for E1 is approximately 42 µs. The nominal conditions for the transmit side are the same as for the receive side. B8ZS and HDB3 line coding also add the same delay.

POINTER LEAK RATE CALCULATIONS

The Pointer Leak Rate register for each channel is 10 bits long (X+017H and X+018H for the A side, and X+067H and X+088H for the B side). The host processor must write the first eight bits (X+017H and X+067H) followed by the remaining two bits of the 10 bit register. If the pointer Leak Rate Register is set to 000H the receive FIFO in the Desynchronizer is bypassed.



Notes:

1. The procedure described in Notes 3 through 8 below must be performed independently for each of the 28 channels in the TEMx28. When both buses are used, the Leak Rate must be calculated independently for each bus. The following notes describe the actions for one channel on one bus.
2. The procedure shown in the diagram above uses a thirty-second sliding window with a resolution of one second. When implementing the Pointer Leak Rate Calculation, while gathering the data from the previous One Second Counter, the PM1S clock and microprocessor read should be synchronized.
3. The FIFO Leak Rate Register must first be set to a value of 13, (00DH) for DS1 or 10, (00AH) for E1.
4. Measure thirty consecutive one-second samples from the Positive and Negative Stuff Counters being used. Store all thirty difference values, i.e.,

   S_1 = POS STUFF $COUNT_1$ - NEG STUFF $COUNT_1$,
   S_2 = POS STUFF $COUNT_2$ - NEG STUFF $COUNT_2$, and so on through
   S_{30} = POS STUFF $COUNT_{30}$ - NEG STUFF $COUNT_{30}$.

   Care should be taken to use the pair appropriate to the programmed configuration of the device.
5. Calculate the leak rate:

   Leak Rate = The smaller of 1023, (3FFH) or (Hex[INT{3300/C}], Hex[INT{500/D}] if D $\geq$ 2, Hex[INT{375/E}] if E $\geq$ 2, Hex[INT{250/F}] if F $\geq$ 2, Hex[INT{125/G}] if G $\geq$ 2) where Hex is the hexadecimal value, INT is the integer value:

   C = Absolute Value [sum(S_i to S_{30+i})], D = Absolute Value [sum(S_{27+i} to S_{30+i})], E = Absolute Value [sum(S_{28+i} to S_{30+i})], F = Absolute Value [sum(S_{29+i} to S_{30+i})], G = Absolute Value [S_{30+i}] and i represents the number of times through the loop shown in the diagram (notes 5, 6 and 7). If the C is 0, 1, 2 or 3 set the Leak Rate to 1023, (3FFH). A pointer will be leaked before another arrives for uniform pointer arrivals. If D, E, F, or G $\geq$ 2, faster pointer leaking accounts for a rapid change in pointer arrival rate (e.g., start up).
6. Set the FIFO Leak Rate Register with the value between 1 and 1023, (3FFH) calculated above, then take another one-second sample (e.g., S_{31}).
7. Recalculate the value of 'C', 'D', 'E', 'F' and 'G' by discarding the oldest value and adding the newest value (i = i + 1).
8. Continue to repeat the steps described in Notes 5, 6 and 7 until AIS, LOP, LOS or NDF is received or until you reset the channel or restart the device.

JITTER MEASUREMENTS

Equipment used in TEMx28 jitter measurements:

- Hewlett-Packard Digital Transmission Analyzer:HP-3784A
- Anritsu Digital Transmission Analyzer:ME520B
- Anritsu STM/SONET Analyzer:MP1560A

Jitter Tolerance Test

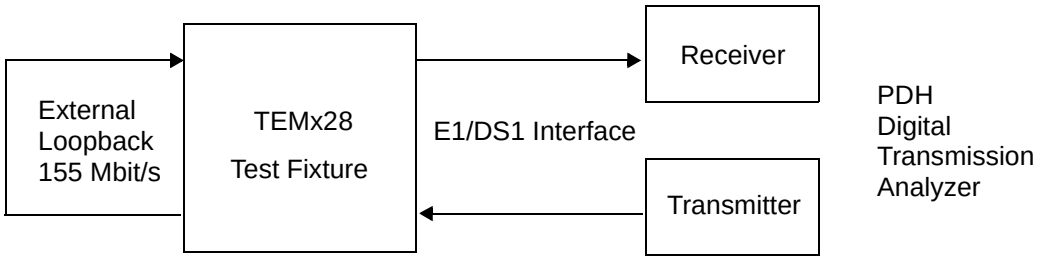
The jitter tolerance test is performed by inserting various jitter levels at selected frequencies into the 2048 kbit/s and the 1544 kbit/s line input of the TEMx28, as shown in Figures 34 and 35. Data is looped back at the SDH/SONET interface and dropped by the same TEMx28 device (see Figure 36). The measured value is the maximum input jitter that the TEMx28 can tolerate at its input without generating bit errors in the loopback path. Figures 36 are plots of the requirement listed in the table.

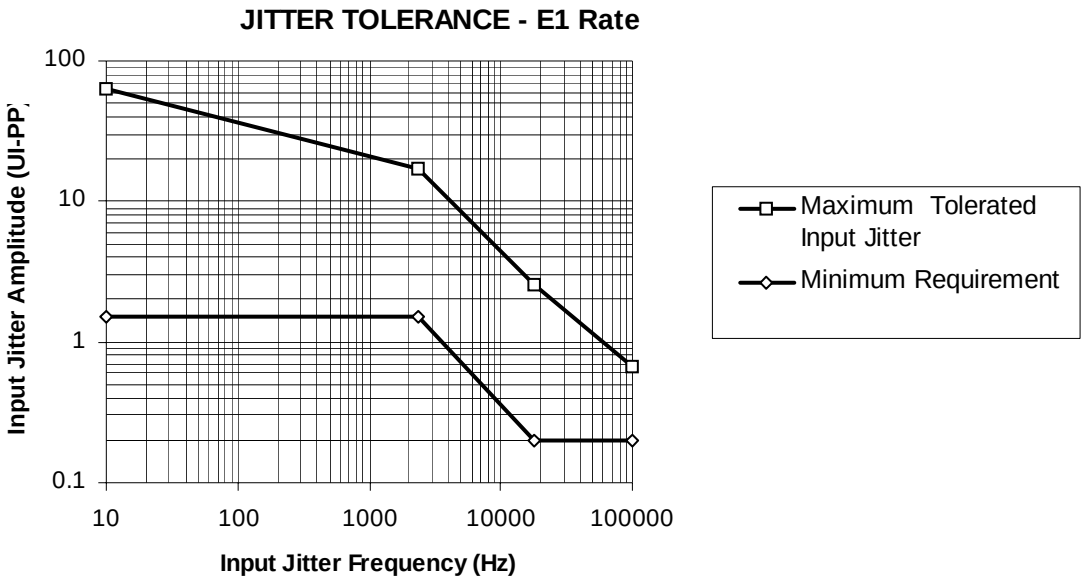
Input Jitter Frequency	Requirement	Maximum Input Jitter Tolerated (UI-PP)
10 Hz	>1.5 UI	62.563
2.4 kHz	> 1.5 UI	17.01
18 kHz	> 0.2 UI	2.518
100 kHz	> 0.2 UI	0.665

Figure 34. E1 (2048 kbit/s) Jitter Tolerance

Input Jitter Frequency		Requirement (UI pp)	Maximum Input Jitter (UI pp)
F1	10 Hz	> 5.0	64
	100 Hz	> 5.0	60
F2	500 Hz	> 5.0	40
	1 kHz	> 1.9	20
F3	8 kHz	> 0.1	2.579
	25 kHz	> 0.1	0.907
F4	40 kHz	> 0.1	0.68

Figure 35. DS1 (1544 kbit/s) Jitter Tolerance





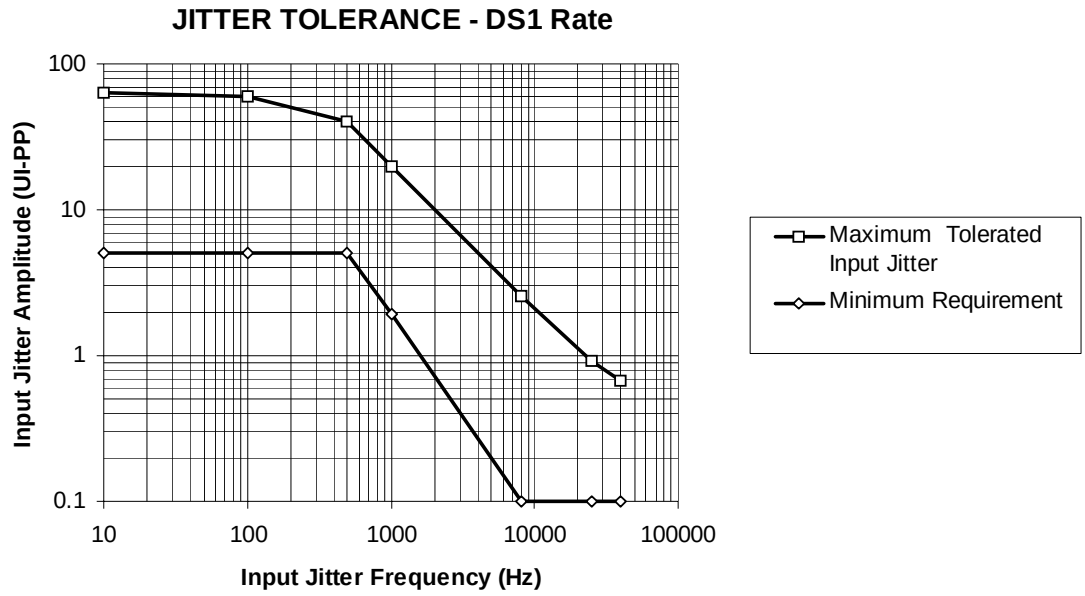
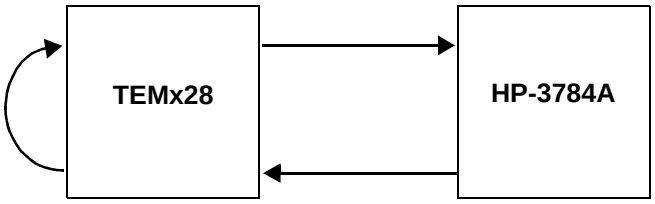


Figure 36. Jitter Tolerance Measurements

Jitter Transfer Test

A fixed jitter level of 1.0 UI (0.6 UI for 1000 Hz) is inserted into the transmitted E1 and DS1 signal as illustrated below. The jitter value measured is achieved using the HP1/LP filter in the PDH receiver. The jitter transfer measurements are provided in the following table and figure.



Test Fixture **Digital Transmission Analyzer**

Input Jitter		Filter Used	Jitter Transfer (UI - PP, Max) E1 Rate	Jitter Transfer (UI - PP, Max) DS1 Rate
Frequency	**Unit Interval**			
10 Hz	1.0 UI	f1-f4 (HP1/LP)	.129	.129
40 Hz	1.0 UI		.0327	.0327
100 Hz	1.0 UI		.0131	.0131
250 Hz	1.0 UI		.0050	.0050
500 Hz	1.0 UI		.0031	.0029
1000 Hz	0.6 UI		.0016	.0012

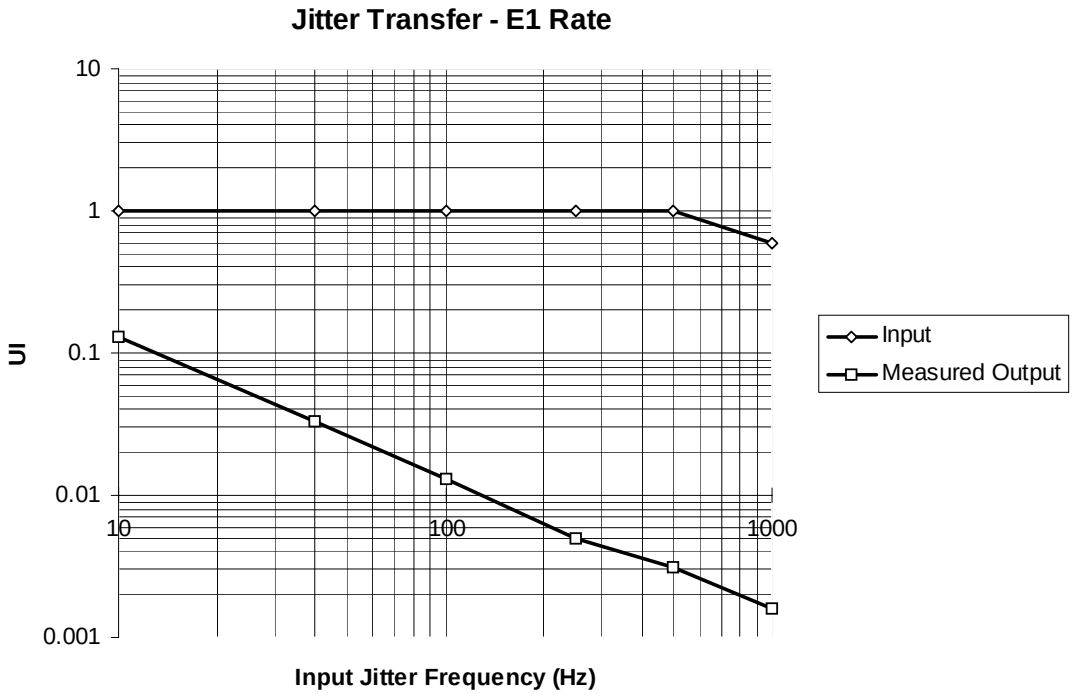


Figure 37. E1 Jitter Transfer Measurements

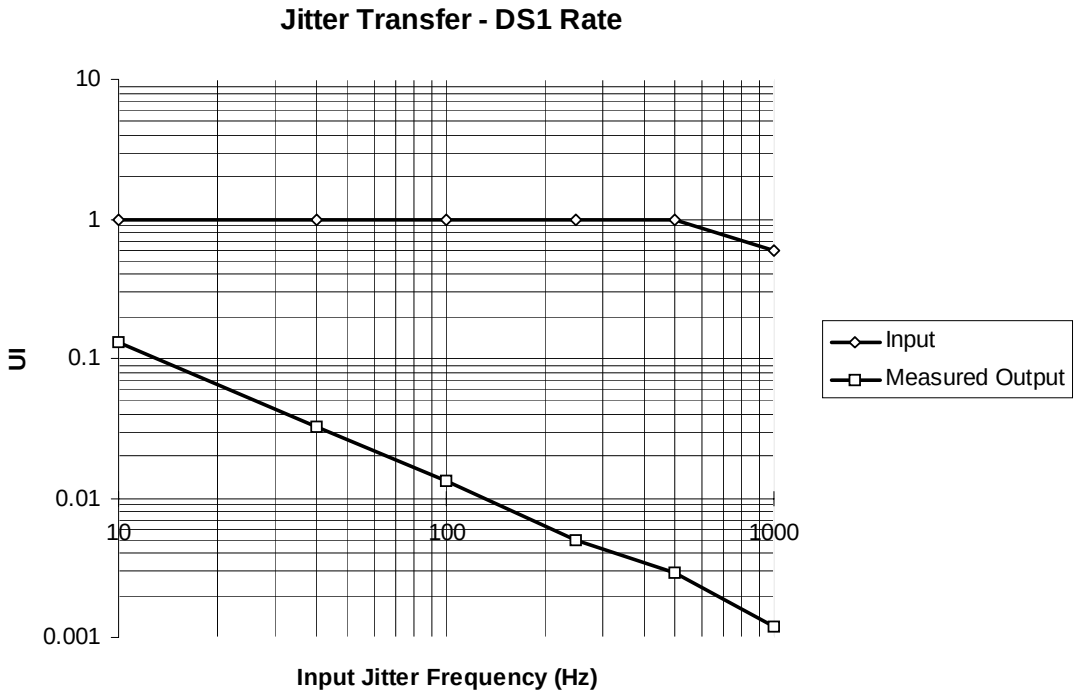
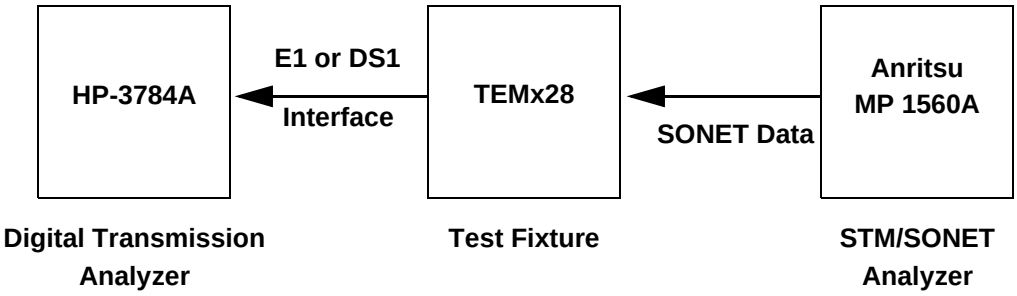


Figure 38. DS1 Jitter Transfer Measurements

Mapping Jitter Measurement

The following table lists the mapping jitter measurements, which are made with the following setup. These mapping jitter measurements were made in the absence of STS or VT(TU) pointer adjustments:



Interface	Filter Characteristics	Maximum Output Jitter (UI-PP)	
		Requirement	Measured Value
E1 - 2048 kbit/s	f1-f4 (HP1/LP)	(Note 1)	0.027
	f3-f4 (HP2/LP)	≤ 0.075 UI	0.020

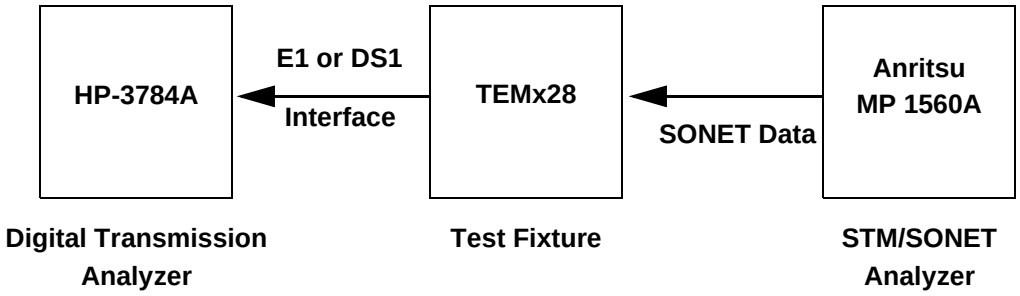
Note 1:These values are for further study.

Interface	Filter Characteristics	Maximum Output Jitter (UI pp)		
		Requirement		Measured
		Per G.783 (Note 1)	Per Bellcore (Note 2)	
DS1 - 1544 kbit/s	f1-f4 (HP1/LP)	(Note 3)	≤ 0.7	0.016
	f1-f4 (HP1/LP)	≤ 0.1	≤ 0.7	0.015

Notes:
1. Per Recommendation ITU-T G.783 (04/97).
2. Per Bellcore GR-253-CORE Issue 2 Dec. 95: Rev 2 Jan. 99.
3. These values are for further study.

Combined Jitter Measurement

The following table lists the combined jitter measurements. This measurement was performed using the following setup.



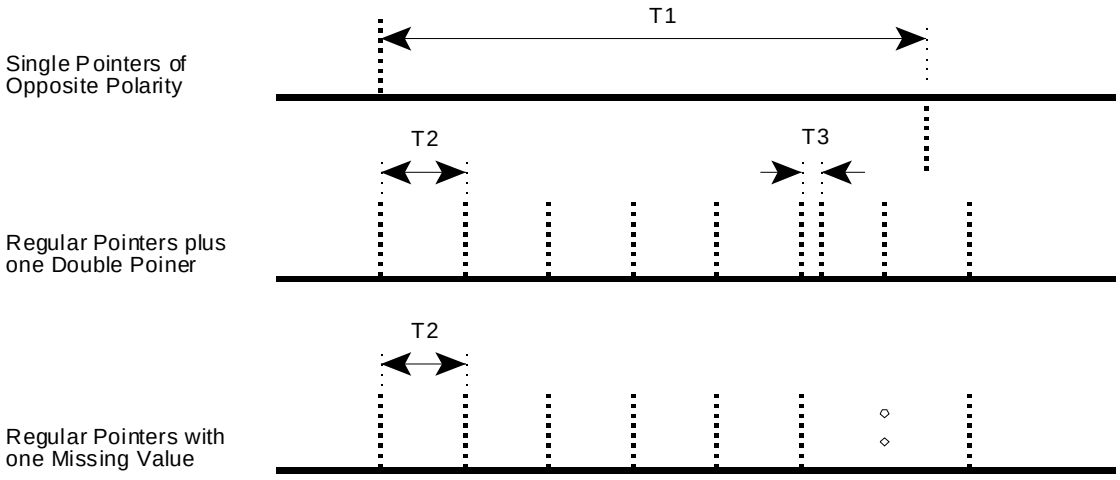
TU-12

Pointer Test Sequence		Filter	Leak Rate (Hex) (Note 1)	Maximum Output Jitter (UI - PP)	
				Requirement	Measured
1	Single Pointers of Opposite Polarity	f1-f4 (HP1/LP)	52H	≤ 0.4 (Note 2)	0.240
2	Regular Pointers Plus One Double Pointer		52H		0.176
3	Regular Pointers with One Missing Pointer		52H		0.187
1	Single Pointers of Opposite Polarity	f3-f4 (HP2/LP)	52H	≤ 0.075 (Note 2)	0.010
2	Regular Pointers Plus One Double Pointer		52H		0.010
3	Regular Pointers with One Missing Pointer		52H		0.010

Note 1: These values are written into the Desynchronizer Pointer Leak Rate Registers.

Note 2: The limit corresponds to the pointer sequences shown in Figure 39 for Standard Pointer Test Sequences, (T1 ≥ 10 s, T2 > 0.75 s, T3 = 30 ms). The T3 value was constrained by test equipment limitations. Value can vary depending on pointer sequence.

Figure 39. TU-12 Standard Pointer Test Sequences



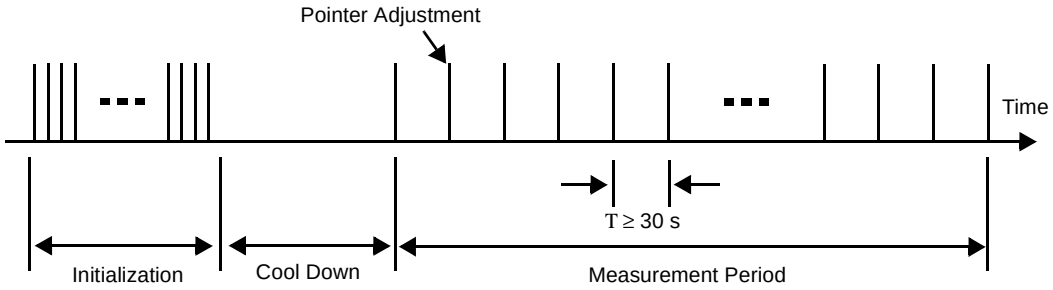
(Ref: ITU-T G.783, Fig. 6-2)

VT1.5

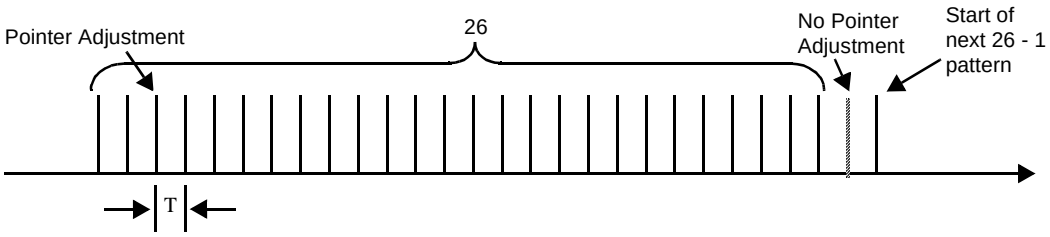
Pointer Test Sequence	Filter	Leak Rate Value (Hex) (Note 3)	Maximum Output Jitter (UI pp)		
			Requirement		Measured
			G.783 (Note 1)	Bellcore (Note 2)	
Single Pointer Adjustment T = 30 s	(f1) (f4) 10 Hz -> 40 kHz	3FFH	≤ 1.5	≤ Ao + 0.60 (Note 4)	0.119
Periodic VT1.5 Pointer Adjustment (26-1 Pattern) T = 0.35 s		25H	≤ 1.5	≤ 1.3	0.222
Periodic VT1.5 Pointer Adjustment (Continuous Pattern) T = 0.2 s		19H	≤ 1.5	≤ 1.3	0.600
Periodic VT1.5 Pointer Adjustment (Continuous Pattern Plus Add) T = 1 s t = 30 ms		7DH	≤ 1.5	≤ 1.9	0.218

Notes:
1. Per Recommendation ITU-T G.783.
2. Per Bellcore GR-253-CORE Issue 2 Dec. 95: Rev 2 Jan. 99.
3. These are values written into the desynchronizer Pointer Leak Rate register
   Normally the Pointer Leak Rate Register is controlled by the external microprocessor through the implementation of the pointer leak rate algorithm shown on page 89.
4. Ao is the mapping jitter generated by the device under test. Please see Mapping Jitter Measurement on the previous page.

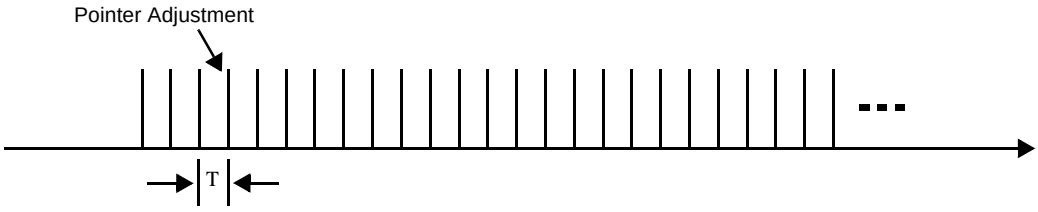
Figure 40. VT1.5 Standard Pointer Test Sequences



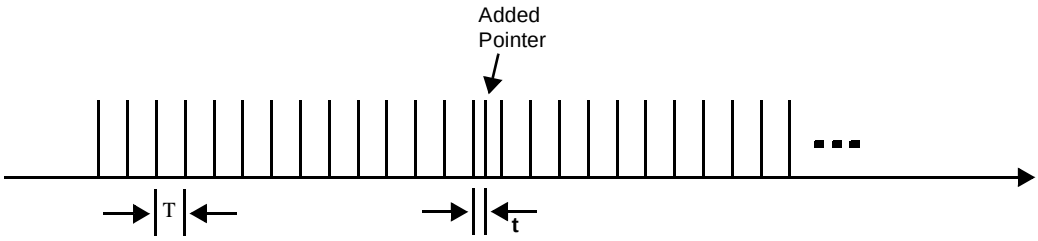
Single Pointer Adjustment Test Sequence



Periodic VT1.5 Pointer Adjustment Test Sequence (26-1 Pattern)



Periodic VT1.5 Pointer Adjustment Test Sequence (Continuous Pattern)



Periodic VT1.5 Pointer Adjustment Test Sequence (Continuous Pattern Plus Add)

BOUNDARY SCAN

Introduction

The Boundary Scan Interface Block provides a five-lead Test Access Port (TAP) that conforms to the IEEE 1149.1 standard. This standard provides external boundary scan functions to read and write the external Input/Output leads from the TAP for board and component test.

The IEEE 1149.1 standard defines the requirements of a boundary scan architecture that has been specified by the IEEE Joint Test Action Group (JTAG). Boundary scan is a specialized scan architecture that provides observability and controllability for the interface leads of the device. As shown in Figure 41, one cell of a boundary scan register is assigned to each input or output lead to be observed or tested (bidirectional leads may have two cells). The boundary scan capability is based on a Test Access Port (TAP) controller, instruction and bypass registers, and a boundary scan register bordering the input and output leads. The boundary scan test bus interface consists of four input signals (Test Clock (TCK), Test Mode Select (TMS), Test Data Input (TDI) and Test Reset ($\overline{\text{TRS}}$)) and a Test Data Output (TDO) output signal. Boundary scan signal timing is shown in Figure 25.

The TAP controller receives external control information via a Test Clock (TCK) signal and a Test Mode Select (TMS) signal, and sends control signals to the internal scan paths. Detailed information on the operation of this state machine can be found in the IEEE 1149.1 standard. The serial scan path architecture consists of an instruction register, a boundary scan register and a bypass register. These three serial registers are connected in parallel between the Test Data Input (TDI) and Test Data Output (TDO) signals, as shown in Figure 41.

The boundary scan function can be reset and disabled by holding lead $\overline{\text{TRS}}$ low. When boundary scan testing is not being performed the boundary scan register is transparent, allowing the input and output signals to pass to and from the TEMx28 device's internal logic. During boundary scan testing, the boundary scan register may disable the normal flow of input and output signals to allow the device to be controlled and observed via scan operations.

Boundary Scan Operation

The maximum frequency the TEMx28 device will support for boundary scan is 10 MHz. The timing diagrams for the boundary scan interface leads are shown in Figure 25.

The instruction register contains three bits. The TEMx28 device performs the following three boundary scan test instructions:

The EXTEST test instruction (000) provides the ability to test the connectivity of the TEMx28 device to external circuitry.

The SAMPLE test instruction (010) provides the ability to examine the boundary scan register contents without interfering with device operation.

The BYPASS test instruction (111) provides the ability to bypass the TEMx28 boundary scan and instruction registers.

Boundary Scan Reset

Specific control of the $\overline{\text{TRS}}$ lead is required in order to ensure that the boundary scan logic does not interfere with normal device operation. This lead must either be held low, asserted low, or asserted low then high (pulsed low), to asynchronously reset the Test Access Port (TAP) controller during power-up of the TEMx28. If boundary scan testing is to be performed and the lead is held low, then a pull-down resistor value should be chosen which will allow the tester to drive this lead high, but still meet the V_{IL} requirements listed in the 'Input, Output and Input/Output Parameters' section of this Data Sheet for worst case leakage currents of all devices sharing this pull-down resistor.

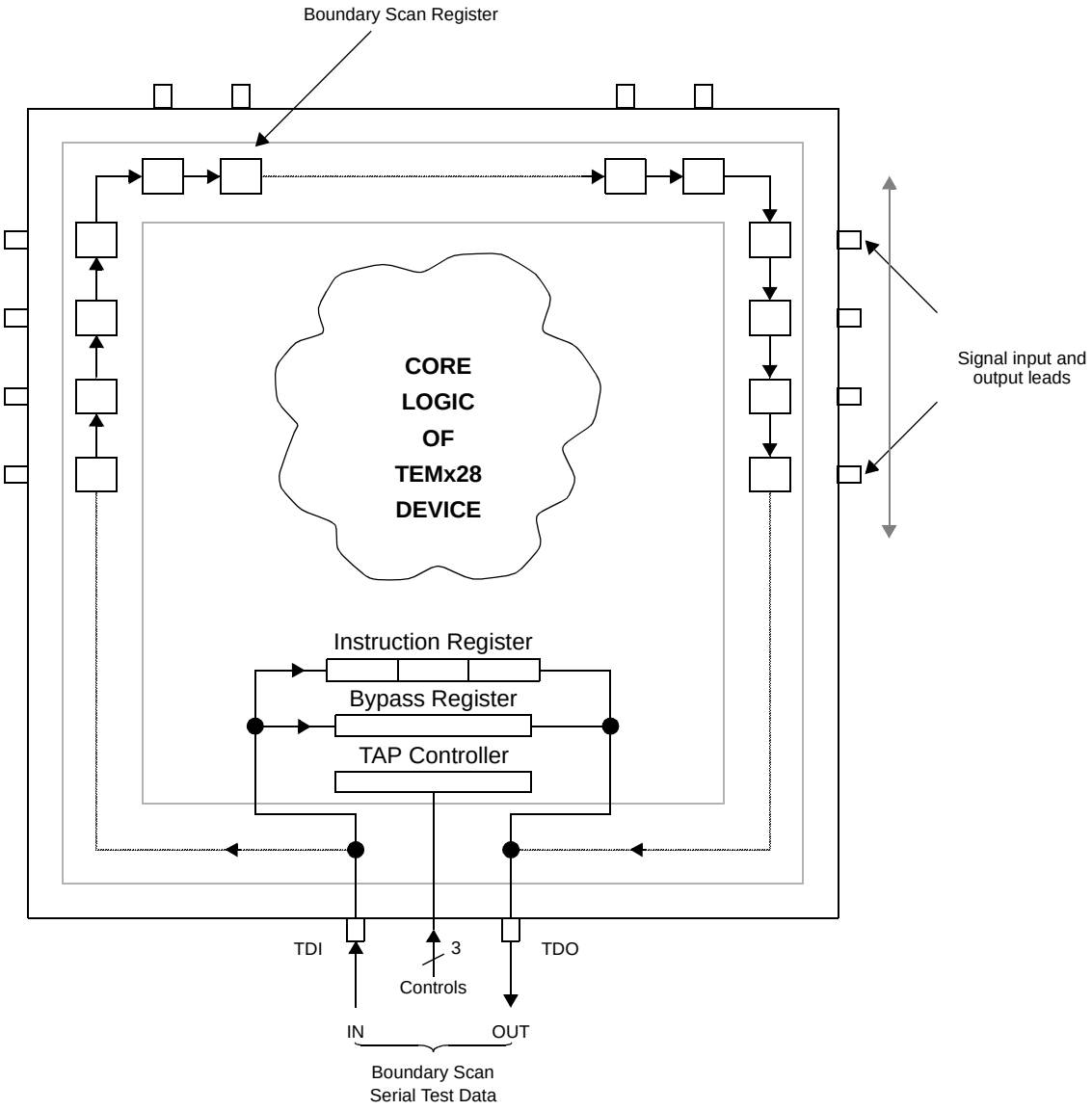


Figure 41. Boundary Scan Schematic

Boundary Scan Chain

There are 330 scan cells in the boundary scan chain associated with TEMx28 core logic functions. Additional scan cells are used for direction control as needed. A boundary scan description language (BSDL) source file is available via the Products page of the TranSwitch Internet World Wide Web site at www.transwitch.com. The following table shows the listed order of the scan cells and their function.

Scan Cell No.	I/O	Lead No.	Symbol	Comments
0	input	C3	tni28	
1	bidir	D5	tclk28	
2	control		*	'1' drives tclk28 to 'Z'
3	input	A2	tpi28	
4	output3	B3	rno28	
5	output3	B4	rclk28	
6	output3	C5	rpo28	
7	control		$\overline{*}$	'1' drives rno28, rclk28, rpo28 to 'Z'
8	input	D6	tni27	
9	bidir	A3	tclk27	
10	control		*	'1' drives tclk27 to 'Z'
11	input	B5	tpi27	
12	output3	C6	rno27	
13	output3	D7	rclk27	
14	output3	A4	rpo27	
15	control		*	'1' drives rno27, rclk27, rpo27 to 'Z'
16	input	A5	tni26	
17	bidir	B6	tclk26	
18	control		*	'1' drives tclk26 to 'Z'
19	input	C7	tpi26	
20	output3	D8	rno26	
21	output3	A6	rclk26	
22	output3	B7	rpo26	
23	control		*	'1' drives rno26, rclk26, rpo26 to 'Z'
24	input	C8	tni25	
25	bidir	D9	tclk25	
26	control		*	'1' drives tclk25 to 'Z'

Scan Cell No.	I/O	Lead No.	Symbol	Comments
27	input	A7	tpi25	
28	output3	B8	rno25	
29	output3	A8	rclk25	
30	output3	C9	rpo25	
31	control		*	'1' drives rno25, rclk25, rpo25 to 'Z'
32	input	D10	tni24	
33	bidir	B9	tclk24	
34	control		*	'1' drives tclk24 to 'Z'
35	input	C10	tpi24	
36	output3	A9	rno24	
37	output3	B10	rclk24	
38	output3	D11	rpo24	
39	control		*	'1' drives rno24, rclk24, rpo24 to 'Z'
40	input	A10	tni23	
41	bidir	C11	tclk23	
42	control		*	'1' drives tclk23 to 'Z'
43	input	B11	tpi23	
44	output3	A11	rno23	
45	output3	A12	rclk23	
46	output3	B12	rpo23	
47	control		$\overline{*}$	'1' drives rno23, rclk23, rpo23 to 'Z'
48	input	C12	tni22	
49	bidir	A13	tclk22	
50	control		$\overline{*}$	'1' drives tclk22 to 'Z'
51	input	D12	tpi22	
52	output3	B13	rno22	
53	output3	C13	rclk22	
54	output3	A14	rpo22	
55	control		*	'1' drives rno22, rclk22, rpo22 to 'Z'
56	input	B14	tni21	
57	bidir	D13	tclk21	

Scan Cell No.	I/O	Lead No.	Symbol	Comments
58	control		*	'1' drives tclk21 to 'Z'
59	input	C14	tpi21	
60	output3	A15	rno21	
61	output3	B15	rclk21	
62	output3	A16	rpo21	
63	control		$\overline{*}$	'1' drives rno21, rclk21, rpo21 to 'Z'
64	input	D14	tni20	
65	bidir	C15	tclk20	
66	control		*	'1' drives tclk20 to 'Z'
67	input	B16	tpi20	
68	output3	A17	rno20	
69	output3	D15	rclk20	
70	output3	C16	rpo20	
71	control		*	'1' drives rno20, rclk20, rpo20 to 'Z'
72	input	B17	tni19	
73	bidir	A18	tclk19	
74	control		*	'1' drives tclk19 to 'Z'
75	input	A19	tpi19	
76	output3	D16	rno19	
77	output3	C17	rclk19	
78	output3	B18	rpo19	
79	control		*	'1' drives rno19, rclk19, rpo19 to 'Z'
80	input	A20	tni18	
81	bidir	D17	tclk18	
82	control		*	'1' drives tclk18 to 'Z'
83	input	C18	tpi18	
84	output3	B19	rno18	
85	output3	A21	rclk18	
86	output3	D18	rpo18	
87	control		$\overline{*}$	'1' drives rno18, rclk18, rpo18 to 'Z'
88	input	B20	tni17	

Scan Cell No.	I/O	Lead No.	Symbol	Comments
89	bidir	C19	tclk17	
90	control		*	'1' drives tclk17 to 'Z'
91	input	B21	tpi17	
92	output3	D20	rno17	
93	output3	C21	rclk17	
94	output3	E19	rpo17	
95	control		*	'1' drives rno17, rclk17, rpo17 to 'Z'
96	input	B22	tni16	
97	bidir	D21	tclk16	
98	control		*	'1' drives tclk16 to 'Z'
99	input	E20	tpi16	
100	output3	F19	rno16	
101	output3	C22	rclk16	
102	output3	E21	rpo16	
103	control		*	'1' drives rno16, rclk16, rpo16 to 'Z'
104	input	F20	tni15	
105	bidir	G19	tclk15	
106	control		$\overline{*}$	'1' drives tclk15 to 'Z'
107	input	D22	tpi15	
108	output3	E22	rno15	
109	output3	F21	rclk15	
110	output3	G20	rpo15	
111	control		*	'1' drives rno15, rclk15, rpo15 to 'Z'
112	input	H19	tni14	
113	bidir	F22	tclk14	
114	control		*	'1' drives tclk14 to 'Z'
115	input	G21	tpi14	
116	output3	H20	rno14	
117	output3	J19	rclk14	
118	output3	G22	rpo14	
119	control		*	'1' drives rno14, rclk14, rpo14 to 'Z'

Scan Cell No.	I/O	Lead No.	Symbol	Comments
120	input	H21	tni13	
121	bidir	H22	tclk13	
122	control		*	'1' drives tclk13 to 'Z'
123	input	J20	tpi13	
124	output3	K19	rno13	
125	output3	J21	rclk13	
126	output3	J22	rpo13	
127	control		*	'1' drives rno13, rclk13, rpo13 to 'Z'
128	input	K20	tni12	
129	bidir	K21	tclk12	
130	control		*	'1' drives tclk12 to 'Z'
131	input	L19	tpi12	
132	output3	K22	rno12	
133	output3	L20	rclk12	
134	output3	L21	rpo12	
135	control		*	'1' drives rno12, rclk12, rpo12 to 'Z'
136	input	L22	tni11	
137	bidir	M22	tclk11	
138	control		*	'1' drives tclk11 to 'Z'
139	input	M21	tpi11	
140	output3	M20	rno11	
141	output3	N22	rclk11	
142	output3	M19	rpo11	
143	control		$\overline{*}$	'1' drives rno11, rclk11, rpo11 to 'Z'
144	input	N21	tni10	
145	bidir	N20	tclk10	
146	control		*	'1' drives tclk10 to 'Z'
147	input	P22	tpi10	
148	output3	P21	rno10	
149	output3	N19	rclk10	
150	output3	P20	rpo10	

Scan Cell No.	I/O	Lead No.	Symbol	Comments
151	control		*	'1' drives rno10, rclk10, rpo10 to 'Z'
152	input	R22	tni9	
153	bidir	R21	tclk9	
154	control		*	'1' drives tclk9 to 'Z'
155	input	T22	tpi9	
156	output3	P19	rno9	
157	output3	R20	rclk9	
158	output3	T21	rpo9	
159	control		*	'1' drives rno9, rclk9, rpo9 to 'Z'
160	input	U22	tni8	
161	bidir	R19	tclk8	
162	control		*	'1' drives tclk8 to 'Z'
163	input	T20	tpi8	
164	output3	U21	rno8	
165	output3	V22	rclk8	
166	output3	W22	rpo8	
167	control		*	'1' drives rno8, rclk8, rpo8 to 'Z'
168	input	T19	tni7	
169	bidir	U20	tclk7	
170	control		*	'1' drives tclk7 to 'Z'
171	input	V21	tpi7	
172	output3	Y22	rno7	
173	output3	U19	rclk7	
174	output3	V20	rpo7	
175	control		*	'1' drives rno7, rclk7, rpo7 to 'Z'
176	input	W21	tni6	
177	bidir	AA22	tclk6	
178	control		*	'1' drives tclk6 to 'Z'
179	input	V19	tpi6	
180	output3	W20	rno6	
181	output3	Y21	rclk6	

Scan Cell No.	I/O	Lead No.	Symbol	Comments
182	output3	AA21	rpo6	
183	control		*	'1' drives rno6, rclk6, rpo6 to 'Z'
184	input	AA20	tni5	
185	bidir	Y19	tclk5	
186	control		*	'1' drives tclk5 to 'Z'
187	input	W18	tpi5	
188	output3	AB21	rno5	
189	output3	Y18	rclk5	
190	output3	AA19	rpo5	
191	control		*	'1' drives rno5, rclk5, rpo5 to 'Z'
192	input	W17	tni4	
193	bidir	ab20	tclk4	
194	control		*	'1' drives tclk4 to 'Z'
195	input	AA18	tpi4	
196	output3	Y17	rno4	
197	output3	W16	rclk4	
198	output3	AB19	rpo4	
199	control		*	'1' drives rno4, rclk4, rpo4 to 'Z'
200	input	AB18	tni3	
201	bidir	AA17	tclk3	
202	control		*	'1' drives tclk3 to 'Z'
203	input	Y16	tpi3	
204	output3	W15	rno3	
205	output3	AB17	rclk3	
206	output3	AA16	rpo3	
207	control		*	'1' drives rno3, rclk3, rpo3 to 'Z'
208	input	Y15	tni2	
209	bidir	W14	tclk2	
210	control		*	'1' drives tclk2 to 'Z'
211	input	AB16	tpi2	
212	output3	AA15	rno2	

Scan Cell No.	I/O	Lead No.	Symbol	Comments
213	output3	AB15	rclk2	
214	output3	Y14	rpo2	
215	control		*	'1' drives rno2, rclk2, rpo2 to 'Z'
216	input	W13	tni1	
217	bidir	AA14	tclk1	
218	control		*	'1' drives tclk1 to 'Z'
219	input	AB14	tpi1	
220	output3	Y13	rno1	
221	output3	AA13	rclk1	
222	output3	W12	rpo1	
223	control		*	'1' drives rno1, rclk1, rpo1 to 'Z'
224	output3	AB13	rdy	
225	control		*	'1' drives rdy to 'Z'
226	input	Y12	moto	
227	output3	AA12	int	
228	control		*	'1' drives int to 'Z'
229	clock	AB12	dsclk	
230	input	AB11	wr	
231	input	AA11	rd	
232	input	Y11	sel	
233	input	AB10	a(0)	
234	input	W11	a(1)	
235	input	AA10	a(2)	
236	input	Y10	a(3)	
237	input	AB9	a(4)	
238	input	AA9	a(5)	
239	input	W10	a(6)	
240	input	Y9	a(7)	
241	input	AB8	a(8)	
242	input	AA8	a(9)	
243	input	AB7	a(10)	

Scan Cell No.	I/O	Lead No.	Symbol	Comments
244	input	W9	a(11)	
245	input	Y8	a(12)	
246	input	AA7	a(13)	
247	input	AB6	a(14)	
248	bidir	W8	d(0)	
249	bidir	Y7	d(1)	
250	bidir	AA6	d(2)	
251	bidir	AB5	d(3)	
252	bidir	AB4	d(4)	
253	bidir	W7	d(5)	
254	bidir	Y6	d(6)	
255	bidir	AA5	d(7)	
256	control		*	'1' drives d(7:0) to 'Z'
257	input	Y5	reset	
258	output3	Y2	scanout(0)	
259	input	W3	scanin(0)	
260	output3	V4	scanout(1)	
261	input	AA1	scanin(1)	
262	output3	W2	scanout(2)	
263	input	V3	scanin(2)	
264	output3	U4	scanout(3)	
265	input	Y1	scanin(3)	
266	input	V2	scanenable	
267	input	U3	test	
268	input	T4	highz	
269	input	V1	abte	
270	input	W1	abust	
271	input	U2	pm1s	
272	output3	T3	tvtfb2	
273	output3	R4	tvtf2	
274	output3	U1	tvtffb15	

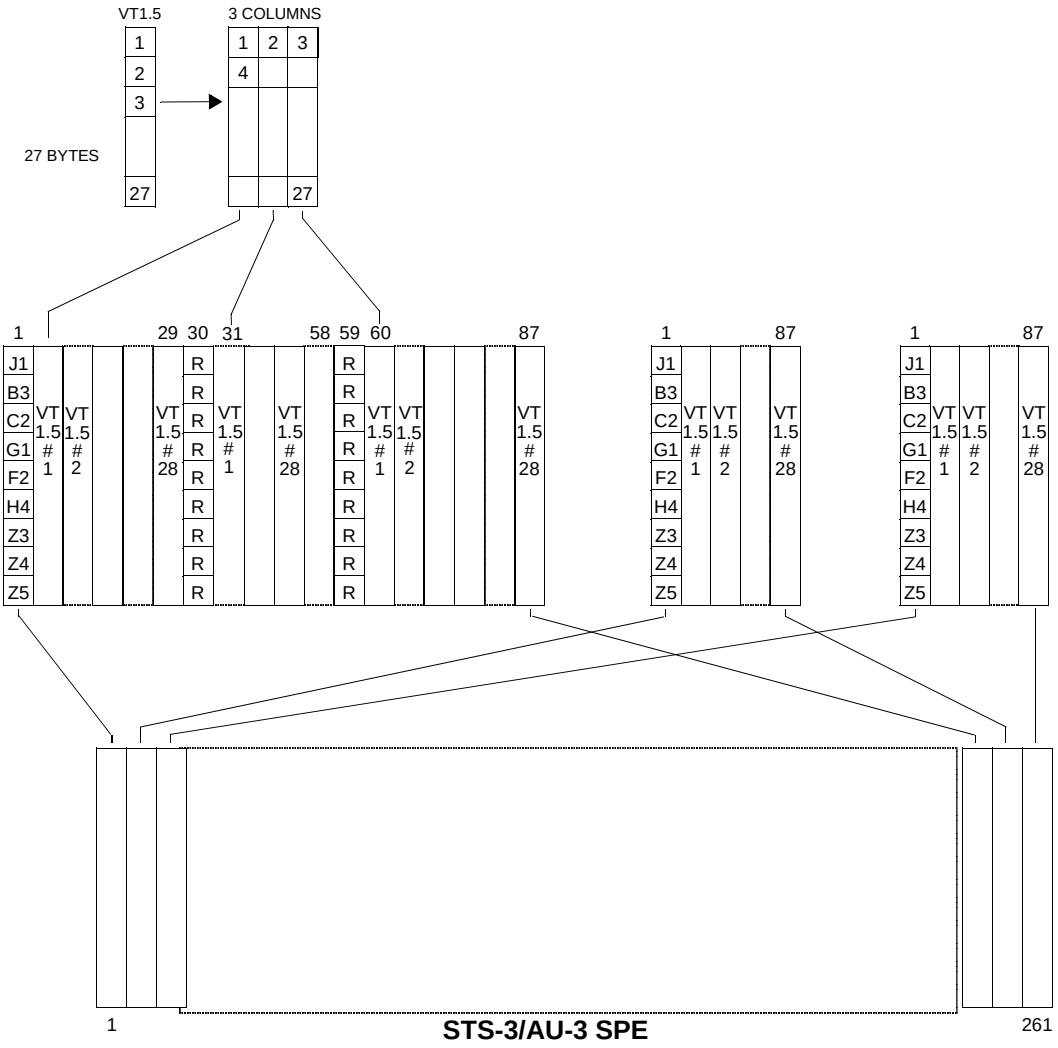
Scan Cell No.	I/O	Lead No.	Symbol	Comments
275	output3	T2	tvtf15	
276	output3	R3	aadd	
277	bidir	P4	aaclk	
278	output3	T1	aapar	
279	bidir	R2	aaspe	
280	bidir	R1	aac1j1v1	
281	control		*	'1' drives aac1j1v1,aaspe,aaclk to 'Z'
282	output3	P3	aa(0)	
283	output3	N4	aa(1)	
284	output3	P2	aa(2)	
285	output3	P1	aa(3)	
286	output3	N3	aa(4)	
287	output3	N2	aa(5)	
288	output3	M4	aa(6)	
289	output3	N1	aa(7)	
290	control		*	'1' drives aa(7:0), aapar to 'Z'
291	output3	M3	badd	
292	control		*	'1' drives aadd, badd, tvtfb15,tvtf15,tvtfb2,tvtf2, scanout(3:0) to 'Z'
293	output3	M2	bapar	
294	bidir	M1	baclk	
295	bidir	L1	baspe	
296	bidir	L2	bac1j1v1	
297	control		*	'1' drives bac1j1v1,baspe, baclk to 'Z'
298	output3	L3	ba(0)	
299	output3	K1	ba(1)	
300	output3	L4	ba(2)	
301	output3	K2	ba(3)	
302	output3	J1	ba(4)	
303	output3	K3	ba(5)	
304	clock	J2	adclk	
305	output3	K4	ba(6)	

Scan Cell No.	I/O	Lead No.	Symbol	Comments
306	output3	J3	ba(7)	
307	control		*	'1' drives ba(7:0), bapar to 'Z'
308	input	H1	adpar	
309	input	H2	adspe	
310	input	G1	adc1j1v1	
311	input	J4	ad(0)	
312	input	H3	ad(1)	
313	input	G2	ad(2)	
314	input	F1	ad(3)	
315	input	H4	ad(4)	
316	input	G3	ad(5)	
317	input	F2	ad(6)	
318	input	E1	ad(7)	
319	input	D1	bdpar	
320	clock	G4	bdclk	
321	input	F3	bdspe	
322	input	E2	bdc1j1v1	
323	input	F4	bd(0)	
324	input	C1	bd(1)	
325	input	D2	bd(2)	
326	input	C2	bd(3)	
327	input	E3	bd(4)	
328	input	E4	bd(5)	
329	input	B1	bd(6)	
330	input	D3	bd(7)	

MULTIPLEX FORMAT AND MAPPING INFORMATION

STS-3/AU-3 VT1.5/TU-11 (1.544 Mbit/s) Multiplex Format Mapping

The following diagram and table illustrate the mapping of the 84 VT1.5/TU-11s into an STS-3/AU-3 SPE. Each STS-3 carries three STS-1s. Column 1 in each STS-1/AU-3 is assigned to carry the path overhead bytes. Please note: the mapper does not insert the overhead bytes into the STS-1.



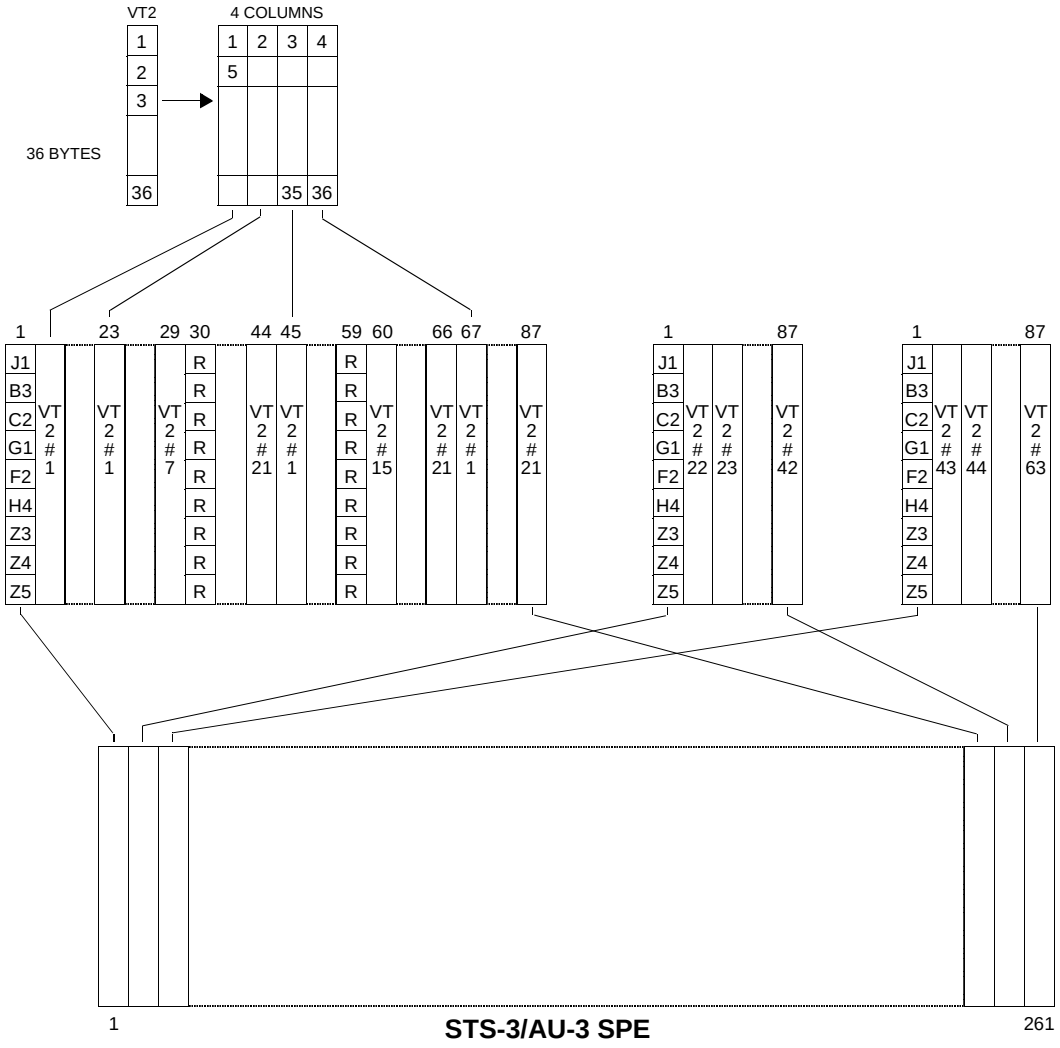
Note: Columns 88, 89, 90, 175, 176 and 177 are fixed stuff.

STS-3/AU-3 Mapping (1.544 Mbit/s)

TU#	VT/TU Assignment 7 6 5 4 3 2 1 0	VT/TU Column Numbers	TU#	VT/TU Assignment Registers 7 6 5 4 3 2 1 0	VT/TU Column Numbers	TU#	VT/TU Assignment 7 6 5 4 3 2 1 0	VT/TU Column Numbers
	0 0 0 0 0 0 0 0	No TU Selected						
1	0 0 1 0 0 1 0 1	4 91 178	29	0 1 0 0 0 1 0 1	5 92 179	57	0 1 1 0 0 1 0 1	6 93 180
2	0 0 1 0 1 0 0 1	7 94 181	30	0 1 0 0 1 0 0 1	8 95 182	58	0 1 1 0 1 0 0 1	9 96 183
3	0 0 1 0 1 1 0 1	10 97 184	31	0 1 0 0 1 1 0 1	11 98 185	59	0 1 1 0 1 1 0 1	12 99 186
4	0 0 1 1 0 0 0 1	13 100 187	32	0 1 0 1 0 0 0 1	14 101 188	60	0 1 1 1 0 0 0 1	15 102 189
5	0 0 1 1 0 1 0 1	16 103 190	33	0 1 0 1 0 1 0 1	17 104 191	61	0 1 1 1 0 1 0 1	18 105 192
6	0 0 1 1 1 0 0 1	19 106 193	34	0 1 0 1 1 0 0 1	20 107 194	62	0 1 1 1 1 0 0 1	21 108 195
7	0 0 1 1 1 1 0 1	22 109 196	35	0 1 0 1 1 1 0 1	23 110 197	63	0 1 1 1 1 1 0 1	24 111 198
8	0 0 1 0 0 1 1 0	25 112 199	36	0 1 0 0 0 1 1 0	26 113 200	64	0 1 1 0 0 1 1 0	27 114 201
9	0 0 1 0 1 0 1 0	28 115 202	37	0 1 0 0 1 0 1 0	29 116 203	65	0 1 1 0 1 0 1 0	30 117 204
10	0 0 1 0 1 1 1 0	31 118 205	38	0 1 0 0 1 1 1 0	32 119 206	66	0 1 1 0 1 1 1 0	33 120 207
11	0 0 1 1 0 0 1 0	34 121 208	39	0 1 0 1 0 0 1 0	35 122 209	67	0 1 1 1 0 0 1 0	36 123 210
12	0 0 1 1 0 1 1 0	37 124 211	40	0 1 0 1 0 1 1 0	38 125 212	68	0 1 1 1 0 1 1 0	39 126 213
13	0 0 1 1 1 0 1 0	40 127 214	41	0 1 0 1 1 0 1 0	41 128 215	69	0 1 1 1 1 0 1 0	42 129 216
14	0 0 1 1 1 1 1 0	43 130 217	42	0 1 0 1 1 1 1 0	44 131 218	70	0 1 1 1 1 1 1 0	45 132 219
15	0 0 1 0 0 1 1 1	46 133 220	43	0 1 0 0 0 1 1 1	47 134 221	71	0 1 1 0 0 1 1 1	48 135 222
16	0 0 1 0 1 0 1 1	49 136 223	44	0 1 0 0 1 0 1 1	50 137 224	72	0 1 1 0 1 0 1 1	51 138 225
17	0 0 1 0 1 1 1 1	52 139 226	45	0 1 0 0 1 1 1 1	53 140 227	73	0 1 1 0 1 1 1 1	54 141 228
18	0 0 1 1 0 0 1 1	55 142 229	46	0 1 0 1 0 0 1 1	56 143 230	74	0 1 1 1 0 0 1 1	57 144 231
19	0 0 1 1 0 1 1 1	58 145 232	47	0 1 0 1 0 1 1 1	59 146 233	75	0 1 1 1 0 1 1 1	60 147 234
20	0 0 1 1 1 0 1 1	61 148 235	48	0 1 0 1 1 0 1 1	62 149 236	76	0 1 1 1 1 0 1 1	63 150 237
21	0 0 1 1 1 1 1 1	64 151 238	49	0 1 0 1 1 1 1 1	65 152 239	77	0 1 1 1 1 1 1 1	66 153 240
22	0 0 1 0 0 1 0 0	67 154 241	50	0 1 0 0 0 1 0 0	68 155 242	78	0 1 1 0 0 1 0 0	69 156 243
23	0 0 1 0 1 0 0 0	70 157 244	51	0 1 0 0 1 0 0 0	71 158 245	79	0 1 1 0 1 0 0 0	72 159 246
24	0 0 1 0 1 1 0 0	73 160 247	52	0 1 0 0 1 1 0 0	74 161 248	80	0 1 1 0 1 1 0 0	75 162 249
25	0 0 1 1 0 0 0 0	76 163 250	53	0 1 0 1 0 0 0 0	77 164 251	81	0 1 1 1 0 0 0 0	78 165 252
26	0 0 1 1 0 1 0 0	79 166 253	54	0 1 0 1 0 1 0 0	80 167 254	82	0 1 1 1 0 1 0 0	81 168 255
27	0 0 1 1 1 0 0 0	82 169 256	55	0 1 0 1 1 0 0 0	83 170 257	83	0 1 1 1 1 0 0 0	84 171 258
28	0 0 1 1 1 1 0 0	85 172 259	56	0 1 0 1 1 1 0 0	86 173 260	84	0 1 1 1 1 1 0 0	87 174 261
	STS-1 #1, AU-3 A			STS-1 #2, AU-3 B			STS-1 #3, AU-3 C	

STS-3/AU-3 VT2/TU-12 (2.048 Mbit/s) Multiplex Format Mapping

The following diagram and table illustrate the mapping of the 63 VT2/TU-12s into an STS-3/AU-3 SPE. Each STS-3 carries three STS-1s. Column 1 in each STS-1/AU-3 is assigned to carry the path overhead bytes.



Note: Columns 88, 89, 90, 175, 176 and 177 are fixed stuff.

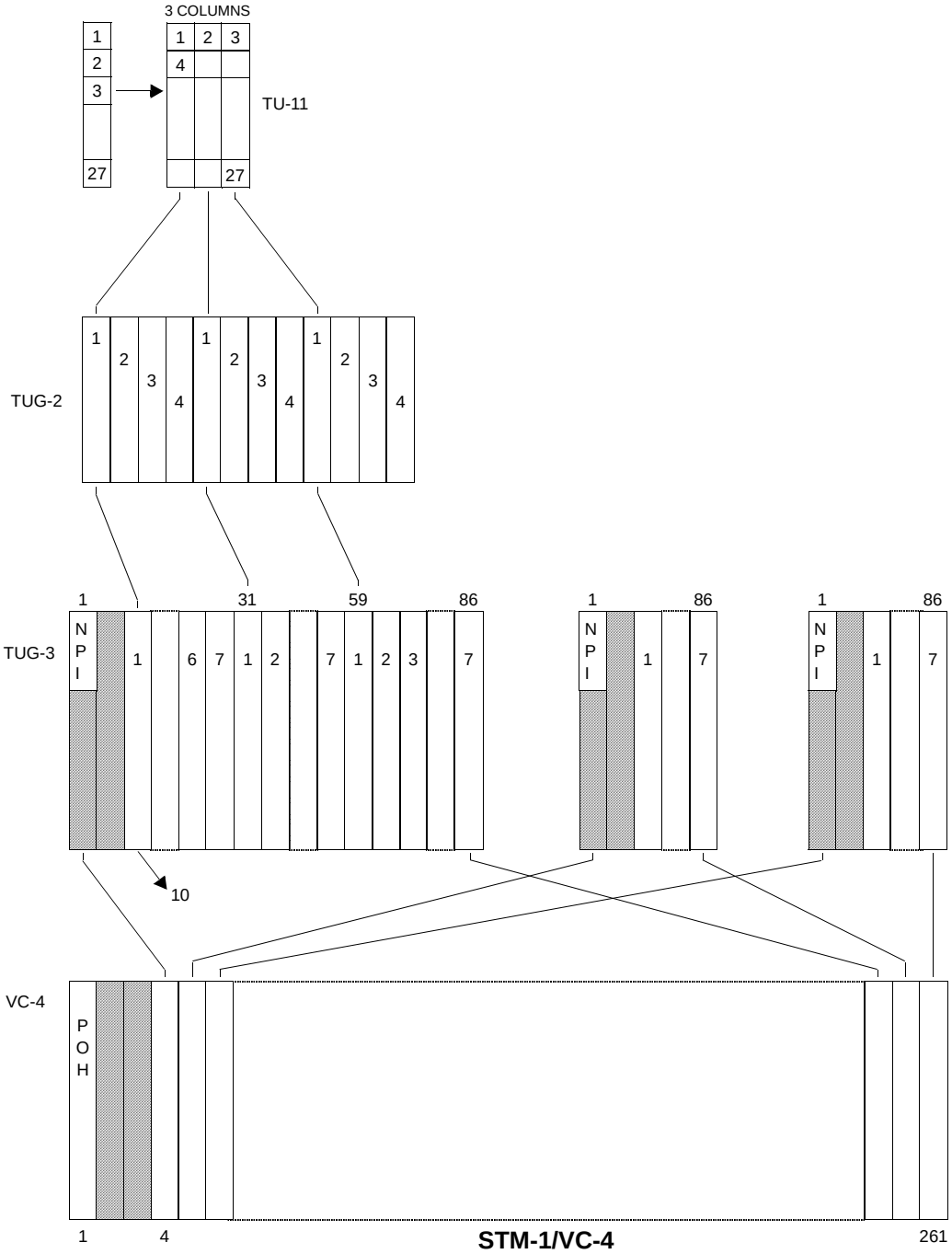
STS-3/AU-3 Mapping (2.048 Mbit/s)

TU/ VT #	VT/TU Assignment Registers 7 6 5 4 3 2 1 0	STS-3/AU-3 Column Numbers*	TU/ VT #	VT/TU Assignment Registers 7 6 5 4 3 2 1 0	STS-3/AU-3 Column Numbers*	TU/ VT #	VT/TU Assignment Registers 7 6 5 4 3 2 1 0	STS-3/AU-3 Column Numbers*
	1 0 0 0 0 0 0 0	No TU/VT Selected						
1	1 0 1 0 0 1 0 1	4, 67, 133, 199	22	1 1 0 0 0 1 0 1	5, 68, 134, 200	43	1 1 1 0 0 1 0 1	6, 69, 135, 201
2	1 0 1 0 1 0 0 1	7, 70, 136, 202	23	1 1 0 0 1 0 0 1	8, 71, 137, 203	44	1 1 1 0 1 0 0 1	9, 72, 138, 204
3	1 0 1 0 1 1 0 1	10, 73, 139, 205	24	1 1 0 0 1 1 0 1	11, 74, 140, 206	45	1 1 1 0 1 1 0 1	12, 75, 141, 207
4	1 0 1 1 0 0 0 1	13, 76, 142, 208	25	1 1 0 1 0 0 0 1	14, 77, 143, 209	46	1 1 1 1 0 0 0 1	15, 78, 144, 210
5	1 0 1 1 0 1 0 1	16, 79, 145, 211	26	1 1 0 1 0 1 0 1	17, 80, 146, 212	47	1 1 1 1 0 1 0 1	18, 81, 147, 213
6	1 0 1 1 1 0 0 1	19, 82, 148, 214	27	1 1 0 1 1 0 0 1	20, 83, 149, 215	48	1 1 1 1 1 0 0 1	21, 84, 150, 216
7	1 0 1 1 1 1 0 1	22, 85, 151, 217	28	1 1 0 1 1 1 0 1	23, 86, 152, 218	49	1 1 1 1 1 1 0 1	24, 87, 153, 219
8	1 0 1 0 0 1 1 0	25, 91, 154, 220	29	1 1 0 0 0 1 1 0	26, 92, 155, 221	50	1 1 1 0 0 1 1 0	27, 93, 156, 222
9	1 0 1 0 1 0 1 0	28, 94, 157, 223	30	1 1 0 0 1 0 1 0	29, 95, 158, 224	51	1 1 1 0 1 0 1 0	30, 96, 159, 225
10	1 0 1 0 1 1 1 0	31, 97, 160, 226	31	1 1 0 0 1 1 1 0	32, 98, 161, 227	52	1 1 1 0 1 1 1 0	33, 99, 162, 228
11	1 0 1 1 0 0 1 0	34, 100, 163, 229	32	1 1 0 1 0 0 1 0	35, 101, 164, 230	53	1 1 1 1 0 0 1 0	36, 102, 165, 231
12	1 0 1 1 0 1 1 0	37, 103, 166, 232	33	1 1 0 1 0 1 1 0	38, 104, 167, 233	54	1 1 1 1 0 1 1 0	39, 105, 168, 234
13	1 0 1 1 1 0 1 0	40, 106, 169, 235	34	1 1 0 1 1 0 1 0	41, 107, 170, 236	55	1 1 1 1 1 0 1 0	42, 108, 171, 237
14	1 0 1 1 1 1 1 0	43, 109, 172, 238	35	1 1 0 1 1 1 1 0	44, 110, 173, 239	56	1 1 1 1 1 1 1 0	45, 111, 174, 240
15	1 0 1 0 0 1 1 1	46, 112, 178, 241	36	1 1 0 0 0 1 1 1	47, 113, 179, 242	57	1 1 1 0 0 1 1 1	48, 114, 180, 243
16	1 0 1 0 1 0 1 1	49, 115, 181, 244	37	1 1 0 0 1 0 1 1	50, 116, 182, 245	58	1 1 1 0 1 0 1 1	51, 117, 183, 246
17	1 0 1 0 1 1 1 1	52, 118, 184, 247	38	1 1 0 0 1 1 1 1	53, 119, 185, 248	59	1 1 1 0 1 1 1 1	54, 120, 186, 249
18	1 0 1 1 0 0 1 1	55, 121, 187, 250	39	1 1 0 1 0 0 1 1	56, 122, 188, 251	60	1 1 1 1 0 0 1 1	57, 123, 189, 252
19	1 0 1 1 0 1 1 1	58, 124, 190, 253	40	1 1 0 1 0 1 1 1	59, 125, 191, 254	61	1 1 1 1 0 1 1 1	60, 126, 192, 255
20	1 0 1 1 1 0 1 1	61, 127, 193, 256	41	1 1 0 1 1 0 1 1	62, 128, 194, 257	62	1 1 1 1 1 0 1 1	63, 129, 195, 258
21	1 0 1 1 1 1 1 1	64, 130, 196, 259	42	1 1 0 1 1 1 1 1	65, 131, 197, 260	63	1 1 1 1 1 1 1 1	66, 132, 198, 261
	STS-1 #1, AU-3 A			STS-1 #2, AU-3 B			STS-1 #3, AU-3 C	

* Note: Columns 88, 89, 90, 175, 176 and 177 are fixed stuff.

STM-1/VC-4 TU-11 (1544 kbit/s) Multiplex Format Mapping

The following diagram and table illustrate the mapping of the 84 TU-11s into an STM-1/VC-4. The TEMx28 permits the mapping of up to 28 T1 line signals into any of the 84 available time slots when the VC-4 is configured to carry TU-11s.

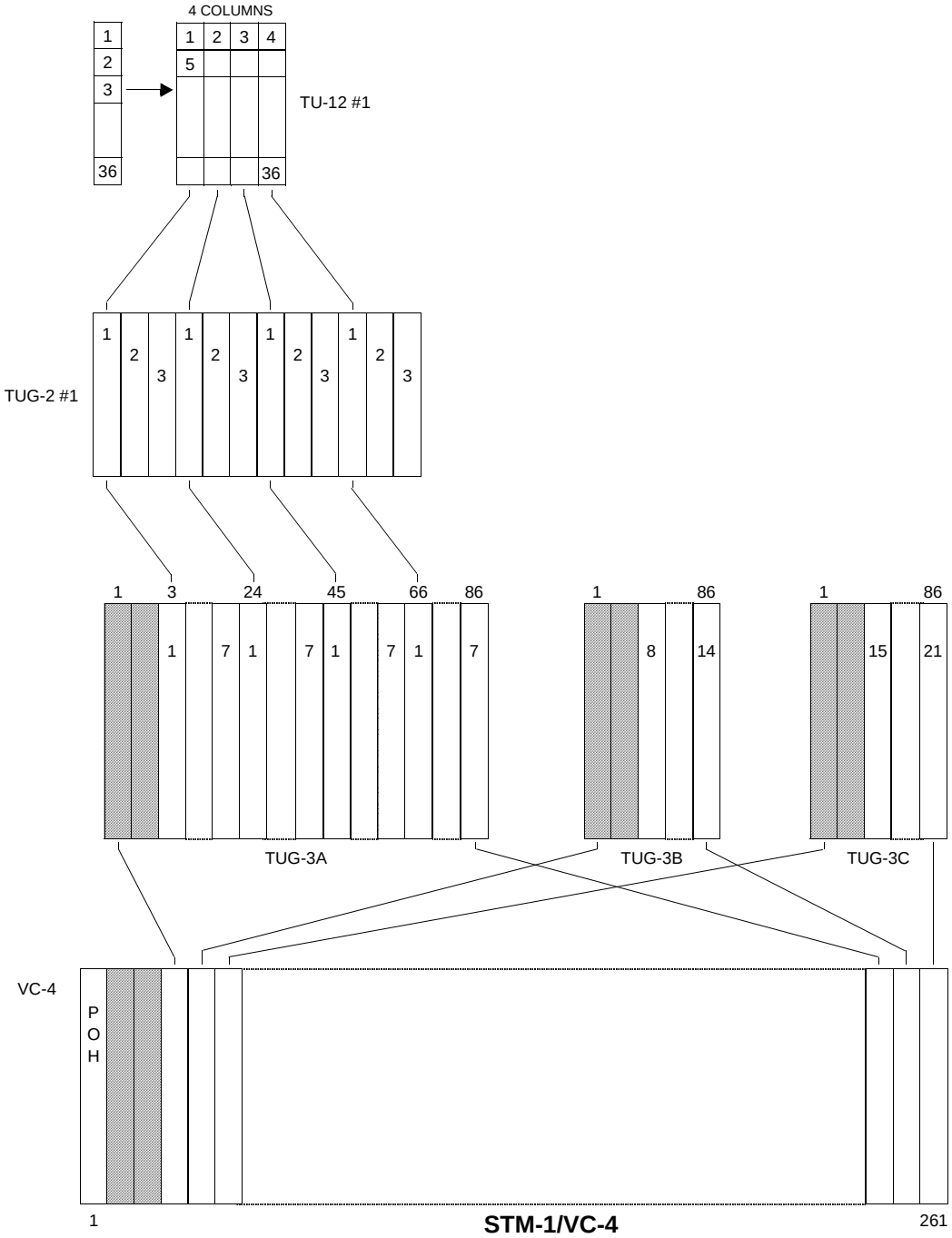


STM-1 VC-4 Mode (1.544 Mbit/s)

TU #	VT/TU Assignment Registers 7 6 5 4 3 2 1 0	VC-4 Column Numbers	TU #	VT/TU Assignment Registers 7 6 5 4 3 2 1 0	VC-4 Column Numbers	TU #	VT/TU Assignment Registers 7 6 5 4 3 2 1 0	VC-4 Column Numbers
	0 0 0 0 0 0 0 0	No TU Selected						
1	0 0 1 0 0 1 0 1	10 94 178	29	0 1 0 0 0 1 0 1	11 95 179	57	0 1 1 0 0 1 0 1	12 96 180
2	0 0 1 0 1 0 0 1	13 97 181	30	0 1 0 0 1 0 0 1	14 98 182	58	0 1 1 0 1 0 0 1	15 99 183
3	0 0 1 0 1 1 0 1	16 100 184	31	0 1 0 0 1 1 0 1	17 101 185	59	0 1 1 0 1 1 0 1	18 102 186
4	0 0 1 1 0 0 0 1	19 103 187	32	0 1 0 1 0 0 0 1	20 104 188	60	0 1 1 1 0 0 0 1	21 105 189
5	0 0 1 1 0 1 0 1	22 106 190	33	0 1 0 1 0 1 0 1	23 107 191	61	0 1 1 1 0 1 0 1	24 108 192
6	0 0 1 1 1 0 0 1	25 109 193	34	0 1 0 1 1 0 0 1	26 110 194	62	0 1 1 1 1 0 0 1	27 111 195
7	0 0 1 1 1 1 0 1	28 112 196	35	0 1 0 1 1 1 0 1	29 113 197	63	0 1 1 1 1 1 0 1	30 114 198
8	0 0 1 0 0 1 1 0	31 115 199	36	0 1 0 0 0 1 1 0	32 116 200	64	0 1 1 0 0 1 1 0	33 117 201
9	0 0 1 0 1 0 1 0	34 118 202	37	0 1 0 0 1 0 1 0	35 119 203	65	0 1 1 0 1 0 1 0	36 120 204
10	0 0 1 0 1 1 1 0	37 121 205	38	0 1 0 0 1 1 1 0	38 122 206	66	0 1 1 0 1 1 1 0	39 123 207
11	0 0 1 1 0 0 1 0	40 124 208	39	0 1 0 1 0 0 1 0	41 125 209	67	0 1 1 1 0 0 1 0	42 126 210
12	0 0 1 1 0 1 1 0	43 127 211	40	0 1 0 1 0 1 1 0	44 128 212	68	0 1 1 1 0 1 1 0	45 129 213
13	0 0 1 1 1 0 1 0	46 130 214	41	0 1 0 1 1 0 1 0	47 131 215	69	0 1 1 1 1 0 1 0	48 132 216
14	0 0 1 1 1 1 1 0	49 133 217	42	0 1 0 1 1 1 1 0	50 134 218	70	0 1 1 1 1 1 1 0	51 135 219
15	0 0 1 0 0 1 1 1	52 136 220	43	0 1 0 0 0 1 1 1	53 137 221	71	0 1 1 0 0 1 1 1	54 138 222
16	0 0 1 0 1 0 1 1	55 139 223	44	0 1 0 0 1 0 1 1	56 140 224	72	0 1 1 0 1 0 1 0	57 141 225
17	0 0 1 0 1 1 1 1	58 142 226	45	0 1 0 0 1 1 1 1	59 143 227	73	0 1 1 0 1 1 1 0	60 144 228
18	0 0 1 1 0 0 1 1	61 145 229	46	0 1 0 1 0 0 1 1	62 146 230	74	0 1 1 1 0 0 1 0	63 147 231
19	0 0 1 1 0 1 1 1	64 148 232	47	0 1 0 1 0 1 1 1	65 149 233	75	0 1 1 1 0 1 1 0	66 150 234
20	0 0 1 1 1 0 1 1	67 151 235	48	0 1 0 1 1 0 1 1	68 152 236	76	0 1 1 1 1 0 1 0	69 153 237
21	0 0 1 1 1 1 1 1	70 154 238	49	0 1 0 1 1 1 1 1	71 155 239	77	0 1 1 1 1 1 1 0	72 156 240
22	0 0 1 0 0 1 0 0	73 157 241	50	0 1 0 0 0 1 0 0	74 158 242	78	0 1 1 0 0 1 0 0	75 159 243
23	0 0 1 0 1 0 0 0	76 160 244	51	0 1 0 0 1 0 0 0	77 161 245	79	0 1 1 0 1 0 0 0	78 162 246
24	0 0 1 0 1 1 0 0	79 163 247	52	0 1 0 0 1 1 0 0	80 164 248	80	0 1 1 0 1 1 0 0	81 165 249
25	0 0 1 1 0 0 0 0	82 166 250	53	0 1 0 1 0 0 0 0	83 167 251	81	0 1 1 1 0 0 0 0	84 168 252
26	0 0 1 1 0 1 0 0	85 169 253	54	0 1 0 1 0 1 0 0	86 170 254	82	0 1 1 1 0 1 0 0	87 171 255
27	0 0 1 1 1 0 0 0	89 172 256	55	0 1 0 1 1 0 0 0	89 173 257	83	0 1 1 1 1 0 0 0	90 174 258
28	0 0 1 1 1 1 0 0	91 175 259	56	0 1 0 1 1 1 0 0	92 176 260	84	0 1 1 1 1 1 0 0	93 177 261
	TUG-3 A			TUG-3 B			TUG-3 C	

STM-1/VC-4 TU-12 (2048 kbit/s) Multiplex Format Mapping

The following diagram and table illustrate the mapping of the 63 TU-12s into an STM-1/VC-4. The TEMx28 permits the mapping of up to 28 E1 line signals into any of the 63 available time slots when the VC-4 is configured to carry TU-12s.



STM-1 VC-4 Mode (2048 kbit/s)

TU #	VT/TU Assignment Registers 7 6 5 4 3 2 1 0	VC-4 Column Numbers	TU #	VT/TU Assignment Registers 7 6 5 4 3 2 1 0	VC-4 Column Numbers	TU #	VT/TU Assignment Registers 7 6 5 4 3 2 1 0	VC-4 Column Numbers
	1 0 0 0 0 0 0 0	No TU Selected						
1	1 0 1 0 0 1 0 1	10, 73, 136, 199	22	1 1 0 0 0 1 0 1	11, 74, 137, 200	43	1 1 1 0 0 1 0 1	12, 75, 138, 201
2	1 0 1 0 1 0 0 1	13, 76, 139, 202	23	1 1 0 0 1 0 0 1	14, 77, 140, 203	44	1 1 1 0 1 0 0 1	15, 78, 141, 204
3	1 0 1 0 1 1 0 1	16, 79, 142, 205	24	1 1 0 0 1 1 0 1	17, 80, 143, 206	45	1 1 1 0 1 1 0 1	18, 81, 144, 207
4	1 0 1 1 0 0 0 1	19, 82, 145, 208	25	1 1 0 1 0 0 0 1	20, 83, 146, 209	46	1 1 1 1 0 0 0 1	21, 84, 147, 210
5	1 0 1 1 0 1 0 1	22, 85, 148, 211	26	1 1 0 1 0 1 0 1	23, 86, 149, 212	47	1 1 1 1 0 1 0 1	24, 87, 150, 213
6	1 0 1 1 1 0 0 1	25, 88, 151, 214	27	1 1 0 1 1 0 0 1	26, 89, 152, 215	48	1 1 1 1 1 0 0 1	27, 90, 153, 216
7	1 0 1 1 1 1 0 1	28, 91, 154, 217	28	1 1 0 1 1 1 0 1	29, 92, 155, 218	49	1 1 1 1 1 1 0 1	30, 93, 156, 219
8	1 0 1 0 0 1 1 0	31, 94, 157, 220	29	1 1 0 0 0 1 1 0	32, 95, 158, 221	50	1 1 1 0 0 1 1 0	33, 96, 159, 222
9	1 0 1 0 1 0 1 0	34, 97, 160, 223	30	1 1 0 0 1 0 1 0	35, 98, 161, 224	51	1 1 1 0 1 0 1 0	36, 99, 162, 225
10	1 0 1 0 1 1 1 0	37, 100, 163, 226	31	1 1 0 0 1 1 1 0	38, 101, 164, 227	52	1 1 1 0 1 1 1 0	39, 102, 165, 228
11	1 0 1 1 0 0 1 0	40, 103, 166, 229	32	1 1 0 1 0 0 1 0	41, 104, 167, 230	53	1 1 1 1 0 0 1 0	42, 105, 168, 231
12	1 0 1 1 0 1 1 0	43, 106, 169, 232	33	1 1 0 1 0 1 1 0	44, 107, 170, 233	54	1 1 1 1 0 1 1 0	45, 108, 171, 234
13	1 0 1 1 1 0 1 0	46, 109, 172, 235	34	1 1 0 1 1 0 1 0	47, 110, 173, 236	55	1 1 1 1 1 0 1 0	48, 111, 174, 237
14	1 0 1 1 1 1 1 0	49, 112, 175, 238	35	1 1 0 1 1 1 1 0	50, 113, 176, 239	56	1 1 1 1 1 1 1 0	51, 114, 177, 240
15	1 0 1 0 0 1 1 1	52, 115, 178, 241	36	1 1 0 0 0 1 1 1	53, 116, 179, 242	57	1 1 1 0 0 1 1 1	54, 117, 180, 243
16	1 0 1 0 1 0 1 1	55, 118, 181, 244	37	1 1 0 0 1 0 1 1	56, 119, 182, 245	58	1 1 1 0 1 0 1 1	57, 120, 183, 246
17	1 0 1 0 1 1 1 1	58, 121, 184, 247	38	1 1 0 0 1 1 1 1	59, 122, 185, 248	59	1 1 1 0 1 1 1 1	60, 123, 186, 249
18	1 0 1 1 0 0 1 1	61, 124, 187, 250	39	1 1 0 1 0 0 1 1	62, 125, 188, 251	60	1 1 1 1 0 0 1 1	63, 126, 189, 252
19	1 0 1 1 0 1 1 1	64, 127, 190, 253	40	1 1 0 1 0 1 1 1	65, 128, 191, 254	61	1 1 1 1 0 1 1 1	66, 129, 192, 255
20	1 0 1 1 1 0 1 1	67, 130, 193, 256	41	1 1 0 1 1 0 1 1	68, 131, 194, 257	62	1 1 1 1 1 0 1 1	69, 132, 195, 258
21	1 0 1 1 1 1 1 1	70, 133, 196, 259	42	1 1 0 1 1 1 1 1	71, 134, 197, 260	63	1 1 1 1 1 1 1 1	72, 135, 198, 261

MEMORY MAP

The TEMx28 mapper memory map consists of control bits, status indications, and counters which may be accessed by the microprocessor. The memory map segment consists of those functions which are common to all channels and per channel address locations. The address field for the TEMx28 consists of 15 bits (A14 -A0). Address bits A14-A10 are used to access a page., while address bits A9-A0 define functions within the page. Address locations within the range of 00+000H to 00+097H are allocated for common device functions for all channels. Address locations between 098H and 3FFH are unassigned.

Address locations between X+000H and X+20BH are allocated for each of the 28 channels. Address locations between X+21BH and X+3FFH are unassigned, where X is equal to 01H for channel 1 and 1CH for channel 28. X equals 00H for the TEMx28 common functions. Address locations for X equal to 1DH and 1FH are unassigned. Unassigned address locations should not be accessed by the microprocessor.

Unused bit positions within a register location may contain unspecified values when read, unless a 0 or 1 value is indicated in the tables below. Unused address locations can be written to by the microprocessor, in which case the unused bit positions must always be set to 0 unless otherwise noted.

Counters other then the one second performance counters may be configured to roll over, or saturating. When the counters are configured as roll-over, a counter will roll-over to the value of 1 on the next count after the counter reaches its maximum value. When the counters are configured to be saturation, a counter that is read by the microprocessor will clear. All counters within the TEMx28 will be cleared when a 1 is written to control bit RESETC (bit 5, 01AH). The low byte (bits 7-0) of a 16 bit counter should be read first immediately followed by reading the high byte (bits 15-8). During a read cycle, counts that occur during the read cycle will be held until the completion of the read cycle. Except for the Tandem Connection feature, current and previous one second counters are provided. The counters are disabled when the one second pulse is not provided. The current one second counters, and previous one counters are updated at one second intervals by the rising edge of the externally generated one second pulse.

All alarm bits have the following status bit locations: unlatched, latched, one second, and previous one second indications. A latched alarm bit position is reset on a microprocessor read cycle. The one second, and previous one second alarm bit positions are disabled when the one second pulse is not provided. An alarm bit latches on a positive transition, negative transition, or a positive or negative transition.

All the register status fields will use the following notations: R=Read; R(L)=Read (Latched); R/W=Read/Write; or W=Write.

DEVICE ID

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
000	R	1	1	0	1	0	1	1	1
001	R	1	1	1	0	0	0	0	0
002	R	0	0	0	0	0	1	1	1
003	R	Revision (Version) Level				0	0	0	1
004	R	Set to 0000				Set to 0000			

COMMON CONTROL REGISTERS - A and B SIDES

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
006	R/W								RESETH

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00B to 017		Reserved							
018	R/W					PRBSA		PRBSG	
019	R/W				CLPBK		DV1SEL	PDDO	DBPE
01A	R/W			RESETC	BLOCK			STS3	CROV
01B	R/W	INTR1	INTR0					PTALTE	V5AL10
01C		Reserved							
01D	R/W	TCTAE	J2AISEN	PLSAISE	UQAISE		UAISE	SE1AIS	HEAISE
01E	R/W					VCAISE	DLCAE	TCUAE	TCAISE
01F	R/W		VCTCE	DLCTE	J2TCE	PLSTCE	UQTCE		USTCE
020	R/W		VCRDIE	DLCRE	PSRDIE		J2RDIE	UQRDIE	URDIE
021 to 038		Reserved							
039	R/W								DRESET
03A	R/W	TJUST	PADO	ABPE	TOBWZ		BAHZE	AAHZE	ADDI
03B	R/W						TB2DIS	ABOD	THRSBY
03C	R/W								TRESET

MASK BITS FOR BUS A AND B STATUS ALARMS

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
005	R/W	HINT		MGDA	MGDB	MGAB	MPCDA	MPCDB	MPCAB
007	R/W		MDVCAIS	MDUNEQ	MDRDIC	MDRDIP	MDRDIS	MDSLER	MDRFI
008	R/W				MDRFFE	MDAIS	MDLOP	MDNDF	MDSIZE
009	R/W		MTAIS	MTFFE	MOOL	MTLOS	MTLOC	MDJ2TIM	MDJ2LOL
00A	R/W	MTCLM	MTCLL	MTCTM	MTCAIS	MTCUQ	MTCRDI	MTCODI	
03D	R/W	Reserved						MBBLOC	MABLOC
03E		Reserved							
03F	R/W	Channel Polling Register (Channels 8-1) Add Alarm Mask Bits							
040	R/W	Channel Polling Register (Channels 16-9) Add Alarm Mask Bits							
041	R/W	Channel Polling Register (Channels 24-17) Add Alarm Mask Bits							
042	R/W	Reserved				Channel Polling Register (Channels 28-25) Add Alarm Mask Bits			

BUS A AND B COMMON STATUS ALARMS

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
050	R			GDA	GDB	GAB	PCDA	PCDB	PCAB
051	R							BBLOC	ABLOC
052	R(L)							LBBLOC	LABLOC
053	R							PBBLOC	PABLOC
054	R							FBBLOC	FABLOC
055	R	Channel Polling Register (Channels 8-1) Add Alarm Bits							
056	R	Channel Polling Register (Channels 16-9) Add Alarm Bits							
057	R	Channel Polling Register (Channels 24-17) Add Alarm Bits							
058	R	Reserved				Channel Polling Register (Channels 28-25) Add Alarm Bits			
059	R	Reserved							RESETD
05A to 05F	R	Reserved							

MASK BITS FOR BUS A DROP ALARMS

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
043	R/W				MA3UAIS	MA2UAIS	MA1UAIS	MADPAR	MADLOC
044	R/W			MA3OOM	MA2OOM	MA1OOM	MA3LOM	MA2LOM	MA1LOM
045	R/W	Channel Polling Register (Channels 8-1) A Bus Drop Alarm Mask Bits							
046	R/W	Channel Polling Register (Channels 16-9) A Bus Drop Alarm Mask Bits							
047	R/W	Channel Polling Register (Channels 24-17) A Bus Drop Alarm Mask Bits							
048	R/W	Reserved				Channel Polling Register (Channels 28-25) A Bus Drop Alarm Mask Bits			

A DROP BUS STATUS REGISTERS AND TOH REGISTERS

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
060	R				A3UAIS	A2UAIS	A1UAIS	ADPAR	ADLOC
061	R			A3HOOM	A2HOOM	A1HOOM	A3HLOM	A2HLOM	A1HLOM
062	R(L)				LA3UAIS	LA2UAIS	LA1UAIS	LADPAR	LADLOC
063	R(L)			LA3HOOM	LA2HOOM	LA1HOOM	LA3HLOM	LA2HLOM	LA1HLOM
064	R				PA3UAIS	PA2UAIS	PA1UAIS	PADPAR	PADLOC
065	R			PA3HOOM	PA2HOOM	PA1HOOM	PA3HLOM	PA2HLOM	PA1HLOM
066	R				FA3UAIS	FA2UAIS	FA1UAIS	FADPAR	FADLOC
067	R			FA3HOOM	FA2HOOM	FA1HOOM	FA3HLOM	FA2HLOM	FA1HLOM
068	R	A Side Drop Bus H1 Pointer Byte (STS-3 STS-1 No. 1, STM-1 VC-4)							
069	R	A Side Drop Bus H1 Pointer Byte (STS-3 STS-1 No. 2)							
06A	R	A Side Drop Bus H1 Pointer Byte (STS-3 STS-1 No. 3)							
06B	R	A Side Drop Bus H2 Pointer Byte (STS-3 STS-1 No. 1, STM-1 VC-4)							
06C	R	A Side Drop Bus H2 Pointer Byte (STS-3 STS-1 No. 2)							
06D	R	A Side Drop Bus H2 Pointer Byte (STS-3 STS-1 No. 3)							
06E	R	A Side Drop Bus H4 Overhead Byte (STS-3 STS-1 No. 1, STM-1 VC-4)							
06F	R	A Side Drop Bus H4 Overhead Byte (STS-3 STS-1 No. 2)							
070	R	A Side Drop Bus H4 Overhead Byte (STS-3 STS-1 No. 3)							
071	R	A Side Drop Bus E1 Overhead Byte (STS-3 STS-1 No. 1, STM-1 VC-4)							
072	R	A Side Drop Bus E1 Overhead Byte (STS-3 STS-1 No. 2)							
073	R	A Side Drop Bus E1 Overhead Byte (STS-3 STS-1 No. 3)							
074	R	A Side Drop Channel Polling Register (Channels 8-1) Alarm Bits							
075	R	A Side Drop Bus Channel Polling Register (Channels 16-9) Alarm Bits							
076	R	A Side Drop Bus Channel Polling Register (Channels 24-17) Alarm Bits							
077	R	Reserved				A Side Drop Channel Polling Register (Channels 28-25) Alarm Bits			
078 to 07F	R	Reserved							

MASK BITS FOR BUS B DROP ALARMS

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
049	R/W				MB3UAIS	MB2UAIS	MB1UAIS	MBDPAR	MBDLOC
04A	R/W			MB3OOM	MB2OOM	MB1OOM	MB3LOM	MB2LOM	MB1LOM
04B	R/W	Channel Polling Register (Channels 8-1) B Bus Drop Alarm Mask Bits							
04C	R/W	Channel Polling Register (Channels 16-9) B Bus Drop Alarm Mask Bits							
04D	R/W	Channel Polling Register (Channels 24-17) B Bus Drop Alarm Mask Bits							
04E	R/W	Reserved				Channel Polling Register (Channels 28-25) B Bus Drop Alarm Mask Bits			
04F	R	Reserved							

B DROP BUS STATUS REGISTERS AND TOH REGISTERS

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
080	R				B3UAIS	B2UAIS	B1UAIS	BDPAR	BDLOC
081	R			B3HOOM	B2HOOM	B1HOOM	B3HLOM	B2HLOM	B1HLOM
082	R(L)				LB3UAIS	LB2UAIS	LB1UAIS	LBDPAR	LBDLOC
083	R(L)			LB3HOOM	LB2HOOM	LB1HOOM	LB3HLOM	LB2HLOM	LB1HLOM
084	R				PB3UAIS	PB2UAIS	PB1UAIS	PBDPAR	PBDLOC
085	R			PB3HOOM	PB2HOOM	PB1HOOM	PB3HLOM	PB2HLOM	PB1HLOM
086	R				FB3UAIS	FB2UAIS	FB1UAIS	FBDPAR	FBDLOC
087	R			FB3HOOM	FB2HOOM	FB1HOOM	FB3HLOM	FB2HLOM	FB1HLOM
088	R	B Side Drop Bus H1 Pointer Byte (STS-3 STS-1 No. 1, STM-1 VC-4)							
089	R	B Side Drop Bus H1 Pointer Byte (STS-3 STS-1 No. 2)							
08A	R	B Side Drop Bus H1 Pointer Byte (STS-3 STS-1 No. 3)							
08B	R	B Side Drop Bus H2 Pointer Byte (STS-3 STS-1 No. 1, STM-1 VC-4)							
08C	R	B Side Drop Bus H2 Pointer Byte (STS-3 STS-1 No. 2)							
08D	R	B Side Drop Bus H2 Pointer Byte (STS-3 STS-1 No. 3)							
08E	R	B Side Drop Bus H4 Overhead Byte (STS-3 STS-1 No. 1, STM-1 VC-4)							
08F	R	B Side Drop Bus H4 Overhead Byte (STS-3 STS-1 No. 2)							
090	R	B Side Drop Bus H4 Overhead Byte (STS-3 STS-1 No. 3)							
091	R	B Side Drop Bus E1 Overhead Byte (STS-3 STS-1 No. 1, STM-1 VC-4)							
092	R	B Side Drop Bus E1 Overhead Byte (STS-3 STS-1 No. 2)							
093	R	B Side Drop Bus E1 Overhead Byte (STS-3 STS-1 No. 3)							
094	R	B Side Drop Channel Polling Register (Channels 8-1) Alarm Bits							
095	R	B Side Drop Channel Polling Register (Channels 16-9) Alarm Bits							
096	R	B Side Drop Channel Polling Register (Channels 24-17) Alarm Bits							
097	R	Reserved				B Side Drop Channel Polling Register (Channels 28-25) Alarm Bits			
098 to 33F	R	Reserved							

CHANNEL n - A AND B DROP AND ADD SIDE CONTROL REGISTERS (n = 1 to 28)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+000	R/W			RnNRZP		RnCLKI	RnB8ZS		RnLAIS
X+001		Reserved							
X+002	R/W	TnLINT1-0		TnNRZP	TnE1SL	TnCLKI	TnB8ZS	TnSAIS	TnAISE
X+003	R/W							EXnLOS	EXnLOSP
X+004	R/W			TnPTG	TnANZ		TnPRN	LnLBK	FnLBK
X+006	R/W	RnLINT1-0		RnOUTL	RnE1SL	FnRDIS	RnSEL	TnSEL1	TnSEL0
X+007	R/W							TnVTVC	TnDISB
X+008	R/W				RnVTVC	RnDIEN	TCnRE	RnAISE	RnSAIS
X+009	R/W								TnRESET
X+00A to X+00F	R	Reserved							

CHANNEL n - A SIDE CONTROL REGISTERS (n = 1 to 28)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+010	R/W			ARnTCEN	ARnSL(1-3)			ARnJ2S1	ARnJ2S0
X+011	R/W								DACHnR
X+012	R/W	A Side Drop Bus Channel n VT/TU Selection							
X+019	R	Reserved							
X+01A	R/W	A Side Add Bus Channel n VT/TU Selection							
X+01B	R	Reserved							
X+01C to X+05B	R/W	A Side Add Bus Channel n J2 Byte 64 Byte Message or A Side Add Bus Channel n J2 Byte 16 Byte Message (01CH - 02BH) Unused - 16 bytes (02CH - 03BH) A Side Add Bus Channel n N2 Byte 16 Byte Message (03CH - 04BH) Unused - 16 bytes (04CH - 05BH)							
X+05C	R/W	A Side Add Bus Channel n V1 Byte							
X+05D	R/W	A Side Add Bus Channel n V2 Byte							
X+05E	R/W	A Side Add Bus Channel n V4 Byte							
X+05F	R/W	A Side Add Bus Channel n O Bits							
X+060	R/W	A Side Add Bus Channel n V5 Byte							
X+061	R/W	A Side Add Bus Channel n N2 Byte							
X+062	R/W	A Side Add Bus Channel n K4 Byte							
X+063	R/W	ATnTCAIS	ATnGAIS	ATnTPTV	AnUQGE	AnUQSU	ATnTCEN	ATnJ2TEN	ATnJ2TSZ
X+064	R/W	ATnRFI	ATnRDIP	ATnRDIC	ATnRDIS	ATnFB2	ATnT-CUQ		ATnV5BS
X+065	R/W		ATnFFB	ATnSL(1-3)				ATnK4PC	AnHIGHZ
X+066	R/W						ATnTCSO	ATnTCSR	ATnV4BS
X+067 to X+07F	R	Reserved							

CHANNEL n - A SIDE DROP POINTER LEAK REGISTERS (n = 1 to 28)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+017	R/W	Pointer Leak Value (Bit 7-0)							
X+018	R/W	Reserved						Pointer Leak Value (Bit 9-8)	

CHANNEL n - B SIDE CONTROL REGISTERS (n = 1 to 28)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+080	R/W			BRnTCEN	BRnSL(1-3)			BRnJ2S1	BRnJ2S0
X+081	R/W								DBCHnR
X+082	R/W	B Side Drop Bus Channel n VT/TU Selection							
X+08A	R/W	B Side Add Bus Channel n VT/TU Selection							
X+08B		Reserved							
X+08C to X+0CB	R/W	B Side Add Bus Channel n J2 Byte 64 Byte Message or B Side Add Bus Channel n J2 Byte 16 Byte Message (0BCH - 09BH) Unused - 16 bytes (09CH - 0ABH) B Side Add Bus Channel n N2 Byte 16 Byte Message (0ACH - 0BBH) Unused - 16 bytes (0BCH - 0CBH)							
X+0CC	R/W	B Side Add Bus Channel n V1 Byte							
X+0CD	R/W	B Side Add Bus Channel n V2 Byte							
X+0CE	R/W	B Side Add Bus Channel n V4 Byte							
X+0CF	R/W	B Side Add Bus Channel n O Bits							
X+0D0	R/W	B Side Add Bus Channel n V5 Byte							
X+0D1	R/W	B Side Add Bus Channel n N2 Byte							
X+0D2	R/W	B Side Add Bus Channel n K4 Byte							
X+0D3	R/W	BTnTCAIS	BTnGAIS	BTnTPTV	BnUQGE	BnUQSU	BTnTCEN	BTnJ2TEN	BTnJ2TSZ
X+0D4	R/W	BTnRFI	BTnRDIP	BTnRDIC	BTnRDIS	BTnFB2	BTnTCUQ		BTnV5BS
X+0D5	R/W		BTnFFB	BTnSL(1-3)				BTnK4PC	BnHIGHZ
X+0D6	R/W						BTnTCSO	BTnTCSR	BTnV4BS
X+0D7 to X+0FF	R	Reserved							

CHANNEL n - B SIDE DROP POINTER LEAK REGISTERS (n = 1 to 28)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+087	R/W	Pointer Leak Value (Bit 7-0)							
X+088	R/W	Reserved						Pointer Leak Value (Bit 9-8)	
X+089	R	Reserved							

CHANNEL n - A AND B SIDE ADD ALARM MASK BIT REGISTERS (n = 1 to 28)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+005	R/W			MnTAIS	MnBTFE	MnATFE	MnOOL	MnTLOS	MnTLOC

CHANNEL n - A AND B SIDE ADD ALARM AND COUNTER REGISTERS (n = 1 to 28)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+100	R			TnAIS	TBnFFE	TAnFFE	CnOOL	TnLOS	TnLOC
X+101	R(L)			LTnAIS	LTBnFFE	LTAnFFE	LCnOOL	LTnLOS	LTnLOC
X+102		Reserved							
X+103	R			PTnAIS	PTBnFFE	PTAnFFE	PCnOOL	PTnLOS	PTnLOC
X+104	R			FTnAIS	FTBnFFE	FTAnFFE	FCnOOL	FTnLOS	FTnLOC
X+105	R/W	Code Violation Counter - Low Order Byte (7-0)							
X+106	R/W	Code Violation Counter - Low Order Byte (15-8)							
X+107	R/W	Previous One Second Code Violation Counter - Low Order Byte (7-0)							
X+108	R/W	Previous One second Code Violation Counter - Low Order Byte (15-8)							
X+109	R/W	Current One second Code Violation Counter - Low Order Byte (7-0)							
X+10A	R/W	Current One Second Code Violation Counter - Low Order Byte (15-8)							
X+10B to X+10F	R	Reserved							

CHANNEL n - A SIDE DROP ALARM MASK BIT REGISTERS (n = 1 to 28)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+013	R/W		MAnVAIS	MAnUQE	MAnRDIC	MAnRDIP	MAnRDIS	MAnSLER	MAnRFI
X+014	R/W				MAnRFE	MAnAIS	MAnLOP	MAnNDF	MAnSIZE
X+015	R/W							MAnJ2TIM	MAnJ2LOL
X+016	R/W	MAnTCLM	MAnTCLL	ManTCTM	MAnTCAIS	MAnTCUQ	MAnTCRDI	MAnTCODI	

CHANNEL n - A SIDE DROP STATUS REGISTERS (n = 1 to 28)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+110	R		AnVCAIS	AnUNEQ	AnRDIC	AnRDIP	AnRDIS	AnSLER	AnRFI
X+111	R				AnRFFE	AnAIS	AnLOP	AnNDF	AnSIZE
X+112	R							AnJ2TIM	AnJ2LOL
X+113	R	AnTCLM	AnTCLL	AnTCTM	AnTCAIS	AnTCUQ	AnTCRDI	AnTCODI	
X+114	R(L)		LAnVCAIS	LAnUNEQ	LAnRDIC	LAnRDIP	LAnRDIS	LAnSLER	LAnRFI
X+115	R(L)				LAnRFFE	LAnAIS	LAnLOP	LAnNDF	LAnSIZE
X+116	R(L)							LAnJ2TIM	LAnJ2LOL
X+117	R(L)	LAnTCLM	LAnTCLL	LAnTCTM	LAnTCAIS	LAnTCUQ	LAnTCRDI	LAnTCODI	
X+118	R		PAnVCAIS	PAnUNEQ	PAnRDIC	PAnRDIP	PAnRDIS	PAnSLER	PAnRFI
X+119	R				PAnRFFE	PAnAIS	PAnLOP	PAnNDF	PAnSIZE
X+11A	R							PAnJ2TIM	PAnJ2LOL
X+11B	R	PAnTCLM	PAnTCLL	PAnTCTM	PAnTCAIS	PAnTCUQ	PAnTCRDI	PAnTCODI	
X+11C	R		FAnVCAIS	FAnUNEQ	FAnRDIC	FAnRDIP	FAnRDIS	FAnSLER	FAnRFI
X+11D	R				FAnRFFE	FAnAIS	FAnLOP	FAnNDF	FAnSIZE
X+11E	R							FAnJ2TIM	FAnJ2LOL
X+11F	R	FAnTCLM	FAnTCLL	FAnTCTM	FAnTCAIS	FAnTCUQ	FAnTCRDI	FAnTCODI	

CHANNEL n - A SIDE DROP COUNTERS (n = 1 to 28)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+120	R/W	A Side Positive Justification Counter for Channel n - 8 bits							
X+121	R/W	A Side Negative Justification Counter for Channel n - 8 bits							

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+122	R/W	A Side REI (V5 byte) Counter for Channel n - 8 bits							
X+123	R/W	A Side BIP-2 (V5 byte) Counter for Channel n - 8 bits							
X+124	R/W	A Side TC OEI (N2 byte) Counter for Channel n - 8 bits							
X+125	R/W	A Side TC REI (N2 byte) Counter for Channel n - 8 bits							
X+126	R/W	A Side TC BIP-2 (N2 byte) Counter for Channel n - 8 bits							
X+127	R	A Side Previous One Second PJ Counter for Channel n - Low Order Count (7-0)							
X+128	R	A Side Previous One Second PJ Counter for Channel n - High Order Count (15-8)							
X+129	R	A Side Previous One Second NJ Counter for Channel n - Low Order Count (7-0)							
X+12A	R	A Side Previous One Second NJ Counter for Channel n - High Order Count (15-8)							
X+12B	R	A Side Previous One Second REI Counter for Channel n - Low Order Count (7-0)							
X+12C	R	A Side Previous One Second REI Counter for Channel n - High Order Count (15-8)							
X+12D	R	A Side Previous One Second BIP-2 Counter for Channel n - Low Order Count (7-0)							
X+12E	R	A Side Previous One Second BIP-2 Counter for Channel n - High Order Count (15-8)							
X+12F to X+134		Reserved							
X+135	R	A Side Current One Second PJ Counter for Channel n - Low Order Count (7-0)							
X+136	R	A Side Current One Second PJ Counter for Channel n - High Order Count (15-8)							
X+137	R	A Side Current One Second NJ Counter for Channel n - Low Order Count (7-0)							
X+138	R	A Side Current One Second NJ Counter for Channel n - High Order Count (15-8)							
X+139	R	A Side Current One Second REI Counter for Channel n - Low Order Count (7-0)							
X+13A	R	A Side Current One Second REI Counter for Channel n - High Order Count (15-8)							
X+13B	R	A Side Current One Second BIP-2 Counter for Channel n - Low Order Count (7-0)							
X+13C	R	A Side Current One Second BIP-2 Counter for Channel n - High Order Count (15-8)							
X+13D to X+142		Reserved							
X+20C to X+3FF		Reserved							

CHANNEL n - A SIDE DROP OVERHEAD BYTE REGISTERS (n = 1 to 28)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+143 to X+162	R	A Side Drop Bus Channel n J2 Byte 64 Byte Message or A Side Drop Bus Channel n J2 Byte 16 Byte Message A Side Drop Bus Channel n N2 Byte 16 Byte Message A Side Channel n Microprocessor written 16 Byte Message A Side Channel n Microprocessor written 16 Byte Message							
X+163 to X+182	R/W								
X+183	R	A Side Drop Bus Channel n V1 Byte							
X+184	R	A Side Drop Bus Channel n V2 Byte							
X+185	R	A Side Drop Bus Channel n V4 Byte							
X+186	R	A Side Drop Bus Channel n V5 Byte							
X+187	R	A Side Drop Bus Channel n J2 Byte							
X+188	R	A Side Drop Bus Channel n N2 Byte							
X+189	R	A Side Drop Bus Channel n K4 Byte							
X+18A	R	A Side Drop Bus Channel n O Bits							
X+18B		Reserved							

CHANNEL n - B SIDE DROP ALARM MASK BIT REGISTERS (n = 1 to 28)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+083	R/W		MBnVAIS	MBnUQE	MBnRDIC	MBnRDIP	MBnRDIS	MBnSLER	MBnRFI
X+084	R/W				MBnRFE	MBnAIS	MBnLOP	MBnNDF	MBnSIZE
X+085	R/W							MBnJ2TIM	MBnJ2LOL
X+086	R/W	MBnTCLM	MBnTCLL	MBnTCTM	MBnTCAIS	MBnTCUQ	MBnTCRDI	MBnTCODI	

CHANNEL n - B SIDE DROP STATUS REGISTERS (n = 1 to 28)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+190	R		BnVCAIS	BnUNEQ	BnRDIC	BnRDIP	BnRDIS	BnSLER	BnRFI
X+191	R				BnRFFE	BnAIS	BnLOP	BnNDF	BnSIZE
X+192	R							BnJ2TIM	BnJ2LOL
X+193	R	BnTCLM	BnTCLL	BnTCTM	BnTCAIS	BnTCUQ	BnTCRDI	BnTCODI	
X+194	R(L)		LBnVCAIS	LBnUNEQ	LBnRDIC	LBnRDIP	LBnRDIS	LBnSLER	LBnRFI
X+195	R(L)				LBnRFFE	LBnAIS	LBnLOP	LBnNDF	LBnSIZE
X+196	R(L)							LBnJ2TIM	LBnJ2LOL
X+197	R(L)	LBnTCLM	LBnTCLL	LBnTCTM	LBnTCAIS	LBnTCUQ	LBnTCRDI	LBnTCODI	
X+198	R		PBnVCAIS	PBnUNEQ	PBnRDIC	PBnRDIP	PBnRDIS	PBnSLER	PBnRFI
X+199	R				PBnRFFE	PBnAIS	PBnLOP	PBnNDF	PBnSIZE
X+19A	R							PBnJ2TIM	PBnJ2LOL
X+19B	R	PBnTCLM	PBnTCLL	PBnTCTM	PBnTCAIS	PBnTCUQ	PBnTCRDI	PBnTCODI	
X+19C	R		FBnVCAIS	FBnUNEQ	FBnRDIC	FBnRDIP	FBnRDIS	FBnSLER	FBnRFI
X+19D	R				FBnRFFE	FBnAIS	FBnLOP	FBnNDF	FBnSIZE
X+19E	R							FBnJ2TIM	FBnJ2LOL
X+19F	R	FBnTCLM	FBnTCLL	FBnTCTM	FBnTCAIS	FBnTCUQ	FBnTCRDI	FBnTCODI	

CHANNEL n - B SIDE DROP COUNTERS (n = 1 to 28)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+1A0	R/W	B Side Positive Justification Counter for Channel n - 8 bits							
X+1A1	R/W	B Side Negative Justification Counter for Channel n - 8 bits							
X+1A2	R/W	B Side REI (V5 byte) Counter for Channel n - 8 bits							
X+1A3	R/W	B Side BIP-2 (V5 byte) Counter for Channel n - 8 bits							
X+1A4	R/W	B Side TC OEI (N2 byte) Counter for Channel n - 8 bits							

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+1A5	R/W	B Side TC REI (N2 byte) Counter for Channel n - 8 bits							
X+1A6	R/W	B Side TC BIP-2 (N2 byte) Counter for Channel n - 8 bits							
X+1A7	R	B Side Previous One Second PJ Counter for Channel n - Low Order Count (7-0)							
X+1A8	R	B Side Previous One Second PJ Counter for Channel n - High Order Count (15-8)							
X+1A9	R	B Side Previous One Second NJ Counter for Channel n - Low Order Count (7-0)							
X+1AA	R	B Side Previous One Second NJ Counter for Channel n - High Order Count (15-8)							
X+1AB	R	B Side Previous One Second REI Counter for Channel n - Low Order Count (7-0)							
X+1AC	R	B Side Previous One Second REI Counter for Channel n - High Order Count (15-8)							
X+1AD	R	B Side Previous One Second BIP-2 Counter for Channel n - Low Order Count (7-0)							
X+1AE	R	B Side Previous One Second BIP-2 Counter for Channel n - High Order Count (15-8)							
X+1AF to X+1B4		Reserved							
X+1B5	R	B Side Current One Second PJ Counter for Channel n - Low Order Count (7-0)							
X+1B6	R	B Side Current One Second PJ Counter for Channel n - High Order Count (15-8)							
X+1B7	R	B Side Current One Second NJ Counter for Channel n - Low Order Count (7-0)							
X+1B8	R	B Side Current One Second NJ Counter for Channel n - High Order Count (15-8)							
X+1B9	R	B Side Current One Second REI Counter for Channel n - Low Order Count (7-0)							
X+1BA	R	B Side Current One Second REI Counter for Channel n - High Order Count (15-8)							
X+1BB	R	B Side Current One Second BIP-2 Counter for Channel n - Low Order Count (7-0)							
X+1BC	R	B Side Current One Second BIP-2 Counter for Channel n - High Order Count (15-8)							
X+1BD to X+1C2		Reserved							

CHANNEL n - B SIDE DROP OVERHEAD BYTE REGISTERS (n = 1 to 28)

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+1C3 to X+1E2	R	B Side Drop Bus Channel n J2 Byte 64 Byte Message or B Side Drop Bus Channel n J2 Byte 16 Byte Message B Side Drop Bus Channel n N2 Byte 16 Byte Message B Side Channel n Microprocessor written 16 Byte Message B Side Channel n Microprocessor written 16 Byte Message							
X+1E3 to X+202	R/W								
X+203	R	B Side Drop Bus Channel n V1 Byte							
X+204	R	B Side Drop Bus Channel n V2 Byte							
X+205	R	B Side Drop Bus Channel n V4 Byte							
X+206	R	B Side Drop Bus Channel n V5 Byte							

Address (Hex)	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X+207	R	B Side Drop Bus Channel n J2 Byte							
X+208	R	B Side Drop Bus Channel n N2 Byte							
X+209	R	B Side Drop Bus Channel n K4 Byte							
X+20A	R	B Side Drop Bus Channel n O Bits							
X+20B		Reserved							

MEMORY MAP DESCRIPTIONS

MANUFACTURER AND DEVICE IDENTIFICATION DESCRIPTION

The manufacturer and device identification are based on the field format given in IEEE standard 1149.1 on Boundary Scan, and the ID assigned by the Solid State Products Engineering Council (JEDEC) to the TranSwitch Corporation. The serial format for this ID, which is located in registers 000H through 003H, is shown below. Bit 7 in register 003H is at the left and bit 0 of register 000H is at the right:

MSB LSB

Revision	Part Number	Manufacturer Identifier	1
4 bits	16 bits	11 bits	

The manufacturer ID assigned for TranSwitch devices is defined as 107 Decimal, located in bits 7 through 1 (LSB) of register 000H, and bits 3 (MSB) through 0 of register 001H. The part number of the TEMx28 is 04222, which is expressed as a binary number in bits 7 through 4 (LSB) in register 001H, bits 7 through 0 in 002H, and bits 3 (MSB) through 0 in 003H. The revision field occupies bits 7 through 4 (LSB) in register 003H. The registers at address 004H is a read/write locations that is reserved for future use.

A AND B SIDE COMMON CONTROL REGISTERS - DESCRIPTIONS

Address	Bit	Symbol	Description
006	7-1		**Not used:**
	0	RESETH	**Reset Device:** This bit is equivalent to the hardware reset. When a 1 is written to this bit, the internal FIFOs and logic are reset to preset values, counters and control bits in the memory map are reset to zero. This bit is self clearing. Four microseconds after this bit is written with a 1, status bit RESETD (bit 0, register 059H) transitions to a 1. This transition indicates that the reset operation is complete and microprocessor access of the device can begin.
018	7-4		**Not used:**
	3	PRBSA	**Test Analyzer Add/Drop Direction:** When a 0 is written into this bit, the PRBS test analyzer for all channels are configured to be in the receive direction. Writing a 1 to this bit configures the PRBS analyzers to be in the transmit direction.
	2		**Not used:**
	1	PRBSG	**Test Generator Add/Drop Direction:** When a 0 is written into this bit, the PRBS test generators for all channels are configured to be in the transmit direction. Writing a 1 to this bit configures the PRBS generators to be in the receive direction.
	0		**Not used:**

Address	Bit	Symbol	Description
019	7-5		**Not used:**
	4	CLPBK	**COMBUS SONET/SDH Local Loopback:** A 1 written to this bit will enable a COMBUS SONET/SDH loopback. This loopback is valid for either the drop bus or add bus timing modes, and only when control bit DV1SEL (bit 2 below) is set to 1. When this loopback is enabled, the drop buses are inhibited from passing VT/TU to the demapper. VT/TU are mapped and demapped according to the VT/TU add and drop selection registers.
	3		**Not used:**
	2	DV1SEL	**Drop Bus V1 Reference Enable:** Common control bit for both the A and B drop buses. When set to 0, bits 7 and 8 in the H4 byte are monitored for the multiframe indication to determine the V1 byte location for all VT/TUs. When set to 1, the V1 pulse in the C1J1V1 signal carries the V1 byte location for all channels. A Drop Bus Reset operation should be performed after modifying this bit. See DRESET bit at address 039H.
	1	PDDO	**A/B Drop Bus Parity Detected on Data Only:** Common control bit for both drop buses. A 1 causes parity to be calculated over the data byte only. A 0 causes parity to be calculated over the data byte, SPE and C1J1V1 signals. Please refer to the table provided below for DBPE control bit.
	0	DBPE	**A/B Drop Bus Even Parity Detected:** This bit works in conjunction with the control bit PDDO above to determine the parity calculation in the drop direction. DBPE PDDO Action (for both A and B Drop buses) 0 0 Odd parity check over drop data, SPE, and C1J1V1. 0 1 Odd parity check over drop data only. 1 0 Even parity check over drop data, SPE, and C1J1V1. 1 1 Even parity check over drop data only. Other than reporting the event, no action is taken upon parity error indication.

Address	Bit	Symbol	Description
01A	7-6		**Not used:**
	5	RESETC	**Reset All Channel Counters.** A 1 written to this control bit causes all performance counters to be reset to a zero value (for saturating counters) or the FE/FFFE Hex values (for 8/16-bit non-saturating counters).
	4	BLOCK	**Block Count:** A 1 enables two BIP-2 errors in the V5 byte and the N2 Tandem Connection byte to be counted as a single error (block) for all performance counters. A 0 enables two BIP-2 errors to be counted as two errors.
	3-2		**Not used:**
	1	STS3	**STS-3 Mode Selection:** The TEMx28 SDH/SONET operating modes are according to the table below. A Drop Bus Reset operation should be performed after modifying this bit. See DRESET bit at address 039 STS3 — Format Selected 1 — STS-3 (STM-1 AU-3) format 0 — STM-1 AU-4 (STS-3c) format
	0	CROV	**Counters Roll-Over Enable:** A 0 configures all counters to be saturating unless otherwise noted. That is, all counters will stop at their specified maximum count value. A microprocessor read cycle will clear a saturating counter. A 1 configures all counters to function in the roll-over mode. That is, when the maximum count is reached in a counter, the next count causes it to roll over and start at a count of 0. A microprocessor read cycle does not clear a counter when the counters are configured in the roll-over mode. Upon power-up, this control bit is set to 0 (saturation mode). The counter will preset to the value FEH for 8-bit counters or the value FFFEH for 16-bit counters, when this control bit is set to 1, followed by writing a 1 to control bit RESETC (bit 5, 01AH). These are values selected to ensure that a roll-over occurs after a few counts.
01B	7 6	INTR1 INTR0	**Interrupt/Latched Alarm Positive/Negative Transition Selection:** An alarm will latch according to the alarm transitions given in the table below. INTR1 — INTR0 — Action 0 — 0 — No event or interrupt indication 1 — 0 — Latch on positive alarm transition 0 — 1 — Latch on negative alarm transition 1 — 1 — Latch on both positive and negative alarm transitions
	5-2		**Not used:**
	1	PTALTE	**Pointer Tracking AIS to LOP Transition Enabled:** A 1 enables the AIS to LOP transition in each of the pointer tracking state machines. A 0 will disables this transition.
	0	V5AL10	**V5 Alarm Detection Select 10:** A 1 selects 10 consecutive RDI assertions for detection and recovery for all channels. A 0 selects 5 consecutive RDI assertions for detection and recovery. The selection is valid for both three bit RDI and single bit RDI.

Address	Bit	Symbol	Description
01D	7	TCTAE	**Tandem Connection Loss Of Lock, Mismatch, Loss Of Multiframe Alarms Line AIS Enable:** A common control bit for both the A and B Drop bus Tandem Connection Loss of Lock (A/BnTCLL), Tandem Connection Mismatch (A/BnTCTM), and Tandem Connection Loss Of Multiframe (A/BLLM) alarms. A 1 enables any of these alarms for the active bus to generate line AIS provided control bit RnAISE is set to 1.
	6	J2AISEN	**J2 Alarm Line AIS Enable:** A common control for both the A and B Drop bus J2 alarms. A 1 enables a J2 Loss Of Lock (A/BnJ2LOL) or J2 Trace Mismatch (A/BJ2TIM) alarm for the active bus to generate line AIS provided control bit RnAISE is set to 1.
	5	PLSAISE	**Path Label Alarm Line AIS Enable:** A common control for both the A and B Drop bus path signal alarm (A/BnSLER). A 1 enables a path signal label mismatch alarm for the active bus to generate line AIS provided control bit RnAISE is set to 1.
	4	UQAISE	**Unequipped Line AIS Enable:** A common control for both the A and B Drop bus unequipped path signal alarm (A/BnUNEQ). A 1 enables a unequipped alarm for the active bus to generate line AIS provided control bit RnAISE is set to 1.
	3		**Not used:**
	2	UAISE	**Upstream AIS Alarm Line AIS Enable:** A common control for both the A and B Drop bus upstream AIS alarm (A/BxUAIS). A 1 enables an upstream AIS alarm for the active bus to generate line AIS provided control bit RnAISE is set to 1. Where x is equaled to the numbered STS-1 in the STS-3.
	1	SE1AIS	**Select E1AIS:** Works in conjunction with the HEAISE control bit described below. The HEAISE bit must be set to 1 in order for this control bit to function. A 1 enables the TOH E1 byte AIS detection circuit. A 0 enables the TOH H1/H2 byte AIS detection circuit.
	0	HEAISE	**A/B H1/H2 or E1 Byte AIS Enable:** Works in conjunction with the SE1AIS control bit described above. Common control for both the A and B Drop buses. A 1 enables AIS detection in either the SDH/SONET H1/H2 bytes (control bit SE1AIS is 0), or in the E1 bytes (control bit SE1AIS is 1). A 0 disables the detection of an upstream AIS state. Note that the TU/VT pointer tracking state machine AIS detection circuitry operates independently of H1/H2 or E1 byte AIS detection circuits.

Address	Bit	Symbol	Description
01E	7-4		**Not used:**
	3	VCAISE	**VC AIS Alarm Line AIS Enable:** A common control for both the A and B Drop bus signal label AIS alarm (A/BnVCAIS). A 1 enables a VC AIS alarm for the active bus to generate line AIS provided control bit RnAISE is set to 1.
	2	DLCAE	**Drop Bus Loss Of Clock Alarm Line AIS Enable:** A common control for both the A and B Drop bus upstream AIS alarm (A/BDLOC). A 1 enables a Drop Bus Loss Of Clock alarm for the active bus to generate line AIS provided control bit RnAISE is set to 1.
	1	TCUAE	**Tandem Connection Unequipped Alarm Line AIS Enable:** A common control for both the A and B Drop bus Tandem Connection unequipped alarm (A/BnTCUQ). A 1 enables an Tandem Connection unequipped alarm for the active bus to generate line AIS provided control bit RnAISE is set to 1.
	0	TCAISE	**Tandem Connection AIS Alarm Line AIS Enable:** A common control for both the A and B Drop bus Tandem Connection AIS alarm (A/BnTCAIS). A 1 enables an Tandem Connection AIS alarm for the active bus to generate line AIS provided control bit RnAISE is set to 1.

Address	Bit	Symbol	Description
01F	7		**Not used:**
	6	VCTCE	**VC AIS Alarm Tandem Connection RDI/ODI Enable:** A common control for both the A and B Drop bus signal label AIS alarm (A/BnVCAIS). A 1 enables a VC AIS alarm for the active bus to generate a Tandem Connection RDI and ODI provided control bit TCnREis set to 1, and the Tandem Connection feature is enabled.
	5	DLCTE	**Drop Bus Loss Of Clock Alarm Tandem Connection RDI/ODI Enable:** A common control for both the A and B Drop bus loss of clock alarm (A/BDLOC). A 1 enables a Drop Bus Loss Of Clock alarm for the active bus to generate a Tandem Connection RDI and ODI provided control bit TCnRE is set to 1, and the Tandem Connection feature is enabled.
	4	J2TCE	**J2 Alarm Tandem Connection RDI/ODI Enable:** A common control for both the A and B Drop bus J2 alarms. A 1 enables a J2 Loss Of Lock (A/BnJ2LOL) or J2 Trace Mismatch (A/BnJ2TIM) alarm for the active bus to generate a Tandem Connection RDI and ODI provided control bit TCnRE is set to 1, and the Tandem Connection feature is enabled.
	3	PLSTCE	**Path Label Alarm Tandem Connection RDI/ODI Enable:** A common control for both the A and B Drop bus path signal alarm (A/BnSLER). A 1 enables a path signal label mismatch alarm for the active bus to generate a Tandem Connection RDI and ODI provided control bit TCnRE is set to 1, and the Tandem Connection feature is enabled.
	2	UQTCE	**Unequipped Alarm Tandem Connection RDI/ODI Enable:** A common control for both the A and B Drop bus unequipped alarm (A/BnUNEQ). A 1 enables a unequipped alarm for the active bus to generate a Tandem Connection RDI and ODI provided control bit TCnRE is set to 1, and the Tandem Connection feature is enabled.
	1		**Not used:**
	0	USTCE	**Upstream AIS Alarm Tandem Connection RDI/ODI Enable:** A common control for both the A and B Drop bus upstream AIS alarm (A/BxUAIS). A 1 enables an upstream AIS alarm for the active bus to generate a Tandem Connection RDI and ODI provided control bit TCnRE is set to 1, and the Tandem Connection feature is enabled.

Address	Bit	Symbol	Description
020	7		**Not used:**
	6	VCRDIE	**VC AIS Alarm RDI Enable:** A common control for both the A and B Drop bus signal label AIS alarm (A/BnVCAIS). A 1 enables a VC AIS alarm for the active bus to generate either a single bit RDI state or a Remote Server Defect Indication (three bit RDI) when control bit RnDIEN is set to 1.
	5	DLCRE	**Drop Bus Loss Of Clock RDI Enable:** A common control for both the A and B Drop bus loss of clock alarm (A/BDLOC). A 1 enables a Drop Bus Loss Of Clock alarm for the active bus to generate either a single bit RDI state or a Remote Server Defect Indication (three bit RDI) when control bit RnDIEN is set to 1.
	4	PSRDIE	**Path Label Alarm RDI Enable:** A common control for both the A and B Drop bus path signal alarm (A/BnSLER). A 1 enables a path signal label mismatch alarm for the active bus to generate a Remote Payload Defect Indication (three bit RDI) when control bit RnDIEN is set to 1.
	3		**Not used:**
	2	J2RDIE	**J2 Alarm RDI Enable:** A common control for both the A and B Drop bus J2 alarms. A 1 enables a J2 Loss Of Lock or J2 Trace Mismatch alarm for the active bus to generate either a single bit RDI state or a Remote Connectivity Defect Indication (three bit RDI) when control bit RnDIEN is set to 1.
	1	UQRDIE	**Unequipped Alarm RDI Enable:** A common control for both the A and B Drop bus unequipped alarm (A/BnUNEQ). A 1 enables a unequipped alarm for the active bus to generate either a single bit RDI state or a Remote Connectivity Defect Indication (three bit RDI) when control bit RnDIEN is set to 1.
	0	URDIE	**Upstream AIS Alarm RDI Enable:** A common control for both the A and B Drop bus upstream AIS alarm (A/BxUAIS). A 1 enables an upstream AIS alarm for the active bus to generate either a single bit RDI state or a Remote Server Defect Indication (three bit RDI) when control bit RnDIEN is set to 1.
039	7-1		**Not used:**
	0	DRESET	**A and B Drop Reset:** Writing a 1 to this control bit clears all performance counters to zero (saturating) or the FE/FFFE hex values (8/16 bit non-saturating) and alarms, and initializes the internal FIFOs and state machines for all channels for the A and B drop buses. It does not clear the control bit settings.

Address	Bit	Symbol	Description
03A	7	TJUST	**Transmit Frequency Justification Control:** When set to 0, the frequency justification states S1 equal to data and S2 equal to stuff will not be provided. When set to 1, full justification according to the ITU standards is enabled.
	6	PADO	**A/B Add Bus Parity Generated on Data Only:** Common control bit for both add buses. A 1 causes parity to be calculated over the data byte only. A 0 causes parity to be calculated over the data byte, and the SPE and C1J1V1 signals if they enabled as outputs in the drop bus timing mode. Please refer to the table provided below for DBPE control bit.
	5	ABPE	**A/B Add Bus Even Parity Generated:** This bit works in conjunction with the PADO control bit to determine the parity calculation in the add direction. Drop Bus Timing Mode I ($\overline{ABUST}$ = High, $\overline{ABTE}$ = Low) ABPE PADO Action (for both A and B Add buses) 0 0 Odd parity generated over add data, SPE, and C1J1V1. 0 1 Odd parity generated over add data only. 1 0 Even parity generated over add data, SPE, and C1J1V1. 1 1 Even parity generated over add data only. Drop Bus Timing Mode II ($\overline{ABUST}$ = High, $\overline{ABTE}$ = High) ABPE PADO Action (for both A and B Add buses) 0 X Odd parity generated over add data only. 1 X Even parity generated over add data only. ADD Bus Timing Mode ($\overline{ABUST}$ = Low, $\overline{ABTE}$ = X) ABPE PADO Action (for both A and B Add buses) 0 X Odd parity generated over add data only. 1 X Even parity generated over add data only.
	4	TOBWZ	**Transmit O-Bit Channel With Zeros:** A common control for all channels. A 0 enables the microprocessor-written values for the O-bit channel to be transmitted. A 1 forces the O-bit channel to be transmitted as zero for all channels.
	3		**Not used:**
	2	BAHZE	**B Side Add Bus High Impedance Enable:** A 0 enables normal operation for the B side Add bus. A 1 forces the data output leads (BA(7-0)), and the parity lead (BAPAR) to a high impedance state. The Add Indicator ($\overline{BADD}$) is turned off. In the drop bus timing mode, if the BACLK, BASPE, and BAC1J1V1 signals are enabled as outputs they will be forced to the high impedance state when this bit is set to 1 in addition to the data output leads and parity lead. The Add indicator ($\overline{AADD}$) is turned off.
	1	AAHZE	**A Side Add Bus High Impedance Enable:** A 0 enables normal operation for the A side Add bus. A 1 forces the data output leads (AA(7-0)), and the parity lead (BAPAR) to a high impedance state. The Add Indicator ($\overline{AADD}$) is turned off. In the drop bus timing mode, if the AACLK, AASPE, and AAC1J1V1 signals are enabled as outputs they will be forced to the high impedance state when this bit is set to 1 in addition to the data output leads and parity lead. The Add indicator ($\overline{BADD}$) is turned off.

Address	Bit	Symbol	Description
03A (cont.)	0	ADDI	**Add Indicator Inversion:** A 1 causes the A and B Add bus output indicator signals (AADD and BADD) to be active high instead of active low for all TU/VT added to the A or B buses.
03B	7-3		**Not used:**
	2	TB2DIS	**Transmit Disable BIP2 Tandem Connection Unequipped:** A 1 disables the BIP2 (in bits 1 and 2) from being transmitted in an unequipped tandem connection (N2) byte.
	1	ABOD	**Add Bus Output Delay:** This bit works in conjunction with the ABTE lead when in Drop timing mode. The add bus data, parity, add indicator, and optionally the C1J1V1 and SPE (when lead ABTE is low) are delayed one clock from the Drop bus timing when ABOD is a 0 and two clocks from the Drop bus timing when ABOD is a 1. In Add bus timing mode, the add bus data, parity, and add indicator are delayed 1 clock from the Add bus timing when ABOD is a 0 and are delayed 2 clocks from the Add bus timing when ABOD is a 1.
	0	THRSBY	**Threshold Modulation Disabled:** A 1 disables the threshold modulation capability in each of the four modulation circuits. A 0 enables threshold modulation capability in each of the four modulation circuits.
03C	7-1		**Not used:**
	0	TRESET	**Transmit A and B (Add) Reset:** Writing a 1 to this bit clears all performance counters to zero (saturating) or the FE/FFFE hex values (8/16 bit non-saturating) and alarms, and initializes the internal FIFOs and state machines for all channels for the A and B add buses. It does not clear the control bit settings.

MASK BITS FOR A AND B BUS STATUS ALARMS

Address	Bit	Symbol	Description
005	7	HINT	**Hardware Interrupt Enable:** A 1 enables a hardware interrupt to occur on a bus alarm or polling bit provided the corresponding interrupt mask enable bits (global indication bits MGDA, MGDB, MGAB, MPCDA, MPCDB, and MPCAB) in the interrupt structure is set to a 1. A 0 disables the hardware interrupt lead.
	6		**Not used:**
	5	MGDA	**Mask Bit for Global Indication for A Drop Bus Alarms:** A 1 enables a hardware interrupt for the global indication (GDA) for A drop bus alarms when control bit HINT is set to 1. A 0 disables the hardware interrupt for the global indication bit GDA.
	4	MGDB	**Mask Bit for Global Indication for B Drop Bus Alarms:** A 1 enables a hardware interrupt for the global indication (GDB) for B drop bus alarms when control bit HINT is set to 1. A 0 disables the hardware interrupt for the global indication bit GDB.
	3	MGAB	**Mask Bit for Global Indication for A and B Add Bus Alarms:** A 1 enables a hardware interrupt for the global indication (GAB) for A/B add bus alarms when control bit HINT is set to 1. A 0 disables the hardware interrupt for the global indication bit GAB.
	2	MPCDA	**Mask Bit for Global Indication for A Drop Channel Alarms:** A 1 enables a hardware interrupt for the global indication (PCDA) for A drop polling registers (A drop alarms for all channels) when control bit HINT is set to 1. A 0 disables the hardware interrupt for the global indication bit PCDA.
	1	MPCDB	**Mask Bit for Global Indication for B Drop Channel Alarms:** A 1 enables a hardware interrupt for the global indication (PCDB) for B drop polling registers (B drop alarms for all channels) when control bit HINT is set to 1. A 0 disables the hardware interrupt for the global indication bit PCDB.
	0	MPCAB	**Mask Bit for Global Indication for A and B Add Channel Alarms:** A 1 enables a hardware interrupt for the global indication (PCAB) for A and B add polling registers (A and B add alarms for all channels) when control bit HINT is set to 1. A 0 disables the hardware interrupt for the global indication bit PCAB.

Address	Bit	Symbol	Description
007	7		**Not used:**
	6	MDVCAIS	**Mask Bit VC AIS Alarm A and B Drop All Channels:** A 1 enables a channel polling register bit for the A and B drop sides to set when a VC AIS latched alarm occurs in any channel. A 0 disables a VC AIS latched alarm in any channel from setting the corresponding polling bit.
	5	MDUNEQ	**Mask Bit Unequipped Alarm A and B Drop All Channels:** A 1 enables a channel polling register bit for the A and B drop sides to set when a unequipped latched alarm occurs in any channel. A 0 disables a unequipped latched alarm in any channel from setting the corresponding polling bit.
	4	MDRDIC	**Mask Bit Remote Connectivity Defect Alarm A and B Drop All Channels:** A 1 enables a channel polling register bit for the A and B drop sides to set when a RDI-C latched alarm occurs in any channel. A 0 disables a RDI-C latched alarm in any channel from setting the corresponding polling bit.
	3	MDRDIP	**Mask Bit Remote Payload Defect Alarm A and B Drop All Channels:** A 1 enables a channel polling register bit for the A and B drop sides to set when a RDI-P latched alarm occurs in any channel. A 0 disables a RDI-P latched alarm in any channel from setting the corresponding polling bit.
	2	MDRDIS	**Mask Bit Remote Server Defect Alarm A and B Drop All Channels:** A 1 enables a channel polling register bit for the A and B drop sides to set when a RDI-S or single bit RDI latched alarm occurs in any channel. A 0 disables a RDI-S or single bit RDI latched alarm in any channel from setting the corresponding polling bit.
	1	MDSLER	**Mask Bit Signal Label Alarm A and B Drop All Channels:** A 1 enables a channel polling register bit for the A and B drop sides to set when a signal label latched alarm occurs in any channel. A 0 disables a signal label latched alarm in any channel from setting the corresponding polling bit.
	0	MDRFI	**Mask Bit Remote Failure Indication Alarm A and B Drop All Channels:** A 1 enables a channel polling register bit for the A and B drop sides to set when a remote failure indication latched alarm occurs in any channel. A 0 disables a RFI latched alarm in any channel from setting the corresponding polling bit.

Address	Bit	Symbol	Description
008	7-5		**Not used:**
	4	MDRFFE	**Mask Bit Desync FIFO Error Alarm A and B Drop All Channels:** A 1 enables a channel polling register bit for the A and B drop sides to set when a desync FIFO error latched alarm occurs in any channel. A 0 disables a desync FIFO error latched alarm in any channel from setting the corresponding polling bit.
	3	MDAIS	**Mask Bit AIS Alarm A and B Drop All Channels:** A 1 enables a channel polling register bit for the A and B drop sides to set when a AIS (V1/V2 bytes) latched alarm occurs in any channel. A 0 disables a AIS label latched alarm in any channel from setting the corresponding polling bit.
	2	MDLOP	**Mask Bit Loss Of Pointer Alarm A and B Drop All Channels:** A 1 enables a channel polling register bit for the A and B drop sides to set when a loss of pointer latched alarm occurs in any channel. A 0 disables a loss of pointer latched alarm in any channel from setting the corresponding polling bit.
	1	MDNDF	**Mask Bit NDF Indication A and B Drop All Channels:** A 1 enables a channel polling register bit for the A and B drop sides to set when a New Data Flag latched alarm occurs in any channel. A 0 disables a NDF latched alarm in any channel from setting the corresponding polling bit.
	0	MDSIZE	**Mask Bit Size Alarm A and B Drop All Channels:** A 1 enables a channel polling register bit for the A and B drop sides to set when a VT/TU size latched alarm occurs in any channel. A 0 disables a VT/TU size latched alarm in any channel from setting the corresponding polling bit.

Address	Bit	Symbol	Description
009	7		**Not used:**
	6	MTAIS	**Mask Bit Transmit Line AIS Alarm All Channels:** A 1 enables a channel polling register bit for the A and B add sides to set when a transmit line AIS latched alarm occurs in any channel. A 0 disables a transmit line AIS label latched alarm in any channel from setting the corresponding polling bit.
	5	MTFFE	**Mask Bit Transmit FIFO Alarm All Channels:** A 1 enables a channel polling register bit for the A and B add sides to set when a transmit FIFO latched alarm occurs in any channel. A 0 disables a transmit FIFO latched alarm in any channel from setting the corresponding polling bit.
	4	MOOL	**Mask Bit PRBS Analyzer Out Of lock Alarm:** A 1 enables a channel polling register bit for the PRBS analyzer to set when an out of lock latched alarm occurs in any channel. A 0 disables a out of lock latched alarm in any channel from setting the corresponding polling bit.
	3	MTLOS	**Mask Bit Transmit Loss Of Signal Alarm All Channels:** A 1 enables a channel polling register bit for the A and B add sides to set when a transmit loss of signal latched alarm occurs in any channel. A 0 disables a transmit LOS latched alarm in any channel from setting the corresponding polling bit.
	2	MTLOC	**Mask Bit Transmit Loss Of Clock Alarm All Channels:** A 1 enables a channel polling register bit for the A and B add sides to set when a transmit loss of clock latched alarm occurs in any channel. A 0 disables a transmit LOC latched alarm in any channel from setting the corresponding polling bit.
	1	MDJ2TIM	**Mask Bit J2 Trace Mismatch Alarm A and B Drop All Channels:** A 1 enables a channel polling register bit for the A and B drop sides to set when a J2 trace mismatch latched alarm occurs in any channel. A 0 disables a J2 trace mismatch latched alarm in any channel from setting the corresponding polling bit.
	0	MDJ2LOL	**Mask Bit J2 Loss Of Lock Alarm A and B Drop All Channels:** A 1 enables a channel polling register bit for the A and B drop sides to set when a J2 loss of lock mismatch latched alarm occurs in any channel. A 0 disables a J2 loss of lock latched alarm in any channel from setting the corresponding polling bit.

Address	Bit	Symbol	Description
00A	7	MTCLM	**Mask Bit Tandem Connection Loss Of Multiframe Alignment Alarm A and B Drop All Channels:** A 1 enables a channel polling register bit for the A and B drop sides to set when a TC loss of multiframe latched alarm occurs in any channel. A 0 disables a TC loss of multiframe latched alarm in any channel from setting the corresponding polling bit.
	6	MTCLL	**Mask Bit Tandem Connection Loss Of Lock Alarm A and B Drop All Channels:** A 1 enables a channel polling register bit for the A and B drop sides to set when a TC loss of lock latched alarm occurs in any channel. A 0 disables a TC loss of lock latched alarm in any channel from setting the corresponding polling bit.
	5	MTCTM	**Mask Bit Tandem Connection Trace Mismatch Alarm A and B Drop All Channels:** A 1 enables a channel polling register bit for the A and B drop sides to set when a TC Trace Mismatch latched alarm occurs in any channel. A 0 disables a TC Trace Mismatch latched alarm in any channel from setting the corresponding polling bit.
	4	MTCAIS	**Mask Bit Tandem Connection AIS Alarm A and B Drop All Channels:** A 1 enables a channel polling register bit for the A and B drop sides to set when a TC AIS latched alarm occurs in any channel. A 0 disables a TC AIS latched alarm in any channel from setting the corresponding polling bit.
	3	MTCUQ	**Mask Bit Tandem Connection Unequipped Alarm A and B Drop All Channels:** A 1 enables a channel polling register bit for the A and B drop sides to set when a TC Unequipped latched alarm occurs in any channel. A 0 disables a TC Unequipped latched alarm in any channel from setting the corresponding polling bit.
	2	MTCRDI	**Mask Bit Tandem Connection Remote Defect Indication Alarm A and B Drop All Channels:** A 1 enables a channel polling register bit for the A and B drop sides to set when a TC RDI latched alarm occurs in any channel. A 0 disables a TC RDI latched alarm in any channel from setting the corresponding polling bit.
	1	MTCODI	**Mask Bit Tandem Connection Outgoing Defect Indication Alarm A and B Drop All Channels:** A 1 enables a channel polling register bit for the A and B drop sides to set when a TC ODI latched alarm occurs in any channel. A 0 disables a TC ODI latched alarm in any channel from setting the corresponding polling bit.
	0		**Not used:**
03D	7-2		**Not used:**
	1	MBBLOC	**Mask Bit B Side Add Bus Loss Of Clock:** A 1 enables the global indication GAB to set when a add bus loss of clock alarm occurs. A 0 disables the global indication bit GAB from setting.
	0	MABLOC	**Mask Bit A Side Add Bus Loss Of Clock:** A 1 enables the global indication GAB to set when a add bus loss of clock alarm occurs. A 0 disables the global indication bit GAB from setting.
03F	7-0	Mask Bits Add Polling Register Channel 8-1	**Mask Bits Polling Registers Channels 8-1 Add Alarms:** A 1 in one or more bits enables an A/B side add alarm in the corresponding channel to set the global indication (PCAB) bit. A 0 disables the channel corresponding to a polling bit from setting the global indication (PCAB) bit. Bit 7 is the mask bit for channel 8 add side alarms.

Address	Bit	Symbol	Description
040	7-0	Mask Bits Add Polling Register Channel 16-9	**Mask Bits Polling Registers Channels 16-9 Add Alarms:** A 1 in one or more bits enables an A/B side add alarm in the corresponding channel to set the global indication (PCAB) bit. A 0 disables the channel corresponding to a polling bit from setting the global indication (PCAB) bit. Bit 7 is the mask bit for channel 16 add side alarms.
041	7-0	Mask Bits Add Polling Register Channel 24-17	**Mask Bits Polling Registers Channels 24-17 Add Alarms:** A 1 in one or more bits enables an A/B side add alarm in the corresponding channel to set the global indication (PCAB) bit. A 0 disables the channel corresponding to a polling bit from setting the global indication (PCAB) bit. Bit 7 is the mask bit for channel 24 add side alarms.
042	7-4		**Not used:**
	3-0	Mask Bits Add Polling Register Channel 28-25	**Mask Bits Polling Registers Channels 28-25 Add Alarms:** A 1 in one or more bits enables an A/B side add alarm in the corresponding channel to set the global indication (PCAB) bit. A 0 disables the channel corresponding to a polling bit from setting the global indication (PCAB) bit. Bit 3 is the mask bit for channel 28 add side alarms.

A AND B DROP AND ADD BUS STATUS ALARM REGISTERS - DESCRIPTIONS)

Address	Bit	Symbol	Description
050	7-6		**Not used:**
	5	GDA	**Global Indication for A Drop Bus Alarms:** This bit position indicates when an A drop bus alarm is detected. This bit sets when any A drop bus latched alarm occurs and the mask bit associated with the alarm is set to 1. An interrupt occurs when the corresponding mask bit MGDA (Bit 5, 005H) is set to 1, and control bit HINT (Bit 7, 005H) is set to 1. This bit clears when the latched alarms for the A drop bus are cleared, or the mask bit associated with the alarm in the interrupt hierarchy is set to 0.
	4	GDB	**Global Indication for B Drop Bus Alarms:** This bit position indicates when a B drop bus alarm is detected. This bit sets when any B drop bus latched alarm occurs and the mask bit associated with the alarm is set to 1. An interrupt occurs when the corresponding mask bit MGDB (Bit 4, 005H) is set to 1, and control bit HINT (Bit 7, 005H) is set to 1. This bit clears when the latched alarms for the B drop bus are cleared, or the mask bit associated with the alarm in the interrupt hierarchy is set to 0.
	3	GAB	**Global Indication for A and B Add Bus Alarms:** This bit position indicates when an A/B add bus alarm is detected. This bit sets when any latched alarm for the A/B add bus occurs and the mask bit associated with the alarm is set to 1. An interrupt occurs when the corresponding mask bit MGAB (Bit 3, 005H) is set to 1, and control bit HINT (Bit 7, 005H) is set to 1. This bit cleared when the latched alarms for the A/B add bus are clears, or the mask bit associated with the alarm in the interrupt hierarchy is set to 0.

Address	Bit	Symbol	Description
050 (cont.)	2	PCDA	**Global Indication for A Drop Channel Alarms:** This bit position indicates when any of the channels has detected an A side drop alarm. This bit sets when any A drop bus latched alarm occurs and the 3 mask bits associated with the alarm are set to 1. An interrupt occurs when the corresponding mask bit MPCDA (Bit 2, 005H) is set to 1, and control bit HINT (Bit 7, 005H) is set to 1. This bit clears when all of the latched alarms for channels 1 through 28 for the A side drop channels are cleared, or one or more latched alarms are asserted, but one or more of the 3 enabling mask bits is set to 0.
	1	PCDB	**Global Indication for B Drop Bus Channel Alarms:** This bit position indicates when any of the channels has detected an B side drop alarm. This bit sets when any B drop bus latched alarm occurs and the 3 mask bits associated with the alarm are set to 1. An interrupt occurs when the corresponding mask bit MPCDB (Bit 1, 005H) is set to 1, and control bit HINT (Bit 7, 005H) is set to 1. This bit clears when all of the latched alarms for channels 1 through 28 for the B side drop channels are cleared, or one or more latched alarms are asserted, but one or more of the 3 enabling mask bits is set to 0.
	0	PCAB	**Global Indication for A and B Add Bus Channel Alarms:** This bit position indicates when any of the channels has detected an A/B side add alarm. This bit sets when any latched alarm for the A/B add bus occurs and the 3 mask bits associated with the alarm are set to 1. An interrupt occurs when the corresponding mask bit MPCAB (Bit 0, 005H) is set to 1, and control bit HINT (Bit 7, 005H) is set to 1. This bit cleared when all of the latched alarms for channels 1 through 28 for the A/B side add channels are clears, or one or more latched alarms are asserted, but one or more of the 3 enabling mask bits is set to 0.
051	7-2		**Not used:**
	1	BBLOC	**B Add Bus Loss Of Clock Alarm Unlatched Alarm Indication:** A 1 indicates that the B side Add bus has detected a loss of clock, when add bus timing is selected. A loss of clock alarm forces the add bus data and parity bit to a high impedance state, and sets the add indicator off for the duration of the alarm. An alarm occurs when the input add clock is stuck high or low for 56 clock cycles of DSCLK. Recovery to 0 occurs on the first clock transition.
	0	ABLOC	**A Add Bus Loss Of Clock Alarm Unlatched Alarm Indication:** A 1 indicates that the A side Add bus has detected a loss of clock, when add bus timing is selected. A loss of clock alarm forces the add bus data and parity bit to a high impedance state, and sets the add indicator off for the duration of the alarm. An alarm occurs when the input add clock is stuck high or low for 56 clock cycles of DSCLK. Recovery to 0 occurs on the first clock transition.

Address	Bit	Symbol	Description
052	7-2		**Not used:**
	1	LBBLOC	**B Add Bus Loss Of Clock Alarm Latched Alarm Indication:** This bit position latches when the B side Add bus has detected a loss of clock when add bus timing is selected. This bit is set on either a positive transition, negative transition or positive and negative transition. This bit is cleared in a read cycle.
	0	LABLOC	**A Add Bus Loss Of Clock Alarm Latched Alarm Indication:** This bit position latches when the A side Add bus has detected a loss of clock when add bus timing is selected. This bit is set on either a positive transition, negative transition or positive and negative transition. This bit is cleared in a read cycle.
053	7-2		**Not used:**
	1	PBBLOC	**B Add Bus Loss Of Clock One Second Alarm Indication:** This bit position is set when the B side add bus loss of clock alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	0	PABLOC	**A Add Bus Loss Of Clock One Second Alarm Indication:** This bit position is set when the A side add bus loss of clock alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
054	7-2		**Not used:**
	1	FBBLOC	**B Add Bus Loss Of Clock Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the B side add bus loss of clock alarm indication is active, but did not become active in the previous one second interval.
	0	FABLOC	**A Add Bus Loss Of Clock Persistent One Second Latched Alarm Indication:** This bit position is set to 1 for the one-second interval, when the A side add bus loss of clock alarm indication is active, but did not become active in the previous one second interval.
055	7-0	Polling Register Add Alarms Channels 8-1	**Polling Registers, Channels 8-1 Alarms:** Bit 7 corresponds to the polling bit for channel 8. A polling bit is set to 1 when one or more A/B add side latched alarms occurs in a channel and the corresponding mask bit is set to 1. This bit is cleared when the add side latched alarms corresponding to the channel that is set to 1 are read, or the mask bit associated with the alarm in the interrupt hierarchy is set to 0.
056	7-0	Polling Register Add Alarms Channels 16-9	**Polling Registers, Channels 16-9 Alarms:** Bit 7 corresponds to the polling bit for channel 16. A polling bit is set to 1 when one or more A/B add side latched alarms occurs in a channel and the corresponding mask bit is set to 1. This bit is cleared when the add side latched alarms corresponding to the channel that is set to 1 are read, or the mask bit associated with the alarm in the interrupt hierarchy is set to 0.

Address	Bit	Symbol	Description
057	7-0	Polling Register Add Alarms Channels 24-17	**Polling Registers, Channels 24-17 Alarms:** Bit 7 corresponds to the polling bit for channel 24. A polling bit is set to 1 when one or more A/B add side latched alarms occurs in a channel and the corresponding mask bit is set to 1. This bit is cleared when the add side latched alarms corresponding to the channel that is set to 1 are read, or the mask bit associated with the alarm in the interrupt hierarchy is set to 0.
058	7-4		**Not used:**
	3-0	Polling Register Add Alarms Channels 28-25	**Polling Registers, Channels 28-25 Alarms:** Bit 3 corresponds to the polling bit for channel 28. A polling bit is set to 1 when one or more A/B add side latched alarms occurs in a channel and the corresponding mask bit is set to 1. This bit is cleared when the add side latched alarms corresponding to the channel that is set to 1 are read, or the mask bit associated with the alarm in the interrupt hierarchy is set to 0.
059	7-1		**Not used:**
	0	RESETD	**Reset Sequence Completed:** Indication that the hardware reset (RESET lead) or software reset (control bit RESETH) is completed. It takes approximately 4 microseconds for this bit to set to a 1 after the hardware reset or software reset control bit has been invoked. Microprocessor access of the TEMx28 is not valid until this bit is set to 1. This bit goes to zero immediately after the hardware or software reset has been invoked.

MASK BITS FOR A DROP BUS STATUS ALARMS

Address	Bit	Symbol	Description
043	7-5		**Not Used:**
	4	MA3UAIS	**Mask Bit for Global Indication for Upstresm AIS indication for A Drop Bus STS-3 STS-1 No.3/STM-1 AU-3 C:** A 1 enables the global indication (GDA) to be set for an upstream AIS indication that has been detected in the H1/H2 bytes or in the E1 byte for STS-3 STS-1 No.3/STM-1 AU-3 C format for the A side drop bus. A 0 disables the global indication bit GDA for this alarm.
	3	MA2UAIS	**Mask Bit for Global Indication for Upstream AIS indication for A Drop Bus STS-3 STS-1 No.2/STM-1 AU-3 B:** A 1 enables the global indication (GDA) to be set for an upstream AIS indication that has been detected in the H1/H2 bytes or in the E1 byte for STS-3 STS-1 No.2/STM-1 AU-3 B format for the A side drop bus. A 0 disables the global indication bit GDA for this alarm.
	2	MA1UAIS	**Mask Bit for Global Indication for Upstream AIS indication for A Drop Bus STS-3 STS-1 No.1/STM-1 AU-3 A and STM-1 VC-4:** A 1 enables the global indication (GDA) to be set for an upstream AIS indication that has been detected in the H1/H2 bytes or in the E1 byte for STS-3 STS-1 No.2/STM-1 AU-3 A or for the STN-1 VC-4 format for the A side drop bus. A 0 disables the global indication bit GDA for this alarm.
	1	MADPAR	**Mask Bit for Global Indication for A Drop Parity Alarm:** A 1 enables the global indication (GDA) to be set for a parity alarm detected for the A side drop bus. A 0 disables the global indication bit GDA for this alarm.
	0	MADLOC	**Mask Bit for Global Indication for A Drop Loss of Clock Alarm:** A 1 enables the global indication (GDA) to be set for a loss of clock alarm detected for the A side drop bus. A 0 disables the global indication bit GDA for this alarm.

Address	Bit	Symbol	Description
044	7-6		**Not Used.**
	5	MA3OOM	**Mask Bit for Global Indication for H4 Out Of Multiframe Indication for A Drop Bus STS-3 STS-1 No.3/STM-1 AU-3 C:** A 1 enables the global indication (GDA) to be set for an H4 Out Of Multiframe indication for STS-3 STS-1 No.3/STM-1 AU-3 C format for the A side drop bus. A 0 disables the global indication bit GDA for this alarm.
	4	MA2OOM	**Mask Bit for Global Indication for H4 Out Of Multiframe Indication for A Drop Bus STS-3 STS-1 No.2/STM-1 AU-3 B:** A 1 enables the global indication (GDA) to be set for an H4 Out Of Multiframe indication for STS-3 STS-1 No.2/STM-1 AU-3 B format for the A side drop bus. A 0 disables the global indication bit GDA for this alarm.
	3	MA1OOM	**Mask Bit for Global Indication for H4 Out Of Multiframe Indication for A Drop Bus STS-3 STS-1 No.1/STM-1 AU-3 A and STM-1 VC-4:** A 1 enables the global indication (GDA) to be set for an H4 Out Of Multiframe indication for STS-3 STS-1 No.1/STM-1 AU-3 A and STM-1 VC-4 format for the A side drop bus. A 0 disables the global indication bit GDA for this alarm.
	2	MA3LOM	**Mask Bit for Global Indication for H4 Loss Of Multiframe Indication for A Drop Bus STS-3 STS-1 No.3/STM-1 AU-3 C:** A 1 enables the global indication (GDA) to be set for an H4 Loss Of Multiframe indication for STS-3 STS-1 No.3/STM-1 AU-3 C format for the A side drop bus. A 0 disables the global indication bit GDA for this alarm.
	1	MA2LOM	**Mask Bit for Global Indication for H4 Loss Of Multiframe Indication for A Drop Bus STS-3 STS-1 No.2/STM-1 AU-3 B:** A 1 enables the global indication (GDA) to be set for an H4 Loss Of Multiframe indication for STS-3 STS-1 No.2/STM-1 AU-3 B format for the A side drop bus. A 0 disables the global indication bit GDA for this alarm.
	0	MA1LOM	**Mask Bit for Global Indication for H4 Loss Of Multiframe Indication for A Drop Bus STS-3 STS-1 No.1/STM-1 AU-3 A and STM-1 VC-4:** A 1 enables the global indication (GDA) to be set for an H4 Loss Of Multiframe indication for STS-3 STS-1 No.1/STM-1 AU-3 A and STM-1 VC-4 format for the A side drop bus. A 0 disables the global indication bit GDA for this alarm.
045	7-0	Mask Bits A Drop Polling Register Channel 8-1	**Mask Bits Polling Registers Channels 8-1 A Drop Alarms:** A 1 in one or more bits enables an A drop side alarm in the corresponding channel to set the global indication (PCDA) bit. A 0 disables the channel corresponding to a polling bit from setting the global indication (PCDA) bit. Bit 7 is the mask bit for channel 8 A drop side alarms.
046	7-0	Mask Bits A Drop Polling Register Channel 16-9	**Mask Bits Polling Registers Channels 16-9 A Drop Alarms:** A 1 in one or more bits enables an A drop side alarm in the corresponding channel to set the global indication (PCDA) bit. A 0 disables the channel corresponding to a polling bit from setting the global indication (PCDA) bit. Bit 7 is the mask bit for channel 16 A drop side alarms.

Address	Bit	Symbol	Description
047	7-0	Mask Bits A Drop Polling Register Channel 24-17	**Mask Bits Polling Registers Channels 24-17 A Drop Alarms:** A 1 in one or more bits enables an A drop side alarm in the corresponding channel to set the global indication (PCDA) bit. A 0 disables the channel corresponding to a polling bit from setting the global indication (PCDA) bit. Bit 7 is the mask bit for channel 24 A drop side alarms.
048	7-4		**Not used:**
	3-0	Mask Bits A Drop Polling Register Channel 28-25	**Mask Bits Polling Registers Channels 28-25 A Drop Alarms:** A 1 in one or more bits enables an A drop side alarm in the corresponding channel to set the global indication (PCDA) bit. A 0 disables the channel corresponding to a polling bit from setting the global indication (PCDA) bit. Bit 3 is the mask bit for channel 28 A drop side alarms.

A SIDE DROP BUS - STATUS REGISTER DESCRIPTIONS

Address	Bit	Symbol	Description
060	7-5		**Not used:**
	4	A3UAIS	**A Side Drop Bus Upstream AIS (Unlatched) Alarm Indication - STS-3 STS-1 No. 3/AU-3 C:** A 1 indicates that AIS has been detected on the A side drop bus in the H1/H2 bytes or in the E13 byte for the STS-3 STS-1 No.3/STM-1 AU-3 C format. Control bits SE1AIS and HEAISE (bits 1 and 0, 01DH) determine whether the H1/H2 bytes or the E13 byte is monitored for AIS detection. This indication is disabled for the STM-1 VC-4 format.
	3	A2UAIS	**A Side Drop Bus Upstream AIS (Unlatched) Alarm Indication - STS-3 STS-1 No. 2/AU-3 B:** A 1 indicates that AIS has been detected on the A side drop bus in the H1/H2 bytes or in the E12 byte for the STS-3 STS-1 No.2/STM-1 AU-3 B format. Control bits SE1AIS and HEAISE (bits 1 and 0, 01DH) determine whether the H1/H2 bytes or the E12 byte is monitored for AIS detection. This indication is disabled for the STM-1 VC-4 format.
	2	A1UAIS	**A Side Drop Bus Upstream AIS (Unlatched) Alarm Indication - STS-3 STS-1 No. 1/AU-3 A, STM-1 VC4:** A 1 indicates that AIS has been detected on the A side drop bus in the H1/H2 bytes or in the E11 byte for the STS-3 STS-1 No.1/STM-1 AU-3 A format or for the STM-1 VC-4 format. Control bits SE1AIS and HEAISE (bits 1 and 0, 01DH) determine whether the H1/H2 bytes or the E11 byte is monitored for AIS detection.
	1	ADPAR	**A Side Drop Bus Parity (Unlatched) Alarm Indication:** A 1 indicates that an even or odd parity error has been detected in the A side Drop bus signals. Other than an alarm indication, no action is taken. Parity is monitored for each drop bus clock cycle.
	0	ADLOC	**A Side Drop Bus Loss Of Clock Unlatched Alarm Indication:** A 1 indicates that the A side Drop bus has detected a loss of clock. An alarm occurs when the input drop clock is stuck high or low for 56 clock cycles (DSCLK clock). Recovery occurs on the first clock transition.

Address	Bit	Symbol	Description
061	7-6		**Not used:**
	5	A3HOOM	**A Side Drop Bus H4 Byte Out Of Multiframe Alignment (Unlatched) Alarm - STS-3 STS-1 No. 3/AU-3 C:** Enabled when control bit DV1SEL is a 0. An Out Of Multiframe alarm for STS-3 STS-1 No. 3/AU-3 C is declared once an error is detected in the bit 7 and 8 sequence in the H4 byte. Recovery occurs when an error-free H4 sequence (00, 01, 10, 11) is found in four consecutive frames.
	4	A2HOOM	**A Side Drop Bus H4 Byte Out Of Multiframe Alignment (Unlatched) Alarm - STS-3 STS-1 No. 2/AU-3 B:** Enabled when control bit DV1SEL is a 0. An Out Of Multiframe alarm for STS-3 STS-1 No. 2/AU-3 B is declared once an error is detected in the bit 7 and 8 sequence in the H4 byte. Recovery occurs when an error-free H4 sequence (00, 01, 10, 11) is found in four consecutive frames.
	3	A1HOOM	**A Side Drop Bus H4 Byte Out Of Multiframe Alignment (Unlatched) Alarm - STS-3 STS-1/AU-3 A, STM-1 VC-4:** Enabled when control bit DV1SEL is a 0. An Out Of Multiframe alarm for STS-3 STS-1 No.1/AU-3 or the STM-1 VC-4 is declared once an error is detected in the bit 7 and 8 sequence in the H4 byte. Recovery occurs when an error-free H4 sequence (00, 01, 10, 11) is found in four consecutive frames.
	2	A3HLOM	**A Side Drop Bus H4 Byte Loss of Multiframe Alignment (Unlatched) Alarm - STS-3 STS-1 No. 3/AU-3 C:** Once in the Out Of Multiframe state, if recovery does not occur within 1 ms, a Loss Of Multiframe alarm is declared. Recovery will occur when the multiframe is recovered. The Loss of Multiframe alarm forces a VT/TU Loss of Pointer alarm (AnLOP) for all channels which have a VT/TU selected for STS-3 STS-1 No. 3/AU-3 C.
	1	A2HLOM	**A Side Drop Bus H4 Byte Loss of Multiframe Alignment (Unlatched) Alarm - STS-3 STS-1No. 2/AU-3 B:** Once in the Out Of Multiframe state, if recovery does not occur within 1 ms, a Loss Of Multiframe alarm is declared. Recovery will occur when the multiframe is recovered. The Loss of Multiframe alarm forces a VT/TU Loss of Pointer alarm (AnLOP) for all channels which have a VT/TU selected for STS-3 STS-1No. 2/AU-3 B.
	0	A1HLOM	**A Side Drop Bus H4 Byte Loss of Multiframe Alignment (Unlatched) Alarm - STS-3 STS-1 No. 1/AU-3 A, STM-1 VC-4:** Once in the Out Of Multiframe state, if recovery does not occur within 1 ms, a Loss Of Multi-frame alarm is declared. Recovery will occur when the multiframe is recovered. The Loss of Multiframe alarm forces a VT/TU Loss of Pointer alarm (AnLOP) for all channels which have a VT/TU selected for STS-3 STS-1 No. 1/AU-3 A, STM-1 VC-4.

Address	Bit	Symbol	Description
062	7-5		**Not used:**
	4	LA3UAIS	**A Side Drop Bus Upstream AIS Latched Alarm Indication - STS-3 STS-1 No. 3/AU-3 C:** This bit position latches for the A side received upstream AIS alarm Indication for the STS-3 STS-1 No. 3/AU-3 C format. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	3	LA2UAIS	**A Side Drop Bus Upstream AIS Latched Alarm Indication - STS-3 STS-1 No. 2/AU-3 B:** This bit position latches for the A side received upstream AIS alarm Indication for the STS-3 STS-1 No. 2/AU-3 B format. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	2	LA1UAIS	**A Side Drop Bus Upstream AIS Latched Alarm Indication - STS-3 STS-1 No. 1/AU-3 A/VC4:** This bit position latches for the A side received upstream AIS alarm Indication for the STS-3 STS-1 No. 1/AU-3 A or STM-1 VC-4 format. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	1	LADPAR	**A Side Drop Bus Parity Latched Alarm Indication:** This bit position latches for the A side parity error. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	0	LADLOC	**A Side Drop Bus Loss Of Clock Latched Alarm Indication:** This bit position latches for the A side loss of clock alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.

Address	Bit	Symbol	Description
063	7-6		**Not used:**
	5	LA3HOOM	**A Side Drop Bus H4 Byte Out Of Multiframe Alignment Latched Alarm Indication - STS-3 STS-1 No. 3/AU-3 C:** This bit position latches for the A side STS-3 STS-1 No. 3/AU-3 C H4 byte Out of Multiframe alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	4	LA2HOOM	**A Side Drop Bus H4 Byte Out Of Multiframe Alignment Latched Alarm Indication - STS-3 STS-1 No. 2/AU-3 B:** This bit position latches for the A side STS-3 STS-1 No.2/AU-3 B H4 byte Out of Multiframe alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	3	LA1HOOM	**A Side Drop Bus H4 Byte Out Of Multiframe Alignment Latched Alarm Indication - STS-3 STS-1 No. 1/AU-3 A, STM-1 VC-4:** This bit position latches for the A side STS-3 STS-1 No.1/AU-3 A, or STM-1 VC-4 H4 byte Out of Multiframe alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	2	LA3HLOM	**A Side Drop Bus H4 Byte Loss Of Multiframe Alignment Latched Alarm Indication - STS-3 STS-1 No. 2/AU-3 C:** This bit position latches for the A side STS-3 STS-1 No. 3/AU-3 C H4 byte Loss of Multiframe alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	1	LA2HLOM	**A Side Drop Bus H4 Byte Loss Of Multiframe Alignment Latched Alarm Indication - STS-3 STS-1 No. 2/AU-3 B:** This bit position latches for the A side STS-3 STS-1 No. 2/AU-3 B H4 byte Loss of Multiframe alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	0	LA1HLOM	**A Side Drop Bus H4 Byte Loss Of Multiframe Alignment Latched Alarm Indication - STS-3 STS-1 No. 1/AU-3 A, STM-1 VC-4:** This bit position latches for the A side STS-3 STS-1 No. 1/AU-3 A, or STM-1 VC-4 H4 byte Loss of Multiframe alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.

Address	Bit	Symbol	Description
064	7-5		**Not used:**
	4	PA3UAIS	**A Side Drop Bus Upstream AIS One Second Alarm Indication - STS-3 STS-1 No. 3/AU-3 C:** This bit position is set when the A side received upstream AIS alarm Indication - STS-3 STS-1 No. 3/AU-3 C has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	3	PA2UAIS	**A Side Drop Bus Upstream AIS One Second Alarm Indication - STS-3 STS-1 No. 2/AU-3 B:** This bit position is set when the A side received upstream AIS alarm Indication - STS-3 STS-1 No. 2/AU-3 B has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	2	PA1UAIS	**A Side Drop Bus Upstream AIS One Second Alarm Indication - STS-1 No. 1/AU-3 A and STM-1 VC-4:** This bit position is set when the A side received upstream AIS alarm Indication - STS-3 STS-1 No. 1/AU-3 A or STM-1 VC-4 has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	1	PADPAR	**A Side Drop Bus Parity One Second Alarm Indication:** This bit position is set when the A side parity error alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	0	PADLOC	**A Side Drop Bus Loss Of Clock One Second Alarm Indication:** This bit position is set when the A side loss of clock alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.

Address	Bit	Symbol	Description
065	7-6		**Not used:**
	5	PA3HOOM	**A Side Drop Bus H4 Byte Out Of Multiframe Alignment One Second Alarm Indication - STS-3 STS-1 No. 3/AU-3 C:** This bit position is set when the A side STS-3 STS-1 No. 3/AU-3 C H4 byte Out Of Multiframe Alignment alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	4	PA2HOOM	**A Side Drop Bus H4 Byte Out Of Multiframe Alignment One Second Alarm Indication - STS-3 STS-1 No. 2/AU-3 B:** This bit position is set when the A side STS-3 STS-1 No. 2/AU-3 B H4 byte Out Of Multiframe Alignment alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	3	PA1HOOM	**A Side Drop Bus H4 Byte Out Of Multiframe Alignment One Second Alarm Indication - STS-3 STS-1 No. 1/AU-3 A, STM-1 VC-4:** This bit position is set when the A side STS-3 STS-1 No. 1/AU-3 A or the STM-1 VC-4 H4 byte Out Of Multiframe Alignment alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	2	PA3HLOM	**A Side Drop Bus H4 Byte Loss Of Multiframe Alignment One Second Alarm Indication - STS-3 STS-1 No. 3/AU-3 C:** This bit position is set when the A side STS-3 STS-1 No. 3/AU-3 C H4 byte Loss Of Multiframe Alignment alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	1	PA2HLOM	**A Side Drop Bus H4 Byte Loss Of Multiframe Alignment One Second Alarm Indication - STS-1 No. 2/AU-3 B:** This bit position is set when the A side STS-3 /STS-1 No. 2/AU-3 B H4 byte Loss Of Multiframe Alignment alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	0	PA1HLOM	**A Side Drop Bus H4 Byte Loss Of Multiframe Alignment One Second Alarm Indication - STS-3 STS-1 No. 1/AU-3 A, STM-1 VC-4:** This bit position is set when the A side STS-3 STS-1 No.1/AU-3 A or the STM-1 VC-4 H4 byte Loss Of Multiframe Alignment alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.

Address	Bit	Symbol	Description
066	7-5		**Not used:**
	4	FA3UAIS	**A Side Received Upstream AIS Persistent One Second Alarm Indication - STS-3 STS-1 No. 3/AU-3 C:** This bit position is set to 1 for the one-second interval, when the A side received upstream AIS alarm Indication - STS-3 STS-1 No. 3/AU-3 C is active, but did not become active in the previous one second interval.
	3	FA2UAIS	**A Side Received Upstream AIS Persistent One Second Alarm Indication - STS-3 STS-1 No. 2/AU-3 B:** This bit position is set to 1 for the one-second interval, when the A side received upstream AIS alarm Indication - STS-3 STS-1 No. 2/AU-3 B is active, but did not become active in the previous one second interval.
	2	FA1UAIS	**A Side Received Upstream AIS Persistent One Second Alarm Indication - STS-3 STS-1 No. 1/AU-3 A and STM-1 VC-4:** This bit position is set to 1 for the one-second interval, when the A side received upstream AIS alarm Indication - STS-3 STS-1 No. 1/AU-3 A or SM-1 VC-4 is active, but did not become active in the previous one second interval.
	1	FADPAR	**A Side Drop Bus Parity Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the A side parity error alarm indication is active, but did not become active in the previous one second interval.
	0	FADLOC	**A Side Drop Bus Loss Of Clock Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the A side loss of clock alarm indication is active, but did not become active in the previous one second interval.

Address	Bit	Symbol	Description
067	7-6		**Not used:**
	5	FA3HOOM	**A Side Drop Bus H4 Byte Out Of Multiframe Alignment Persistent One Second Alarm Indication - STS-3 STS-1 No. 3/AU-3 C:** This bit position is set to 1 for the one-second interval, when the A side STS-3 STS-1 No. 3/AU-3 C H4 byte Out Of Multiframe alarm indication is active, but did not become active in the previous one second interval.
	4	FA2HOOM	**A Side Drop Bus H4 Byte Out Of Multiframe Alignment Persistent One Second Alarm Indication - STS-3 STS-1 No. 2/3AU-3 B:** This bit position is set to 1 for the one-second interval, when the A side STS-3 STS-1 No. 2/AU-3 B H4 byte Out Of Multiframe alarm indication is active, but did not become active in the previous one second interval.
	3	FA1HOOM	**A Side Drop Bus H4 Byte Out Of Multiframe Alignment Persistent One Second Alarm Indication - STS-3 STS-1 No. 1/AU-3 A, STM-1 VC-4:** This bit position is set to 1 for the one-second interval, when the A side STS-3 STS-1 No. 1/AU-3 A, or the STM-1 VC-4 H4 byte Out Of Multiframe alarm indication is active, but did not become active in the previous one second interval.
	2	FA3HLOM	**A Side Drop Bus H4 Byte Loss Of Multiframe Alignment Persistent One Second Alarm Indication - STS-3 STS-1 No. 3/AU-3 C:** This bit position is set to 1 for the one-second interval, when the A side STS-3 STS-1 No. 3/AU-3 C H4 byte Loss Of Multiframe alarm indication is active, but did not become active in the previous one second interval.
	1	FA2HLOM	**A Side Drop Bus H4 Byte Loss Of Multiframe Alignment Persistent One Second Alarm Indication - STS-3 STS-1 No. 2/AU-3 B:** This bit position is set to 1 for the one-second interval, when the A side STS-3 STS-1 No. 2/AU-3 B H4 byte Loss Of Multiframe alarm indication is active, but did not become active in the previous one second interval.
	0	FA1HLOM	**A Side Drop Bus H4 Byte Loss Of Multiframe Alignment Persistent One Second Alarm Indication - STS-3 STS-1 No. 1/AU-3 A, STM-1 VC-4:** This bit position is set to 1 for the one-second interval, when the A side STS-3 STS-1 No. 1/AU-3 A, or the STM-1 VC-4 H4 byte Loss Of Multiframe alarm indication is active, but did not become active in the previous one second interval.
068	7-0	A Side Drop Bus H1 Byte	**A Side Drop Bus H1 Pointer Byte for STS-3 STS-1 No. 1/AU-3 A or STM-1 VC-4:** The value in this location is dropped H1 Pointer byte in the A Drop Bus STS-3 STS-1 No. 1/AU-3 A or VC-4 format. This register location is updated every 125 microseconds. Bits 7-0 of the register correspond to bits 1-8 of the H1 byte.
069	7-0	A Side Drop Bus H1 Byte	**A Side Drop Bus H1 Pointer Byte for STS-3 STS-1 No. 2/AU-3 B:** The value in this location is dropped H1 Pointer byte in the A Drop Bus STS-3 STS-1 No. 2/AU-3 B format. This register location is updated every 125 microseconds. Bits 7-0 of the register correspond to bits 1-8 of the H1 byte.

Address	Bit	Symbol	Description
06A	7-0	A Side Drop Bus H1 Byte	**A Side Drop Bus H1 Pointer Byte for STS-3 STS-1 No. 3/AU-3 C:** The value in this location is dropped H1 Pointer byte in the A Drop Bus STS-3 STS-1 No. 3/AU-3 C format. This register location is updated every 125 microseconds. Bits 7-0 of the register correspond to bits 1-8 of the H1 byte.
06B	7-0	A Side Drop Bus H2 Byte	**A Side Drop Bus H2 Pointer Byte for STS-3 STS-1 No. 1/AU-3 A or STM-1 VC-4:** The value in this location is dropped H2 Pointer byte in the A Drop Bus STS-3 STS-1 No. 1/AU-3 A or VC-4 format. This register location is updated every 125 microseconds. Bits 7-0 of the register correspond to bits 1-8 of the H2 byte.
06C	7-0	A Side Drop Bus H2 Byte	**A Side Drop Bus H2 Pointer Byte for STS-3 STS-1 No. 2/AU-3 B:** The value in this location is dropped H2 Pointer byte in the A Drop Bus STS-3 STS-1 No. 2/AU-3 B format. This register location is updated every 125 microseconds. Bits 7-0 of the register correspond to bits 1-8 of the H2 byte.
06D	7-0	A Side Drop Bus H2 Byte	**A Side Drop Bus H2 Pointer Byte for STS-3 STS-1 No. 3/AU-3 C:** The value in this location is dropped H2 Pointer byte in the A Drop Bus STS-3 STS-1 No. 3/AU-3 C format. This register location is updated every 125 microseconds. Bits 7-0 of the register correspond to bits 1-8 of the H2 byte.
06E	7-0	A Side Drop Bus H4 Byte	**A Side Drop Bus H4 Path Overhead Byte for STS-3 STS-1 No. 1/AU-3 A or STM-1 VC-4:** The value in this location is dropped H4 path overhead byte in the A Drop Bus STS-3 STS-1 No. 1/AU-3 A or VC-4 format. This register location is updated every 125 microseconds. Bits 7-0 of the register correspond to bits 1-8 of the H4 byte.
06F	7-0	A Side Drop Bus H4 Byte	**A Side Drop Bus H4 Path Overhead Byte for STS-3 STS-1 No. 2/AU-3 B:** The value in this location is dropped H4 path overhead byte in the A Drop Bus STS-3 STS-1 No. 2/AU-3 B format. This register location is updated every 125 microseconds. Bits 7-0 of the register correspond to bits 1-8 of the H4 byte.
070	7-0	A Side Drop Bus H4 Byte	**A Side Drop Bus H4 Path Overhead Byte for STS-3 STS-1 No. 3/AU-3 C:** The value in this location is dropped H4 path overhead byte in the A Drop Bus STS-3 STS-1 No. 3/AU-3 C format. This register location is updated every 125 microseconds. Bits 7-0 of the register correspond to bits 1-8 of the H4 byte.
071	7-0	A Side Drop Bus E1 Byte	**A Side Drop Bus E1 Overhead Byte for STS-3 STS-1 No. 1/AU-3 A or STM-1 VC-4:** The value in this location is dropped E1 overhead byte in the A Drop Bus STS-3 STS-1 No. 1/AU-3 A or VC-4 format. This register location is updated every 125 microseconds. Bits 7-0 of the register correspond to bits 1-8 of the E1 byte.
072	7-0	A Side Drop Bus E1 Byte	**A Side Drop Bus E12 Overhead Byte for STS-3 STS-1 No. 2/AU-3 B:** The value in this location is dropped E1 overhead byte in the A Drop Bus STS-3 STS-1 No. 2/AU-3 B format. This register location is updated every 125 microseconds. Bits 7-0 of the register correspond to bits 1-8 of the E1 byte.

Address	Bit	Symbol	Description
073	7-0	A Side Drop Bus E1 Byte	**A Side Drop Bus E1 Overhead Byte for STS-3 STS-1 No. 3/AU-3 C:** The value in this location is dropped E1 overhead byte in the A Drop Bus STS-3 STS-1 No. 3/AU-3 C format. This register location is updated every 125 microseconds. Bits 7-0 of the register correspond to bits 1-8 of the E1 byte.
074	7-0	A Side Drop Bus Polling Bits Channels 8-1	**A Side Drop Polling Registers, Channels 8-1:** Bit 7 corresponds to the polling bit for channel 8. A polling bit is set to 1 when one or more A side drop alarms are detected in a channel and the corresponding mask bit is set to 1. This bit is cleared when the A side latched alarms corresponding to the channel that is set to 1 are read, or the mask bit associated with the alarm in the interrupt hierarchy is set to 0.
075	7-0	A Side Drop Polling Bits Channels 16-9	**A Side Drop Polling Registers, Channels 16-9:** Bit 7 corresponds to the polling bit for channel 16. A polling bit is set to 1 when one or more A side drop alarms are detected in a channel and the corresponding mask bit is set to 1. This bit is cleared when the A side latched alarms corresponding to the channel that is set to 1 are read, or the mask bit associated with the alarm in the interrupt hierarchy is set to 0.
076	7-0	A Side Drop Polling Bits Channels 24-17	**A Side Drop Polling Registers, Channels 24-17:** Bit 7 corresponds to the polling bit for channel 24. A polling bit is set to 1 when one or more A side drop alarms are detected in a channel and the corresponding mask bit is set to 1. This bit is cleared when the A side latched alarms corresponding to the channel that is set to 1 are read, or the mask bit associated with the alarm in the interrupt hierarchy is set to 0.
077	7-4		**Not used:**
	3-0	A Side Drop Polling Bits Channels 28-25	**A Side Drop Polling Registers, Channels 28-25:** Bit 3 corresponds to the polling bit for channel 28. A polling bit is set to 1 when one or more A side drop alarms are detected in a channel and the corresponding mask bit is set to 1. This bit is cleared when the A side latched alarms corresponding to the channel that is set to 1 are read, or the mask bit associated with the alarm in the interrupt hierarchy is set to 0.

MASK BITS FOR B DROP BUS STATUS ALARMS

Address	Bit	Symbol	Description
049	7-5		**Not used:**
	4	MB3UAIS	**Mask Bit for Global Indication for Upstream AIS indication for B Drop Bus STS-3 STS-1 No.3/STM-1 AU-3 C:** A 1 enables the global indication (GDB) to be set for an upstream AIS indication that has been detected in the H1/H2 bytes or in the E1 byte for STS-3 STS-1 No.3/STM-1 AU-3 C format for the B side drop bus. A 0 disables the global indication bit GDB for this alarm.
	3	MB2UAIS	**Mask Bit for Global Indication for Upstream AIS indication for B Drop Bus STS-3 STS-1 No.2/STM-1 AU-3 B:** A 1 enables the global indication (GDB) to be set for an upstream AIS indication that has been detected in the H1/H2 bytes or in the E1 byte for STS-3 STS-1 No.2/STM-1 AU-3 B format for the B side drop bus. A 0 disables the global indication bit GDB for this alarm.
	2	MB1UAIS	**Mask Bit for Global Indication for Upstream AIS indication for B Drop Bus STS-3 STS-1 No.1/STM-1 AU-3 A and STM-1 VC-4:** A 1 enables the global indication (GDB) to be set for an upstream AIS indication that has been detected in the H1/H2 bytes or in the E1 byte for STS-3 STS-1 No.2/STM-1 AU-3 A or for the STN-1 VC-4 format for the B side drop bus. A 0 disables the global indication bit GDB for this alarm.
	1	MBDPAR	**Mask Bit for Global Indication for B Drop Parity Alarm:** A 1 enables the global indication (GDB) to be set for a parity alarm detected for the B side drop bus. A 0 disables the global indication bit GDB for this alarm.
	0	MBDLOC	**Mask Bit for Global Indication for B Drop Loss of Clock Alarm:** A 1 enables the global indication (GDB) to be set for a loss of clock alarm detected for the B side drop bus. A 0 disables the global indication bit GDB for this alarm.

Address	Bit	Symbol	Description
04A	7-6		**Not used:**
	5	MB3OOM	**Mask Bit for Global Indication for H4 Out Of Multiframe Indication for B Drop Bus STS-3 STS-1 No.3/STM-1 AU-3 C:** A 1 enables the global indication (GDB) to be set for an H4 Out Of Multiframe indication for STS-3 STS-1 No.3/STM-1 AU-3 C format for the B side drop bus. A 0 disables the global indication bit GDB for this alarm.
	4	MB2OOM	**Mask Bit for Global Indication for H4 Out Of Multiframe Indication for B Drop Bus STS-3 STS-1 No.2/STM-1 AU-3 B:** A 1 enables the global indication (GDB) to be set for an H4 Out Of Multiframe indication for STS-3 STS-1 No.2/STM-1 AU-3 B format for the B side drop bus. A 0 disables the global indication bit GDB for this alarm.
	3	MB1OOM	**Mask Bit for Global Indication for H4 Out Of Multiframe Indication for B Drop Bus STS-3 STS-1 No.1/STM-1 AU-3 A and STM-1 VC-4:** A 1 enables the global indication (GDB) to be set for an H4 Out Of Multiframe indication for STS-3 STS-1 No.1/STM-1 AU-3 A and STM-1 VC-4 format for the B side drop bus. A 0 disables the global indication bit GDB for this alarm.
	2	MB3LOM	**Mask Bit for Global Indication for H4 Loss Of Multiframe Indication for B Drop Bus STS-3 STS-1 No.3/STM-1 AU-3 C:** A 1 enables the global indication (GDB) to be set for an H4 Loss Of Multiframe indication for STS-3 STS-1 No.3/STM-1 AU-3 C format for the B side drop bus. A 0 disables the global indication bit GDB for this alarm.
	1	MB2LOM	**Mask Bit for Global Indication for H4 Loss Of Multiframe Indication for B Drop Bus STS-3 STS-1 No.2/STM-1 AU-3 B:** A 1 enables the global indication (GDB) to be set for an H4 Loss Of Multiframe indication for STS-3 STS-1 No.2/STM-1 AU-3 B format for the B side drop bus. A 0 disables the global indication bit GDB for this alarm.
	0	MB1LOM	**Mask Bit for Global Indication for H4 Loss Of Multiframe Indication for B Drop Bus STS-3 STS-1 No.1/STM-1 AU-3 A and STM-1 VC-4:** A 1 enables the global indication (GDB) to be set for an H4 Loss Of Multiframe indication for STS-3 STS-1 No.1/STM-1 AU-3 A and STM-1 VC-4 format for the B side drop bus. A 0 disables the global indication bit GDB for this alarm.
04B	7-0	Mask Bits B Drop Polling Register Channel 8-1	**Mask Bits Polling Registers Channels 8-1 B Drop Alarms:** A 1 in one or more bits enables a B side drop alarm in the corresponding channel to set the global indication (PCDB) bit. A 0 disables the channel corresponding to a polling bit from setting the global indication (PCDB) bit. Bit 7 is the mask bit for channel 8 B drop side alarms.
04C	7-0	Mask Bits B Drop Polling Register Channel 16-9	**Mask Bits Polling Registers Channels 16-9 B Drop Alarms:** A 1 in one or more bits enables a B side drop alarm in the corresponding channel to set the global indication (PCDB) bit. A 0 disables the channel corresponding to a polling bit from setting the global indication (PCDB) bit. Bit 7 is the mask bit for channel 16 B drop side alarms.
04D	7-0	Mask Bits B Drop Polling Register Channel 24-17	**Mask Bits Polling Registers Channels 24-17 B Drop Alarms:** A 1 in one or more bits enables a B side drop alarm in the corresponding channel to set the global indication (PCDB) bit. A 0 disables the channel corresponding to a polling bit from setting the global indication (PCDB) bit. Bit 7 is the mask bit for channel 24 B drop side alarms.

Address	Bit	Symbol	Description
04E	7-4		**Not used:**
	3-0	Mask Bits B Drop Polling Register Channel 28-25	**Mask Bits Polling Registers Channels 28-25 B Drop Alarms:** A 1 in one or more bits enables B side drop alarm in the corresponding channel to set the global indication (PCDB) bit. A 0 disables the channel corresponding to a polling bit from setting the global indication (PCDB) bit. Bit 3 is the mask bit for channel 28 B drop side alarms.

B SIDE DROP BUS - STATUS REGISTER DESCRIPTIONS

Address	Bit	Symbol	Description
080	7-5		**Not used:**
	4	B3UAIS	**B Side Drop Bus Upstream AIS (Unlatched) Alarm Indication - STS-3 STS-1 No. 3/AU-3 C:** A 1 indicates that AIS has been detected on the B side drop bus in the H1/H2 bytes or in the E13 byte for the STS-3 STS-1 No.3/STM-1 AU-3 C format. Control bits SE1AIS and HEAISE (bits 1 and 0, 01DH) determine whether the H1/H2 bytes or the E13 byte is monitored for AIS detection. This indication is disabled for the STM-1 VC-4 format.
	3	B2UAIS	**B Side Drop Bus Upstream AIS (Unlatched) Alarm Indication - STS-3 STS-1 No. 2/AU-3 B:** A 1 indicates that AIS has been detected on the B side drop bus in the H1/H2 bytes or in the E12 byte for the STS-3 STS-1 No.2/STM-1 AU-3 B format. Control bits SE1AIS and HEAISE (bits 1 and 0, 01DH) determine whether the H1/H2 bytes or the E12 byte is monitored for AIS detection. This indication is disabled for the STM-1 VC-4 format.
	2	B1UAIS	**B Side Drop Bus Upstream AIS (Unlatched) Alarm Indication - STS-3 STS-1 No. 1/AU-3 A, STM-1 VC4:** A 1 indicates that AIS has been detected on the B side drop bus in the H1/H2 bytes or in the E11 byte for the STS-3 STS-1 No.1/STM-1 AU-3 A format or for the STM-1 VC-4 format. Control bits SE1AIS and HEAISE (bits 1 and 0, 01DH) determine whether the H1/H2 bytes or the E11 byte is monitored for AIS detection.
	1	BDPAR	**B Side Drop Bus Parity (Unlatched) Alarm Indication:** A 1 indicates that an even or odd parity error has been detected in the B side Drop bus signals. Other than an alarm indication, no action is taken. Parity is monitored for each drop bus clock cycle.
	0	BDLOC	**B Side Drop Bus Loss Of Clock (Unlatched) Alarm Indication:** A 1 indicates that the B side Drop bus has detected a loss of clock. An alarm occurs when the input drop clock is stuck high or low for 56 clock cycles (DSCLK clock). Recovery occurs on the first clock transition.

Address	Bit	Symbol	Description
081	7-6		**Not used:**
	5	B3HOOM	**B Side Drop Bus H4 Byte Out Of Multiframe Alignment (Unlatched) Alarm - STS-3 STS-1 No. 3/AU-3 C:** Enabled when control bit DV1SEL is a 0. An Out Of Multiframe alarm for STS-3 STS-1 No. 3/AU-3 C is declared once an error is detected in the bit 7 and 8 sequence in the H4 byte. Recovery occurs when an error-free H4 sequence (00, 01, 10, 11) is found in four consecutive frames.
	4	B2HOOM	**B Side Drop Bus H4 Byte Out Of Multiframe Alignment (Unlatched) Alarm - STS-3 STS-1 No. 2/AU-3 B:** Enabled when control bit DV1SEL is a 0. An Out Of Multiframe alarm for STS-3 STS-1 No. 2/AU-3 B is declared once an error is detected in the bit 7 and 8 sequence in the H4 byte. Recovery occurs when an error-free H4 sequence (00, 01, 10, 11) is found in four consecutive frames.
	3	B1HOOM	**B Side Drop Bus H4 Byte Out Of Multiframe Alignment (Unlatched) Alarm - STS-3 STS-1/AU-3 A, STM-1 VC-4:** Enabled when control bit DV1SEL is a 0. An Out Of Multiframe alarm for STS-3 STS-1 No.1/AU-3 or the STM-1 VC-4 is declared once an error is detected in the bit 7 and 8 sequence in the H4 byte. Recovery occurs when an error-free H4 sequence (00, 01, 10, 11) is found in four consecutive frames.
	2	B3HLOM	**B Side Drop Bus H4 Byte Loss of Multiframe Alignment (Unlatched) Alarm - STS-3 STS-1 No. 3/AU-3 C:** Once in the Out Of Multiframe state, if recovery does not occur within 1 ms, a Loss Of Multiframe alarm is declared. Recovery will occur when the multiframe is recovered. The Loss of Multiframe alarm forces a VT/TU Loss of Pointer alarm (BnLOP) for all channels which have a VT/TU selected for STS-3 STS-1 No. 3/AU-3 C.
	1	B2HLOM	**B Side Drop Bus H4 Byte Loss of Multiframe Alignment (Unlatched) Alarm - STS-3 STS-1No. 2/AU-3 B:** Once in the Out Of Multiframe state, if recovery does not occur within 1 ms, a Loss Of Multiframe alarm is declared. Recovery will occur when the multiframe is recovered. The Loss of Multiframe alarm forces a VT/TU Loss of Pointer alarm (BnLOP) for all channels which have a VT/TU selected for STS-3 STS-1No. 2/AU-3 B.
	0	B1HLOM	**B Side Drop Bus H4 Byte Loss of Multiframe Alignment (Unlatched) Alarm - STS-3 STS-1 No. 1/AU-3 A, STM-1 VC-4:** Once in the Out Of Multiframe state, if recovery does not occur within 1 ms, a Loss Of Multi-frame alarm is declared. Recovery will occur when the multiframe is recovered. The Loss of Multiframe alarm forces a VT/TU Loss of Pointer alarm (BnLOP) for all channels which have a VT/TU selected for STS-3 STS-1 No. 1/AU-3 A, STM-1 VC-4.

Address	Bit	Symbol	Description
082	7-5		**Not used:**
	4	LB3UAIS	**B Side Drop Bus Upstream AIS Latched Alarm Indication - STS-3 STS-1 No. 3/AU-3 C:** This bit position latches for the B side received upstream AIS alarm Indication for the STS-3 STS-1 No. 3/AU-3 C format. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	3	LB2UAIS	**B Side Drop Bus Upstream AIS Latched Alarm Indication - STS-3 STS-1 No. 2/AU-3 B:** This bit position latches for the B side received upstream AIS alarm Indication for the STS-3 STS-1 No. 2/AU-3 B format. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	2	LB1UAIS	**B Side Drop Bus Upstream AIS Latched Alarm Indication - STS-3 STS-1 No. 1/AU-3 A/VC4:** This bit position latches for the B side received upstream AIS alarm Indication for the STS-3 STS-1 No. 1/AU-3 A or STM-1 VC-4 format. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	1	LBDPAR	**B Side Drop Bus Parity Latched Alarm Indication:** This bit position latches for the B side parity error. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	0	LBDLOC	**B Side Drop Bus Loss Of Clock Latched Alarm Indication:** This bit position latches for the B side loss of clock alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.

Address	Bit	Symbol	Description
083	7-6		**Not used:**
	5	LB3HOOM	**B Drop Bus H4 Byte Out Of Multiframe Alignment Latched Alarm Indication - STS-3 STS-1 No. 3/AU-3 C:** This bit position latches for the B side STS-3 STS-1 No. 3/AU-3 C H4 byte Out of Multiframe alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	4	LB2HOOM	**B Drop Bus H4 Byte Out Of Multiframe Alignment Latched Alarm Indication - STS-3 STS-1 No. 2/AU-3 B:** This bit position latches for the B side STS-3 STS-1 No.2/AU-3 B H4 byte Out of Multiframe alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	3	LB1HOOM	**B Drop Bus H4 Byte Out Of Multiframe Alignment Latched Alarm Indication - STS-3 STS-1 No. 1/AU-3 A, STM-1 VC-4:** This bit position latches for the B side STS-3 STS-1 No.1/AU-3 A, or STM-1 VC-4 H4 byte Out of Multiframe alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	2	LB3HLOM	**B Drop Bus H4 Byte Loss Of Multiframe Alignment Latched Alarm Indication - STS-3 STS-1 No. 2/AU-3 C:** This bit position latches for the B side STS-3 STS-1 No. 3/AU-3 C H4 byte Loss of Multiframe alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	1	LB2HLOM	**B Drop Bus H4 Byte Loss Of Multiframe Alignment Latched Alarm Indication - STS-3 STS-1 No. 2/AU-3 B:** This bit position latches for the B side STS-3 STS-1 No. 2/AU-3 B H4 byte Loss of Multiframe alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	0	LB1HLOM	**B Drop Bus H4 Byte Loss Of Multiframe Alignment Latched Alarm Indication - STS-3 STS-1 No. 1/AU-3 A, STM-1 VC-4:** This bit position latches for the B side STS-3 STS-1 No. 1/AU-3 A, or STM-1 VC-4 H4 byte Loss of Multiframe alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.

Address	Bit	Symbol	Description
084	7-5		**Not used:**
	4	PB3UAIS	**B Side Drop Bus Upstream AIS One Second Alarm Indication - STS-3 STS-1 No. 3/AU-3 C:** This bit position is set when the B side received upstream AIS alarm Indication - STS-3 STS-1 No. 3/AU-3 C has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	3	PB2UAIS	**B Side Drop Bus Upstream AIS One Second Alarm Indication - STS-3 STS-1 No. 2/AU-3 B:** This bit position is set when the B side received upstream AIS alarm Indication - STS-3 STS-1 No. 2/AU-3 B has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	2	PB1UAIS	**B Side Drop Bus Upstream AIS One Second Alarm Indication - STS-1 No. 1/AU-3 A and STM-1 VC-4:** This bit position is set when the B side received upstream AIS alarm Indication - STS-3 STS-1 No. 1/AU-3 A or STM-1 VC-4 has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	1	PBDPAR	**B Side Drop Bus Parity One Second Alarm Indication:** This bit position is set when the B side parity error alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	0	PBDLOC	**B Side Drop Bus Loss Of Clock One Second Alarm Indication:** This bit position is set when the B side loss of clock alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.

Address	Bit	Symbol	Description
085	7-6		**Not used:**
	5	PB3HOOM	**B Side Drop Bus H4 Byte Out Of Multiframe Alignment One Second Alarm Indication - STS-3 STS-1 No. 3/AU-3 C:** This bit position is set when the B side STS-3 STS-1 No. 3/AU-3 C H4 byte Out Of Multiframe Alignment alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	4	PB2HOOM	**B Side Drop Bus H4 Byte Out Of Multiframe Alignment One Second Alarm Indication - STS-3 STS-1 No. 2/AU-3 B:** This bit position is set when the B side STS-3 STS-1 No. 2/AU-3 B H4 byte Out Of Multiframe Alignment alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	3	PB1HOOM	**B Side Drop Bus H4 Byte Out Of Multiframe Alignment One Second Alarm Indication - STS-3 STS-1 No. 1/AU-3 A, STM-1 VC-4:** This bit position is set when the B side STS-3 STS-1 No. 1/AU-3 A or the STM-1 VC-4 H4 byte Out Of Multiframe Alignment alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	2	PB3HLOM	**B Side Drop Bus H4 Byte Loss Of Multiframe Alignment One Second Alarm Indication - STS-3 STS-1 No. 3/AU-3 C:** This bit position is set when the B side STS-3 STS-1 No. 3/AU-3 C H4 byte Loss Of Multiframe Alignment alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	1	PB2HLOM	**B Side Drop Bus H4 Byte Loss Of Multiframe Alignment One Second Alarm Indication - STS-1 No. 2/AU-3 B:** This bit position is set when the B side STS-3 /STS-1 No. 2/AU-3 B H4 byte Loss Of Multiframe Alignment alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	0	PB1HLOM	**B Side Drop Bus H4 Byte Loss Of Multiframe Alignment One Second Alarm Indication - STS-3 STS-1 No. 1/AU-3 A, STM-1 VC-4:** This bit position is set when the B side STS-3 STS-1 No.1/AU-3 A or the STM-1 VC-4 H4 byte Loss Of Multiframe Alignment alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.

Address	Bit	Symbol	Description
086	7-5		**Not used:**
	4	FB3UAIS	**B Side Drop Bus Upstream AIS Persistent One Second Alarm Indication - STS-3 STS-1 No. 3/AU-3 C:** This bit position is set to 1 for the one-second interval, when the B side received upstream AIS alarm Indication - STS-3 STS-1 No. 3/AU-3 C is active, but did not become active in the previous one second interval.
	3	FB2UAIS	**B Side Drop Bus Upstream AIS Persistent One Second Alarm Indication - STS-3 STS-1 No. 2/AU-3 B:** This bit position is set to 1 for the one-second interval, when the B side received upstream AIS alarm Indication - STS-3 STS-1 No. 2/AU-3 B is active, but did not become active in the previous one second interval.
	2	FB1UAIS	**B Side Drop Bus Upstream AIS Persistent One Second Alarm Indication - STS-3 STS-1 No. 1/AU-3 A and STM-1 VC-4:** This bit position is set to 1 for the one-second interval, when the B side received upstream AIS alarm Indication - STS-3 STS-1 No. 1/AU-3 A or SM-1 VC-4 is active, but did not become active in the previous one second interval.
	1	FBDPAR	**B Side Drop Bus Parity Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the B side parity error alarm indication is active, but did not become active in the previous one second interval.
	0	FBDLOC	**B Side Drop Bus Loss Of Clock Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the B side loss of clock alarm indication is active, but did not become active in the previous one second interval.

Address	Bit	Symbol	Description
087	7-6		**Not used:**
	5	FB3HOOM	**B Side Drop Bus H4 Byte Out Of Multiframe Alignment Persistent One Second Alarm Indication - STS-3 STS-1 No. 3/AU-3 C:** This bit position is set to 1 for the one-second interval, when the B side STS-3 STS-1 No. 3/AU-3 C H4 byte Out Of Multiframe alarm indication is active, but did not become active in the previous one second interval.
	4	FB2HOOM	**B Side Drop Bus H4 Byte Out Of Multiframe Alignment Persistent One Second Alarm Indication - STS-3 STS-1 No. 2/3AU-3 B:** This bit position is set to 1 for the one-second interval, when the B side STS-3 STS-1 No. 2/AU-3 B H4 byte Out Of Multiframe alarm indication is active, but did not become active in the previous one second interval.
	3	FB1HOOM	**B Side Drop Bus H4 Byte Out Of Multiframe Alignment Persistent One Second Alarm Indication - STS-3 STS-1 No. 1/AU-3 A, STM-1 VC-4:** This bit position is set to 1 for the one-second interval, when the B side STS-3 STS-1 No. 1/AU-3 A, or the STM-1 VC-4 H4 byte Out Of Multiframe alarm indication is active, but did not become active in the previous one second interval.
	2	FB3HLOM	**B Side Drop Bus H4 Byte Loss Of Multiframe Alignment Persistent One Second Alarm Indication - STS-3 STS-1 No. 3/AU-3 C:** This bit position is set to 1 for the one-second interval, when the B side STS-3 STS-1 No. 3/AU-3 C H4 byte Loss Of Multiframe alarm indication is active, but did not become active in the previous one second interval.
	1	FB2HLOM	**B Side Drop Bus H4 Byte Loss Of Multiframe Alignment Persistent One Second Alarm Indication - STS-3 STS-1 No. 2/AU-3 B:** This bit position is set to 1 for the one-second interval, when the B side STS-3 STS-1 No. 2/AU-3 B H4 byte Loss Of Multiframe alarm indication is active, but did not become active in the previous one second interval.
	0	FB1HLOM	**B Side Drop Bus H4 Byte Loss Of Multiframe Alignment Persistent One Second Alarm Indication - STS-3 STS-1 No. 1/AU-3 A, STM-1 VC-4:** This bit position is set to 1 for the one-second interval, when the B side STS-3 STS-1 No. 1/AU-3 A, or the STM-1 VC-4 H4 byte Loss Of Multiframe alarm indication is active, but did not become active in the previous one second interval.
088	7-0	B Side Drop Bus H1 Byte	**B Side Drop Bus H1 Pointer Byte for STS-3 STS-1 No. 1/AU-3 A or STM-1 VC-4:** The value in this location is dropped H1 Pointer byte in the B Drop Bus STS-3 STS-1 No. 1/AU-3 A or VC-4 format. This register location is updated every 125 microseconds. Bits 7-0 of the register correspond to bits 1-8 of the H1 byte.
089	7-0	B Side Drop Bus H1 Byte	**B Side Drop Bus H1 Pointer Byte for STS-3 STS-1 No. 2/AU-3 B:** The value in this location is dropped H1 Pointer byte in the B Drop Bus STS-3 STS-1 No. 2/AU-3 B format. This register location is updated every 125 microseconds. Bits 7-0 of the register correspond to bits 1-8 of the H1 byte.

Address	Bit	Symbol	Description
08A	7-0	B Side Drop Bus H1 Byte	**B Side Drop Bus H1 Pointer Byte for STS-3 STS-1 No. 3/AU-3 C:** The value in this location is dropped H1 Pointer byte in the B Drop Bus STS-3 STS-1 No. 3/AU-3 C format. This register location is updated every 125 microseconds. Bits 7-0 of the register correspond to bits 1-8 of the H1 byte.
08B	7-0	B Side Drop Bus H2 Byte	**B Side Drop Bus H2 Pointer Byte for STS-3 STS-1 No. 1/AU-3 A or STM-1 VC-4:** The value in this location is dropped H21 Pointer byte in the B Drop Bus STS-3 STS-1 No. 1/AU-3 A or VC-4 format. This register location is updated every 125 microseconds. Bits 7-0 of the register correspond to bits 1-8 of the H2 byte.
08C	7-0	B Side Drop Bus H2 Byte	**B Side Drop Bus H2 Pointer Byte for STS-3 STS-1 No. 2/AU-3 B:** The value in this location is dropped H2 Pointer byte in the B Drop Bus STS-3 STS-1 No. 2/AU-3 B format. This register location is updated every 125 microseconds. Bits 7-0 of the register correspond to bits 1-8 of the H2 byte.
08D	7-0	B Side Drop Bus H2 Byte	**B Side Drop Bus H2 Pointer Byte for STS-3 STS-1 No. 3/AU-3 C:** The value in this location is dropped H2 Pointer byte in the B Drop Bus STS-3 STS-1 No. 3/AU-3 C format. This register location is updated every 125 microseconds. Bits 7-0 of the register correspond to bits 1-8 of the H2 byte.
08E	7-0	B Side Drop Bus H4 Byte	**B Side Drop Bus H4 Path Overhead Byte for STS-3 STS-1 No. 1/AU-3 A or STM-1 VC-4:** The value in this location is dropped H4 path overhead byte in the B Drop Bus STS-3 STS-1 No. 1/AU-3 A or VC-4 format. This register location is updated every 125 microseconds. Bits 7-0 of the register correspond to bits 1-8 of the H4 byte.
08F	7-0	B Side Drop Bus H4 Byte	**B Side Drop Bus H4 Path Overhead Byte for STS-3 STS-1 No. 2/AU-3 B:** The value in this location is dropped H4 path overhead byte in the B Drop Bus STS-3 STS-1 No. 2/AU-3 B format. This register location is updated every 125 microseconds. Bits 7-0 of the register correspond to bits 1-8 of the H4 byte.
090	7-0	B Side Drop Bus H4 Byte	**B Side Drop Bus H4 Path Overhead Byte for STS-3 STS-1 No. 3/AU-3 C:** The value in this location is dropped H4 path overhead byte in the B Drop Bus STS-3 STS-1 No. 3/AU-3 C format. This register location is updated every 125 microseconds. Bits 7-0 of the register correspond to bits 1-8 of the H4 byte.
091	7-0	B Side Drop Bus E1 Byte	**B Side Drop Bus E1 Overhead Byte for STS-3 STS-1 No. 1/AU-3 A or STM-1 VC-4:** The value in this location is dropped E1 overhead byte in the B Drop Bus STS-3 STS-1 No. 1/AU-3 A or VC-4 format. This register location is updated every 125 microseconds. Bits 7-0 of the register correspond to bits 1-8 of the E1 byte.
092	7-0	B Side Drop Bus E1 Byte	**B Side Drop Bus E1 Overhead Byte for STS-3 STS-1 No. 2/AU-3 B:** The value in this location is dropped E1 overhead byte in the B Drop Bus STS-3 STS-1 No. 2/AU-3 B format. This register location is updated every 125 microseconds. Bits 7-0 of the register correspond to bits 1-8 of the E1 byte.

Address	Bit	Symbol	Description
093	7-0	B Side Drop Bus E1 Byte	**B Side Drop Bus E1 Overhead Byte for STS-3 STS-1 No. 3/AU-3 C:** The value in this location is dropped E1 overhead byte in the B Drop Bus STS-3 STS-1 No. 3/AU-3 C format. This register location is updated every 125 microseconds. Bits 7-0 of the register correspond to bits 1-8 of the E1 byte.
094	7-0	B Side Drop Bus Polling Bits Channels 8-1	**B Side Drop Polling Registers, Channels 8-1:** Bit 7 corresponds to the polling bit for channel 8. A polling bit is set to 1 when one or more B side drop alarms are detected in a channel and the corresponding mask bit is set to 1. This bit is cleared when the B side latched alarms corresponding to the channel that is set to 1 are read, or the mask bit associated with the alarm in the interrupt hierarchy is set to 0.
095	7-0	B Side Drop Polling Bits Channels 16-9	**B Side Drop Polling Registers, Channels 16-9:** Bit 7 corresponds to the polling bit for channel 16. A polling bit is set to 1 when one or more B side drop alarms are detected in a channel and the corresponding mask bit is set to 1. This bit is cleared when the B side latched alarms corresponding to the channel that is set to 1 are read, or the mask bit associated with the alarm in the interrupt hierarchy is set to 0.
096	7-0	B Side Drop Polling Bits Channels 24-17	**B Side Drop Polling Registers, Channels 24-17:** Bit 7 corresponds to the polling bit for channel 24. A polling bit is set to 1 when one or more B side drop alarms are detected in a channel and the corresponding mask bit is set to 1. This bit is cleared when the B side latched alarms corresponding to the channel that is set to 1 are read, or the mask bit associated with the alarm in the interrupt hierarchy is set to 0.
097	7-4		**Not used:**
	3-0	B Side Drop Polling Bits Channels 28-25	**B Side Drop Polling Registers, Channels 28-25:** Bit 3 corresponds to the polling bit for channel 28. A polling bit is set to 1 when one or more B side drop alarms are detected in a channel and the corresponding mask bit is set to 1. This bit is cleared when the B side latched alarms corresponding to the channel that is set to 1 are read, or the mask bit associated with the alarm in the interrupt hierarchy is set to 0.

CHANNEL n - A AND B SIDE DROP AND ADD BUS CONTROL REGISTER DESCRIPTIONS (n = 1 to 28)

Address	Bit	Symbol	Description
X+000	7-6		**Not used:**
	5	RnNRZP	**Receive Data Invert Enable for NRZ Data:** A 1 inverts the receive NRZ data stream when the NRZ interface is selected. A 0 enables normal operation.
	4		**Not used:**
	3	RnCLKI	**Receive Clock Invert Enable:** Valid for all interfaces. When this control bit is set to 1, data and any other line signals, shall be clocked out on positive transitions of the clock. When set to 0, the line signals are clocked out on negative transitions of the clock.
	2	RnB8ZS	**Receive B8ZS Line Code Enable.** When the receive line is configured for rail operation, a 1 selects the B8ZS line code for DS1 line interfaces. A 0 selects the AMI code. For E1 interfaces this bit must be set to 1 for the HDB3 line code. When set to 0, the AMI code is selected.
	1		**Not used:**
	0	RnLAIS	**Receive AIS Sent On Line Loopback:** This bit works in conjunction with control bit LnLBK according to the following table: RnLAIS / LnLBK / Receive Line Interface X / 0 / Normal Operation. 0 / 1 / Line Loopback enabled. Receive data is provided. 1 / 1 / Line Loopback enabled. Receive AIS is sent. X= don't care
X+001	7-0		**Reserved**

Address	Bit	Symbol	Description
X+002	7 6	TnLINT1 TnLINT0	**Transmit Line Interface Selection:** The transmit line interface is selected according to the following table: TnLINT1 / TnLINT0 / Line Interface Selected 0 / 0 / Not used. 0 / 1 / NRZ Interface. The negative rail lead may be used to input an external loss of signal indication or external coding violations. 1 / 0 / Rail Interface. B8ZS or AMI line code for the DS1 line rate. HDB3 or AMI line code for the E1 line rate. 1 / 1 / VT/TU Interface. The TnSEL1 and TnSEL0 control bits cannot be set to 11 (dual unidirectional ring mode).
	5	TnNRZP	**Transmit Data Invert Enable for NRZ Data:** A 1 inverts the transmit NRZ data stream when the NRZ interface is selected. A 0 enables normal operation.
	4	TnE1SL	**Transmit Line Rate Selection:** A 1 selects the E1 line rate for channel n. A 0 selects the DS1 line rate.
	3	TnCLKI	**Transmit Clock Invert Enable:** Valid for all interfaces. When this control bit is set to 0, data and any other line signals, shall be clocked in on negative transitions of the clock. When set to 1, the line signals are clocked in on positive transitions of the clock.
	2	TnB8ZS	**Transmit B8ZS Line Code Enable:** When the transmit line is configured for rail operation, a 1 selects the B8ZS line code for T1 line interfaces. A 0 selects the AMI code. For E1 interfaces this bit must be set to 1 for the HDB3 line code. When set to 0, the AMI code is selected.
	1	TnSAIS	**Sent Transmit Line AIS:** A 1 forces either a DS1 or E1 line AIS signal to be transmitted for the VT/TU selected in the add direction independent of the add side alarms.

	0	TnAISE	**Transmit Line AIS Enable:** Enables a DS1 or E1 line AIS to be sent for the following conditions:
			
			- When control bit TnAISE is a 1
			  - Transmit Loss Of Clock alarm (TnLOC)
			  - Transmit Loss Of Signal alarm (TnLOS) when the rail interface is selected
			  - External Loss Of Signal alarm (TnLOS) when NRZ interface is selected and control bit EXnLOS is a 1
			  - Control bit TnSAIS is a 1
			
			- When control bit TnAISE is a 0
			  - Control bit TnSAIS is a 1
			Note: When control bit TnAISE is a 0 and the Transmit Loss of Clock (TnLOC) alarm occurs, transmit line AIS may be generated regardless of the state of control bit TnSAIS

Address	Bit	Symbol	Description
X+003	7-2		**Not used:**
	1	EXnLOS	**Transmit External Loss Of Signal Enable:** Enabled only when the transmit NRZ interface is selected. A 1 configures the negative rail interface lead for an external loss of signal indication, A 0 configures the negative rail interface lead for external coding violations. The coding violation active true state is positive.
	0	EXnLOSP	**Transmit External Loss Of Signal Sense Selection:** Enabled only when control bit EXnLOS above is a 1. A 1 configures the loss of signal active true state to be positive. A 0 configures the loss of signal active true state to be negative.
X+004	7-6		**Not used:**
	5	TnPTG	**PBRS Generator Enable:** A 1 enables the PRBS generator for channel n. The PRBS pattern is selected by control bit TnPRN.
	4	TnANZ	**PRBS Analyzer Enable:** A 1 enables the PRBS analyzer for channel n. The PRBS pattern is selected by control bit TnPRN.
	3		**Not used:**
	2	TnPRN	**PRBS Pattern Selection:** The test generator and analyzer PRBS pattern is selected according to the following table. TnPRN — PRBS Pattern 0 — 2^{15}-1 pattern. 1 — 2^{20}-1 QRS pattern.
	1	LnLBK	**Line Loopback:** A 1 enables a DS1 or E1 line side loopback for channel n. The receive line side DS1 or E1 clock and data output signals are looped back internally as the DS1 or E1 transmit input signals. The external DS1 or E1 transmit clock and data input signals are disabled. The DS1 or E1 receive clock and data output signals or line AIS are provided at the receive interface, depending on the sate of control bit RnLAIS (bit 0, X+000H). This control bit works in conjunction with control bit FnLBK (see bit 0 below) to provide a bidirectional loopback. When this control bit and FnLBK are both set to 1, bidirectional loopback is enabled. In this mode of operation, the transmit data is looped back as receive data, and the output of the demapper is looped back as transmit data. The RnCLKI (bit 3, register X+000H) and TnCLKI (bit 3, register X+002H) control bits must be programmed for opposite edges when using Line Loopback or Bidirectional Loopback.
	0	FnLBK	**Facility Loopback:** A 1 enables a DS1 or E1 facility (side) loopback for channel n. The DS1 or E1 transmit clock and data output signals are looped back internally as the DS1 or E1 receive clock and data input signals. The external DS1 or E1 receive input signals are disabled. The DS1 or E1 transmit clock and data output signals are provided at the interface.

<table>
<tr><th>Address</th><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td rowspan="6">X+006</td><td>7
6</td><td>RnLINT1
RnLINT0</td><td>Receive Line Interface Selection: The receive line interface for channel n is selected according to the following table:

<table>
<tr><th>RnLINT1</th><th>RnLINT0</th><th>Line Interface Selected</th></tr>
<tr><td>0</td><td>0</td><td>High Z or 0 depending on the state of the RnOUTL control bit.</td></tr>
<tr><td>0</td><td>1</td><td>NRZ Interface.</td></tr>
<tr><td>1</td><td>0</td><td>Rail Interface. B8ZS or AMI line code for the DS1 line rate. HDB3 or AMI line code for the E1 line rate.</td></tr>
<tr><td>1</td><td>1</td><td>VT/TU Interface.</td></tr>
</table></td></tr>
<tr><td>5</td><td>RnOUTL</td><td>Receive Line Interface High Z or 0 Selection: Enabled only when the RnLINT1 and RnLINT0 controls bits are set to 00. A 0 forces the line interface output signals to a high Z state. A 1 forces the line interface output signals to the 0 state. The TU/VT must be selected to drive the receive output low. If using Single Unidirectional Ring mode, forcing outputs to zero state is inhibited.</td></tr>
<tr><td>4</td><td>RnE1SL</td><td>Receive Line Rate Selection: A 1 selects the E1 line rate for channel n. A 0 selects the DS1 line rate.</td></tr>
<tr><td>3</td><td>FnRDIS</td><td>REI and RDI Disabled: Enabled when the single unidirectional mode (control bits TnSEL1, TnSEL0 are equal to 01) is selected. A 1 disables receive side alarms or an out of range condition from generating RDI. In addition, the REI value is transmitted as a zero.</td></tr>
<tr><td>2
1
0</td><td>RnSEL
TnSEL1
TnSEL0</td><td>Channel n A/B Drop/Add Bus Selection: The table below lists the selection criteria for the eight available modes of operation of channel n:

<table>
<tr><th>TnSEL1</th><th>TnSEL0</th><th>RnSEL</th><th>Operating Mode</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>A Drop only (Drop)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>B Drop only (Drop)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>A Drop A Add (Single Unidirectional Ring)</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>B Drop B Add (Single Unidirectional Ring)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>A Drop B Add (Multiplexer)</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>B Drop A Add (Multiplexer)</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>A Drop A and B Add (Dual Unidirectional Ring)</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>B Drop B and A Add (Dual Unidirectional Ring)</td></tr>
</table></td></tr>
<tr><td rowspan="3">X+007</td><td>7-2</td><td></td><td>Not used:</td></tr>
<tr><td>1</td><td>TnVTVC</td><td>Transmit VT/TU Overhead Byte Selection: Enabled with the VT/TU transmit line interface is selected. A 0 enables the output clock TVTCn to be gapped during the four overhead byte times. A 1 enables the clock to be symmetrical. Except for bits 1 and 2 in the K4 byte, the remaining bits in the four overhead bytes are ignored.</td></tr>
<tr><td>0</td><td>TnDISB</td><td>Transmit Single Bit RDI Enable: A 1 configures the A and B add sides for channel n for single bit RDI operation. A 0 configured add channel for three bit RDI.</td></tr>
</table>

Address	Bit	Symbol	Description
X+008	7-5		**Not used:**
	4	RnVTVC	**Receive VT/TU Overhead Byte Selection:** Enabled with the VT/TU receive line interface is selected. A 0 causes the output clock RVTCn to be gapped during the four overhead byte times. A 1 causes the clock to be symmetrical, and enables the four overhead bytes to be clocked out of the mapper.
	3	RnDIEN	**Remote Defect Indication Enable:** When this bit is set to 1, alarms detected in the A or B drop side VT/TU selected are enabled to send three bit RDI (remote payload, server or connectivity defect indication) or single bit RDI. The alarms for causing RDI are described in the operations section. Note: The microprocessor may send an RDI independent of the setting of this control bit. To prevent contention between the internal logic and microprocessor control, this bit should be written with a 0.
	2	TCnRE	**Tandem Connection RDI/ODI Enable:** When this bit is set to 1, alarms detected in the A or B drop side VT/TU selected are enabled to send Tandem Connection RDI and ODI. The alarms for causing TC RDI and ODI are described in the operations section. Note: The microprocessor may send an TC RDI (bit 8 in frame 73) or ODI (bit 7 in frame 74) independent of the setting of this control bit. To prevent contention between the internal logic and microprocessor control, this bit should be written with a 0.
	1	RnAISE	**Receive Line AIS Enable:** When this bit is set to 1, alarms detected in the A or B drop side VT/TU selected are enabled to send receive DS1 or E1 line AIS. The alarms for causing received AIS to be sent are described in the operations section. Note: The microprocessor may send line AIS independent of the setting of this control bit. To prevent contention between the internal logic and microprocessor control, this bit should be written with a 0.
	0	RnSAIS	**Receive Line Interface Send AIS:** A 1 forces either a DS1 or E1 line AIS signal to be sent in the receive direction independent of the drop side alarms for the VT/TU selected.
X+009	7-1		**Not used:**
	0	TnRESET	**Transmit Reset:** A 1 clears all performance counters to zero (saturating) or the FE/FFFE hex values (8/16 bit non-saturating), and initializes the internal FIFOs and state machines for the A and B add bus VT/TU channel selected.

CHANNEL n A SIDE ADD AND DROP BUS CONTROL REGISTER DESCRIPTIONS (n = 1 to 28)

The following control bits and registers are for the A side drop and add buses. Control bits TnSEL1, TnSEL0 and RnSEL determine the drop bus that the data is dropped from, and the add bus(es) data will be added to. The drop side is the receive side, while the add side is the transmit side.

Address	Bit	Symbol	Description
X+010	7-6		**Not used:**
	5	ARnTCEN	**A Side Drop Bus Channel n Tandem Connection Enable:** A 1 enables the A side drop bus Tandem Connection feature for the VT/TU selected for channel n. A 0 disables the TC feature. Please note the Tandem Connection feature can only be enabled when the J2 byte is configured for a 16 byte message (control bit ARnJ2S1 is a 0).
	4-2	ARnSL1 ARnSL2 ARnSL3	**A Side Drop Bus Channel n Microprocessor Written Signal Label Value:** The bits written into this register are compared against the received signal for a mismatch signal label detector. The three bit positions correspond to the three signal label bits found in bits 5 through 7 in the V5 byte for the TU/VT selected. Bit 4 in this register corresponds to bit 5 in the V5 byte.
	1-0	ARnJ2S1 ARnJ2S0	**A Side Drop Bus Channel n J2 Byte Mode Selection:** The J2 byte is processed according to the settings in following table. Please note: the Tandem Connection feature for a channel is disabled with the J2 byte is configured for a message size of 64 bytes. ARnJ2S1 / ARnJ2S0 / Action 0 / 0 / The J2 memory map segment is configured for 16 byte messages. Received bytes are written into this segment on a rotating basis starting with an arbitrary address. The J2 message comparison circuit is disabled. 0 / 1 / The J2 memory map segment is configured for 16 byte messages. Received bytes are written into this segment aligned to the multi frame pattern. The J2 message comparison circuit is enabled. 1 / 0 / The J2 memory map segment is configured for 64 byte messages. Received bytes are written into this segment on a rotating basis starting with an arbitrary address. 1 / 1 / The J2 memory map segment is configured for 64 byte messages. Received bytes are written into this segment aligned to CR/LF sequence. The J2 message comparison circuit is disabled.
X+011	7-1		**Not used:**
	0	DACHnR	**A Side Drop Channel n Reset:** Writing a 1 to this control bit clears all performance counters to zero (saturating) or the FE/FFFE hex values (8/16 bit non-saturating), and initializes the internal FIFOs and state machines for the A drop bus VT/TU channel selected. It does not clear the control bit settings, or latched alarms for the channel selected.

Address	Bit	Symbol	Description
X+012	7-0	A Side Drop TU/VT Selection	**A Side Drop Channel n VT/TU Selection:** The eight-bit binary code written into this location selects the TU/VT that is to be dropped from the A side drop bus. Please refer to the operations section for the description for selecting a VT/TU for a STS-1 in the STS-3 format, and for a TUG-3 in the STM-1 VC-4 format.
X+01A	7-0	A Side Add Bus TU/VT Selection	**A Side Add Bus Channel n TU/VT Selection:** The eight-bit binary code written into this location selects the TU/VT that is to be added to the A side add bus. Please refer to the operations section for the description for selecting a VT/TU for a STS-1 in the STS-3 format, and for a TUG-3 in the STM-1 VC-4 format.
X+01B	7-0		**Reserved**
X+01C to X+05B	7-0	A Side Add J2 & N2 Byte Message Segments	**A Side Add Bus Channel n J2 and N2 Message Segments:** The following locations store the transmit 64-byte J2 message when control bit ATnJ2TSZ is a 1, and the transmit microprocessor-written 16-byte J2 message and 16 byte N2 message when this control bit ATnJ2TSZ is a 0. Location — Message Segment 01C-05B — Transmit J2 message segment (64 bytes). 01C-02B — Transmit J2 message segment (16 bytes). 02C-03B — Unused (16 bytes). 03C-04B — Transmit N2 message segment (16 bytes). 04C-05B — Unused (16 bytes).
X+05C	7-0	A Side Add Bus Test V1 Byte	**A Side Add Bus Channel n V1 Byte:** The value written to this location is transmitted as the V1 byte for the VT/TU selected for the A side add bus and when control bit ATnTPTV is a 1. Please note: the VT/TU is still sent with a fixed pointer offset. Bits 7-0 of the register correspond to bits 1-8 of the V1 byte.
X+05D	7-0	A Side Add Bus Test V2 Byte	**A Side Add Bus Channel n V2 Byte:** The value written to this location is transmitted as the V2 byte for the VT/TU selected for the A side add bus and when control bit ATnTPTV is a 1. Please note: the VT/TU is still sent with a fixed pointer offset. Bits 7-0 of the register correspond to bits 1-8 of the V2 byte.
X+05E	7-0	A Side Add Bus V4 Byte	**A Side Add Bus Channel n V4 Byte:** The value written to this location is transmitted as the V4 byte for the VT/TU selected for the A side add bus and when control bit ATnV4BS is a 1. When control bit ATnV4BS is a 0, the V4 byte is transmitted with a 0 value. Bits 7-0 of the register correspond to bits 1-8 of the V4 byte.
X+05F	7-0	A Side Add Bus O-bits	**A side Add Bus Channel n O Bits:** The value written to this location is transmitted as the O bits for the VT/TU selected for the A side add bus and when control bit TOBWZ is 0. Bits 7 through 4 correspond to bits 3 through 6 in the first justification control byte. Bits 3 through 0 correspond to bits 3 through 6 in the second justification control byte. When control bit TOBWZ is a 1, the O bits in all channels are transmitted with a value equal to 0.
X+060	7-0	A Side Add Bus V5 Byte	**A side Add Bus Channel n V5 Byte:** The value written to this location is transmitted as the V5 byte for the VT/TU selected for the A side add bus and when control bit ATnV5BS (bit 0, register X+064H) is 1. When control bit ATnV5BS is set to 0, a normal V5 byte is transmitted. Bits 7-0 of the register correspond to bits 1-8 of the V5 byte.

Address	Bit	Symbol	Description
X+061	7-0	A Side Add Bus N2 Byte	**A side Add Bus Channel n N2 byte:** The value written to this location is transmitted as the N2 byte for the VT/TU selected for the A side add bus and when control bit ATnTCEN (bit 2, register X+063H) is 0. Bits 7-0 of the register correspond to bits 1-8 of the N2 byte.
X+062	7-0	A Side Add Bus K4 Byte	**A Side Add Bus Channel n K4 Byte:** The value written to this location is transmitted as the K4 byte for the VT/TU selected for the A side add bus and when control bit ATnK4PC (bit 1, register 065H) is 1. When control bit ATnK4PC is set to 0, the bits transmitted from this register are a function of the RDI and line interface options. When the three bit RDI feature is enabled, the values in bits 5, 6, and 7 are ignored. When the single bit RDI feature is enabled, bits 5, 6, and 7 from this register are transmitted. When the VT symmetrical clock interface is enabled, bits 1 and 2 in this register are ignored. Bits 3, 4, and 8 are always transmitted from this register. Bits 7-0 of the register correspond to bits 1-8 of the K4 byte.
X+063	7	ATnTCAIS	**A Side Add Bus Channel n Transmit Tandem Connection AIS:** Enabled when control bit ATnTCEN is a 1. A 1 causes bit 4 in the N2 byte to be transmitted as a 1.
	6	ATnGAIS	**A Side Add Bus Channel n Transmit VT/TU AIS:** A 1 enables a TU/VT AIS to be transmitted for the TU/VT selected for the A side add bus. A TU/VT AIS consists of all ones in the entire TU/VT, including the V1 through V4 bytes.
	5	ATnTPTV	**A Side Add Bus Channel n Transmit VT/TU V1/V2 Test Pointer Bytes:** A 1 enables the test pointer value written to registers X+05CH (V1 byte) and X+05DH (V2 byte) by the microprocessor to be transmitted. Please note that the pointer offset for the overhead bytes (e.g., V5 byte) and the payload will remain fixed.

Address	Bit	Symbol	Description
X+063 (cont.)	4	AnUQGE	**A Side Add Bus Channel n Unequipped Channel Generation:** This control bit works in conjunction with the AnUQSU control bit according to the following table: AnUQGE / AnUQSU / Action 0 / X / Normal Operation. 1 / 0 / Unequipped TU/VT generated. An unequipped VT/TU consists of a normal NDF, size bits equal to 10 (VT2/TU-12) or 11 (VT1.5/TU-11), a fixed pointer equal to 105 (VT2/TU-12) or 78 (VT1.5/TU-11), and all other bytes equal to 00H. 1 / 1 / Unequipped supervisory VT/TU generated. An unequipped supervisory TU/VT consists of a normal NDF, size bits equal to 10 (VT2/TU-12) or 11 (VT1.5/TU-11), a fixed pointer equal to 105 (VT2/TU-12) or 78 (VT1.5/TU-11), and a valid J2 byte. The V5 byte will consist of a valid BIP-2, signal label set to 0. The N2 byte will be sent as zero. The RDI bits, V5 bit 8 and K4 bits 5, 6 and 7 will be controlled by the microprocessor and the payload will set to zeros. Note: X = don't care (0 or 1).
	3	AnUQSU	**A Side Add Bus Channel n Unequipped Supervisory Channel Enabled:** Works in conjunction with the AnUQGE control bit according to the table given above.
	2	ATnTCEN	**A Side Add Bus Channel n Tandem Connection Enable:** Works in conjunction with the ATnJ2TSZ bit according to the following table: ATnTCEN / ATnJ2TSZ / Action 0 / X / Tandem Connection feature is disabled. The N2 byte transmitted is the microprocessor written value at register X+061H. 1 / 0 / Tandem Connection feature is enabled. The J2 64 byte message RAM segment is used on a shared basis. The Transmit J2 message and N2 byte are configured for 16-byte message sizes. 1 / 1 / The J2 message segment is configured for a 64 message size. The single byte microprocessor written value is repeated and transmitted 16 times along with the multiframe alignment pattern, and TC ODI and TC RDI. Note: X = don't care (0 or 1).

Address	Bit	Symbol	Description
X+063 (cont.)	1	ATnJ2TEN	**A Side Add Bus Channel n Transmit J2 Message Type:** Works in conjunction with the ATnJ2TSZ bit according to the following table: ATnJ2TEN ATnJ2TSZ Action 0 0 Transmit J2 message segment configured for a 16-byte message size. 0 1 Transmit J2 message segment configured for a 64-byte message size. 1 X J2 message segment transmitted as 00H. Note: X = don't care (0 or 1).
	0	ATnJ2TSZ	**A Side Add Bus Channel n Transmit J2 Message Size Segment:** Works in conjunction with the ATnJ2TEN bit according to the table described above.
X+064	7	ATnRFI	**A Side Add Bus Channel n Transmit RFI (Remote Failure Indication):** A 1 causes the RFI bit (bit 4 in the V5 byte) to be transmitted as a 1. A 0 transmits this bit as a 0.
	6	ATnRDIP	**A Side Add Bus Channel n Transmit Remote Payload Defect Indication:** Enabled only for three bit RDI operation (control bit TnDISB is set to 0). A 1 transmits a remote payload defect indication (bits 5, 6, and 7 in the K4 byte equals 010, and bit 8 in the V5 equals 0) independent of the alarms.
	5	ATnRDIC	**A Side Add Bus Channel n Transmit Remote Connectivity Defect Indication:** Enabled only for three bit RDI operation (control bit TnDISB is set to 0). A 1 transmits a remote connectivity defect indication (bits 5, 6, and 7 in the K4 byte equals 110, and bit 8 in the V5 equals 1) independent of the alarms.
	4	ATnRDIS	**A Side Add Bus Channel n Transmit Remote Server Defect Indication or Single Bit RDI:** For three bit RDI operation (control bit TnDISB is set to 0), a 1 transmits a remote server defect indication (bits 5, 6, and 7 in the K4 byte equals 101, and bit 8 in the V5 equals 1) independent of the alarms. For single bit RDI operation, a 1 transmit a remote defect indication (bit 8 in the V5 equals 1).
	3	ATnFB2	**A Side Add Bus Channel n Transmit BIP-2 Error:** A 1 causes bits 1 and 2 (the BIP-2 value) in the V5 byte to be inverted from the calculated value and transmitted for one frame. To send another error, this bit must be written with a 0 followed by a 1.
	2	ATnTCUQ	**A Side Add Bus Channel n Transmit TC Unequipped Status:** Enabled when control bit ATnTCEN is a 1. A 1 causes bits a TC unequipped byte to be transmitted.
	1		**Not used:**
	0	ATnV5BS	**A Side Add Bus Channel n Transmit V5 Byte Register Value:** A 1 enables the microprocessor written V5 byte value at register X+060H to be transmitted.

Address	Bit	Symbol	Description
X+065	7		**Not used:**
	6	ATnFFB	**A Side Add Bus Channel n Transmit REI Error:** A 1 causes bit 3 (REI) of the V5 byte to be transmitted as a 1 for one multiframe. To send another error, this bit must be written with a 0 followed by a 1. Please note that if a FEBE is being sent as a result of a receive BIP-2 error, the REI error set by this bit is transmitted afterwards.
	5 4 3	ATnSL1 ATnSL2 ATnSL3	**A Side Add Bus Channel n Transmit Microprocessor Written Signal Label Value:** The value written into this field is sent as the signal label in the V5 byte. The three bit positions correspond to the three signal label bits found in bits 5 through 7 in the V5 byte for the TU/VT selected. Bit 5 in this register corresponds to bit 5 in the V5 byte.
	2		**Not used:**
	1	ATnK4PC	**A Side Add Bus Channel n Transmit K4 Byte Register Value:** A 1 enables the microprocessor written value for the K4 byte to be transmitted. When set to 0, 3-bit RDI controls bits 5 - 7 when enabled, and the VT interface controls bits 1 and 2 when enabled and the symmetrical clock output is selected. Otherwise these bits are sourced from the microprocesor written value. Bits 3, 4, 8 are always sourced from the microprocessor written value.
	0	AnHIGHZ	**A Side Add Bus Channel n Force High Impedance for the VT/TU selected:** A 1 forces the time slots corresponding to the VT/TU selected to the high impedance state.
X+066	7-3		**Not used:**
	2	ATnTCSO	**A Side Add Bus Channel n Transmit Tandem Connection ODI:** Enabled when control bit ATnTCEN is a 1. A 1 causes bit 7 in frame 74 in the N2 byte to be transmitted as a 1 independent of TC alarms.
	1	ATnTCSR	**A Side Add Bus Channel n Transmit Tandem Connection RDI:** Enabled when control bit ATnTCEN is a 1. A 1 causes bit 8 in frame 73 in the N2 byte to be transmitted as a 1 independent of TC alarms.
	0	ATnV4BS	**A Side Add Bus Channel n Transmit V4 Byte Register Value:** A 1 enables the microprocessor written value for the V4 byte to be transmitted. When set to 0, the transmitted V4 byte value is 00H.

CHANNEL n - A SIDE DESYNCHRONIZER REGISTER DESCRIPTION (n = 1 to 28)

Address	Bit	Symbol	Description
X+017	7-0	A Drop Pointer Leak Rate Value (Bit 7-0)	**A Side Drop Bus Channel n Desynchronizer Pointer Leak Rate Register Bits 7-0:** This register contains the first 8 bits in a 10 bit pointer leak register. The value written into this location and the next location is used for the internal leak rate buffer, and represents the average leak rate based on a count. A count of one represents 8 frames, or 2 multiframes, between bits leaked. Bit 0 is the LSB. Note: If the 10 bit register is set to 0 the pointer leak buffer in the Desynchronizer is bypassed. The following alarms will cause the contents of locations X+017H and X+018H to be reset to their default values: AnLOP, AnAIS, A1UAIS, A2UAIS, A3UAIS or A1HLOM, A2HLOM, or A3HLOM. Following these alarms, 3 rising edges of PM1S are required before X+017H and X+018H can be written to.
X+018	7-2		**Not used:**
	1-0	A Drop Pointer Leak Rate Value (Bits 9-8)	**A Side Drop Bus Channel n Desynchronizer Pointer Leak Rate Register Bits 9-8:** This register contains the last two bits in a 10 bit pointer leak register. The value written into this location along with the register is used for the internal leak rate buffer, and represents the average leak rate based on a count. A count of one represents 8 frames, or 2 multiframes, between bits leaked. Bit 9 is the MSB. Note: If the 10 bit register is set to 0 the pointer leak buffer in the Desynchronizer is bypassed.

CHANNEL n - B SIDE ADD AND DROP BUS CONTROL REGISTER DESCRIPTIONS (n = 1 to 28)

The following control bits and registers are for the A side drop and add buses. Control bits TnSEL1, TnSEL0 and RnSEL determine the drop bus that the data is dropped from, and the add bus(es) data will be added to. The drop side is the receive side, while the add side is the transmit side.

Address	Bit	Symbol	Description
X+080	7-6		**Not used:**
	5	BRnTCEN	**B Side Drop Bus Channel n Tandem Connection Enable:** A 1 enables the B side drop bus Tandem Connection feature for the VT/TU selected for channel n. A 0 disables the TC feature. Please note the Tandem Connection feature can only be enabled when the J2 byte is configured for a 16 byte message.
	4-2	BRnSL1 BRnSL2 BRnSL3	**B Side Drop Bus Channel n Microprocessor Written Signal Label Value:** The bits written into this register are compared against the received signal for a mismatch signal label detector. The three bit positions correspond to the three signal label bits found in bits 5 through 7 in the V5 byte for the TU/VT selected. Bit 4 in this register corresponds to bit 5 in the V5 byte.
	1-0	BRnJ2S1 BRnJ2S0	**B Side Drop Bus Channel n J2 Byte Mode Selection:** The J2 byte is processed according to the settings in following table. Please note: the Tandem Connection feature for a channel is disabled with the J2 byte is configured for a message size of 64 bytes. BRnJ2S1 / BRnJ2S0 / Action 0 / 0 / The J2 memory map segment is configured for 16 byte messages. Received bytes are written into this segment on a rotating basis starting with an arbitrary address. The J2 message comparison circuit is disabled. 0 / 1 / The J2 memory map segment is configured for 16 byte messages. Received bytes are written into this segment aligned to the multi frame pattern. The J2 message comparison circuit is enabled. 1 / 0 / The J2 memory map segment is configured for 64 byte messages. Received bytes are written into this segment on a rotating basis starting with an arbitrary address. 1 / 1 / The J2 memory map segment is configured for 64 byte messages. Received bytes are written into this segment aligned to CR/LF sequence. The J2 message comparison circuit is disabled.
X+081	7-1		**Not used:**
	0	DBCHnR	**B Side Drop Channel n Reset:** Writing a 1 to this control bit clears all performance counters to zero (saturating) or the FE/FFFE hex values (8/16 bit non-saturating), and initializes the internal FIFOs and state machines for the B drop bus VT/TU channel selected. It does not clear the control bit settings, or latched alarms for the channel selected.

Address	Bit	Symbol	Description
X+082	7-0	B Side Drop TU/VT Selection	**B Side Drop Channel n VT/TU Selection:** The eight-bit binary code written into this location selects the TU/VT that is to be dropped from the B side drop bus. Please refer to the operations section for the description for selecting a VT/TU for a STS-1 in the STS-3 format, and for a TUG-3 in the STM-1 VC-4 format.
X+08A	7-0	B Side Add Bus TU/VT Selection	**B Side Add Bus Channel n TU/VT Selection:** The eight-bit binary code written into this location selects the TU/VT that is to be added to the B side add bus. Please refer to the operations section for the description for selecting a VT/TU for a STS-1 in the STS-3 format, and for a TUG-3 in the STM-1 VC-4 format.
X+08B	7-0		**Reserved**
X+08C to X+0CB	7-0	B Side Add J2 & N2 Byte Message Segments	**B Side Add Bus Channel n J2 and N2 Message Segments:** The following locations store the transmit 64-byte J2 message when control bit BTnJ2TSZ is a 1, and the transmit microprocessor-written 16-byte J2 message and 16 byte N2 message when this control bit BTnJ2TSZ is a 0. Location — Message Segment 08C-0CB — Transmit J2 message segment (64 bytes). 08C-09B — Transmit J2 message segment (16 bytes). 09C-0AB — Unused (16 bytes). 0AC-0BB — Transmit N2 message segment (16 bytes). 0BC-0CB — Unused (16 bytes).
X+0CC	7-0	B Side Add Bus Test V1 Byte	**B Side Add Bus Channel n V1 Byte:** The value written to this location is transmitted as the V1 byte for the VT/TU selected for the B side add bus and when control bit BTnTPTV is a 1. Please note: the VT/TU is still sent with a fixed pointer offset. Bits 7-0 of the register correspond to bits 1-8 of the V1 byte.
X+0CD	7-0	B Side Add Bus Test V2 Byte	**B Side Add Bus Channel n V2 Byte:** The value written to this location is transmitted as the V2 byte for the VT/TU selected for the B side add bus and when control bit BTnTPTV is a 1. Please note: the VT/TU is still sent with a fixed pointer offset. Bits 7-0 of the register correspond to bits 1-8 of the V2 byte.
X+0CE	7-0	B Side Add Bus V4 Byte	**B Side Add Bus Channel n V4 Byte:** The value written to this location is transmitted as the V4 byte for the VT/TU selected for the B side add bus and when control bit BTnV4BS is a 1. When control bit BTnV4BS is a 0, the V4 byte is transmitted with a 0 value. Bits 7-0 of the register correspond to bits 1-8 of the V4 byte.
X+0CF	7-0	B Side Add Bus O-bits	**B side Add Bus Channel n O Bits:** The value written to this location is transmitted as the O bits for the VT/TU selected for the B side add bus and when control bit TOBWZ is 0. Bits 7 through 4 correspond to bits 3 through 6 in the first justification control byte. Bits 3 through 0 correspond to bits 3 through 6 in the second justification control byte. When control bit TOBWZ is a 1, the O bits in all channels are transmitted with a value equal to 0.
X+0D0	7-0	B Side Add Bus V5 Byte	**B side Add Bus Channel n V5 Byte:** The value written to this location is transmitted as the V5 byte for the VT/TU selected for the B side add bus and when control bit BTnV5BS (bit 0, register X+0D4H) is 1. When control bit BTnV5BS is set to 0, a normal V5 byte is transmitted. Bits 7-0 of the register correspond to bits 1-8 of the V5 byte.

Address	Bit	Symbol	Description
X+0D1	7-0	B Side Add Bus N2 Byte	**B side Add Bus Channel n N2 byte:** The value written to this location is transmitted as the N2 byte for the VT/TU selected for the B side add bus and when control bit ATnTCEN (bit 2, register X+0D3H) is 0. Bits 7-0 of the register correspond to bits 1-8 of the N2 byte.
X+0D2	7-0	B Side Add Bus K4 Byte	**B Side Add Bus Channel n K4 Byte:** The value written to this location is transmitted as the K4 byte for the VT/TU selected for the B side add bus and when control bit BTnK4PC (bit 1, register 0D5H) is 1. When control bit BTnK4PC is set to 0, the bits transmitted from this register are a function of the RDI and line interface options. When the three bit RDI feature is enabled, the value in bits 5, 6, and 7 are ignored. When the single bit RDI feature is enabled, bits 5, 6, and 7 from this register are transmitted. When the VT symmetrical clock interface is enabled, bits 1 and 2 in this register are ignored. Bits 3, 4, and 8 are always transmitted from this register. Bits 7-0 of the register correspond to bits 1-8 of the K4 byte.
X+0D3	7	BTnTCAIS	**B Side Add Bus Channel n Transmit Tandem Connection AIS:** Enabled when control bit BTnTCEN is a 1. A 1 causes bit 4 in the N2 byte to be transmitted as a 1.
	6	BTnGAIS	**B Side Add Bus Channel n Transmit VT/TU AIS:** A 1 enables a TU/VT AIS to be transmitted for the TU/VT selected for the B side add bus. A TU/VT AIS consists of all ones in the entire TU/VT, including the V1 through V4 bytes.
	5	BTnTPTV	**B Side Add Bus Channel n Transmit VT/TU V1/V2 Test Pointer Bytes:** A 1 enables the test pointer value written to registers X+0CCH (V1 byte) and X+0CDH (V2 byte) by the microprocessor to be transmitted. Please note that the pointer offset for the overhead bytes (e.g., V5 byte) and the payload will remain fixed.

Address	Bit	Symbol	Description
X+0D3 (cont.)	4	BnUQGE	**B Side Add Bus Channel n Unequipped Channel Generation:** This control bit works in conjunction with the BnUQSU control bit according to the following table: BnUQGE / BnUQSU / Action 0 / X / Normal Operation. 1 / 0 / Unequipped TU/VT generated. An unequipped VT/TU consists of a normal NDF, size bits equal to 10 (VT2/TU-12) or 11 (VT1.5/TU-11), a fixed pointer equal to 105 (VT2/TU-12) or 78 (VT1.5/TU-11), and all other bytes equal to 00H. 1 / 1 / Unequipped supervisory VT/TU generated. An unequipped supervisory TU/VT consists of a normal NDF, size bits equal to 10 (VT2/TU-12) or 11 (VT1.5/TU-11), a fixed pointer equal to 105 (VT2/TU-12) or 78 (VT1.5/TU-11), and a valid J2 byte. The V5 byte will consist of a valid BIP-2, signal label set to 0. The N2 byte will be sent as zero. The RDI bits, V5 bit 8 and K4 bits 5, 6 and 7 will be controlled by the microprocessor and the payload will set to zeros. Note: X = don't care (0 or 1).
	3	BnUQSU	**B Side Add Bus Channel n Unequipped Supervisory Channel Enabled:** Works in conjunction with the BnUQGE control bit according to the table given above.
	2	BTnTCEN	**B Side Add Bus Channel n Tandem Connection Enable:** Works in conjunction with the BTnJ2TSZ bit according to the following table: BTnTCEN / BTnJ2TSZ / Action 0 / X / Tandem Connection feature is disabled. The N2 byte transmitted is the microprocessor written value at register X+0D1H. 1 / 0 / Tandem Connection feature is enabled. The J2 64 byte message RAM segment is used on a shared basis. The Transmit J2 message and N2 byte are configured for 16-byte message sizes. 1 / 1 / The J2 message segment is configured for a 64 message size. The single byte microprocessor written value is repeated and transmitted 16 times along with the multiframe alignment pattern, and TC ODI and TC RDI. Note: X = don't care (0 or 1).

Address	Bit	Symbol	Description
X+0D3 (cont.)	1	BTnJ2TEN	**B Side Add Bus Channel n Transmit J2 Message Type:** Works in conjunction with the BTnJ2TSZ bit according to the following table: BTnJ2TEN BTnJ2TSZ Action 0 0 Transmit J2 message segment configured for a 16-byte message size. 0 1 Transmit J2 message segment configured for a 64-byte message size. 1 X J2 message segment transmitted as 00H. Note: X = don't care (0 or 1).
	0	BTnJ2TSZ	**B Side Add Bus Channel n Transmit J2 Message Size Segment:** Works in conjunction with the BTnJ2TEN bit according to the table described above.
X+0D4	7	BTnRFI	**B Side Add Bus Channel n Transmit RFI (Remote Failure Indication):** A 1 causes the RFI bit (bit 4 in the V5 byte) to be transmitted as a 1. A 0 transmits this bit as a 0.
	6	BTnRDIP	**B Side Add Bus Channel n Transmit Remote Payload Defect Indication:** Enabled only for three bit RDI operation (control bit TnDISB is set to 0). A 1 transmits a remote payload defect indication (bits 5, 6, and 7 in the K4 byte equals 010, and bit 8 in the V5 equals 0) independent of the alarms.
	5	BTnRDIC	**B Side Add Bus Channel n Transmit Remote Connectivity Defect Indication:** Enabled only for three bit RDI operation (control bit TnDISB is set to 0). A 1 transmits a remote connectivity defect indication (bits 5, 6, and 7 in the K4 byte equals 110, and bit 8 in the V5 equals 1) independent of the alarms.
	4	BTnRDIS	**B Side Add Bus Channel n Transmit Remote Server Defect Indication or Single Bit RDI:** For three bit RDI operation (control bit TnDISB is set to 0), a 1 transmits a remote server defect indication (bits 5, 6, and 7 in the K4 byte equals 101, and bit 8 in the V5 equals 1) independent of the alarms. For single bit RDI operation, a 1 transmit a remote defect indication (bit 8 in the V5 equals 1).
	3	BTnFB2	**B Side Add Bus Channel n Transmit BIP-2 Error:** A 1 causes bits 1 and 2 (the BIP-2 value) in the V5 byte to be inverted from the calculated value and transmitted for one frame. To send another error, this bit must be written with a 0 followed by a 1.
	2	BTnTCUQ	**B Side Add Bus Channel n Transmit TC Unequipped Status:** Enabled when control bit BTnTCEN is a 1. A 1 causes bits a TC unequipped byte to be transmitted.
	1		**Not used:**
	0	BTnV5BS	**B Side Add Bus Channel n Transmit V5 Byte Register Value:** A 1 enables the microprocessor written V5 byte value at register X+0D0H to be transmitted.

Address	Bit	Symbol	Description
X+0D5	7		**Not used:**
	6	BTnFFB	**B Side Add Bus Channel n Transmit REI Error:** A 1 causes bit 3 (REI) of the V5 byte to be transmitted as a 1 for one multiframe. To send another error, this bit must be written with a 0 followed by a 1. Please note that if a REI count is being sent as a result of a receive BIP-2 error, the REI error set by this bit is transmitted afterwards.
	5 4 3	BTnSL1 BTnSL2 BTnSL3	**B Side Add Bus Channel n Transmit Microprocessor Written Signal Label Value:** The value written into this field is sent as the signal label in the V5 byte. The three bit positions correspond to the three signal label bits found in bits 5 through 7 in the V5 byte for the TU/VT selected. Bit 5 in this register corresponds to bit 5 in the V5 byte.
	2		**Not used:**
	1	BTnK4PC	**B Side Add Bus Channel n Transmit K4 Byte Register Value:** A 1 enables the microprocessor written value for the K4 byte to be transmitted. When set to 0, 3-bit RDI controls bits 5 - 7 when enabled, and the VT interface controls bits 1 and 2 when enabled and the symmetrical clock output is selected. Otherwise, these bits are sourced from the microprocessor written value. Bits 3, 4 and 8 are always sourced from the microprocessor written value.
	0	BnHIGHZ	**B Side Add Bus Channel n Force High Impedance for the VT/TU selected.** A 1 forces the time slots corresponding to the VT/TU selected to the high impedance state.
X+0D6	7-3		**Not used:**
	2	BTnTCSO	**B Side Add Bus Channel n Transmit Tandem Connection ODI:** Enabled when control bit BTnTCEN is a 1. A 1 causes bit 7 in frame 74 in the N2 byte to be transmitted as a 1 independent of TC alarms.
	1	BTnTCSR	**B Side Add Bus Channel n Transmit Tandem Connection RDI:** Enabled when control bit BTnTCEN is a 1. A 1 causes bit 8 in frame 73 in the N2 byte to be transmitted as a 1 independent of TC alarms.
	0	BTnV4BS	**B Side Add Bus Channel n Transmit V4 Byte Register Value:** A 1 enables the microprocessor written value for the V4 byte to be transmitted. When set to 0, the transmitted V4 byte value is 00H.

CHANNEL n - B SIDE DESYNCHRONIZER REGISTER DESCRIPTION (n = 1 to 28)

Address	Bit	Symbol	Description
X+087	7-0	B Drop Pointer Leak Rate Value (Bit 7-0)	**B Side Drop Bus Channel n Desynchronizer Pointer Leak Rate Register Bits 7-0:** This register contains the first 8 bits in a 10 bit pointer leak register. The value written into this location and the next location is used for the internal leak rate buffer, and represents the average leak rate based on a count. A count of one represents 8 frames, or 2 multiframes, between bits leaked. Bit 0 is the LSB. Note: If the 10 bit register is set to 0 the pointer leak buffer in the Desynchronizer is bypassed. The following alarms will cause the contents of locations X+087H and X+088H to be reset to their default values: BnLOP, BnAIS, B1UAIS, B2UAIS, B3UAIS or B1HLOM, B2HLOM, or B3HLOM. Following these alarms, 3 rising edges of PM1S are required before X+087H and X+088H can be written to.
X+088	7-2		**Not used:**
	1-0	B Drop Pointer Leak Rate Value (Bits 9-8)	**B Side Drop Bus Channel n Desynchronizer Pointer Leak Rate Register Bits 9-8:** This register contains the last two bits in a 10 bit pointer leak register. The value written into this location along with the register is used for the internal leak rate buffer, and represents the average leak rate based on a count. A count of one represents 8 frames, or 2 multiframes, between bits leaked. Bit 9 is the MSB. Note: If the 10 bit register is set to 0 the pointer leak buffer in the Desynchronizer is bypassed.

CHANNEL n - A AND B SIDE ADD BUS ALARM MASK BITS (n = 1 to 28)

Address	Bit	Symbol	Description
X+005	7-6		**Not used:**
	5	MnTAIS	**Transmit Channel n Line AIS Alarm Mask Bit:** A 1 enables the hardware interrupt for a Line AIS for channel n.
	4	MnBTFE	**Transmit B Side Add Bus Channel n FIFO Error Indication Mask Bit:** A 1 enables the hardware interrupt for a B side FIFO error indication for channel n.
	3	MnATFE	**Transmit A Side Add Bus Channel n FIFO Error Indication Mask Bit:** A 1 enables the hardware interrupt for a A side FIFO error indication for channel n.
	2	MnOOL	**Channel n Test Analyzer Out Of Lock Alarm Mask Bit:** A 1 enables the hardware interrupt for a test analyzer out of lock alarm for channel n.
	1	MnTLOS	**Transmit Channel n Loss Of Signal Alarm Mask Bit:** A 1 enables the hardware interrupt for a transmit loss of signal alarm for channel n.
	0	MnTLOC	**Transmit Channel n Loss Of Clock Alarm mask Bit:** A 1 enables the hardware interrupt for a transmit loss of clock alarm for channel n.

CHANNEL n - A AND B SIDE ADD BUS STATUS REGISTER AND COUNTER DESCRIPTIONS

The following descriptions pertain to the status registers and counters assigned to channel n. The status registers provide four readable bit positions per alarm. The alarm status are provided as unlatched alarm indications, latched alarm indications, one second indications, and previous one second indications. The counters provide three readable counters per counter. The counters are provided as current count, previous second bit (in the preceding even-numbered address) provides the alarm status as an latched alarm indication. A latched bit position is set on positive, negative, or both positive and negative transitions of the alarm. A latched alarm is cleared on a microprocessor read cycle of its address. During a read cycle for a counter, internal logic holds any increment to the counter until the read cycle is complete, and then updates the counter afterwards.

Address	Bit	Symbol	Description
X+100	7-6		**Not used:**
	5	TnAIS	**Transmit Channel n Line AIS Alarm Indication:** Line AIS is defined as an unframed all ones signal. A 1 indicates that line AIS has been detected. A DS1 AIS is declared when 99.9% or more ones are detected in the signal in a period of 48 ms. Recovery occurs when the line signal ANSI has fewer then 99.9% of ones in a 48 ms period. For the E1 line rate, AIS is declared when line signal has two or less zeros in each of two consecutive double frame periods (four frames). Recovery occurs when each of the two consecutive double frame periods contain three or more zeros. Other than reporting the alarm, no action is taken. Other than reporting the alarm, no action is taken.
	4	TBnFFE	**Transmit B Add Bus Channel n FIFO Error Indication:** A 1 indicates that the B Add bus FIFO has overflowed or underflowed. The FIFO is recentered and is held reset for up to two multiframes automatically. VT/TU AIS is transmitted for the VT/TU and bus selected for up to two multiframes when a FIFO error occurs.
	3	TAnFFE	**Transmit A Add Bus Channel n FIFO Error Indication:** A 1 indicates that the A Add bus FIFO has overflowed or underflowed. The FIFO is recentered and is held reset for up to two multiframes automatically. VT/TU AIS is transmitted for the VT/TU and bus selected for up to two multiframes when a FIFO error occurs.
	2	CnOOL	**Channel n Test Analyzer Out Of Lock Alarm:** Enabled when control bit TnANZ is a 1. An analyzer out of lock is declared when there is a mismatch in the PRBS pattern Recovery occurs when: The data is in lock for 25 clock cycles for the $2^{15}+1$ PRBS pattern. The data is in lock for 32 clock cycles for the $2^{20}+1$ PRBS pattern.

Address	Bit	Symbol	Description
X+100 (cont.)	1	TnLOS	**Transmit Channel n Loss Of Signal Alarm:** The loss of signal detector is enabled for the rail interface only. A DS1 Loss Of Signal is declared when there are no signal transitions detected on the positive rail and the negative rail for a period of 175 +/- 75 consecutive pulse positions. Recovery occurs when the average pulse density of at least 12.5% occurs over a period of 175 +/- 75 consecutive pulse positions. A Loss Of Signal alarm for the E1 line rate alarm is declared when there are no signal transitions detected on the positive rail and the negative rail for a period of 256 consecutive pulse positions. Recovery occurs when there are at least 32 transitions counted for 256 consecutive pulse positions. When the NRZ interface is selected, a external loss of signal may be inputted using the negative rail lead when control bit EXnLOS is a 1. The input sense is determined by control bit EXnLOSP. When control bit EXnLOSP is a 1, the loss of signal indication should be active high.
	0	TnLOC	**Transmit Channel n Loss Of Clock Alarm:** A 1 indicates that the transmit clock (TCIn) for port n has stuck high or low for 6 or more clock cycles. Recovery occurs on the first clock transition.
X+101	7-6		**Not used:**
	5	LTnAIS	**Transmit Channel n Line AIS Latched Alarm Indication:** This bit position latches for a transmit line AIS alarm indication. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	4	LTBnFFE	**Transmit Channel n B Side Add Bus FIFO Latched Alarm Indication:** This bit position latches for a transmit B side Add Bus FIFO alarm indication. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	3	LTAnFFE	**Transmit Channel n A Side Add Bus FIFO Latched Alarm Indication:** This bit position latches for a transmit A side Add Bus FIFO alarm indication. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	2	LCnOOL	**Channel n Test Analyzer Out Of Lock Latched Alarm:** This bit position latches for a PRBS analyzer out of lock alarm indication. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle. Note that the only resets which operate on this bit are the RESET lead and the software reset (RESETH).
	1	LTnLOS	**Transmit Channel n Loss Of Signal Latched Alarm Indication:** This bit position latches for a transmit loss of signal alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	0	LTnLOC	**Transmit Channel n Loss Of Clock Latched Alarm Indication:** This bit position latches for a transmit loss of clock alarm indication. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.

Address	Bit	Symbol	Description
X+103	7-6		**Not used:**
	5	PTnAIS	**Transmit Channel n Line AIS One Second Alarm Indication:** This bit position is set when the transmit AIS alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	4	PTBnFFE	**Transmit Channel n B Side Add Bus FIFO One Second Alarm Indication:** This bit position is set when the transmit B side Add Bus FIFO alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	3	PTAnFFE	**Transmit Channel n A Side Add Bus FIFO One Second Alarm Indication:** This bit position is set when the transmit A side Add Bus FIFO alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	2	PCnOOL	**Channel n Test Analyzer Out Of Lock One Second Alarm:** This bit position is set when the PRBS Test Analyzer out of lock alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	1	PTnLOS	**Transmit Channel n Loss Of Signal One Second Alarm Indication:** This bit position is set when the transmit loss of signal alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	0	PTnLOC	**Transmit Channel n Loss Of Clock One Second Alarm Indication:** This bit position is set when the transmit loss of clock alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.

Address	Bit	Symbol	Description
X+104	7-6		**Not used:**
	5	FTnAIS	**Transmit Channel n Line AIS Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the transmit line AIS alarm indication is active, but did not become active in the previous one second interval.
	4	FTBnFFE	**Transmit Channel n B Side Add Bus FIFO Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the transmit B side add bus FIFO alarm indication is active, but did not become active in the previous one second interval.
	3	FTAnFFE	**Transmit Channel n A Side Add Bus FIFO Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the transmit A side add bus FIFO alarm indication is active, but did not become active in the previous one second interval.
	2	FCnOOL	**Channel n Test Analyzer Out Of Lock Persistent One Second Alarm:** This bit position is set to 1 for the one-second interval, when the PRBS test analyzer out of lock alarm indication is active, but did not become active in the previous one second interval.
	1	FTnLOS	**Transmit Channel n Loss Of Signal Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the transmit loss of clock alarm indication is active, but did not become active in the previous one second interval.
	0	FTnLOC	**Transmit Channel n Loss Of Clock Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the transmit loss of clock alarm indication is active, but did not become active in the previous one second interval.
X+105	7-0	Transmit Coding Violation Counter (7-0)	**Transmit Channel n Coding Violation Counter - Low Order Byte:** Low order byte of a 16-bit counter which counts the number of coding errors that have occurred in the DS1 B8ZS or E1 HDB3 line code. This low order byte must be read before the high order byte for the same channel is read, which is located in the following address.
X+106	7-0	Transmit Coding Violation Counter (15-8)	**Transmit Channel n Coding Violation Counter - High order Byte:** High order byte of an 16 counter which counts the number of coding errors that have occurred in the DS1 B8ZS or E1 HDB3 line codes. This high order byte must be read after the low order byte for the same channel, which is located in the preceding address, but before the next read of the low order byte for any channel.
X+107	7-0	Transmit Coding Violation Previous 1 second Counter (7-0)	**Transmit Channel n Previous One Second Coding Violation Counter - Low Order Byte:** This counter holds the lower 8 bits of a 16 bit counter for coding violation counts that occurred in the previous one second interval. This location is updated from the Coding Violation counter at one second intervals.

Address	Bit	Symbol	Description
X+108	7-0	Transmit Coding Violation Previous 1 second Counter (15-8)	**Transmit Channel n Previous One Second Coding Violation Counter - High Order Byte:** This counter holds the higher 8 bits of a 16 bit counter for coding violation counts that occurred in the previous one second interval. This location is updated from the coding violation counter at one second intervals.
X+109	7-0	Transmit Coding Violation Current 1 second Counter (7-0)	**Transmit Channel n Current One Second Coding Violation Counter - Low Order Byte:** This counter holds the lower 8 bits of a 16 bit counter for coding violation counts that occurred in the current one second interval. This location is updated from the coding violation counter at one second intervals.
X+10A	7-0	Transmit Coding Violation Current 1 second Counter (15-8)	**Transmit Channel n Current One Second Coding Violation Counter - High Order Byte:** This counter holds the higher 8 bits of a 16 bit counter for coding violation counts that occurred in the current one second interval. This location is updated from the coding violation counter at one second intervals.

CHANNEL n - A SIDE DROP BUS ALARM MASK BITS (n = 1 to 28)

Address	Bit	Symbol	Description
X+013	7		**Not used:**
	6	MAnVAIS	**A Side Drop Bus Channel n VC AIS Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a A side Drop bus VC AIS latched bit alarm indication for channel n.
	5	MAnUQE	**A Side Drop Bus Channel n Unequipped Indication Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a A side unequipped latched bit alarm indication for channel n.
	4	MAnRDIC	**A Side Drop Bus Channel n Remote Connectivity Defect Indication Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a A side remote connectivity defect latched bit alarm indication for channel n.
	3	MAnRDIP	**A Side Drop Bus Channel n Remote Payload Defect Indication Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a A side remote payload defect latched bit alarm indication for channel n.

Address	Bit	Symbol	Description
X+013 (cont.)	2	MAnRDIS	**A Side Drop Bus Channel n Remote Server Defect Indication or Single Bit RDI Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a A side remote server defect or single bit RDI latched bit alarm indication for channel n.
	1	MAnSLER	**A Side Drop Bus Channel n Signal Label Mismatch Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a A side signal label alarm latched bit alarm indication for channel n.
	0	MAnRFI	**A Side Drop Bus Channel n Remote Failure Indication Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a A side remote failure indication alarm for channel n.
X+014	7-5		**Not used:**
	4	MAnRFE	**A Side Drop Bus Channel n FIFO Error Indication Mask Bit:** Setting this bit to 1 A 1 enables the hardware interrupt for a A side FIFO error indication latched bit alarm indication for channel n.
	3	MAnAIS	**A Side Drop Bus Channel n VT/TU AIS Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a A side VT/TU AIS alarm latched bit alarm indication for channel n.
	2	MAnLOP	**A Side Drop Bus Channel n VT/TU Loss Of Pointer Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a A side loss of pointer alarm latched bit alarm indication for channel n.
	1	MAnNDF	**A Side Drop Bus Channel n VT/TU New Data Flag Indication Indication Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a A side NDF latched bit indication for channel n.
	0	MAnSIZE	**A Side Drop Bus Channel n VT/TU Incorrect Pointer Size Indication Mask bit:** Setting this bit to 1 enables the hardware interrupt for a A side VT/TU incorrect pointer latched bit indication for channel n.
X+015	7-2		**Not used:**
	1	MAnJ2TIM	**A Side Drop Bus Channel n J2 Loss Of Lock Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a A side J2 loss of lock alarm latched bit indication for channel n.
	0	MAnJ2LOL	**A Side Drop Bus Channel n J2 Trail Trace Mismatch Alarm mask Bit:** Setting this bit to 1 enables the hardware interrupt for a A side J2 mismatch alarm latched bit indication for channel n.
X+016	7	MAnTCLM	**A Side Drop Bus Channel n Tandem Connection Loss Of Multiframe Alarm mask Bit:** Setting this bit to 1 enables the hardware interrupt for a A side TC loss of multiframe alarm latched bit indication for channel n.
	6	MAnTCLL	**A Side Drop Bus Channel n Tandem Connection Loss Of Lock Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a A side TC loss of lock alarm latched bit indication for channel n.
	5	MAnTCTM	**A Side Drop Bus Channel n Tandem Connection Trail Trace Message Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a A side TC mismatch alarm latched bit indication for channel n.

Address	Bit	Symbol	Description
X+016 (cont.)	4	MAnTCAIS	**A Side Drop Bus Channel n Tandem Connection AIS Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a A side TC AIS alarm latched bit indication for channel n.
	3	MAnTCUQ	**A Side Drop Bus Channel n Tandem Connection Unequipped Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a A side TC unequipped alarm latched bit indication for channel n.
	2	MAnT-CRDI	**A Side Drop Bus Port n Tandem Connection RDI Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a A side TC RDI alarm latched bit indication for channel n.
	1	MAnT-CODI	**A Side Drop Bus Channel n Tandem Connection ODI Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a A side TC ODI alarm latched bit indication for channel n.
	0		**Not used:**

CHANNEL n - A SIDE DROP STATUS REGISTER DESCRIPTIONS (n = 1 to 28)

The following descriptions pertain to the status registers assigned to channel n for the A side Drop Bus. The status registers provide four readable bit positions per alarm. The alarm status are provides as unlatched alarm indications, latched alarm indications, one second indications, and previous one second indications. The latched bit position is set on positive, negative, or both positive and negative transitions of the alarm. A latched alarm is cleared on a microprocessor read cycle of its address.

Address	Bit	Symbol	Description
X+110	7		**Not used:**
	6	AnVCAIS	**A Side Drop Bus Channel n VC AIS (Unlatched) Detected:** A VC AIS state is defined as a signal label equal to 111 (bits 5-7 in V5 byte). A 1 indicates that an VC AIS has been detected in the V5 signal label for the TU/VT selected for five or more consecutive received VC AIS signal labels. Recovery occurs when five or more consecutive signal labels are received not equal to 111.
	5	AnUNEQ	**A Side Drop Bus Channel n Unequipped Indication (Unlatched) Detected:** A 1 indicates that an unequipped status has been detected in the V5 signal label (Bits 5-7 in V5 byte are equal to 000) for the TU/VT selected for five or more consecutive received unequipped signal labels. Recovery occurs when five or more consecutive signal labels are received not equal to 000.
	4	AnRDIC	**A Side Drop Bus Channel n Remote Connectivity Defect Indication (Unlatched) Detected:** A 1 indicates that a remote connectivity defect alarm has been detected. The number of consecutive events used for detection and recovery is determined by control bit V5AL10.

Address	Bit	Symbol	Description
X+110 (cont.)	3	AnRDIP	**A Side Drop Bus Channel n Remote Payload Defect Indication (Unlatched) Detected:** A 1 indicates that a remote payload defect alarm has been detected. The number of consecutive events used for detection and recovery is determined by control bit V5AL10.
	2	AnRDIS	**A Side Drop Bus Channel n Remote Server Defect Indication or Single Bit RDI (Unlatched) Detected:** A 1 indicates that a remote server defect alarm or a single bit RDI state has been detected. The number of consecutive events used for detection and recovery is determined by control bit V5AL10.
	1	AnSLER	**A Side Drop Bus Channel n Signal Label Mismatch Detected (Unlatched):** A 1 indicates that the dropped signal label (Bits 5-7 in V5 byte) for the VT/TU selected does not match the microprocessor-written signal label for five or more consecutive events. Recovery occurs when five or more consecutive correct signal labels are detected.
	0	AnRFI	**A Side Drop Bus Channel n Remote Failure Indication Detected (Unlatched):** A 1 indicates that bit 4 in the V5 byte is equal to 1 for the VT/TU selected. The detection and recovery time is five consecutive multiframes.
X+111	7-5		**Not used:**
	4	AnRFFE	**A Side Drop Bus Channel n FIFO Error (Unlatched):** A 1 indicates that the receive FIFO in the desynchronizer for channel n has overflowed or underflowed for the VT/TU selected. The FIFO is reset automatically. Line AIS will be sent for two multiframes when enabled.
	3	AnAIS	**A Side Drop Bus Channel n VT/TU AIS Detected (Unlatched):** A 1 indicates that a AIS state has been detected in the V1/V2 pointer bytes for the VT/TU selected.
	2	AnLOP	**A Side Drop Bus Channel n VT/TU Loss Of Pointer Detected (Unlatched):** A 1 indicates that a loss of pointer (LOP) has been detected in the V1/V2 pointer bytes for the VT/TU selected.
	1	AnNDF	**A Side Drop Bus Channel n VT/TU New Data Flag Indication Detected (Unlatched):** A 1 indicates that a New Data Flag (1001 or 0001/1101/1011/1000) has been detected in the V1 pointer byte for the VT/TU selected (i.e., bits 1-4 in the V1 byte are the inverse of the normal 0110 pattern or differ in only one bit, with a correct size indicator and a valid pointer value).
	0	AnSIZE	**A Side Drop Bus Channel n VT/TU Incorrect Pointer Size Detected (Unlatched):** A 1 indicates that the receive size indicator in the pointer (Bits 5 and 6 in the V1 pointer byte) is not 11 (DS1) or 10 (E1) for the VT/TU selected. The detection and recovery time is immediate.

Address	Bit	Symbol	Description
X+112	7-2		**Not used:**
	1	AnJ2TIM	**A Side Drop Bus Channel n J2 Trail Trace Mismatch (Unlatched) Alarm:** Enabled when control bit ARnJ2nS1 and ARnJ2S0 are equal to 01. A 1 indication occurs when the alignment of the 16-byte J2 trace identifier label (message) has not been established.
	0	AnJ2LOL	**A Side Drop Bus Channel n J2 Loss Of Lock (Unlatched) Alarm:** Enabled when control bit ARnJ2nS1 and ARnJ2S0 are equal to 01. A 1 indicates that the stable 16-byte message did not match for three message time. Recovery occurs when the J2 state machine loses lock and then acquires lock with a 16-byte stable J2 message that matches the J2 comparison message written by the microprocessor three consecutive times.

Address	Bit	Symbol	Description
X+113	7	AnTCLM	**A Side Drop Bus Channel n Tandem Connection Loss Of Multiframe (Unlatched) Alarm:** A 1 indicates that two or more consecutive errored multiframes have been detected in bits 7 and 8 in the N2 byte. Recovery occurs when one consecutive non-errored multiframes (1111 1111 1111 1110) are detected.
	6	AnTCLL	**A Side Drop Bus Channel n Tandem Connection Trail Trace Message Loss Of Lock (Unlatched) Alarm:** A 1 indicates that the stable 16-byte message did not match for three message times. Recovery occurs when the N2 state machine loses lock and then acquires lock with a 16-byte stable N2 message that matches the N2 comparison message written by the microprocessor three consecutive times.
	5	AnTCTM	**A Side Drop Bus Channel n Bus Tandem Connection Trail Trace Message Mismatch (Unlatched) Alarm:** A 1 indicates that the stable Tandem Connection 16-byte message did not match for one message time. Recovery occurs when the N2 byte TC message state machine loses lock and then acquires lock with a 16-byte stable N2 byte message that matches the N2 byte comparison message written by the microprocessor.
	4	AnTCAIS	**A Side Drop Bus Channel n Tandem Connection AIS (Unlatched) Alarm:** A 1 indicates that bit 4 in the N2 byte is equal to 1 for five or more consecutive frames. Recovery occurs when bit 4 is a 0 for five or more consecutive frames.
	3	AnTCUQ	**A Side Drop Bus Channel n Tandem Connection Unequipped (Unlatched) Alarm:** A 1 indicates that bit 3 through 8 in the N2 byte is equal to 0 for 5 or more consecutive frames. Recovery occurs when bits 3 through 8 are not all equal to 0 for 5 or more consecutive frames.
	2	AnTCRDI	**A Side Drop Bus Channel n Tandem Connection RDI (Unlatched) Alarm:** A 1 indicates that in the N2 byte bit 8 in frame 73 is equal to 1 for five or more consecutive frames. Recovery occurs when bit 8 is a 0 for five or more consecutive frames.
	1	AnTCODI	**A Side Drop Bus Channel n Tandem Connection ODI (Unlatched) Alarm:** A 1 indicates that in the N2 byte bit 7 in frame 74 is equal to 1 for five or more consecutive frames. Recovery occurs when bit 7 is a 0 for five or more consecutive frames.
	0		**Not used:**

Address	Bit	Symbol	Description
X+114	7		**Not used:**
	6	LAnVCAIS	**A Side Drop Bus Channel n VC AIS Latched Alarm Indication:** This bit position latches for a A side VC AIS alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	5	LAnUNEQ	**A Side Drop Bus Channel n Unequipped Latched Alarm Indication:** This bit position latches for a A side unequipped alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	4	LAnRDIC	**A Side Drop Bus Channel n Remote Connectivity Defect Latched Alarm Indication:** This bit position latches for a A side remote connectivity defect alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	3	LAnRDIP	**A Side Drop Bus Channel n Remote Payload Defect Latched Alarm Indication:** This bit position latches for a A side remote payload defect alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	2	LAnRDIS	**A Side Drop Bus Channel n Remote Server Defect Indication or Single Bit RDI Latched Alarm Indication:** This bit position latches for a A side remote server defect alarm or a single bit RDI alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared by writing a 0 into this bit location.
	1	LAnSLER	**A Side Drop Bus Channel n Signal Label Mismatched Latched Alarm Indication:** This bit position latches for a A side signal label mismatch alarm indication. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	0	LAnRFI	**A Side Drop Bus Channel n Remote Failure Latched Alarm Indication:** This bit position latches for a A side remote failure indication. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.

Address	Bit	Symbol	Description
X+115	7-5		**Not used:**
	4	LAnRFFE	**A Side Drop Bus Channel n Latched Desynchronizer FIFO Error Indication:** This bit position latches for a A side desynchronizer FIFO error indication. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	3	LAnAIS	**A Side Drop Bus Channel n VT/TU AIS Latched Alarm Indication:** This bit position latches for a A side VT/TU AIS alarm indication. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	2	LAnLOP	**A Side Drop Bus Channel n VT/TU Loss Of Pointer Latched Alarm Indication:** This bit position latches for a A side VT/TU LOP alarm indication. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	1	LAnNDF	**A Side Drop Bus Channel n VT/TU New Data Flag Indication Latched Indication:** This bit position latches for a A side VT/TU NDF indication. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	0	LAnSIZE	**A Side Drop Bus Channel n VT/TU Incorrect Pointer Size Latched Indication:** This bit position latches for a A side VT/TU incorrect pointer indication. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
X+116	7-2		**Not used:**
	1	LAnJ2TIM	**A Side Drop Bus Channel n J2 Trail Trace Mismatch Latched Alarm Indication:** This bit position latches for a A side J2 mismatch alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	0	LAnJ2LOL	**A Side Drop Bus Channel n J2 Loss Of Lock Latched Alarm Indication:** This bit position latches for a A side J2 loss of lock alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.

Address	Bit	Symbol	Description
X+117	7	LAnTCLM	**A Side Drop Bus Channel n Tandem Connection Loss Of Multiframe Latched Alarm Indication:** This bit position latches for a A side TC loss of multiframe alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	6	LAnTCLL	**A Side Drop Bus Channel n Tandem Connection Trail Trace Message Loss Of Lock Latched Alarm Indication:** This bit position latches for a A side TC loss of lock alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	5	LAnTCTM	**A Side Drop Bus Channel n Bus Tandem Connection Trail Trace Message Mismatch Latched Alarm:** This bit position latches for a A side TC mismatch alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	4	LAnTCAIS	**A Side Drop Bus Channel n Tandem Connection AIS Latched Alarm Indication:** This bit position latches for a A side TC AIS alarm indication. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	3	LAnTCUQ	**A Side Drop Bus Channel n Tandem Connection Unequipped Latched Alarm Indication:** This bit position latches for a A side TC unequipped alarm indication. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	2	LAnTCRDI	**A Side Drop Bus Channel n Tandem Connection RDI Latched Alarm Indication:** This bit position latches for a A side TC RDI alarm indication. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	1	LAnTCODI	**A Side Drop Bus Channel n Tandem Connection ODI Latched Alarm Indication:** This bit position latches for a A side TC ODI alarm indication. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	0		**Not used:**

Address	Bit	Symbol	Description
X+118	7		**Not used:**
	6	PAnVCAIS	**A Side Drop Bus Channel n VC AIS One Second Alarm Indication:** This bit position is set when the A side VC AIS alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	5	PAnUNEQ	**A Side Drop Bus Channel n Unequipped One Second Alarm Indication:** This bit position is set when the A side unequipped alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	4	PAnRDIC	**A Side Drop Bus Channel n Remote Connectivity Defect One Second Alarm Indication:** This bit position is set when the A side remote connectivity defect alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	3	PAnRDIP	**A Side Drop Bus Channel n Remote Payload Defect One Second Alarm Indication:** This bit position is set when the A side remote payload defect alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	2	PAnRDIS	**A Side Drop Bus Channel n Remote Server Defect Indication or Single Bit RDI One Second Alarm Indication:** This bit position is set when the A side remote server defect alarm or single bit RDI indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	1	PAnSLER	**A Side Drop Bus Channel n Signal label Mismatch One Second Alarm Indication:** This bit position is set when the A side signal label mismatch alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	0	PAnRFI	**A Side Drop Bus Channel n Remote Failure One Second Alarm Indication:** This bit position is set when the A side remote failure indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.

Address	Bit	Symbol	Description
X+119	7-5		**Not used:**
	4	PAnRFFE	**A Side Drop Bus Channel n Desynchronizer One Second FIFO Error Indication:** This bit position is set when the A side desynchronizer FIFO error indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	3	PAnAIS	**A Side Drop Bus Channel n VT/TU AIS One Second Alarm Indication:** This bit position is set when the A side VT/TU AIS alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	2	PAnLOP	**A Side Drop Bus Channel n VT/TU Loss Of Pointer One Second Alarm Indication:** This bit position is set when the A side VT/TU LOP alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	1	PAnNDF	**A Side Drop Bus Channel n VT/TU New Data Flag Indication One Second Indication:** This bit position is set when the A side VT/TU NDF indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	0	PAnSIZE	**A Side Drop Bus Channel n VT/TU Incorrect Pointer Size One Second Indication:** This bit position is set when the A side VT/TU incorrect size indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
X+11A	7-2		**Not used:**
	1	PAnJ2TIM	**A Side Drop Bus Channel n J2 Trail Trace Mismatch One Second Alarm Indication:** This bit position is set when the A side J2 mismatch alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	0	PAnJ2LOL	**A Side Drop Bus Channel n J2 Loss Of Lock One Second Alarm Indication:** This bit position is set when the A side J2 loss of lock alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.

Address	Bit	Symbol	Description
X+11B	7	PAnTCLM	**A Side Drop Bus Channel n Tandem Connection Loss Of Multiframe One Second Alarm Indication:** This bit position is set when the A side TC loss of multiframe alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	6	PAnTCLL	**A Side Drop Bus Channel n Tandem Connection Trail Trace Message Loss Of Lock One Second Alarm Indication:** This bit position is set when the A side TC loss of lock alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	5	PAnTCTM	**A Side Drop Bus Channel n Bus Tandem Connection Trail Trace Message Mismatch One Second Alarm:** This bit position is set when the A side TC mismatch alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	4	PAnTCAIS	**A Side Drop Bus Channel n Tandem Connection AIS One Second Alarm Indication:** This bit position is set when the A side TC AIS alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	3	PAnTCUQ	**A Side Drop Bus Channel n Tandem Connection Unequipped One Second Alarm Indication:** This bit position is set when the A side TC unequipped alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	2	PAnTCRDI	**A Side Drop Bus Channel n Tandem Connection RDI One Second Alarm Indication:** This bit position is set when the A side TC RDI alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	1	PAnTCODI	**A Side Drop Bus Channel n Tandem Connection ODI One Second Alarm Indication:** This bit position is set when the A side TC ODI alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	0		**Not used:**

Address	Bit	Symbol	Description
X+11C	7		**Not used:**
	6	FAnVCAIS	**A Side Drop Bus Channel n VC AIS Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the A side BIP-2 error indication is active, but did not become active in the previous one second interval.
	5	FAnUNEQ	**A Side Drop Bus Channel n Unequipped Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the A side unequipped alarm indication is active, but did not become active in the previous one second interval.
	4	FAnRDIC	**A Side Drop Bus Channel n Remote Connectivity Defect Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the A side remote connectivity defect alarm indication is active, but did not become active in the previous one second interval.
	3	FAnRDIP	**A Side Drop Bus Channel n Remote Payload Defect Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the A side remote payload defect alarm indication is active, but did not become active in the previous one second interval.
	2	FAnRDIS	**A Side Drop Bus Channel n Remote Server Defect Indication or Single Bit RDI Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the A side remote server defect or single bit RDI alarm indication is active, but did not become active in the previous one second interval.
	1	FAnSLER	**A Side Drop Bus Channel n Signal label Mismatch Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the A side signal label mismatch alarm indication is active, but did not become active in the previous one second interval.
	0	FAnRFI	**A Side Drop Bus Channel n Remote Failure Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the A side remote failure indication is active, but did not become active in the previous one second interval.

Address	Bit	Symbol	Description
X+11D	7-5		**Not used:**
	4	FAnRFFE	**A Side Drop Bus Channel n Desynchronizer Persistent One Second FIFO Error Indication:** This bit position is set to 1 for the one-second interval, when the A side desynchronizer FIFO error indication is active, but did not become active in the previous one second interval.
	3	FAnAIS	**A Side Drop Bus Channel n VT/TU AIS Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the A side VT/TU AIS alarm indication is active, but did not become active in the previous one second interval.
	2	FAnLOP	**A Side Drop Bus Channel n VT/TU Loss Of Pointer Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the A side VT/TU LOP alarm indication is active, but did not become active in the previous one second interval.
	1	FAnNDF	**A Side Drop Bus Channel n VT/TU New Data Flag Indication Persistent One Second Indication:** This bit position is set to 1 for the one-second interval, when the A side VT/TU NDF indication is active, but did not become active in the previous one second interval.
	0	FAnSIZE	**A Side Drop Bus Channel n VT/TU Incorrect Pointer Size Persistent One Second Indication:** This bit position is set to 1 for the one-second interval, when the A side VT/TU incorrect size indication is active, but did not become active in the previous one second interval.
X+11E	7-2		**Not used:**
	1	FAnJ2TIM	**A Side Drop Bus Channel n J2 Trail Trace Mismatch Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the A side J2 mismatch alarm indication is active, but did not become active in the previous one second interval.
	0	FAnJ2LOL	**A Side Drop Bus Channel n J2 Loss Of Lock Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the A side J2 loss of lock alarm indication is active, but did not become active in the previous one second interval.
X+11F	7	FAnTCLM	**A Side Drop Bus Channel n Tandem Connection Loss Of Multiframe Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the A side TC loss of multiframe alarm indication is active, but did not become active in the previous one second interval.
	6	FAnTCLL	**A Side Drop Bus Channel n Tandem Connection Trail Trace Message Loss Of Lock Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the A side TC loss of lock alarm indication is active, but did not become active in the previous one second interval.
	5	FAnTCTM	**A Side Drop Bus Channel n Bus Tandem Connection Trail Trace Message Mismatch Persistent One Second Alarm:** This bit position is set to 1 for the one-second interval, when the A side TC mismatch alarm indication is active, but did not become active in the previous one second interval.

Address	Bit	Symbol	Description
X+11F (cont.)	4	FAnTCAIS	**A Side Drop Bus Channel n Tandem Connection AIS Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the A side TC AIS alarm indication is active, but did not become active in the previous one second interval.
	3	FAnTCUQ	**A Side Drop Bus Channel n Tandem Connection Unequipped Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the A side TC unequipped alarm indication is active, but did not become active in the previous one second interval.
	2	FAnTCRDI	**A Side Drop Bus Channel n Tandem Connection RDI Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the A side TC RDI alarm indication is active, but did not become active in the previous one second interval.
	1	FAnTCODI	**A Side Drop Bus Channel n Tandem Connection ODI Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the A side ODI alarm indication is active, but did not become active in the previous one second interval.
	0		**Not used:**

CHANNEL n - A SIDE DROP COUNTER DESCRIPTIONS (n = 1 to 28)

Address	Bit	Symbol	Description
X+120	7-0	AnPJ Counter	**A Side Drop Bus Channel n Positive Pointer Justification Counter:** An eight bit counter that increments on a positive pointer movement for the VT/TU selected.
X+121	7-0	AnNJ Counter	**A Side Drop Bus Channel n Negative Pointer Justification Counter:** An eight bit counter that increments on a negative pointer movement for the VT/TU selected.
X+122	7-0	AnREI Counter	**A Side Drop Bus Channel n REI Counter:** An 8-bit counter which counts the number of REI errors detected in bit 3 in V5 byte for the VT/TU selected.
X+123	7-0	AnBIP2 Counter	**A Side Drop Bus Channel n BIP-2 Counter:** An 8-bit counter which counts the number of BIP-2 errors detected for the VT/TU selected when control bit BLOCK is set to 0. A maximum of two errors can occur each frame. When the BLOCK control bit is set to 1, one or two errors is counted as a single block error.
X+124	7-0	AnTC OEI Error Counter	**A Side Drop Bus Channel n Tandem Connection OEI Counter:** An 8-bit counter which counts the number of OEI errors detected in bit 6 in the N2 byte for the TU/VT selected when the tandem connection feature is enabled.
X+125	7-0	AnTC REI Error Counter	**A Side Drop Bus Channel n Tandem Connection REI Counter:** An 8-bit counter which counts the number of REI errors detected in bit 5 in the N2 byte for the VT/TU selected when the tandem connection feature is enabled.

Address	Bit	Symbol	Description
X+126	7-0	AnTC BIP-2 Error Counter	**A side Drop Bus Channel n Tandem Connection BIP-2 Counter:** An 8-bit counter which counts the number of TC BIP-2 errors detected for the VT/TU selected when control bit BLOCK is set to 0. A maximum of two errors can occur each frame. When the BLOCK control bit is set to 1, one or two errors is counted as a single block error.
X+127	7-0	AnPJ Previous 1 second Counter (7-0)	**A Side Drop Bus Channel n Previous One Second Positive Pointer Justification Counter - Low Order Byte:** This counter holds the lower 8 bits of a 16 bit counter for positive pointer justification counts that occurred in the previous one second interval. This location is updated from the A side positive justification counter at one second intervals.
X+128	7-0	AnPJ Previous 1 second Counter (15-8)	**A Side Drop Bus Channel n Previous One Second Positive Pointer Justification Counter - High Order Byte:** This counter holds the higher 8 bits of a 16 bit counter for positive pointer justification counts that occurred in the previous one second interval. This location is updated from the A side positive justification counter at one second intervals.
X+129	7-0	AnNJ Previous 1 second Counter (7-0)	**A Side Drop Bus Channel n Previous One Second Negative Pointer Justification Counter- Low Order Byte:** This counter holds the lower 8 bits of a 16 bit counter for negative pointer justification counts that occurred in the previous one second interval. This location is updated from the A side current one second negative justification counter at one second intervals.
X+12A	7-0	AnNJ Previous 1 second Counter (15-8)	**A Side Drop Bus Channel n Previous One Second Negative Pointer Justification Counter - High Order Byte:** This counter holds the higher 8 bits of a 16 bit counter for negative pointer justification counts that occurred in the previous one second interval. This location is updated from the A side current one second negative justification counter at one second intervals.
X+12B	7-0	AnREI Previous 1 second Counter (7-0)	**A Side Drop Bus Channel n Previous One Second REI Counter - Low Order Byte:** This counter holds the lower 8 bits of a 16 bit counter for REI counts that occurred in the previous one second interval. This location is updated from the A side current one second REI counter at one second intervals.
X+12C	7-0	AnREI Previous 1 second Counter (15-8)	**A Side Drop Bus Channel n Previous One Second REI Counter - High Order Byte:** This counter holds the higher 8 bits of a 16 bit counter for REI counts that occurred in the previous one second interval. This location is updated from the A side current one second REI counter at one second intervals.
X+12D	7-0	AnBIP2 Previous 1 second Counter (7-0)	**A Side Drop Bus Channel n Previous One Second BIP-2 Counter - Low Order Byte:** This counter holds the lower 8 bits of a 16 bit counter for BIP-2 counts that occurred in the previous one second interval. This location is updated from the A side current one second BIP-2 counter at one second intervals.
X+12E	7-0	AnBIP2 Previous 1 second Counter (15-8)	**A Side Drop Bus Channel n Previous One Second BIP-2 Counter - High Order Byte:** This counter holds the higher 8 bits of a 16 bit counter for BIP-2 counts that occurred in the previous one second interval. This location is updated from the A side current one second BIP-2 counter at one second intervals.

Address	Bit	Symbol	Description
X+135	7-0	AnPJ Current 1 second Counter (7-0)	**A Side Drop Bus Channel n Current One Second Positive Pointer Justification Counter - Low Order Byte:** This counter holds the lower 8 bits of a 16 bit counter for positive pointer justification counts that occurred in the current one second interval. This location is updated from the A side positive justification counter at one second intervals.
X+136	7-0	AnPJ Current 1 second Counter (15-8)	**A Side Drop Bus Channel n Current One Second Positive Pointer Justification Counter - High Order Byte:** This counter holds the higher 8 bits of a 16 bit counter for positive pointer justification counts that occurred in the current one second interval. This location is updated from the A side positive justification counter at one second intervals.
X+137	7-0	AnNJ Current 1 second Counter (7-0)	**A Side Drop Bus Channel n Current One Second Negative Pointer Justification Counter- Low Order Byte:** This counter holds the lower 8 bits of a 16 bit counter for negative pointer justification counts that occurred in the current one second interval. This location is updated from the A side current one second negative justification counter at one second intervals.
X+138	7-0	AnNJ Current 1 second Counter (15-8)	**A Side Drop Bus Channel n Current One Second Negative Pointer Justification Counter - High Order Byte:** This counter holds the higher 8 bits of a 16 bit counter for negative pointer justification counts that occurred in the current one second interval. This location is updated from the A side current one second negative justification counter at one second intervals.
X+139	7-0	AnREI Current 1 second Counter (7-0)	**A Side Drop Bus Channel n Current One Second REI Counter - Low Order Byte:** This counter holds the lower 8 bits of a 16 bit counter for REI counts that occurred in the current one second interval. This location is updated from the A side current one second REI counter at one second intervals.
X+13A	7-0	AnREI Current 1 second Counter (15-8)	**A Side Drop Bus Channel n Current One Second REI Counter - High Order Byte:** This counter holds the higher 8 bits of a 16 bit counter for REI counts that occurred in the current one second interval. This location is updated from the A side current one second REI counter at one second intervals.
X+13B	7-0	AnBIP2 Current 1 second Counter (7-0)	**A Side Drop Bus Channel n Current One Second BIP-2 Counter - Low Order Byte:** This counter holds the lower 8 bits of a 16 bit counter for BIP-2 counts that occurred in the current one second interval. This location is updated from the A side current one second BIP-2 counter at one second intervals.
X+13C	7-0	AnBIP2 Current 1 second Counter (15-8)	**A Side Drop Bus Channel n Current One Second BIP-2 Counter - High Order Byte:** This counter holds the higher 8 bits of a 16 bit counter for BIP-2 counts that occurred in the current one second interval. This location is updated from the A side current one second BIP-2 counter at one second intervals.

CHANNEL n - A SIDE DROP BUS OVERHEAD BYTE REGISTER DESCRIPTIONS (n = 1 to 28)

Address	Bit	Symbol	Description
X+143 to X+182	7-0	A Side Drop Bus J2 and N2 Message Segments	**A Side Drop Bus Channel n J2 and N2 Byte Message Segments:** The following locations store the A side drop bus 64-byte J2 message when control bit AnJ2S1 is a 1, and 16-byte J2 and N2 drop and microprocessor written comparison messages when control bit ARnJ2S1 is a 0. The following list the location of the drop message segments and the microprocessor written segments. Location — Message Segment 143H - 182H — A side Drop Bus - J2 byte 64 byte Message. or 143H - 152H — A side Drop Bus - J2 byte 16 byte Message 153H - 162H — A side Drop Bus - N2 byte 16 byte Message 163H - 172H — A side Microprocessor - J2 byte 16 byte Message 173H - 182H — A side Microprocessor - N2 byte 16 byte Message
X+183	7-0	A Side Drop Bus V1 Byte	**A Side Drop Bus Channel n V1 Byte:** This register is updated every 500 microseconds. This location stores the A side drop bus V1 byte pointer byte for the VT/TU selected. Bit 7 in this register corresponds to bit 1 in the V1 byte.
X+184	7-0	A Side Drop Bus V2 Byte	**A Side Drop Bus Channel n V2 Byte:** This register is updated every 500 microseconds. This location stores the A side drop bus V2 byte pointer byte for the VT/TU selected. Bit 7 in this register corresponds to bit 1 in the V2 byte.
X+185	7-0	A Side Drop Bus V4 Byte	**A Side Drop Bus Channel n V4 Byte:** This register is updated every 500 microseconds. This location stores the A side drop bus V4 byte for the VT/TU selected. Bit 7 in this register corresponds to bit 1 in the V4 byte.
X+186	7-0	A Side Drop Bus V5 Byte	**A Side Drop Bus Channel n V5 Overhead Byte:** This register is updated every 500 microseconds. This location stores the A side drop bus V5 overhead byte for the VT/TU selected. Bit 7 in this register corresponds to bit 1 in the V5 byte.
X+187	7-0	A Side Drop Bus J2 Byte	**A Side Drop Bus Channel n J2 Overhead Byte:** This register is updated every 500 microseconds. This location stores the A side drop bus J2 overhead J2 byte for the VT/TU selected. Bit 7 in this register corresponds to bit 1 in the V5 byte.
X+188	7-0	A Side Drop Bus N2 Byte	**A Side Drop Bus Channel n N2 Overhead Byte:** This register is updated every 500 microseconds. This location stores the A side drop bus N2 overhead byte for the VT/TU selected. Bit 7 in this register corresponds to bit 1 in the N2 byte.
X+189	7-0	A Side Drop Bus K4 Byte	**A Side Drop Bus Channel n K4 Overhead Byte:** This register is updated every 500 microseconds. This location stores the A side drop bus K4 overhead byte for the VT/TU selected. Bit 7 in this register corresponds to bit 1 in the K4 byte.

Address	Bit	Symbol	Description
X+18A	7-0	A Side Drop Bus O-Bits	**A Side Drop Bus Channel n O-bits:** The two nibbles (bits 7-4 and 3-0) in this register correspond to the two sets of four overhead communication bits for the VT/TU selected. Bit 7 corresponds to bit 3 in the first justification control byte, while bit 0 corresponds to bit 6 in the second justification control byte. The two nibbles written into this register location will be from the same frame, updated every 500 microseconds.

CHANNEL n - B SIDE DROP BUS ALARM MASK BITS (n = 1 to 28)

Address	Bit	Symbol	Description
X+083	7		**Not used:**
	6	MBnVAIS	**B Side Drop Bus Channel n VC AIS Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a B side Drop bus VC AIS latched bit alarm indication for channel n.
	5	MBnUQE	**B Side Drop Bus Channel n Unequipped Indication Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a B side unequipped latched bit alarm indication for channel n.
	4	MBnRDIC	**B Side Drop Bus Channel n Remote Connectivity Defect Indication Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a B side remote connectivity defect latched bit alarm indication for channel n.
	3	MBnRDIP	**B Side Drop Bus Channel n Remote Payload Defect Indication Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a B side remote payload defect latched bit alarm indication for channel n.
	2	MBnRDIS	**B Side Drop Bus Channel n Remote Server Defect Indication or Single Bit RDI Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a B side remote server defect or single bit RDI latched bit alarm indication for channel n.
	1	MBnSLER	**B Side Drop Bus Channel n Signal Label Mismatch Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a B side signal label alarm latched bit alarm indication for channel n.
	0	MBnRFI	**B Side Drop Bus Channel n Remote Failure Indication Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a B side remote failure indication alarm for channel n.
X+084	7-5		**Not used:**
	4	MBnRFE	**B Side Drop Bus Channel n FIFO Error Indication Mask Bit:** Setting this bit to 1 A 1 enables the hardware interrupt for a B side FIFO error indication latched bit alarm indication for channel n.
	3	MBnAIS	**B Side Drop Bus Channel n VT/TU AIS Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a B side VT/TU AIS alarm latched bit alarm indication for channel n.

Address	Bit	Symbol	Description
X+084 (cont.)	2	MBnLOP	**B Side Drop Bus Channel n VT/TU Loss Of Pointer Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a B side loss of pointer alarm latched bit alarm indication for channel n.
	1	MBnNDF	**B Side Drop Bus Channel n VT/TU New Data Flag Indication Indication Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a B side NDF latched bit indication for channel n.
	0	MBnSIZE	**B Side Drop Bus Channel n VT/TU Incorrect Pointer Size Indication Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a B side VT/TU incorrect pointer latched bit indication for channel n.
X+085	7-2		**Not used:**
	1	MBnJ2TIM	**B Side Drop Bus Channel n J2 Loss Of Lock Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a B side J2 loss of lock alarm latched bit indication for channel n.
	0	MBnJ2LOL	**B Side Drop Bus Channel n J2 Trail Trace Mismatch Alarm mask Bit:** Setting this bit to 1 enables the hardware interrupt for a B side J2 mismatch alarm latched bit indication for channel n.
X+086	7	MBnTCLM	**B Side Drop Bus Channel n Tandem Connection Loss Of Multiframe Alarm mask Bit:** Setting this bit to 1 enables the hardware interrupt for a B side TC loss of multiframe alarm latched bit indication for channel n.
	6	MBnTCLL	**B Side Drop Bus Channel n Tandem Connection Loss Of Lock Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a B side TC loss of lock alarm latched bit indication for channel n.
	5	MBnTCTM	**B Side Drop Bus Channel n Tandem Connection Trail Trace Message Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a B side TC mismatch alarm latched bit indication for channel n.
	4	MBnTCAIS	**B Side Drop Bus Channel n Tandem Connection AIS Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a B side TC AIS alarm latched bit indication for channel n.
	3	MBnTCUQ	**B Side Drop Bus Channel n Tandem Connection Unequipped Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a B side TC unequipped alarm latched bit indication for channel n.
	2	MBnTCRDI	**B Side Drop Bus Port n Tandem Connection RDI Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a B side TC RDI alarm latched bit indication for channel n.
	1	MBnTCODI	**B Side Drop Bus Channel n Tandem Connection ODI Alarm Mask Bit:** Setting this bit to 1 enables the hardware interrupt for a B side TC ODI alarm latched bit indication for channel n.
	0		**Not used:**

CHANNEL n - B SIDE DROP STATUS REGISTER DESCRIPTIONS (n = 1 to 28)

The following descriptions pertain to the status registers assigned to channel n for the B side Drop Bus. The status registers provide four readable bit positions per alarm. The alarm status are provided as unlatched alarm indications, latched alarm indications, one second indications, and previous one second indications. The latched bit position is set on positive, negative, or both positive and negative transitions of the alarm. B latched alarm is cleared on a microprocessor read cycle of its address.

Address	Bit	Symbol	Description
X+190	7		**Not used:**
	6	BnVCAIS	**B Side Drop Bus Channel n VC AIS Indication (Unlatched) Detected:** A VC AIS state is defined as a signal label equal to 111 (bits 5-7 in V5 byte). A 1 indicates that an VC AIS has been detected in the V5 signal label for the TU/VT selected for five or more consecutive received VC AIS signal labels. Recovery occurs when five or more consecutive signal labels are received not equal to 111.
	5	BnUNEQ	**B Side Drop Bus Channel n Unequipped Indication (Unlatched) Detected:** A 1 indicates that an unequipped status has been detected in the V5 signal label (Bits 5-7 in V5 byte are equal to 000) for the TU/VT selected for five or more consecutive received unequipped signal labels. Recovery occurs when five or more consecutive signal labels are received not equal to 000.
	4	BnRDIC	**B Side Drop Bus Channel n Remote Connectivity Defect Indication (Unlatched) Detected:** A 1 indicates that a remote connectivity defect alarm has been detected. The number of consecutive events used for detection and recovery is determined by control bit V5AL10.
	3	BnRDIP	**B Side Drop Bus Channel n Remote Payload Defect Indication (Unlatched) Detected:** A 1 indicates that a remote payload defect alarm has been detected. The number of consecutive events used for detection and recovery is determined by control bit V5AL10.
	2	BnRDIS	**B Side Drop Bus Channel n Remote Server Defect Indication or Single Bit RDI (Unlatched) Detected:** A 1 indicates that a remote server defect alarm or a single bit RDI state has been detected. The number of consecutive events used for detection and recovery is determined by control bit V5AL10.
	1	BnSLER	**B Side Drop Bus Channel n Signal Label Mismatch Detected (Unlatched):** A 1 indicates that the dropped signal label (Bits 5-7 in V5 byte) for the VT/TU selected does not match the microprocessor-written signal label for five or more consecutive events. Recovery occurs when five or more consecutive correct signal labels are detected.
	0	BnRFI	**B Side Drop Bus Channel n Remote Failure Indication Detected (Unlatched):** A 1 indicates that bit 4 in the V5 byte is equal to 1 for the VT/TU selected. The detection and recovery time is five consecutive multiframes.

Address	Bit	Symbol	Description
X+191	7-5		**Not used:**
	4	BnRFFE	**B Side Drop Bus Channel n FIFO Error (Unlatched):** A 1 indicates that the receive FIFO in the desynchronizer for channel n has overflowed or underflowed for the VT/TU selected. The FIFO is reset automatically. Line AIS will be sent for two multiframes when enabled.
	3	BnAIS	**B Side Drop Bus Channel n VT/TU AIS Detected (Unlatched):** A 1 indicates that a AIS state has been detected in the V1/V2 pointer bytes for the VT/TU selected.
	2	BnLOP	**B Side Drop Bus Channel n VT/TU Loss Of Pointer Detected (Unlatched):** A 1 indicates that a loss of pointer (LOP) has been detected in the V1/V2 pointer bytes for the VT/TU selected.
	1	BnNDF	**B Side Drop Bus Channel n VT/TU New Data Flag Indication Detected (Unlatched):** A 1 indicates that a New Data Flag (1001 or 0001/1101/1011/1000) has been detected in the V1 pointer byte for the VT/TU selected (i.e., bits 1-4 in the V1 byte are the inverse of the normal 0110 pattern or differ in only one bit, with a correct size indicator and a valid pointer value).
	0	BnSIZE	**B Side Drop Bus Channel n VT/TU Incorrect Pointer Size Detected (Unlatched):** A 1 indicates that the receive size indicator in the pointer (Bits 5 and 6 in the V1 pointer byte) is not 11 (DS1) or 10 (e1) for the VT/TU selected. The detection and recovery time is immediate.
X+192	7-2		**Not used:**
	1	BnJ2TIM	**B Side Drop Bus Channel n J2 Trail Trace Mismatch (Unlatched) Alarm:** Enabled when control bit BRnJ2S1 and BRnJ2S0 are equal to 01. A 1 indication occurs when the alignment of the 16-byte J2 trace identifier label (message) has not been established.
	0	BnJ2LOL	**B Side Drop Bus Channel n J2 Loss Of Lock (Unlatched) Alarm:** Enabled when control bit BRnJ2S1 and BRnJ2S0 are equal to 01. A 1 indicates that the stable 16-byte message did not match for three message time. Recovery occurs when the J2 state machine loses lock and then acquires lock with a 16-byte stable J2 message that matches the J2 comparison message written by the microprocessor for three consecutive times.

Address	Bit	Symbol	Description
X+193	7	BnTCLM	**B Side Drop Bus Channel n Tandem Connection Loss Of Multiframe (Unlatched) Alarm:** A 1 indicates that two or more consecutive errored multiframes have been detected in bits 7 and 8 in the N2 byte. Recovery occurs when one consecutive non-errored multiframes (1111 1111 1111 1110) are detected.
	6	BnTCLL	**B Side Drop Bus Channel n Tandem Connection Trail Trace Message Loss Of Lock (Unlatched) Alarm:** A 1 indicates that the stable 16-byte message did not match for three message times. Recovery occurs when the N2 state machine loses lock and then acquires lock with a 16-byte stable N2 message that matches the N2 comparison message written by the microprocessor for 3 consecutive times.
	5	BnTCTM	**B Side Drop Bus Channel n Bus Tandem Connection Trail Trace Message Mismatch (Unlatched) Alarm:** A 1 indicates that the stable Tandem Connection 16-byte message did not match for one message time. Recovery occurs when the N2 byte TC message state machine loses lock and then acquires lock with a 16-byte stable N2 byte message that matches the N2 byte comparison message written by the microprocessor.
	4	BnTCAIS	**B Side Drop Bus Channel n Tandem Connection AIS (Unlatched) Alarm:** A 1 indicates that bit 4 in the N2 byte is equal to 1 for five or more consecutive frames. Recovery occurs when bit 4 is a 0 for five or more consecutive frames.
	3	BnTCUQ	**B Side Drop Bus Channel n Tandem Connection Unequipped (Unlatched) Alarm:** A 1 indicates that bit 3 through 8 in the N2 byte is equal to 0 for 5 or more consecutive frames. Recovery occurs when bits 3 through 8 are not all equal to 0 for 5 or more consecutive frames.
	2	BnTCRDI	**B Side Drop Bus Channel n Tandem Connection RDI (Unlatched) Alarm:** A 1 indicates that in the N2 byte bit 8 in frame 73 is equal to 1 for five or more consecutive frames. Recovery occurs when bit 8 is a 0 for five or more consecutive frames.
	1	BnTCODI	**B Side Drop Bus Channel n Tandem Connection ODI (Unlatched) Alarm:** A 1 indicates that in the N2 byte bit 7 in frame 74 is equal to 1 for five or more consecutive frames. Recovery occurs when bit 7 is a 0 for five or more consecutive frames.
	0		**Not used:**

Address	Bit	Symbol	Description
X+194	7		**Not used:**
	6	LBnVCAIS	**B Side Drop Bus Channel n VC AIS Latched Alarm Indication:** This bit position latches for a B side VC AIS alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	5	LBnUNEQ	**B Side Drop Bus Channel n Unequipped Latched Alarm Indication:** This bit position latches for a B side unequipped alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	4	LBnRDIC	**B Side Drop Bus Channel n Remote Connectivity Defect Latched Alarm Indication:** This bit position latches for a B side remote connectivity defect alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	3	LBnRDIP	**B Side Drop Bus Channel n Remote Payload Defect Latched Alarm Indication:** This bit position latches for a B side remote payload defect alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	2	LBnRDIS	**B Side Drop Bus Channel n Remote Server Defect Indication or Single Bit RDI Latched Alarm Indication:** This bit position latches for a B side remote server defect alarm or a single bit RDI alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	1	LBnSLER	**B Side Drop Bus Channel n Signal Label Mismatched Latched Alarm Indication:** This bit position latches for a B side signal label mismatch alarm indication. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	0	LBNRFI	**B Side Drop Bus Channel n Remote Failure Latched Alarm Indication:** This bit position latches for a B side remote failure indication. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.

Address	Bit	Symbol	Description
X+195	7-5		**Not used:**
	4	LBnRFFE	**B Side Drop Bus Channel n Latched Desynchronizer FIFO Error Indication:** This bit position latches for a B side desynchronizer FIFO error indication. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	3	LBnAIS	**B Side Drop Bus Channel n VT/TU AIS Latched Alarm Indication:** This bit position latches for a B side VT/TU AIS alarm indication. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	2	LBnLOP	**B Side Drop Bus Channel n VT/TU Loss Of Pointer Latched Alarm Indication:** This bit position latches for a B side VT/TU LOP alarm indication. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	1	LBnNDF	**B Side Drop Bus Channel n VT/TU New Data Flag Indication Latched Indication:** This bit position latches for a B side VT/TU NDF indication. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	0	LBnSIZE	**B Side Drop Bus Channel n VT/TU Incorrect Pointer Size Latched Indication:** This bit position latches for a B side VT/TU incorrect pointer indication. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
X+196	7-2		**Not used:**
	1	LBnJ2TIM	**B Side Drop Bus Channel n J2 Trail Trace Mismatch Latched Alarm Indication:** This bit position latches for a B side J2 mismatch alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	0	LBnJ2LOL	**B Side Drop Bus Channel n J2 Loss Of Lock Latched Alarm Indication:** This bit position latches for a B side J2 loss of lock alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.

Address	Bit	Symbol	Description
X+197	7	LBnTCLM	**B Side Drop Bus Channel n Tandem Connection Loss Of Multiframe Latched Alarm Indication:** This bit position latches for a B side TC loss of multiframe alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	6	LBnTCLL	**B Side Drop Bus Channel n Tandem Connection Trail Trace Message Loss Of Lock Latched Alarm Indication:** This bit position latches for a B side TC loss of lock alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	5	LBnTCTM	**B Side Drop Bus Channel n Bus Tandem Connection Trail Trace Message Mismatch Latched Alarm:** This bit position latches for a B side TC mismatch alarm. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	4	LBnTCAIS	**B Side Drop Bus Channel n Tandem Connection AIS Latched Alarm Indication:** This bit position latches for a B side TC AIS alarm indication. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	3	LBnTCUQ	**B Side Drop Bus Channel n Tandem Connection Unequipped Latched Alarm Indication:** This bit position latches for a B side TC unequipped alarm indication. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	2	LBnTCRDI	**B Side Drop Bus Channel n Tandem Connection RDI Latched Alarm Indication:** This bit position latches for a B side TC RDI alarm indication. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	1	LBnTCODI	**B Side Drop Bus Channel n Tandem Connection ODI Latched Alarm Indication:** This bit position latches for a B side TC ODI alarm indication. This bit is set on either a positive transition, negative transition or positive and negative alarm transition. This bit is cleared on a read cycle.
	0		**Not used:**

Address	Bit	Symbol	Description
X+198	7		**Not used:**
	6	PBnVCAIS	**B Side Drop Bus Channel n VC AIS One Second Alarm Indication:** This bit position is set when the B side VC AIS alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	5	PBnUNEQ	**B Side Drop Bus Channel n Unequipped One Second Alarm Indication:** This bit position is set when the B side unequipped alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	4	PBnRDIC	**B Side Drop Bus Channel n Remote Connectivity Defect One Second Alarm Indication:** This bit position is set when the B side remote connectivity defect alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	3	PBnRDIP	**B Side Drop Bus Channel n Remote Payload Defect One Second Alarm Indication:** This bit position is set when the B side remote payload defect alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	2	PBnRDIS	**B Side Drop Bus Channel n Remote Server Defect Indication or Single Bit RDI One Second Alarm Indication:** This bit position is set when the B side remote server defect alarm or single bit RDI indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	1	PBnSLER	**B Side Drop Bus Channel n Signal label Mismatch One Second Alarm Indication:** This bit position is set when the B side signal label mismatch alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	0	PBnRFI	**B Side Drop Bus Channel n Remote Failure One Second Alarm Indication:** This bit position is set when the B side remote failure indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.

Address	Bit	Symbol	Description
X+199	7-5		**Not used:**
	4	PBnRFFE	**B Side Drop Bus Channel n Desynchronizer One Second FIFO Error Indication:** This bit position is set when the B side desynchronizer FIFO error indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	3	PBnAIS	**B Side Drop Bus Channel n VT/TU AIS One Second Alarm Indication:** This bit position is set when the B side VT/TU AIS alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	2	PBnLOP	**B Side Drop Bus Channel n VT/TU Loss Of Pointer One Second Alarm Indication:** This bit position is set when the B side VT/TU LOP alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	1	PBAnNDF	**B Side Drop Bus Channel n VT/TU New Data Flag Indication One Second Indication:** This bit position is set when the B side VT/TU NDF indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	0	PBnSIZE	**B Side Drop Bus Channel n VT/TU Incorrect Pointer Size One Second Indication:** This bit position is set when the B side VT/TU incorrect size indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
X+19A	7-2		**Not used:**
	1	PBnJ2TIM	**B Side Drop Bus Channel n J2 Trail Trace Mismatch One Second Alarm Indication:** This bit position is set when the B side J2 mismatch alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	0	PBnJ2LOL	**B Side Drop Bus Channel n J2 Loss Of Lock One Second Alarm Indication:** This bit position is set when the B side J2 loss of lock alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.

Address	Bit	Symbol	Description
X+19B	7	PBnTCLM	**B Side Drop Bus Channel n Tandem Connection Loss Of Multiframe One Second Alarm Indication:** This bit position is set when the B side TC loss of multiframe alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	6	PBnTCLL	**B Side Drop Bus Channel n Tandem Connection Trail Trace Message Loss Of Lock One Second Alarm Indication:** This bit position is set when the B side TC loss of lock alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	5	PBnTCTM	**B Side Drop Bus Channel n Bus Tandem Connection Trail Trace Message Mismatch One Second Alarm:** This bit position is set when the B side TC mismatch alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	4	PBnTCAIS	**B Side Drop Bus Channel n Tandem Connection AIS One Second Alarm Indication:** This bit position is set when the B side TC AIS alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	3	PBnTCUQ	**B Side Drop Bus Channel n Tandem Connection Unequipped One Second Alarm Indication:** This bit position is set when the B side TC unequipped alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	2	PBnTCRDI	**B Side Drop Bus Channel n Tandem Connection RDI One Second Alarm Indication:** This bit position is set when the B side TC RDI alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	1	PBnTCODI	**B Side Drop Bus Channel n Tandem Connection ODI One Second Alarm Indication:** This bit position is set when the B side TC ODI alarm indication has changed state in the last one second interval or is 1 at the end of the interval. This bit is disabled if the one second pulse is not applied. This indication does not cause an interrupt.
	0		**Not used:**

Address	Bit	Symbol	Description
X+19C	7		**Not used:**
	6	FBnVCAIS	**B Side Drop Bus Channel n VC AIS Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the B side BIP-2 error indication is active, but did not become active in the previous one second interval.
	5	FBnUNEQ	**B Side Drop Bus Channel n Unequipped Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the B side unequipped alarm indication is active, but did not become active in the previous one second interval.
	4	FBnRDIC	**B Side Drop Bus Channel n Remote Connectivity Defect Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the B side remote connectivity defect alarm indication is active, but did not become active in the previous one second interval.
	3	FBnRDIP	**B Side Drop Bus Channel n Remote Payload Defect Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the B side remote payload defect alarm indication is active, but did not become active in the previous one second interval.
	2	FBnRDIS	**B Side Drop Bus Channel n Remote Server Defect Indication or Single Bit RDI Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the B side remote server defect or single bit RDI alarm indication is active, but did not become active in the previous one second interval.
	1	FBnSLER	**B Side Drop Bus Channel n Signal label Mismatch Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the B side signal label mismatch alarm indication is active, but did not become active in the previous one second interval.
	0	FBnRFI	**B Side Drop Bus Channel n Remote Failure Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the B side remote failure indication is active, but did not become active in the previous one second interval.

Address	Bit	Symbol	Description
X+19D	7-5		**Not used:**
	4	FBnRFFE	**B Side Drop Bus Channel n Desynchronizer Persistent One Second FIFO Error Indication:** This bit position is set to 1 for the one-second interval, when the B side desynchronizer FIFO error indication is active, but did not become active in the previous one second interval.
	3	FBnAIS	**B Side Drop Bus Channel n VT/TU AIS Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the B side VT/TU AIS alarm indication is active, but did not become active in the previous one second interval.
	2	FBnLOP	**B Side Drop Bus Channel n VT/TU Loss Of Pointer Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the B side VT/TU LOP alarm indication is active, but did not become active in the previous one second interval.
	1	FBnNDF	**B Side Drop Bus Channel n VT/TU New Data Flag Indication Persistent One Second Indication:** This bit position is set to 1 for the one-second interval, when the B side VT/TU NDF indication is active, but did not become active in the previous one second interval.
	0	FBnSIZE	**B Side Drop Bus Channel n VT/TU Incorrect Pointer Size Persistent One Second Indication:** This bit position is set to 1 for the one-second interval, when the B side VT/TU incorrect size indication is active, but did not become active in the previous one second interval
X+19E	7-2		**Not used:**
	1	FBnJ2TIM	**B Side Drop Bus Channel n J2 Trail Trace Mismatch Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the B side J2 mismatch alarm indication is active, but did not become active in the previous one second interval.
	0	FBnJ2LOL	**B Side Drop Bus Channel n J2 Loss Of Lock Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the B side J2 loss of lock alarm indication is active, but did not become active in the previous one second interval.

Address	Bit	Symbol	Description
X+19F	7	FBnTCLM	**B Side Drop Bus Channel n Tandem Connection Loss Of Multiframe Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the B side TC loss of multiframe alarm indication is active, but did not become active in the previous one second interval.
	6	FBnTCLL	**B Side Drop Bus Channel n Tandem Connection Trail Trace Message Loss Of Lock Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the B side TC loss of lock alarm indication is active, but did not become active in the previous one second interval.
	5	FBnTCTM	**B Side Drop Bus Channel n Bus Tandem Connection Trail Trace Message Mismatch Persistent One Second Alarm:** This bit position is set to 1 for the one-second interval, when the B side TC mismatch alarm indication is active, but did not become active in the previous one second interval.
	4	FBnTCAIS	**B Side Drop Bus Channel n Tandem Connection AIS Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the B side TC AIS alarm indication is active, but did not become active in the previous one second interval.
	3	FBnTCUQ	**B Side Drop Bus Channel n Tandem Connection Unequipped Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the B side TC unequipped alarm indication is active, but did not become active in the previous one second interval.
	2	FBnTCRDI	**B Side Drop Bus Channel n Tandem Connection RDI Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the B side TC RDI alarm indication is active, but did not become active in the previous one second interval.
	1	FBnTCODI	**B Side Drop Bus Channel n Tandem Connection ODI Persistent One Second Alarm Indication:** This bit position is set to 1 for the one-second interval, when the B side ODI alarm indication is active, but did not become active in the previous one second interval.
	0		**Not used:**

CHANNEL n - B SIDE DROP COUNTER DESCRIPTIONS (n = 1 to 28)

Address	Bit	Symbol	Description
X+1A0	7-0	BnPJ Counter	**B Side Drop Bus Channel n Positive Pointer Justification Counter:** An eight bit counter that increments on a positive pointer movement for the VT/TU selected.
X+1A1	7-0	BnNJ Counter	**B Side Drop Bus Channel n Negative Pointer Justification Counter:** An eight bit counter that increments on a negative pointer movement for the VT/TU selected.
X+1A2	7-0	BnREI Counter	**B Side Drop Bus Channel n REI Counter:** An 8-bit counter which counts the number of REI errors detected in bit 3 in V5 byte for the VT/TU selected.

Address	Bit	Symbol	Description
X+1A3	7-0	BnBIP2 Counter	**B Side Drop Bus Channel n BIP-2 Counter:** An 8-bit counter which counts the number of BIP-2 errors detected for the VT/TU selected when control bit BLOCK is set to 0. A maximum of two errors can occur each frame. When the BLOCK control bit is set to 1, one or two errors is counted as a single block error.
X+1A4	7-0	BnTC OEI Error Counter	**B Side Drop Bus Channel n Tandem Connection OEI Counter:** An 8-bit counter which counts the number of OEI errors detected in bit 6 in the N2 byte for the TU/VT selected when the tandem connection feature is enabled.
X+1A5	7-0	BnTC REI Error Counter	**B Side Drop Bus Channel n Tandem Connection REI Counter:** An 8-bit counter which counts the number of REI errors detected in bit 5 in the N2 byte for the VT/TU selected when the tandem connection feature is enabled.
X+1A6	7-0	BnTC BIP-2 Error Counter	**B side Drop Bus Channel n Tandem Connection BIP-2 Counter:** An 8-bit counter which counts the number of TC BIP-2 errors detected for the VT/TU selected when control bit BLOCK is set to 0. A maximum of two errors can occur each frame. When the BLOCK control bit is set to 1, one or two errors is counted as a single block error.
X+1A7	7-0	BnPJ Previous 1 second Counter (7-0)	**B Side Drop Bus Channel n Previous One Second Positive Pointer Justification Counter - Low Order Byte:** This counter holds the lower 8 bits of a 16 bit counter for positive pointer justification counts that occurred in the previous one second interval. This location is updated from the B side positive justification counter at one second intervals.
X+1A8	7-0	BnPJ Previous 1 second Counter (15-8)	**B Side Drop Bus Channel n Previous One Second Positive Pointer Justification Counter - High Order Byte:** This counter holds the higher 8 bits of a 16 bit counter for positive pointer justification counts that occurred in the previous one second interval. This location is updated from the B side positive justification counter at one second intervals.
X+1A9	7-0	BnNJ Previous 1 second Counter (7-0)	**B Side Drop Bus Channel n Previous One Second Negative Pointer Justification Counter- Low Order Byte:** This counter holds the lower 8 bits of a 16 bit counter for negative pointer justification counts that occurred in the previous one second interval. This location is updated from the B side current one second negative justification counter at one second intervals.
X+1AA	7-0	BnNJ Previous 1 second Counter (15-8)	**B Side Drop Bus Channel n Previous One Second Negative Pointer Justification Counter - High Order Byte:** This counter holds the higher 8 bits of a 16 bit counter for negative pointer justification counts that occurred in the previous one second interval. This location is updated from the B side current one second negative justification counter at one second intervals.
X+1AB	7-0	BnREI Previous 1 second Counter (7-0)	**B Side Drop Bus Channel n Previous One Second REI Counter - Low Order Byte:** This counter holds the lower 8 bits of a 16 bit counter for REI counts that occurred in the previous one second interval. This location is updated from the B side current one second REI counter at one second intervals.

Address	Bit	Symbol	Description
X+1AC	7-0	BnREI Previous 1 second Counter (15-8)	**B Side Drop Bus Channel n Previous One Second REI Counter - High Order Byte:** This counter holds the higher 8 bits of a 16 bit counter for REI counts that occurred in the previous one second interval. This location is updated from the B side current one second REI counter at one second intervals.
X+1AD	7-0	BnBIP2 Previous 1 second Counter (7-0)	**B Side Drop Bus Channel n Previous One Second BIP-2 Counter - Low Order Byte:** This counter holds the lower 8 bits of a 16 bit counter for BIP-2 counts that occurred in the previous one second interval. This location is updated from the B side current one second BIP-2 counter at one second intervals.
X+1AE	7-0	BnBIP2 Previous 1 second Counter (15-8)	**B Side Drop Bus Channel n Previous One Second BIP-2 Counter - High Order Byte:** This counter holds the higher 8 bits of a 16 bit counter for BIP-2 counts that occurred in the previous one second interval. This location is updated from the B side current one second BIP-2 counter at one second intervals.
X+1B5	7-0	BnPJ Current 1 second Counter (7-0)	**B Side Drop Bus Channel n Current One Second Positive Pointer Justification Counter - Low Order Byte:** This counter holds the lower 8 bits of a 16 bit counter for positive pointer justification counts that occurred in the current one second interval. This location is updated from the B side positive justification counter at one second intervals.
X+1B6	7-0	BnPJ Current 1 second Counter (15-8)	**B Side Drop Bus Channel n Current One Second Positive Pointer Justification Counter - High Order Byte:** This counter holds the higher 8 bits of a 16 bit counter for positive pointer justification counts that occurred in the current one second interval. This location is updated from the B side positive justification counter at one second intervals.
X+1B7	7-0	BnNJ Current 1 second Counter (7-0)	**B Side Drop Bus Channel n Current One Second Negative Pointer Justification Counter- Low Order Byte:** This counter holds the lower 8 bits of a 16 bit counter for negative pointer justification counts that occurred in the current one second interval. This location is updated from the B side current one second negative justification counter at one second intervals.
X+1B8	7-0	BnNJ Current 1 second Counter (15-8)	**B Side Drop Bus Channel n Current One Second Negative Pointer Justification Counter - High Order Byte:** This counter holds the higher 8 bits of a 16 bit counter for negative pointer justification counts that occurred in the current one second interval. This location is updated from the B side current one second negative justification counter at one second intervals.
X+1B9	7-0	BnREI Current 1 second Counter (7-0)	**B Side Drop Bus Channel n Current One Second REI Counter - Low Order Byte:** This counter holds the lower 8 bits of a 16 bit counter for REI counts that occurred in the current one second interval. This location is updated from the B side current one second REI counter at one second intervals.
X+1BA	7-0	BnREI Current 1 second Counter (15-8)	**B Side Drop Bus Channel n Current One Second REI Counter - High Order Byte:** This counter holds the higher 8 bits of a 16 bit counter for REI counts that occurred in the current one second interval. This location is updated from the B side current one second REI counter at one second intervals.

Address	Bit	Symbol	Description
X+1BB	7-0	BnBIP2 Current 1 second Counter (7-0)	**B Side Drop Bus Channel n Current One Second BIP-2 Counter - Low Order Byte:** This counter holds the lower 8 bits of a 16 bit counter for BIP-2 counts that occurred in the current one second interval. This location is updated from the B side current one second BIP-2 counter at one second intervals.
X+1BC	7-0	BnBIP2 Current 1 second Counter (15-8)	**B Side Drop Bus Channel n Current One Second BIP-2 Counter - High Order Byte:** This counter holds the higher 8 bits of a 16 bit counter for BIP-2 counts that occurred in the current one second interval. This location is updated from the B side current one second BIP-2 counter at one second intervals.

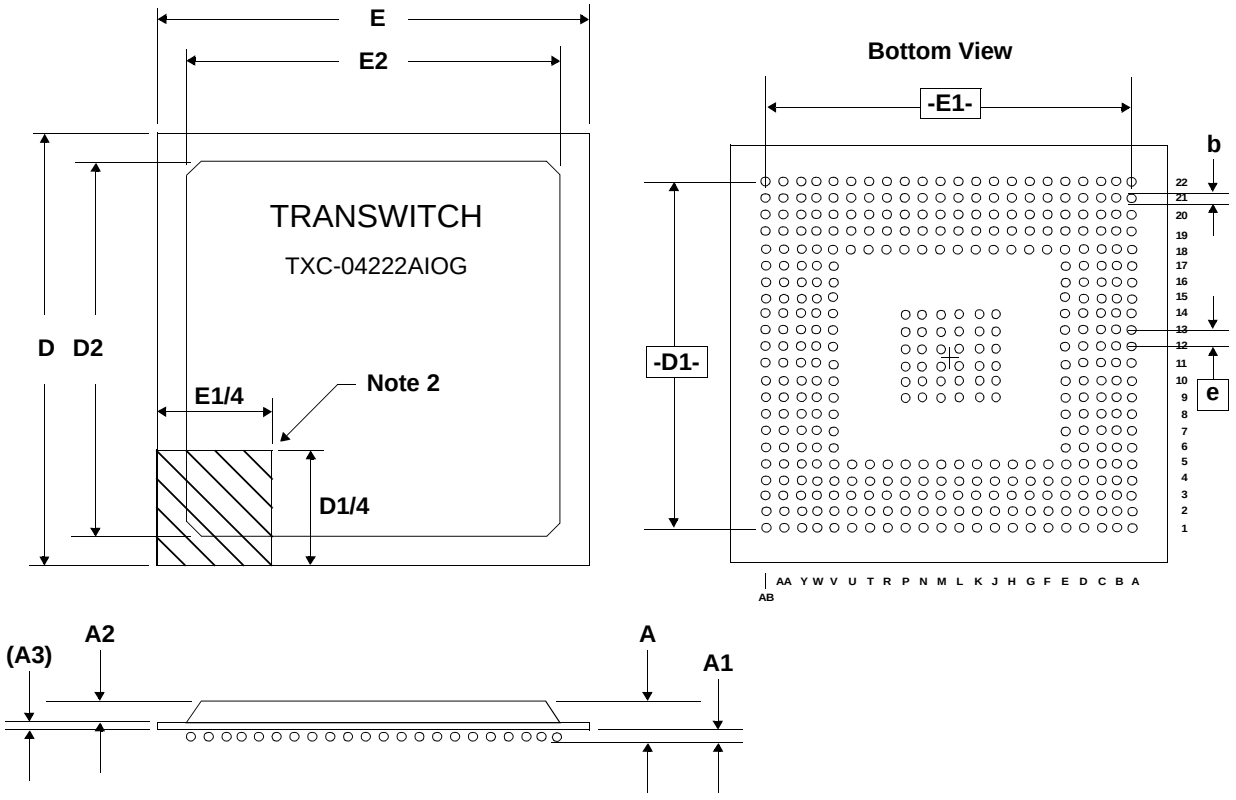
CHANNEL n - B SIDE DROP BUS OVERHEAD BYTE REGISTER DESCRIPTIONS (n = 1 to 28)

Address	Bit	Symbol	Description
X+1C3 to X+202	7-0	B Side Drop Bus J2 and N2 Message Segments	**B Side Drop Bus Channel n J2 and N2 Byte Message Segments:** The following locations store the B side drop bus 64-byte J2 message when control bit BnJ2S1 is a 1, and 16-byte J2 and N2 drop and microprocessor written comparison messages when control bit BnJ2S1 is a 0. The following list the location of the drop message segments and the microprocessor written segments. Location — Message Segment 1C3H - 202 — B side Drop Bus - J2 byte 64 byte Message. or 1C3H - 1D2H — B side Drop Bus - J2 byte 16 byte Message 1D3H - 1E2H — B side Drop Bus - N2 byte 16 byte Message 1E3H - 1F2H — B side Microprocessor - J2 byte 16 byte Message 1F3H - 202H — B side Microprocessor - N2 byte 16 byte Message
X+203	7-0	B Side Drop Bus V1 Byte	**B Side Drop Bus Channel n V1 Byte:** This register is updated every 500 microseconds. This location stores the B side drop bus V1 byte pointer byte for the VT/TU selected. Bit 7 in this register corresponds to bit 1 in the V1 byte.
X+204	7-0	B Side Drop Bus V2 Byte	**B Side Drop Bus Channel n V2 Byte:** This register is updated every 500 microseconds. This location stores the B side drop bus V2 byte pointer byte for the VT/TU selected. Bit 7 in this register corresponds to bit 1 in the V2 byte.
X+205	7-0	B Side Drop Bus V4 Byte	**B Side Drop Bus Channel n V4 Byte:** This register is updated every 500 microseconds. This location stores the B side drop bus V4 byte for the VT/TU selected. Bit 7 in this register corresponds to bit 1 in the V4 byte.
X+206	7-0	B Side Drop Bus V5 Byte	**B Side Drop Bus Channel n V5 Overhead Byte:** This register is updated every 500 microseconds. This location stores the B side drop bus V5 overhead byte for the VT/TU selected. Bit 7 in this register corresponds to bit 1 in the V5 byte.

Address	Bit	Symbol	Description
X+207	7-0	B Side Drop Bus J2 Byte	**B Side Drop Bus Channel n J2 Overhead Byte:** This register is updated every 500 microseconds. This location stores the B side drop bus J2 overhead J2 byte for the VT/TU selected. Bit 7 in this register corresponds to bit 1 in the V5 byte.
X+208	7-0	B Side Drop Bus N2 Byte	**B Side Drop Bus Channel n N2 Overhead Byte:** This register is updated every 500 microseconds. This location stores the B side drop bus N2 overhead byte for the VT/TU selected. Bit 7 in this register corresponds to bit 1 in the N2 byte.
X+209	7-0	B Side Drop Bus K4 Byte	**B Side Drop Bus Channel n K4 Overhead Byte:** This register is updated every 500 microseconds. This location stores the B side drop bus K4 overhead byte for the VT/TU selected. Bit 7 in this register corresponds to bit 1 in the K4 byte.
X+20A	7-0	B Side Drop Bus O-Bits	**B Side Drop Bus Channel n O-bits:** The two nibbles (bits 7-4 and 3-0) in this register correspond to the two sets of four overhead communication bits for the VT/TU selected. Bit 7 corresponds to bit 3 in the first justification control byte, while bit 0 corresponds to bit 6 in the second justification control byte. The two nibbles written into this register location will be from the same frame, updated every 500 microseconds.

PACKAGE INFORMATION

The TEMx28 device is packaged in a 376-lead plastic ball grid array (PBGA) package suitable for surface mounting, as illustrated in Figure 42.



Notes:
1. All dimensions are in millimeters. Values shown are for reference only.
2. Identification of the solder ball A1 corner is contained within this shaded zone. Package corner may not be a 90° angle.
3. Size of array: 22 x 22, JEDEC code MO-151.

Dimension (Note 1)	Min	Max
A A1 A2	2.02 0.40 1.12	2.44 0.60 1.22
A3 (Ref.)	0.56	
b	0.50	0.70
D	23.00	
D1 (Nom)	21.00	
D2	19.45	20.20
E	23.00	
E1 (Nom)	21.00	
E2	19.45	20.20
e (Ref.)	1.00	

Figure 42. TEMx28 TXC-04222 376-Lead Plastic Ball Grid Array Package

ORDERING INFORMATION

Part Number: TXC-04222AIOG 376-lead Plastic Ball Grid Array Package (PBGA)

RELATED PRODUCTS

TXC-03103, QT1F-*Plus* Device (Quad T1 Framer-*Plus*). A 4-channel framer for voice and data applications. This device handles all logical interfacing functionality to a T1 line. This device requires a 5.0 volt supply. The new TXC-03103C device provides the same functionality but can operate either from a 5 volt supply or from a 3.3 volt supply at lower power dissipation.

TXC-03108, T1Fx8 Device (8-Channel T1 Framer). An eight-channel DS1 (1544 kbit/s) framer for voice and data communications applications. This device handles all logical interfacing functionality to a T1 line and operates from a power supply of 3.3 volts.

TXC-03109, E1Fx8 Device (8-Channel E1 Framer). The E1Fx8 is an eight-channel E1 (2048 kbit/s) framer designed with extended features for voice and data communications applications. AMI and HDB3 line codes are supported with full alarm detection and generation per ITU-T G.703, G.775 and I.431.

TXC-03114, QE1F-*Plus* Device (Quad E1 Framer-*Plus*). The QE1F-*Plus* is a four-channel E1 (2048 kbit/s) framer designed for voice and data communications applications. A dual unipolar or NRZ line interface is supported with full alarm detection and generation per ITU-T G.703 and operates from a power supply of 3.3 or 5 volts.

TXC-06103, PHAST-3N Device (SONET/SDH STM-1, STS-3 or STS-3c Overhead Terminator) The PHAST-3N provides a Telecom Bus interface for downstream devices and operates from a power supply of 3.3 volts.

REFERENCE DOCUMENTS

- ITU-T, Bellcore TR-253
- ANSI T1.105

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute
25 West 43rd Street
New York, New York 10036

Tel: (212) 642-4900
Fax: (212) 398-0023
Web: www.ansi.org

The ATM Forum (U.S.A., Europe, Asia):

404 Balboa Street
San Francisco, CA 94118

Tel: (415) 561-6275
Fax: (415) 561-6120
Web: www.atmforum.com

ATM Forum Europe Office

Kingsland House - 5th Floor
361-373 City Road
London EC1 1PQ, England

Tel: 20 7837 7882
Fax: 20 7417 7500

ATM Forum Asia-Pacific Office

Hamamatsucho Suzuki Building 3F
1-2-11, Hamamatsucho, Minato-ku
Tokyo 105-0013, Japan

Tel: 3 3438 3694
Fax: 3 3438 3698

Bellcore (See Telcordia)

CCITT (See ITU-T)

EIA (U.S.A.):

Electronic Industries Association
Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112

Tel: (800) 854-7179 (within U.S.A.)
Tel: (303) 397-7956 (outside U.S.A.)
Fax: (303) 397-2740
Web: www.global.ihs.com

ETSI (Europe):

European Telecommunications Standards Institute
650 route des Lucioles
06921 Sophia-Antipolis Cedex, France

Tel: 4 92 94 42 00
Fax: 4 93 65 47 16
Web: www.etsi.org

GO-MVIP (U.S.A.):

The Global Organization for Multi-Vendor Integration Protocol (GO-MVIP)
3220 N Street NW, Suite 360
Washington, DC 20007

Tel: (800) 669-6857 (within U.S.A.)
Tel: (903) 769-3717 (outside U.S.A.)
Fax: (903) 769-3818
Web: www.mvip.org

ITU-T (International):

Publication Services of International Telecommunication Union
Telecommunication Standardization Sector
Place des Nations, CH 1211
Geneve 20, Switzerland

Tel: 22 730 5852
Fax: 22 730 5853
Web: www.itu.int

JEDEC (International):

Joint Electron Device Engineering Council
2500 Wilson Boulevard
Arlington, VA 22201-3834

Tel: (703) 907-7559
Fax: (703) 907-7583
Web: www.jedec.org

MIL-STD (U.S.A.):

DODSSP Standardization Documents Ordering Desk
Building 4 / Section D
700 Robbins Avenue
Philadelphia, PA 19111-5094

Tel: (215) 697-2179
Fax: (215) 697-1462
Web: www.dodssp.daps.mil

PCI SIG (U.S.A.):

PCI Special Interest Group
5440 SW Westgate Dr., #217
Portland, OR 97221

Tel: (800) 433-5177 (within U.S.A.)
Tel: (503) 291-2569 (outside U.S.A.)
Fax: (503) 297-1090
Web: www.pcisig.com

Telcordia (U.S.A.):

Telcordia Technologies, Inc.
Attention - Customer Service
8 Corporate Place Rm 3A184
Piscataway, NJ 08854-4157

Tel: (800) 521-2673 (within U.S.A.)
Tel: (732) 699-2000 (outside U.S.A.)
Fax: (732) 336-2559
Web: www.telcordia.com

TTC (Japan):

TTC Standard Publishing Group of the Telecommunication Technology Committee
Hamamatsu-cho Suzuki Building
1-2-11, Hamamatsu-cho, Minato-ku
Tokyo 105-0013, Japan

Tel: 3 3432 1551
Fax: 3 3432 1553
Web: www.ttc.or.jp

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated Edition 6 TEMx28 device Data Sheet that have significant differences relative to the Edition 5 TEMx28 device Data Sheet.

Updated TEMx28 device Data Sheet: Edition 6, June 2003

Previous TEMx28 device Data Sheet: *PRELIMINARY* Edition 5, July 2002

The page numbers indicated below of this updated Data Sheet include significant changes relative to the previous data sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date. Deleted all references to PRELIMINARY status, including explanatory text paragraphs on pages 1 and 245.
18	Changed Name/Function for Symbol VDD2.
26	Changed Name/Function for Symbol RDY/$\overline{\text{DTACK}}$.
27	Changed Name/Function for Symbol $\overline{\text{TRS}}$.
28	Changed Note 3 below Absolute Maximum Ratings and Environmental Limitations table.
31	Changed Test Conditions for Parameters V_{OH} and V_{OL} in the first table.
198	Changed “disables” to “enables” in the Descriptions for Address X+005H.
203, 204, 205	Changed “disables” to “enables” in the Descriptions for Addresses X+013H, X+014H, X+015H and X+016H.
203	Changed “AnJ2S1” to “ARnJ2S1” in the Description for Addresses X+143H to X+182H.
221, 222	Changed “disables” to “enables” in the Descriptions for Addresses X+083H, X+084H, X+085H and X+086H.
244	Replaced List of Data Sheet Changes section.

- NOTES -

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