TMXF84622 *Ultramapper* ™
622/155 Mbits/s SONET/SDH x DS3/E3/DS2/DS1/E1/DS0

1 Introduction

The last issue of this data sheet was July 12, 2004 - Revision 9. A change history is included in Section 13, Change History, on page 72. Red change bars have been installed on all text, figures and tables that were added or changed. All changes to the text are highlighted in red. Changes within figures, and the figure title itself, are highlighted in red, if feasible. Formatting or grammatical changes have not been highlighted. Deleted sections, paragraphs, figures or tables will be specifically mentioned.

The documentation package for the TMXF84622 *Ultramapper* 622/155 Mbits/s SONET/SDH x DS3/E3/DS2/DS1/E1/DS0 system chip consists of the following documents:

- The Register Description and the System Design Guide. These two documents are available on a password-protected website.
- The *Ultramapper* Product Description, and the *Ultramapper* Hardware Design Guide (this document). These two documents are available on the public website shown below.

If the reader displays this document using *Acrobat Reader* ®, clicking on any blue text will bring the reader to that reference point.

To access related documents, including the documents mentioned above, please go to the following public website, or contact your Agere representative (see the last page of this document).

http://www.agere.com/enterprise_metro_access/index.html

This document describes the hardware interfaces to the Agere Systems Inc. TMXF84622 *Ultramapper* device. Information relevant to the use of the device in a board design is covered. Pin descriptions, dc electrical characteristics, timing diagrams, ac timing parameters, packaging, and operating conditions are included.

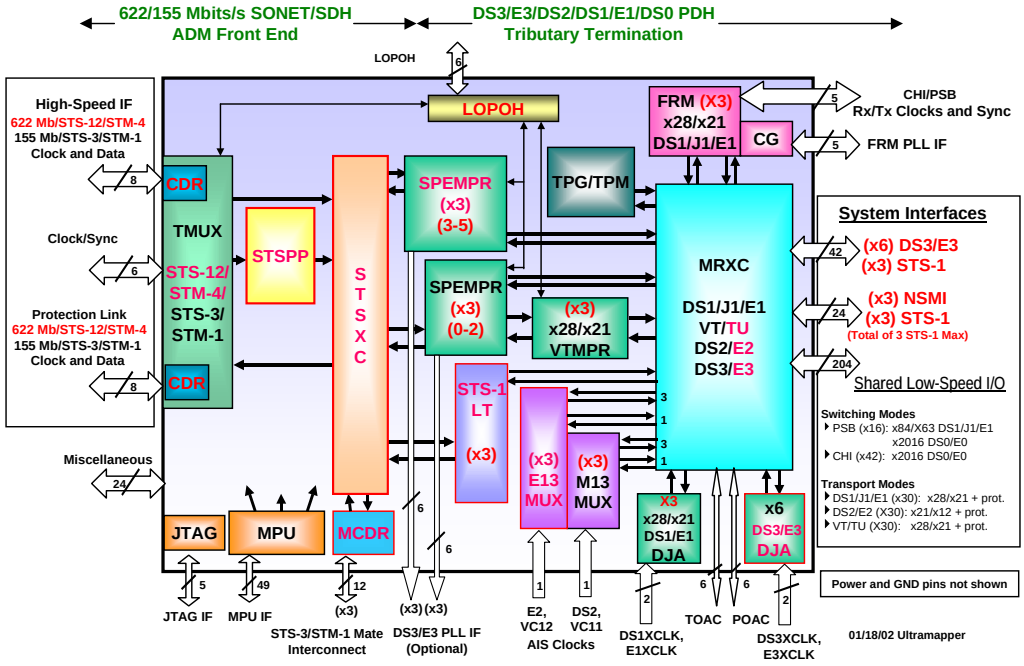

Figure 1-1. *Ultramapper* Block Diagram and High-Level Interface Definition

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2 Pin Information

2.1 Ball Diagram

The TMXF84622 *Ultramapper* is housed in a 700-pin plastic ball grid array. Figure 1-1 shows the ball assignment viewed from the top of the package. The pins are spaced on a 1.0 mm pitch.

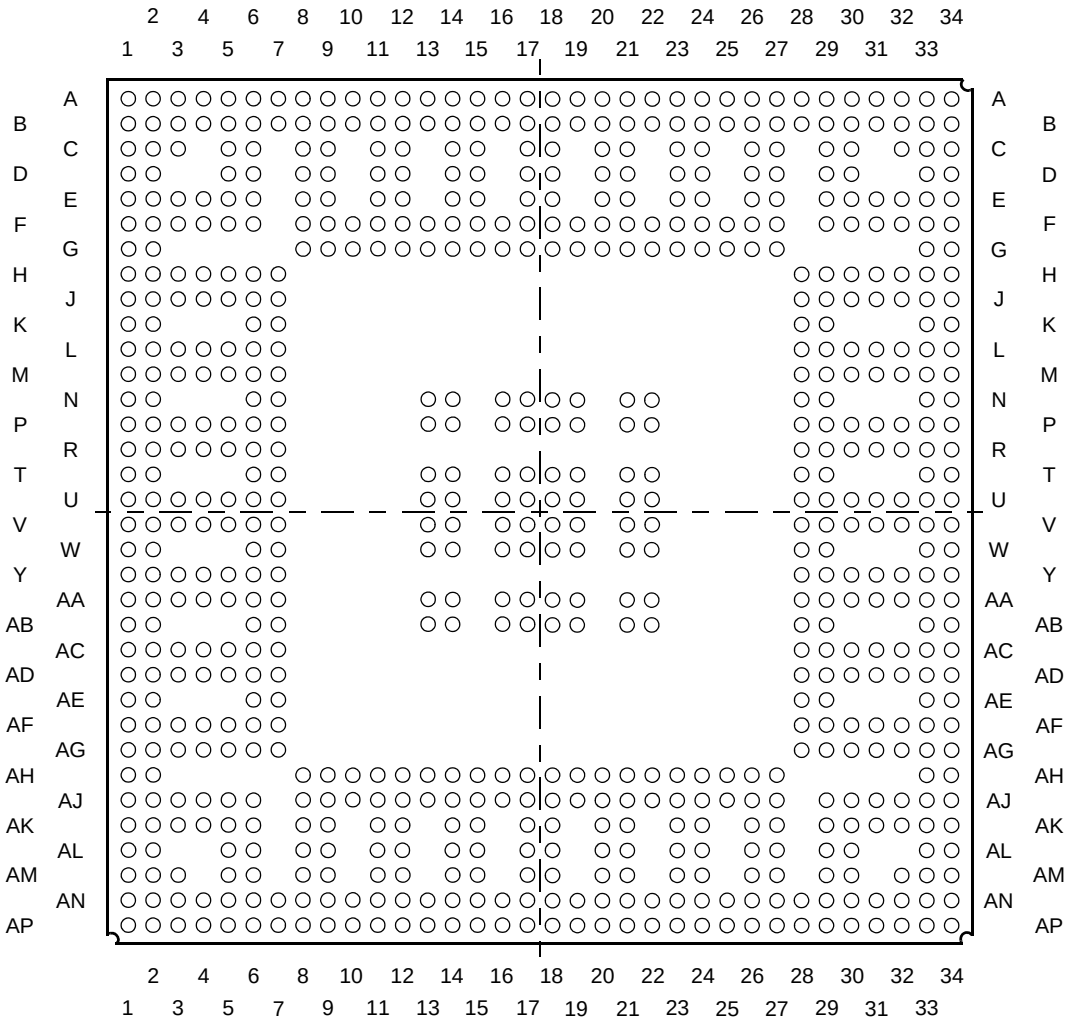


Figure 2-1. *Ultramapper* Package Diagram (Top View)

2.2 Package Pin Assignments

Table 2-1. Package Pin Assignments in Signal Name Order

Signal Name	Pin	Signal Name	Pin
ADDR[0]	E2	CHIRXDATA[21]	R29
ADDR[1]	F3	CHIRXDATA[22]	N34
ADDR[2]	D1	CHIRXDATA[23]	P32
ADDR[3]	H5	CHIRXDATA[24]	N33
ADDR[4]	F2	CHIRXDATA[25]	P30
ADDR[5]	E1	CHIRXDATA[26]	M34
ADDR[6]	G2	CHIRXDATA[27]	P29
ADDR[7]	J6	CHIRXDATA[28]	M33
ADDR[8]	J5	CHIRXDATA[29]	L34
ADDR[9]	F1	CHIRXDATA[30]	M32
ADDR[10]	K6	CHIRXDATA[31]	N29
ADDR[11]	H3	CHIRXDATA[32]	L33
ADDR[12]	H2	CHIRXDATA[33]	K34
ADDR[13]	L6	CHIRXDATA[34]	L32
ADDR[14]	G1	CHIRXDATA[35]	M30
ADDR[15]	J3	CHIRXDATA[36]	J34
ADDR[16]	J2	CHIRXDATA[37]	K33
ADDR[17]	H1	CHIRXDATA[38]	M29
ADDR[18]	L5	CHIRXDATA[39]	L30
ADDR[19]	M6	CHIRXDATA[40]	H34
ADDR[20]	K2	CHIRXDATA[41]	J33
ADSN	D2	CHIRXDATA[42]	J32
APS_INTN	R2	CHIRXGFS	Y33
BYPASS	AJ15	CHIRXGCLK	W29
CG_PLLCLKOUT	AL33	CHIRXGTCLK	Y32
CHIRXDATA[1]	Y34	CHITXDATA[1]	AJ27
CHIRXDATA[2]	V29	CHITXDATA[2]	AN31
CHIRXDATA[3]	W33	CHITXDATA[3]	AP32
CHIRXDATA[4]	W34	CHITXDATA[4]	AK29
CHIRXDATA[5]	V30	CHITXDATA[5]	AJ29
CHIRXDATA[6]	V32	CHITXDATA[6]	AJ30
CHIRXDATA[7]	V33	CHITXDATA[7]	AM34
CHIRXDATA[8]	U33	CHITXDATA[8]	AG30
CHIRXDATA[9]	U32	CHITXDATA[9]	AJ33
CHIRXDATA[10]	U30	CHITXDATA[10]	AK34
CHIRXDATA[11]	T34	CHITXDATA[11]	AH33
CHIRXDATA[12]	T33	CHITXDATA[12]	AF29
CHIRXDATA[13]	U29	CHITXDATA[13]	AF30
CHIRXDATA[14]	R34	CHITXDATA[14]	AJ34
CHIRXDATA[15]	R33	CHITXDATA[15]	AE29
CHIRXDATA[16]	T29	CHITXDATA[16]	AG32
CHIRXDATA[17]	R32	CHITXDATA[17]	AG33
CHIRXDATA[18]	P34	CHITXDATA[18]	AD29
CHIRXDATA[19]	R30	CHITXDATA[19]	AH34
CHIRXDATA[20]	P33	CHITXDATA[20]	AF32

Table 2-1. Package Pin Assignments in Signal Name Order (continued)

Signal Name	Pin	Signal Name	Pin
CHITXDATA[21]	AF33	DATA[15]	R6
CHITXDATA[22]	AG34	DS1XCLK	AK20
CHITXDATA[23]	AD30	DS2AISCLK	R1
CHITXDATA[24]	AC29	DS3DATAINCLK[1]	U5
CHITXDATA[25]	AE33	DS3DATAINCLK[2]	V2
CHITXDATA[26]	AF34	DS3DATAINCLK[3]	W1
CHITXDATA[27]	AC30	DS3DATAINCLK[4]	W2
CHITXDATA[28]	AD32	DS3DATAINCLK[5]	Y3
CHITXDATA[29]	AE34	DS3DATAINCLK[6]	Y5
CHITXDATA[30]	AD33	DS3DATAOUTCLK[1]	Y6
CHITXDATA[31]	AB29	DS3DATAOUTCLK[2]	AC2
CHITXDATA[32]	AC32	DS3DATAOUTCLK[3]	AC3
CHITXDATA[33]	AD34	DS3DATAOUTCLK[4]	AD3
CHITXDATA[34]	AC33	DS3DATAOUTCLK[5]	AG1
CHITXDATA[35]	AA29	DS3DATAOUTCLK[6]	AD6
CHITXDATA[36]	AC34	DS3NEGDATAIN[1]	T1
CHITXDATA[37]	AA30	DS3NEGDATAIN[2]	U2
CHITXDATA[38]	AB33	DS3NEGDATAIN[3]	V5
CHITXDATA[39]	AA32	DS3NEGDATAIN[4]	V6
CHITXDATA[40]	AB34	DS3NEGDATAIN[5]	Y1
CHITXDATA[41]	Y29	DS3NEGDATAIN[6]	AA2
CHITXDATA[42]	AA33	DS3NEGDATAOUT[1]	AB1
CHITXGCLK	Y30	DS3NEGDATAOUT[2]	AA6
CHITXGFS	AA34	DS3NEGDATAOUT[3]	AD2
CLKIN_PLL	AJ32	DS3NEGDATAOUT[4]	AF1
CSN	C1	DS3NEGDATAOUT[5]	AC6
CTAPRH	AK8	DS3NEGDATAOUT[6]	AF3
CTAPRP	AK9	DS3POSDATAIN[1]	T2
CTAPTH	AJ9	DS3POSDATAIN[2]	U3
CTAPTL	AJ13	DS3POSDATAIN[3]	V3
DATA[0]	J1	DS3POSDATAIN[4]	W6
DATA[1]	M5	DS3POSDATAIN[5]	Y2
DATA[2]	L3	DS3POSDATAIN[6]	AA1
DATA[3]	K1	DS3POSDATAOUT[1]	AB2
DATA[4]	L2	DS3POSDATAOUT[2]	AA5
DATA[5]	N6	DS3POSDATAOUT[3]	AD1
DATA[6]	M3	DS3POSDATAOUT[4]	AE1
DATA[7]	L1	DS3POSDATAOUT[5]	AD5
DATA[8]	M2	DS3POSDATAOUT[6]	AF2
DATA[9]	P6	DS3RXCLKOUT[1]	AA3
DATA[10]	M1	DS3RXCLKOUT[2]	AC1
DATA[11]	P5	DS3RXCLKOUT[3]	AB6
DATA[12]	N2	DS3RXCLKOUT[4]	AC5
DATA[13]	P3	DS3RXCLKOUT[5]	AE2
DATA[14]	N1	DS3RXCLKOUT[6]	AH1

Table 2-1. Package Pin Assignments in Signal Name Order (continued)

Signal Name	Pin	Signal Name	Pin
DS3XCLK	A21	LINERXDATA[4]	C17
DSN	E3	LINERXDATA[5]	A16
DTN	P1	LINERXDATA[6]	F17
E1XCLK	AP21	LINERXDATA[7]	B15
E2AISCLK	U6	LINERXDATA[8]	C15
E3XCLK	F18	LINERXDATA[9]	E15
ECSEL	AM15	LINERXDATA[10]	F15
ETOGGLE	AJ16	LINERXDATA[11]	C14
EXDNUP	AL17	LINERXDATA[12]	E14
HP_INTN	R3	LINERXDATA[13]	F14
IC3STATEN	AP24	LINERXDATA[14]	A11
IDDQ	AM24	LINERXDATA[15]	F13
LINERXCLK[1]	A19	LINERXDATA[16]	A10
LINERXCLK[2]	C18	LINERXDATA[17]	E12
LINERXCLK[3]	B17	LINERXDATA[18]	B10
LINERXCLK[4]	E17	LINERXDATA[19]	E11
LINERXCLK[5]	B16	LINERXDATA[20]	B9
LINERXCLK[6]	A15	LINERXDATA[21]	A7
LINERXCLK[7]	F16	LINERXDATA[22]	B8
LINERXCLK[8]	A14	LINERXDATA[23]	F10
LINERXCLK[9]	B14	LINERXDATA[24]	E9
LINERXCLK[10]	A13	LINERXDATA[25]	B7
LINERXCLK[11]	B13	LINERXDATA[26]	B6
LINERXCLK[12]	A12	LINERXDATA[27]	A4
LINERXCLK[13]	B12	LINERXDATA[28]	B5
LINERXCLK[14]	C12	LINERXDATA[29]	F8
LINERXCLK[15]	B11	LINERXDATA[30]	A3
LINERXCLK[16]	C11	LINETXCLK[1]	L29
LINERXCLK[17]	A9	LINETXCLK[2]	H32
LINERXCLK[18]	F12	LINETXCLK[3]	F34
LINERXCLK[19]	A8	LINETXCLK[4]	J29
LINERXCLK[20]	C9	LINETXCLK[5]	E34
LINERXCLK[21]	F11	LINETXCLK[6]	H30
LINERXCLK[22]	C8	LINETXCLK[7]	F32
LINERXCLK[23]	A6	LINETXCLK[8]	E32
LINERXCLK[24]	F9	LINETXCLK[9]	D33
LINERXCLK[25]	A5	LINETXCLK[10]	F30
LINERXCLK[26]	E8	LINETXCLK[11]	F29
LINERXCLK[27]	C6	LINETXCLK[12]	A32
LINERXCLK[28]	C5	LINETXCLK[13]	F27
LINERXCLK[29]	B4	LINETXCLK[14]	B30
LINERXCLK[30]	E6	LINETXCLK[15]	A31
LINERXDATA[1]	B19	LINETXCLK[16]	B29
LINERXDATA[2]	E18	LINETXCLK[17]	B28
LINERXDATA[3]	B18	LINETXCLK[18]	E26

Table 2-1. Package Pin Assignments in Signal Name Order (continued)

Signal Name	Pin	Signal Name	Pin
LINETXCLK[19]	F25	LOPOHVALIDIN	A22
LINETXCLK[20]	B27	LOPOHVALIDOUT	E20
LINETXCLK[21]	A28	LOSEXT	AN21
LINETXCLK[22]	B26	LP_INTN	T6
LINETXCLK[23]	E24	MODE0_PLL	AG29
LINETXCLK[24]	B25	MODE1_PLL	AK32
LINETXCLK[25]	E23	MODE2_PLL	AK30
LINETXCLK[26]	A25	MPCLK	F5
LINETXCLK[27]	F22	MPMODE	F6
LINETXCLK[28]	A24	NSMIRXCLK[1]	AP26
LINETXCLK[29]	F21	NSMIRXCLK[2]	AP27
LINETXCLK[30]	E21	NSMIRXCLK[3]	AJ24
LINETXDATA[1]	G34	NSMIRXDATA[1]	AK23
LINETXDATA[2]	H33	NSMIRXDATA[2]	AK24
LINETXDATA[3]	K29	NSMIRXDATA[3]	AP28
LINETXDATA[4]	J30	NSMIRXSYNC[1]	AN25
LINETXDATA[5]	G33	NSMIRXSYNC[2]	AN26
LINETXDATA[6]	F33	NSMIRXSYNC[3]	AN27
LINETXDATA[7]	D34	NSMITXCLK[1]	AP29
LINETXDATA[8]	E33	NSMITXCLK[2]	AP30
LINETXDATA[9]	H29	NSMITXCLK[3]	AM29
LINETXDATA[10]	C34	NSMITXDATA[1]	AJ25
LINETXDATA[11]	E30	NSMITXDATA[2]	AN28
LINETXDATA[12]	E29	NSMITXDATA[3]	AP31
LINETXDATA[13]	B31	NSMITXSYNC[1]	AK26
LINETXDATA[14]	C30	NSMITXSYNC[2]	AN29
LINETXDATA[15]	C29	NSMITXSYNC[3]	AN30
LINETXDATA[16]	E27	PAR[0]	P2
LINETXDATA[17]	A30	PAR[1]	R5
LINETXDATA[18]	F26	PHASEDETDOWN[1]	AG3
LINETXDATA[19]	A29	PHASEDETDOWN[2]	AG5
LINETXDATA[20]	C27	PHASEDETDOWN[3]	AF6
LINETXDATA[21]	F24	PHASEDETDOWN[4]	AK1
LINETXDATA[22]	C26	PHASEDETDOWN[5]	AJ1
LINETXDATA[23]	A27	PHASEDETDOWN[6]	AJ3
LINETXDATA[24]	F23	PHASEDETUP[1]	AG2
LINETXDATA[25]	A26	PHASEDETUP[2]	AE6
LINETXDATA[26]	C24	PHASEDETUP[3]	AF5
LINETXDATA[27]	B24	PHASEDETUP[4]	AH2
LINETXDATA[28]	C23	PHASEDETUP[5]	AJ2
LINETXDATA[29]	B23	PHASEDETUP[6]	AL1
LINETXDATA[30]	A23	PMRST	AM21
LOPOHCLKIN	B22	REF10	AJ6
LOPOHCLKOUT	F20	REF14	AK6
LOPOHDATAIN	C21	RESHI	AP3
LOPOHDATAOUT	B21	RESLO	AJ8

Table 2-1. Package Pin Assignments in Signal Name Order (continued)

Signal Name	Pin	Signal Name	Pin
RHSCN	AN5	TLSDATAP[2]	AN15
RHSCP	AN4	TLSDATAP[3]	AN17
RHSDN	AM6	TMS	AP23
RHSDP	AM5	TPOACCLK	AN20
RHSFSYNCN	AJ20	TPOACDATA	AJ19
RLSCLK	AK15	TPOACSYNC	AM20
RLSDATAN[1]	AP14	TPSCN	AP9
RLSDATAN[2]	AP16	TPSCP	AP8
RLSDATAN[3]	AP18	TPSDN	AP11
RLSDATAP[1]	AP13	TPSDP	AP10
RLSDATAP[2]	AP15	TRST	AJ21
RLSDATAP[3]	AP17	TSTMODE	AK17
RPOACCLK	AN19	TSTPHASE	AJ14
RPOACDATA	AJ18	TSTSFTLD	AM14
RPOACSYNC	AP20	TTOACCLK	AL18
RPSCN	AN11	TTOACDATA	AP19
RPSCP	AN10	TTOACSYNC	AK18
RPSDN	AM9	TXDATAEN[1]	AJ26
RPSDP	AM8	TXDATAEN[2]	AK27
RSTN	AP22	TXDATAEN[3]	AM30
RTOACCLK	AM17	V_{DD15}	G9
RTOACDATA	AJ17	V_{DD15}	G10
RTOACSYNC	AM18	V_{DD15}	G11
RWN	H6	V_{DD15}	G12
RXDATAEN[1]	AJ23	V_{DD15}	G13
RXDATAEN[2]	AM26	V_{DD15}	G14
RXDATAEN[3]	AM27	V_{DD15}	G15
SCAN_EN	AN24	V_{DD15}	G16
SCANMODE	AP25	V_{DD15}	G19
SCK1	AM23	V_{DD15}	G20
SCK2	AJ22	V_{DD15}	G21
TCK	AN22	V_{DD15}	G22
TDI	AK21	V_{DD15}	G23
TDO	AN23	V_{DD15}	G24
THSCN	AP7	V_{DD15}	G25
THSCON	AP5	V_{DD15}	G26
THSCOP	AP4	V_{DD15}	J7
THSCP	AP6	V_{DD15}	J28
THSDN	AN8	V_{DD15}	K7
THSDP	AN7	V_{DD15}	K28
THSSYNC	AL15	V_{DD15}	L7
TLSCLK	AL14	V_{DD15}	L28
TLSDATAN[1]	AN14	V_{DD15}	M7
TLSDATAN[2]	AN16	V_{DD15}	M28
TLSDATAN[3]	AN18	V_{DD15}	N7
TLSDATAP[1]	AN13	V_{DD15}	N16

Table 2-1. Package Pin Assignments in Signal Name Order (continued)

Signal Name	Pin	Signal Name	Pin
VDD15	N17	VDD15	AC7
VDD15	N18	VDD15	AC28
VDD15	N19	VDD15	AD7
VDD15	N28	VDD15	AD28
VDD15	P7	VDD15	AE7
VDD15	P16	VDD15	AE28
VDD15	P17	VDD15	AF7
VDD15	P18	VDD15	AF28
VDD15	P19	VDD15	AH9
VDD15	P28	VDD15	AH10
VDD15	R7	VDD15	AH11
VDD15	R28	VDD15	AH12
VDD15	T7	VDD15	AH13
VDD15	T13	VDD15	AH14
VDD15	T14	VDD15	AH15
VDD15	T21	VDD15	AH16
VDD15	T22	VDD15	AH19
VDD15	T28	VDD15	AH20
VDD15	U13	VDD15	AH21
VDD15	U14	VDD15	AH22
VDD15	U21	VDD15	AH23
VDD15	U22	VDD15	AH24
VDD15	V13	VDD15	AH25
VDD15	V14	VDD15	AH26
VDD15	V21	VDD15A_CDR1	AK11
VDD15	V22	VDD15A_CDR2	AJ10
VDD15	W7	VDD15A_DS3PLL	C20
VDD15	W13	VDD15A_E3PLL	B20
VDD15	W14	VDD15A_X4PLL	AK14
VDD15	W21	VDD33	A2
VDD15	W22	VDD33	A33
VDD15	W28	VDD33	B1
VDD15	Y7	VDD33	B3
VDD15	Y28	VDD33	B32
VDD15	AA7	VDD33	B34
VDD15	AA16	VDD33	C2
VDD15	AA17	VDD33	C33
VDD15	AA18	VDD33	D5
VDD15	AA19	VDD33	D8
VDD15	AA28	VDD33	D11
VDD15	AB7	VDD33	D14
VDD15	AB16	VDD33	D17
VDD15	AB17	VDD33	D20
VDD15	AB18	VDD33	D23
VDD15	AB19	VDD33	D26
VDD15	AB28	VDD33	D29

Table 2-1. Package Pin Assignments in Signal Name Order (continued)

Signal Name	Pin	Signal Name	Pin
VDD33	E31	VDD33	AN34
VDD33	F4	VDD33	AP2
VDD33	G8	VDD33	AP33
VDD33	G17	VDD33A_SFPLL	AK33
VDD33	G18	VSS	A1
VDD33	G27	VSS	A17
VDD33	H7	VSS	A18
VDD33	H28	VSS	A34
VDD33	H31	VSS	B2
VDD33	J4	VSS	B33
VDD33	L31	VSS	C3
VDD33	M4	VSS	C32
VDD33	P31	VSS	D6
VDD33	R4	VSS	D9
VDD33	U7	VSS	D12
VDD33	U28	VSS	D15
VDD33	U31	VSS	D18
VDD33	V4	VSS	D21
VDD33	V7	VSS	D24
VDD33	V28	VSS	D27
VDD33	Y31	VSS	D30
VDD33	AA4	VSS	E4
VDD33	AC31	VSS	E5
VDD33	AD4	VSS	F31
VDD33	AF31	VSS	H4
VDD33	AG4	VSS	J31
VDD33	AG7	VSS	L4
VDD33	AG28	VSS	M31
VDD33	AH8	VSS	N13
VDD33	AH17	VSS	N14
VDD33	AH18	VSS	N21
VDD33	AH27	VSS	N22
VDD33	AJ31	VSS	P4
VDD33	AK4	VSS	P13
VDD33	AL6	VSS	P14
VDD33	AL9	VSS	P21
VDD33	AL12	VSS	P22
VDD33	AL21	VSS	R31
VDD33	AL24	VSS	T16
VDD33	AL27	VSS	T17
VDD33	AL30	VSS	T18
VDD33	AM2	VSS	T19
VDD33	AM33	VSS	U1
VDD33	AN1	VSS	U4
VDD33	AN3	VSS	U16
VDD33	AN32	VSS	U17

Table 2-1. Package Pin Assignments in Signal Name Order (continued)

Signal Name	Pin	Signal Name	Pin
VSS	U18	VSS	AK2
VSS	U19	VSS	AK3
VSS	U34	VSS	AK5
VSS	V1	VSS	AK31
VSS	V16	VSS	AL2
VSS	V17	VSS	AL5
VSS	V18	VSS	AL8
VSS	V19	VSS	AL11
VSS	V31	VSS	AL20
VSS	V34	VSS	AL23
VSS	W16	VSS	AL26
VSS	W17	VSS	AL29
VSS	W18	VSS	AM1
VSS	W19	VSS	AM3
VSS	Y4	VSS	AM11
VSS	AA13	VSS	AM12
VSS	AA14	VSS	AM32
VSS	AA21	VSS	AN2
VSS	AA22	VSS	AN6
VSS	AA31	VSS	AN9
VSS	AB13	VSS	AN12
VSS	AB14	VSS	AN33
VSS	AB21	VSS	AP1
VSS	AB22	VSS	AP12
VSS	AC4	VSS	AP34
VSS	AD31	VSSA_CDR1	AK12
VSS	AF4	VSSA_CDR2	AJ12
VSS	AG6	VSSA_DS3PLL	F19
VSS	AG31	VSSA_E3PLL	A20
VSS	AJ4	VSSA_SFPLL	AL34
VSS	AJ5	VSSA_X4PLL	AJ11

2.3 Pin Matrix

Table 2-2. Package Pin Matrix

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	VSS	VDD33	LINERXDATA[30]	LINERXDATA [27]	LINERXCLK[25]	LINERXCLK[23]	LINERXDATA [21]	LINERXCLK[19]	LINERXCLK[17]	LINERXDATA [16]	LINERXDATA [14]	LINERXCLK[12]	LINERXCLK[10]	LINERXCLK[8]	LINERXCLK[6]	LINERXDATA[5]	VSS
B	VDD33	VSS	VDD33	LINERXCLK [29]	LINERXDATA[28]	LINERXDATA[26]	LINERXDATA [25]	LINERXDATA [22]	LINERXDATA [20]	LINERXDATA [18]	LINERXCLK [15]	LINERXCLK[13]	LINERXCLK[11]	LINERXCLK[9]	LINERXDATA[7]	LINERXCLK[5]	LINERXCLK[3]
C	CSN	VDD33	VSS	—	LINERXCLK[28]	LINERXCLK[27]	—	LINERXCLK[22]	LINERXCLK[20]	—	LINERXCLK [16]	LINERXCLK[14]	—	LINERXDATA [11]	LINERXDATA[8]	—	LINERXDATA[4]
D	ADDR[2]	ADSN	—	—	VDD33	VSS	—	VDD33	VSS	—	VDD33	VSS	—	VDD33	VSS	—	VDD33
E	ADDR[5]	ADDR[0]	DSN	VSS	VSS	LINERXCLK[30]	—	LINERXCLK[26]	LINERXDATA [24]	—	LINERXDATA [19]	LINERXDATA [17]	—	LINERXDATA [12]	LINERXDATA[9]	—	LINERXCLK[4]
F	ADDR[9]	ADDR[4]	ADDR[1]	VDD33	MPCLK	MPMODE	—	LINERXDATA [29]	LINERXCLK [24]	LINERXDATA [23]	LINERXCLK [21]	LINERXCLK [18]	LINERXDATA [15]	LINERXDATA [13]	LINERXDATA [10]	LINERXCLK[7]	LINERXDATA[6]
G	ADDR[14]	ADDR[6]	—	—	—	—	—	VDD33	VDD15	VDD15	VDD15	VDD15	VDD15	VDD15	VDD15	VDD15	VDD33
H	ADDR[17]	ADDR[12]	ADDR[11]	VSS	ADDR[3]	RWN	VDD33	—	—	—	—	—	—	—	—	—	—
J	DATA[0]	ADDR[16]	ADDR[15]	VDD33	ADDR[8]	ADDR[7]	VDD15	—	—	—	—	—	—	—	—	—	—
K	DATA[3]	ADDR[20]	—	—	—	ADDR[10]	VDD15	—	—	—	—	—	—	—	—	—	—
L	DATA[7]	DATA[4]	DATA[2]	VSS	ADDR[18]	ADDR[13]	VDD15	—	—	—	—	—	—	—	—	—	—
M	DATA[10]	DATA[8]	DATA[6]	VDD33	DATA[1]	ADDR[19]	VDD15	—	—	—	—	—	—	—	—	—	—
N	DATA[14]	DATA[12]	—	—	—	DATA[5]	VDD15	—	—	—	—	—	VSS	VSS	—	VDD15	VDD15
P	DTN	PAR[0]	DATA[13]	VSS	DATA[11]	DATA[9]	VDD15	—	—	—	—	—	VSS	VSS	—	VDD15	VDD15
R	DS2AISCLK	APS_INTN	HP_INTN	VDD33	PAR[1]	DATA[15]	VDD15	—	—	—	—	—	—	—	—	—	—
T	DS3NEGDATAIN[1]	DS3POSDATAIN[1]	—	—	—	LP_INTN	VDD15	—	—	—	—	—	VDD15	VDD15	—	VSS	VSS
U	VSS	DS3NEGDATAIN[2]	DS3POSDATAIN[2]	VSS	DS3DATAINCLK[1]	E2AISCLK	VDD33	—	—	—	—	—	VDD15	VDD15	—	VSS	VSS
V	VSS	DS3DATAINCLK[2]	DS3POSDATAIN[3]	VDD33	DS3NEGDATAIN[3]	DS3NEGDATAIN[4]	VDD33	—	—	—	—	—	VDD15	VDD15	—	VSS	VSS
W	DS3DATAINCLK[3]	DS3DATAINCLK[4]	—	—	—	DS3POSDATAIN[4]	VDD15	—	—	—	—	—	VDD15	VDD15	—	VSS	VSS
Y	DS3NEGDATAIN[5]	DS3POSDATAIN[5]	DS3DATAINCLK[5]	VSS	DS3DATAINCLK[6]	DS3DATAOUTCLK[1]	VDD15	—	—	—	—	—	—	—	—	—	—
AA	DS3POSDATAIN[6]	DS3NEGDATAIN[6]	DS3RXCLKOUT[1]	VDD33	DS3POSDATAOUT[2]	DS3NEGDATAOUT[2]	VDD15	—	—	—	—	—	VSS	VSS	—	VDD15	VDD15
AB	DS3NEGDATAOUT [1]	DS3POSDATAOUT [1]	—	—	—	DS3RXCLKOUT[3]	VDD15	—	—	—	—	—	VSS	VSS	—	VDD15	VDD15
AC	DS3RXCLKOUT[2]	DS3DATAOUTCLK [2]	DS3DATAOUTCLK [3]	VSS	DS3RXCLKOUT[4]	DS3NEGDATAOUT[5]	VDD15	—	—	—	—	—	—	—	—	—	
AD	DS3POSDATAOUT [3]	DS3NEGDATAOUT [3]	DS3DATAOUTCLK [4]	VDD33	DS3POSDATAOUT[5]	DS3DATAOUTCLK[6]	VDD15	—	—	—	—	—	—	—	—	—	—
AE	DS3POSDATAOUT [4]	DS3RXCLKOUT[5]	—	—	—	PHASEDETUP[2]	VDD15	—	—	—	—	—	—	—	—	—	—
AF	DS3NEGDATAOUT [4]	DS3POSDATAOUT [6]	DS3NEGDATAOUT [6]	VSS	PHASEDETUP[3]	PHASEDETDOWN[3]	VDD15	—	—	—	—	—	—	—	—	—	—
AG	DS3DATAOUTCLK [5]	PHASEDETUP[1]	PHASEDETDOWN [1]	VDD33	PHASEDETDOWN[2]	VSS	VDD33	—	—	—	—	—	—	—	—	—	—
AH	DS3RXCLKOUT[6]	PHASEDETUP[4]	—	—	—	—	—	VDD33	VDD15	VDD15	VDD15	VDD15	VDD15	VDD15	VDD15	VDD15	VDD33
AJ	PHASEDETDOWN [5]	PHASEDETUP[5]	PHASEDETDOWN [6]	VSS	VSS	REF10	—	RESLO	CTAPTH	VDD15A_CDR2	VSSA_X4PLL	VSSA_CDR2	CTAPTL	TSTPHASE	BYPASS	ETOGGLE	RTOACDATA
AK	PHASEDETDOWN [4]	VSS	VSS	VDD33	VSS	REF14	—	CTAPRH	CTAPRP	—	VDD15A_CDR1	VSSA_CDR1	—	VDD15A_X4PLL	RLSCLK	—	TSTMODE
AL	PHASEDETUP[6]	VSS	—	—	VSS	VDD33	—	VSS	VDD33	—	VSS	VDD33	—	TLSCLK	THSSYNC	—	EXDNUP
AM	VSS	VDD33	VSS	—	RHSDP	RHSDN	—	RPSDP	RPSDN	—	VSS	VSS	—	TSTSFTLD	ECSEL	—	RTOACCLK
AN	VDD33	VSS	VDD33	RHSCP	RHSCN	VSS	THSDP	THSDN	VSS	RPSCP	RPSCN	VSS	TLSDATAP[1]	TLSDATAN[1]	TLSDATAP[2]	TLSDATAN[2]	TLSDATAP[3]
AP	VSS	VDD33	RESHI	THSCOP	THSCON	THSCP	THSCN	TPSCP	TPSCN	TPSDP	TPSDN	VSS	RLSDATAP[1]	RLSDATAN[1]	RLSDATAP[2]	RLSDATAN[2]	RLSDATAP[3]

Table 2-2. Package Pin Matrix (continued)

	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
A	VSS	LINERXCLK[1]	VSSA_E3PLL	DS3XCLK	LOPOHVALIDIN	LINETXDATA[30]	LINETXCLK [28]	LINETXCLK[26]	LINETXDATA [25]	LINETXDATA [23]	LINETXCLK[21]	LINETXDATA [19]	LINETXDATA [17]	LINETXCLK[15]	LINETXCLK[12]	VDD33	VSS
B	LINERXDATA[3]	LINERXDATA[1]	VDD15A_E3PLL	LOPO-HDATAOUT	LOPOHCLKIN	LINETXDATA[29]	LINETXDATA [27]	LINETXCLK[24]	LINETXCLK[22]	LINETXCLK[20]	LINETXCLK[17]	LINETXLCK[16]	LINETXCLK[14]	LINETXDATA [13]	VDD33	VSS	VDD33
C	LINERXCLK[2]	—	VDD15A_DS3PLL	LOPO-HDATAIN	—	LINETXDATA[28]	LINETXDATA [26]	—	LINETXDATA [22]	LINETXDATA [20]	—	LINETXDATA [15]	LINETXDATA [14]	—	VSS	VDD33	LINETXDATA [10]
D	VSS	—	VDD33	VSS	—	VDD33	VSS	—	VDD33	VSS	—	VDD33	VSS	—	—	LINETXCLK[9]	LINETXDATA[7]
E	LINERXDATA[2]	—	LOPOHVALIDOUT	LINETXCLK [30]	—	LINETXCLK[25]	LINETXCLK [23]	—	LINETXCLK[18]	LINETXDATA [16]	—	LINETXDATA [12]	LINETXDATA [11]	VDD33	LINETXCLK[8]	LINETXDATA[8]	LINETXCLK[5]
F	E3XCLK	VSSA_DS3PLL	LOPOHCLKOUT	LINETXCLK [29]	LINETXCLK[27]	LINETXDATA[24]	LINETXDATA [21]	LINETXCLK [19]	LINETXDATA [18]	LINETXCLK[13]	—	LINETXCLK[11]	LINETXCLK[10]	VSS	LINETXCLK[7]	LINETXDATA[6]	LINETXCLK[3]
G	VDD33	VDD15	VDD15	VDD15	VDD15	VDD15	VDD15	VDD15	VDD15	VDD33	—	—	—	—	—	LINETXDATA[5]	LINETXDATA[1]
H	—	—	—	—	—	—	—	—	—	—	VDD33	LINETXDATA[9]	LINETXCLK[6]	VDD33	LINETXCLK[2]	LINETXDATA[2]	CHIRXDATA[40]
J	—	—	—	—	—	—	—	—	—	—	VDD15	LINETXCLK[4]	LINETXDATA[4]	VSS	CHIRXDATA[42]	CHIRXDATA[41]	CHIRXDATA[36]
K	—	—	—	—	—	—	—	—	—	—	VDD15	LINETXDATA[3]	—	—	—	CHIRXDATA[37]	CHIRXDATA[33]
L	—	—	—	—	—	—	—	—	—	—	VDD15	LINETXCLK[1]	CHIRXDATA[39]	VDD33	CHIRXDATA[34]	CHIRXDATA[32]	CHIRXDATA[29]
M	—	—	—	—	—	—	—	—	—	—	VDD15	CHIRXDATA[38]	CHIRXDATA[35]	VSS	CHIRXDATA[30]	CHIRXDATA[28]	CHIRXDATA[26]
N	VDD15	VDD15	—	VSS	VSS	—	—	—	—	—	VDD15	CHIRXDATA[31]	—	—	—	CHIRXDATA[24]	CHIRXDATA[22]
P	VDD15	VDD15	—	VSS	VSS	—	—	—	—	—	VDD15	CHIRXDATA[27]	CHIRXDATA[25]	VDD33	CHIRXDATA[23]	CHIRXDATA[20]	CHIRXDATA[18]
R	—	—	—	—	—	—	—	—	—	—	VDD15	CHIRXDATA[21]	CHIRXDATA[19]	VSS	CHIRXDATA[17]	CHIRXDATA[15]	CHIRXDATA[14]
T	VSS	VSS	—	VDD15	VDD15	—	—	—	—	—	VDD15	CHIRXDATA[16]	—	—	—	CHIRXDATA[12]	CHIRXDATA[11]
U	VSS	VSS	—	VDD15	VDD15	—	—	—	—	—	VDD33	CHIRXDATA[13]	CHIRXDATA[10]	VDD33	CHIRXDATA[9]	CHIRXDATA[8]	VSS
V	VSS	VSS	—	VDD15	VDD15	—	—	—	—	—	VDD33	CHIRXDATA[2]	CHIRXDATA[5]	VSS	CHIRXDATA[6]	CHIRXDATA[7]	VSS
W	VSS	VSS	—	VDD15	VDD15		—	—	—	—	VDD15	CHIRXGCLK	—	—	—	CHIRXDATA[3]	CHIRXDATA[4]
Y	—	—	—			—	—	—	—	—	VDD15	CHITXDATA[41]	CHITXGCLK	VDD33	CHIRXGTCLK	CHIRXGFS	CHIRXDATA[1]
AA	VDD15	VDD15	—	VSS	VSS	—	—	—	—	—	VDD15	CHITXDATA[35]	CHITXDATA[37]	VSS	CHITXDATA[39]	CHITXDATA[42]	CHITXGFS
AB	VDD15	VDD15	—	VSS	VSS	—	—	—	—	—	VDD15	CHITXDATA[31]	—	—	—	CHITXDATA[38]	CHITXDATA[40]
AC	—	—	—	—	—	—	—	—	—	—	VDD15	CHITXDATA[24]	CHITXDATA[27]	VDD33	CHITXDATA[32]	CHITXDATA[34]	CHITXDATA[36]
AD	—	—	—	—	—	—	—	—	—	—	VDD15	CHITXDATA[18]	CHITXDATA[23]	VSS	CHITXDATA[28]	CHITXDATA[30]	CHITXDATA[33]
AE	—	—	—	—	—	—	—	—	—	—	VDD15	CHITXDATA[15]	—	—	—	CHITXDATA[25]	CHITXDATA[29]
AF	—	—	—	—	—	—	—	—	—	—	VDD15	CHITXDATA[12]	CHITXDATA[13]	VDD33	CHITXDATA[20]	CHITXDATA[21]	CHITXDATA[26]
AG	—	—	—	—	—	—	—	—	—	—	VDD33	MODE0_PLL	CHITXDATA[8]	VSS	CHITXDATA[16]	CHITXDATA[17]	CHITXDATA[22]
AH	VDD33	VDD15	VDD15	VDD15	VDD15	VDD15	VDD15	VDD15	VDD15	VDD33	—	—	—	—	—	CHITXDATA[11]	CHITXDATA[19]
AJ	RPOACDATA	TPOACDATA	RHSFSYNCN	TRST	SCK2	RXDATAEN[1]	NSMIRX-CLK[3]	NSMITXDATA[1]	TXDATAEN[1]	CHITXDATA[1]	—	CHITXDATA[5]	CHITXDATA[6]	VDD33	CLKIN_PLL	CHITXDATA[9]	CHITXDATA[14]
AK	TTOACSYNC	—	DS1XCLK	TDI	—	NSMIRXDATA[1]	NSMIRX-DATA[2]	—	NSMITX-SYNC[1]	TXDATAEN[2]	—	CHITXDATA[4]	MODE2_PLL	VSS	MODE1_PLL	VDD33A_SFPLL	CHITXDATA[10]
AL	TTOACCLK	—	VSS	VDD33	—	VSS	VDD33	—	VSS	VDD33	—	VSS	VDD33	—	—	CG_PLLCLKOUT	VSSA_SFPLL
AM	RTOACSYNC	—	TPOACSYNC	PMRST	—	SCK1	IDDQ	—	RXDATAEN[2]	RXDATAEN[3]	—	NMITXCLK[3]	TXDATAEN[3]	—	VSS	VDD33	CHITXDATA[7]
AN	TLSDATAN[3]	RPOACCLK	TPOACCLK	LOSEXT	TCK	TDO	SCAN_EN	NSMIRXSYNC [1]	NSMIRXSYNC [2]	NSMIRXSYNC [3]	NSMITXDATA[2]	NSMITXSYNC [2]	NSMITXSYNC [3]	CHITXDATA[2]	VDD33	VSS	VDD33
AP	RLSDATAN[3]	TTOACDATA	RPOACSYNC	E1XCLK	RSTN	TMS	IC3STATEN	SCANMODE	NSMIRXCLK[1]	NSMIRXCLK[2]	NSMIRXDATA [3]	NSMITXCLK[1]	NSMITXCLK[2]	NSMITXDATA[3]	CHITXDATA[3]	VDD33	VSS

2.4 Pin Types

Table 2-3 describes each type of input, output, and I/O pin used in the *Ultramapper*.

Table 2-3. Pin Types

Type Label	Description
I	**LVCMOS Input, LVTTL Switching Thresholds.**
I pd	**LVCMOS Input, LVTTL Switching Thresholds with Internal 50 kΩ Pull-Down Resistor.**
I pu	**LVCMOS Input, LVTTL Switching Thresholds with Internal 50 kΩ Pull-Up Resistor.**
O	**LVCMOS Output.**
O od	**Open Drain Output.**
LIN	**LVDS Inputs.**
LOUT	**LVDS Outputs.**
I/O	**Bidirectional Pin.** LVCMOS input with LVTTL switching thresholds and LVCMOS output.
I/O pd	**Bidirectional Pin.** LVCMOS input with LVTTL switching thresholds with internal 50 kΩ pull-down resistor and LVCMOS output.
—	**Power, Ground, Analog Inputs for External Resistors, Capacitors, Voltage References, etc.**

2.5 Pin Definitions

This section describes the function of each of the device pins. All LVDS input buffers have built-in 100 Ω terminating resistor with a center tap pin available for external capacitor connection. All unused LVDS inputs may be left unconnected. Pin functionality is descriptive information. The actual functionality is dependent upon the device configuration via the registers.

Table 2-4. TMUX Block, High-Speed Interface I/O

Pin	Symbol	Type	Name/Description
AM5	RHSDP	LIN	**Receive High-Speed Data.** 622/155 Mbits/s input data. Also, input to internal clock and data recovery (CDR). CDR may be bypassed in 155 Mbits/s mode. In 622 Mbits/s mode, the internal CDR must be used.
AM6	RHSDN		
AN4	RHSCP	LIN	**Receive High-Speed Clock.** 155 MHz input clock for 155 Mbits/s data if CDR is bypassed. Not used in 622 Mbits/s mode.
AN5	RHSCN		
AK8	CTAPRH	—	**Center Tap RH.** LVDS buffer terminator center tap for RHSDP/N and RHSCP/N. An optional 0.1 µF capacitor, connected between CTAP pin and ground, will improve the common-mode rejection of the LVDS input buffers.
AN21	LOSEXT	I pu	**External Loss of Signal Input.** Active level is programmable by register TMUX_LOSEXT_LEVEL. Default to active-low. This pin can be part of the high-priority interrupt when active. Usually connected to optical transceiver to indicate loss of signal.
AN7	THSDP	LOUT	**Transmit High-Speed Data.** 622/155 Mbits/s output data. The frame location in slave mode is determined by THSSYNC and transmit high-speed control parameter register (TMUX_TFRAMEOFFSETA). In master mode the frame timing is arbitrary.
AN8	THSDN		
AP4	THSCOP	LOUT	**Transmit High-Speed Clock Output.** 622/155 MHz transmit output clock associated with THSDP/N.
AP5	THSCON		
AP3, AJ8	RESHI, RESLO	—	**Resistor.** A 100 Ω, 1% resistor is required between RESHI and RESLO pins as a reference for the LVDS input buffer termination.
AJ6	REF10*	I	**Reference 1.0 V.** External 1 V reference voltage pin. (Optional).
AK6	REF14*	I	**Reference 1.4 V.** External 1.4 V reference voltage pin. (Optional).

* Optional: selected by MPU/top-level register UMPR_LVDS_REF_SEL. External reference voltage can be sourced from a low-impedance resistor (less than 1 kΩ) divider circuit decoupled with a 0.1 µF capacitor. Please refer to Table 4-4 LVDS Interface dc Characteristics, on page 40 for additional information.

Table 2-5. TMUX Block, Protection Link I/O

Pin	Symbol	Type	Name/Description
AM8	RPSDP	LIN	**Receive Protection High-Speed Data.** 622/155 Mbits/s protection input data. Also input to internal protection CDR. CDR may be bypassed in 155 Mbits/s mode. In 622 Mbits/s mode, the internal CDR must be used.
AM9	RPSDN		
AN10	RPSCP	LIN	**Receive Protection High-Speed Clock.** 155 MHz input clock for 155 Mbits/s data if protection CDR is bypassed. Not used in 622 Mbits/s mode.
AN11	RPSCN		
AK9	CTAPRP	—	**Center Tap RP.** LVDS buffer terminator center tap for RPSDP/N and RPSCP/N. An optional 0.1 µF capacitor, connected between the CTAP pin and ground, will improve the common-mode rejection of the LVDS input buffers.
AP10	TPSDP	LOUT	**Transmit Protection High-Speed Data.** 622/155 Mbits/s protection output data.
AP11	TPSDN		
AP8	TPSCP	LOUT	**Transmit Protection High-Speed Clock.** 622/155 MHz transmit output clock associated with TPSDP/N.
AP9	TPSCN		

Table 2-6. TMUX Block, Clock, and Sync I/O

Pin	Symbol	Type	Name/Description
AP6	THSCP	LIN	**Transmit High-Speed Clock.** 622 MHz/155 MHz input clock for transmit 622/155 Mbits/s data. Also used as a reference clock for all CDRs. There are five CDR circuits. The high-speed data and protection high-speed data have CDRs which operate at 155 MHz or 622 MHz. The mate inputs have three CDRs which operate at 155 MHz. The clock on this pin is also internally routed to the DS1/E1 framers and is used as an internal master clock. **Note:** A 622 MHz clock must be supplied when the device operates in 622 Mbits/s mode. A 155 MHz clock must be supplied when the device operates in 155 Mbits/s mode. For version 3.0 devices and later, the following applies: A 622 MHz clock must be supplied when the device operates in 622 Mbits/s mode. A 155 MHz or 622 MHz clock can be supplied when the device operates in 155 Mbits/s mode (choice provisionable via UMPR_OC3THSC_MODE).
AP7	THSCN		
AJ9	CTAPTH	—	**Center Tap TH.** LVDS buffer terminator center tap for THSCP/N. An optional 0.1 µF capacitor, connected between CTAP pin and ground, will improve the common-mode rejection of the LVDS input buffers.
AJ20	RHSFSYNCN	O	**Receive High-Speed Frame Sync.** This output indicates the start of the frame in the high-speed data input. Only present when a valid frame signal is detected on the RHSDP/N inputs. It is an active-low pulse with width almost equal to one E1 clock period or approximately 500 ns.
AK15	RLSCLK	O	**Receive Low-Speed Clock.** 19.44 MHz receive output clock divided down from either RHSCP/N or the recovered high-speed clock (when the CDR is used). May be used as a system timing reference.
AL14	TLSCLK	O	**Transmit Low-Speed Clock.** 19.44 MHz transmit output clock divided down from THSCP/N.
AL15	THSSYNC	I/O pd	**Transmit High-Speed Frame Sync.** 2 kHz/8 kHz composite frame sync signal that identifies the locations of the $J0$, $J1\text{-}1$, $J1\text{-}2$, $J1\text{-}3$ . . . $J1\text{-}12$, and $V1\text{-}1$ bytes. This signal is used to align transmit frames before multiplexing. **Note:** $J0$, $J1\text{-}1$, $J1\text{-}2$, and $J1\text{-}3$ . . . , $J1\text{-}12$ occur every 125 µs. $V1\text{-}1$ occurs every 500 µs. If register MPU_MASTER_SLAVE = 1, THSSYNC is an output; otherwise, THSSYNC is an input. The positive 8 kHz and 2 kHz pulses are synchronized to TLSCLK (in master mode only). The rising edge is referenced for frame location. For master/slave configuration, the THSSYNC of all *Ultramappers* (up to four) must be connected together. The master can be one of the *Ultramappers*, and it sources the frame sync pulse to other *Ultramappers*. All *Ultramappers* can also be configured as slaves and receive frame sync from the external system frame sync.

Table 2-7. STS Cross Connect (STSXC) Block, STS-3/STM-1 Mate Interconnect

Pin	Symbol	Type	Name/Description
AP17, AP15, AP13	RLSDATAP[3:1]	LOUT	**Receive Low-Speed Data.** These pins are usually used in 622 Mbits/s applications (however, they can be used in a 155 Mbits/s application). These pins are used on the device interfacing to the high-speed STS-N/STM-N line. Connect these pins to the high-speed data inputs (RHSDP/N) of the slave devices. This 155 Mbits/s signal uses a SONET structure. The overheads supported are the A1/A2 and B2 bytes and line RDI. The data is scrambled. Data from the RHSD is routed via the STSXC.
AP18, AP16, AP14	RLSDATAN[3:1]		
AN17, AN15, AN13	TLSDATAP[3:1]	LIN	**Transmit Low-Speed Data.** These pins are usually used in 622 Mbits/s applications (however, they can be used in a 155 Mbits/s application). These pins are used on the device interfacing to the high-speed STS-N/STM-N line. Connect these pins to the high-speed data outputs (THSDP/N) of the slave devices. This 155 Mbits/s input receives data from the slave high-speed outputs. These inputs have built-in clock and data recovery (CDR). The frame location expects a fixed relationship to the high-speed transmit frame sync (THSSYNC).
AN18, AN16, AN14	TLSDATAN[3:1]		
AJ13	CTAPTL	—	**Center Tap TL.** LVDS buffer terminator center tap for TLSDATAP/N. An optional 0.1 µF capacitor, connected between CTAP pin and ground, will improve the common-mode rejection of the LVDS input buffers.

Table 2-8. Synchronous Payload Envelope (SPE) Mapper Block, External PLL Control

Pin	Symbol	Type	Name/Description
AL1, AJ2, AH2, AF5, AE6, AG2	PHASEDETUP[6:1]	O	**Phase Detector Up.** Signal out to external PLL filter and oscillator circuits. Used if SPEMPR outputs DS3/E3 data without going through internal DS3/E3 DJA. If TSTMODE is high, then these pins are used for TSTMUX[5:0] (test mode output). For version 3.0 devices and later, these pins are no longer used. Therefore, the DS3/E3 DJA must be used. PHASEDETUP [6] becomes a transmit CHI frame sync output (CHITXGFS_O) which is only applicable in CHI compression mode.
AJ3, AJ1, AK1, AF6, AG5, AG3	PHASEDETDOWN[6:1]	O	**Phase Detector Down.** Signal out to external PLL filter and oscillator circuits. Used if SPEMPR outputs DS3/E3 data without going through internal DS3/E3 DJA. If TSTMODE is high, PHASEDETDOWN[4:1] are used for TSTMUX[9:6] (test mode output). For version 3.0 devices and later, these pins are no longer used. Therefore, the DS3/E3 DJA must be used.

Table 2-9. Multirate Cross Connect (MRXC) Block, TOAC Input and Output Channels

Pin	Symbol	Type	Name/Description
AM17	RTOACCLK	O	**Receive Transport Overhead Access Channel Clock.** The frequency of this clock is determined by the TOAC provisioning registers.
AJ17	RTOACDATA	O	**Receive Transport Overhead Access Channel Data.** 622/155 Mbits/s transport overhead bytes are output on this pin. The content is determined by the TOAC provisioning registers.
AM18	RTOACSYNC	O	**Receive Transport Overhead Access Channel Sync.** Active-high 8 kHz frame sync. It is active during the clock period of the first bit of each frame.
AL18	TTOACCLK	O	**Transmit Transport Overhead Access Channel Clock.** The frequency of this clock is determined by the TOAC provisioning registers.
AP19	TTOACDATA	I pd	**Transmit Transport Overhead Access Channel Data.** Input for the transport overhead bytes.
AK18	TTOACSYNC	O	**Transmit Transport Overhead Access Channel Sync.** Active-high 8 kHz frame sync. It is active during the clock period of the first bit of each frame.

Table 2-10. Multirate Cross Connect (MRXC) Block, POAC Input and Output Channels

Pin	Symbol	Type	Name/Description
AN19	RPOACCLK	O	**Receive Path Overhead Access Channel Clock.** Output for the path overhead bytes. This is a 3-state output pin controlled by register provisioning.
AJ18	RPOACDATA	O	**Receive Path Overhead Access Channel Data.** Output for the path overhead bytes. This pin can be 3-stated.
AP20	RPOACSYNC	O	**Receive Path Overhead Access Channel Sync.** Output for POAC channel. Active-high during the first bit of each frame when the POAC is connected to either the TMUX or STS1LT. Active-high during the LSB of the last byte of the frame when connected to the SPEMPR. This pin can be individually 3-stated.
AN20	TPOACCLK	O	**Transmit Path Overhead Access Channel Clock.** Serial access channel clock output for the path overhead bytes. This pin can be individually 3-stated.
AJ19	TPOACDATA	I pd	**Transmit Path Overhead Access Channel Data.** Serial access channel data input for the path overhead bytes.
AM20	TPOACSYNC	O	**Transmit Path Overhead Access Channel Sync.** Output for POAC channel. Active-high during the first bit of each frame when the POAC is connected to either the TMUX, the STS1LT, or the SPEMPR. This pin can be individually 3-stated.

Table 2-11. DS3/E3/STS-1 Out

Pin	Symbol	Type	Name/Description
AF2, AD5, AE1, AD1, AA5, AB2	DS3POSDATAOUT[6:1]	O	**DS3/E3/STS-1 Positive Data Output.** Contains either the positive rail of the B3ZS/HDB3 encoded output data, or single rail NRZ data.
AF3, AC6, AF1, AD2, AA6, AB1	DS3NEGDATAOUT[6:1]	O	**DS3/E3/STS-1 Negative Data Output.** Negative rail B3ZS/HDB3 encoded output data. Not used in single rail mode (held low in this case).
AD6, AG1, AD3, AC3, AC2, Y6	DS3DATAOUTCLK[6:1]	I pd	**DS3/E3/STS-1 Data Output Clock.** 44.736 MHz, 34.368 MHz, or 51.84 MHz clock input and is typically connected to a crystal oscillator or clocking chip. This clock is required for M13, E13, or STS1LT applications. For DS3/E3 to SONET/SDH mapping applications, this clock is required only if an external clock smoothing PLL is used. If the DS3/E3 DJA is used, this clock is not required. DS3XCLK/E3XCLK is needed for DS3/E3 DJA in this case. For STS-1 to SONET mapping applications, the TMUX can be used to supply the STS-1 rate DATAOUT clock and this clock is therefore not needed. For STS-1 ↔ PDH applications, a 51.84 MHz clock must be supplied at this pin.
AH1, AE2, AC5, AB6, AC1, AA3	DS3RXCLKOUT[6:1]	O	**DS3/E3/STS-1 Receive Clock Output.** 44.736 MHz DS3/34.368 MHz E3/51.84 MHz STS-1 clock out to external circuit.

Table 2-12. DS3/E3/STS-1 In

Pin	Symbol	Type	Name/Description
AA1, Y2, W6, V3, U3, T2	DS3POSDATAIN[6:1]	I pd	**DS3/E3/STS-1 Positive Data Input.** Contains either the positive rail of the B3ZS/HDB3 encoded input data, or single rail NRZ data.
AA2, Y1, V6, V5, U2, T1	DS3NEGDATAIN[6:1]	I pd	**DS3/E3/STS-1 Negative Data Input.** Contains either the negative rail of the B3ZS/HDB3 encoded input data or, in single rail mode, this input may be used to count bipolar violations.
Y5, Y3, W2, W1, V2, U5	DS3DATAINCLK[6:1]	I pd	**DS3/E3/STS-1 Data Input Clock.** 44.736 MHz, 34.368 MHz, or 51.84 MHz clock for the DS3/E3/STS-1 positive and negative data inputs.

Table 2-13. NSMI/STS-1 In

Pin	Symbol	Type	Name/Description
AP28, AK24, AK23	NSMIRXDATA[3:1]	I pd	**Network Serial Multiplex Interface (NSMI) Receive* Data.** Used in the following applications: ■ 51.84 Mbits/s serial data input that is used to bring in multiplexed DS1 or E1 channels to FRM. ■ STS-1 rate clear-channel receive data to SPEMPR. ■ DS3/E3 rate clear-channel receive data to M13/E13. Additionally, it could be used as a SONET compliant STS-1 input signal to STS1LT from external LIU. For V3.0 devices, these pins may also be used for DS3 clear channel (positive-rail or single-rail) input data (to the SPEMPR block).
AJ24, AP27, AP26	NSMIRXCLK[3:1]	I/O pd	**NSMI Receive Clock.** Used in the following applications: ■ Input (51.84 MHz) for the DS1/E1 application. ■ Output (51.84 MHz) for the STS-1 rate clear-channel application. ■ Output (44.736/34.368 MHz) for the DS3/E3 application. Additionally, it could be used as an input clock for SONET compliant STS-1 to STS1LT from external LIU. For V3.0 devices, these pins may also be used for DS3 clear channel DS3 rate input clock for positive (and negative) data inputs.
AN27, AN26, AN25	NSMIRXSYNC[3:1]	I/O pd	**NSMI Receive Frame Sync.** Used in the following applications: ■ Input receive NSMI control for FRM. ■ Output receive control frame sync signal for M13/E13. ■ Output receive control frame sync signal for SPEMPR. Additionally, it could be used to carry STS-1 input transmit clock for STS1LTs. For V3.0 devices, these pins may also be used for DS3 clear channel negative-rail input data (to the SPEMPR block).
AM27, AM26, AJ23	RXDATAEN[3:1]	O	**NSMI Receive Data Enable.** In FRM NSMI mode, this pin is not used. In the SPEMPR NSMI mode, the signal on this output will be high during the POH of the SPE. In M13 NSMI mode, the signal output on this pin goes low during the M1 byte of the first M1 frame of the DS3 frame. In E13 NSMI mode, the signal output on this pin goes low during the overhead bytes and control bits of the E3 frame.

* The transmit path is toward the high-speed fiber output and the receive path is from the high-speed input. Low-speed inputs, e.g., NSMIRXDATA, on the transmit path are labeled **receive**. Low-speed outputs, e.g., NSMITXDATA on the receive path are labeled **transmit**.

Table 2-14. NSMI/STS-1 Out

Pin	Symbol	Type	Name/Description
AP31, AN28, AJ25	NSMITXDATA[3:1]	O	**NSMI Transmit* Data.** NSMI outputs or STS-1 Tx data outputs from STS1LTs. NSMI output data from either the FRM, SPEMPR, or M13/E13 block. For V3.0 devices, these pins may also be used for DS3 clear channel (positive-rail or single-rail) output data (from the DS3 DJA block).
AM29, AP30, AP29	NSMITXCLK[3:1]	O	**NSMI Transmit Clock Output or STS-1 Tx Clock Outputs from STS1LTs.** Output clock at 51.84 MHz for the DS1/E1 application, the (51.84 MHz) STS-1 rate clear-channel application, or a (44.736 MHz/ 34.368 MHz) output clock for the DS3/E3 application. For V3.0 devices, these pins may also be used for DS3 clear channel DS3 rate output clock (from the DS3 DJA block).
AN30, AN29, AK26	NSMITXSYNC[3:1]	O	**Transmit System Frame Sync Output.** Output transmit control frame sync signal from FRM, M13/E13, or SPEMPR. For V3.0 devices, these pins may also be used for DS3 clear channel negative-rail output data (from the DS3 DJA block).
AM30, AK27, AJ26	TXDATAEN[3:1]	O	**Transmit Data Enable for NSMI Mode.** This output is used to request data for a particular link when the FRM NSMI is operating in nonloop timing mode. This output acts as a sync signal when the FRM NSMI operates in loop-timing mode. In the SPEMPR NSMI mode, the signal on this output will be high during the POH of the SPE. In M13 NSMI mode, the signal output on this pin goes low during the M1 byte of the first M1 frame of the DS3 frame. In E13 NSMI mode, the signal output on this pin goes low during the overhead bytes and control bits of the E3 frame.

* The transmit path is toward the high-speed fiber output and the receive path is from the high-speed input. Low-speed inputs, e.g., NSMIRXDATA, on the transmit path are labeled **receive**. Low-speed outputs, e. g., NSMITXDATA on the receive path are labeled **transmit**.

The transmit path is toward the high-speed fiber output and the receive path is from the high-speed input. Low-speed inputs, e.g., LINERXDATA, on the transmit path are labeled **receive**. Low-speed outputs, e. g., LINETXDATA, on the receive path are labeled **transmit**.

Table 2-15. Shared Low-Speed Line In

Pin	Symbol	Type	Name/Description
A3, F8, B5, A4, B6, B7, E9, F10, B8, A7, B9, E11, B10, E12, A10, F13, A11, F14, E14, C14, F15, E15, C15, B15, F17, A16, C17, B18, E18, B19	LINERXDATA[30:1]	I pd	**Line Receive Data [30:1].** Inputs to the internal multirate cross connect. The signals support a variety of transport modes such as DS1, E1, VT, or VC. The signals are used for received positive-rail or single-rail DS1/ E1 line data input sourced from an external LIU. In this mode, these signals will be routed via the cross connect to the VT mapper, the M13 multiplexer, E13 multiplexer, or the receive line inputs of the DS1/E1 framers. These signals may also be used as input data for DS2/E2 applications (see the *Ultramapper Family System Design Guide*).
E6, B4, C5, C6, E8, A5, F9, A6, C8, F11, C9, A8, F12, A9, C11, B11, C12, B12, A12, B13, A13, B14, A14, F16, A15, B16, E17, B17, C18, A19	LINERXCLK[30:1]	I/O pd	**Line Receive Clock [30:1].** Configurable inputs to the internal multirate cross connect. These inputs are typically used for asynchronous clocks associated with the line receive data inputs from external line interface units or payload termination functions. For transport mode only. In certain cases, this input can be used as an output. These pins may be used for DS2/E2 clocks in DS2/E2 applications. More information can be found in an application note: *Configuring Ultramapper Family of Devices for Ported DS2 Applications.* For input specifications, Table 6-21 applies to these pins.

The transmit path is toward the high-speed fiber output and the receive path is from the high-speed input. Low-speed inputs, e.g., LINERXDATA, on the transmit path are labeled **receive**. Low-speed outputs, e. g., LINETXDATA, on the receive path are labeled **transmit**.

Table 2-16. Shared Low-Speed Line Out

Pin	Symbol	Type	Name/Description
A23, B23, C23, B24, C24, A26, F23, A27, C26, F24, C27, A29, F26, A30, E27, C29, C30, B31, E29, E30, C34, H29, E33, D34, F33,G33, J30, K29, H33, G34	LINETXDATA[30:1]	O	**Line Transmit Data [30:1].** Outputs from the internal multirate cross connect. The outputs support a variety of transport modes such as asynchronous DS1, E1, and synchronous VT or VC. The signals are used to transmit positive-rail or single-rail DS1/E1 line data output sourced to an external LIU. In this mode, these signals will be routed via the cross connect from the VT mapper, the M13 multiplexer, E13 multiplexer, or the transmit line outputs of the DS1/E1 framers. Each of these outputs comes from the internal MRXC and can be individually set to high-impedance. These pins may be used for output data in DS2/E2 applications (see the *Ultramapper Family System Design Guide*).
E21, F21, A24, F22, A25, E23, B25, E24, B26, A28, B27, F25, E26, B28, B29, A31, B30, F27, A32, F29, F30, D33, E32, F32, H30, E34, J29, F34, H32, L29	LINETXCLK[30:1]	I/O pd	**Line Transmit Clock [30:1].** Configurable outputs from the internal multirate cross connect. These outputs are typically used for asynchronous clocks associated with the line transmit data outputs to external line interface units or payload termination functions. For transport mode only. Each of these outputs comes from the internal MRXC and can be individually set to high impedance. In certain cases (DS2/E2 applications), this output is used as an input (input DS2/E2 clocks). More information can be found in an application note: *Configuring Ultramapper ™ Family of Devices for Ported DS2 Applications.* For output specifications, Table 6-22 applies to these pins.

The transmit path is toward the high-speed fiber output and the receive path is from the high-speed input. Low-speed inputs, e.g., CHIRXDATA, on the transmit path are labeled **receive**. Low-speed outputs, e.g., CHITXDATA, on the receive path are labeled **transmit**.

Table 2-17. TDM Concentration Highway (CHI) In

Pin	Symbol	Type	Name/Description
J32, J33, H34, L30, M29, K33, J34, M30, L32, K34, L33, N29, M32, L34, M33, P29, M34, P30, N33, P32, N34, R29, P33, R30, P34, R32, T29, R33, R34, U29, T33, T34, U30, U32, U33, V33, V32, V30, W34, W33, V29, Y34	CHIRXDATA[42:1]	I pd	**CHI Receive Data [42:1].** Configurable synchronous TDM inputs to the internal multirate cross connect. Can be used in one of the following modes: CHI mode: Receive TDM input highways. Can be configured to operate at 2.048 Mbits/s, 4.096 Mbits/s, 8.192 Mbits/s, or 16.384 Mbits/s. Parallel system bus mode: The parallel system bus is a 16-bit wide 19.44 Mbits/s synchronous TDM highway. Bits [16:9] are used for time-slot data. Bits [8:1] are used for robbed-bit signaling data in a ASM like fashion and are optional. CHIRXGFS is the frame synchronization input for the parallel system bus and CHIRXGCLK is the 19.44 MHz clock input. CHIRXDATA[42:17] are not used. Asynchronous mode: In this mode, these inputs are used for DS1/E1 received negative rail data. May also be used for 8 kHz frame synchronization inputs that indicate the position of the F-bits in the line receive data. VT mapper mode: 8 kHz sync for DS1/E1 or 2 kHz sync signal for VC. These pins may be used as input data for DS2/E2 applications. More information can be found in an application note: *Configuring Ultramapper Family of Devices for Ported DS2 Applications.*

The transmit path is toward the high-speed fiber output and the receive path is from the high-speed input. Low-speed inputs, e.g., CHIRXDATA, on the transmit path are labeled **receive**. Low-speed outputs, e. g., CHITXDATA, on the receive path are labeled **transmit**.

Table 2-18. TDM Concentration Highway (CHI) Out

Pin	Symbol	Type	Name/Description
AA33, Y29, AB34, AA32, AB33, AA30, AC34, AA29, AC33, AD34, AC32, AB29, AD33, AE34, AD32, AC30, AF34, AE33, AC29, AD30, AG34, AF33, AF32, AH34, AD29, AG33, AG32, AE29, AJ34, AF30, AF29, AH33, AK34, AJ33, AG30, AM34, AJ30, AJ29, AK29, AP32, AN31, AJ27	CHITXDATA[42:1]	I/O	**CHI Transmit Data [42:1].** Configurable synchronous TDM outputs from the internal multirate cross connect. Can be used in one of the following modes: CHI mode: Transmit TDM output highways. Can be configured to operate at 2.048 Mbits/s, 4.096 Mbits/s, 8.192 Mbits/s, or at 16.384 Mbits/s. Parallel system bus mode: The parallel system bus is a 16-bit wide 19.44 Mbits/s synchronous TDM highway. Bits [16:9] are used for time-slot data. Bits [8:1] are used for robbed-bit signaling data in a ASM like fashion and are optional. CHITXGFS is the frame synchronization input for the parallel system bus and CHITXGCLK is the 19.44 MHz clock input. CHITXDATA[42:17] are not used. Asynchronous mode: In this mode, these outputs are used for DS1/E1 transmit negative rail data. May also be used for 8 kHz frame synchronization outputs that indicate the position of the F-bits in the line transmit data. VT mapper mode: 8 kHz frame sync output for DS1/E1 or 2 kHz frame sync output signal for VC. Each of these outputs comes from the internal MRXC and can be individually set to high impedance. In rare cases, this output can be used as an input. These pins have various functionalities in DS2/E2 applications. More information can be found in an application note: *Configuring Ultramapper Family of Devices for Ported DS2 Applications.* When running in CHI compression mode, CHITXDATA[17] becomes a frame sync output from the device, which signifies the beginning of the CHI output frame. This feature is only available in V3.0 devices and later.

Table 2-19. Framer (FRM) Block, CHI/Parallel System Bus (PSB) Clock and Sync

Pin	Symbol	Type	Name/Description
Y32	CHIRXGTCLK	I pd	**Global Transmit Line Clock.** This is the transmit line clock for the DS1 or E1 framer. Normally this input is not used and the transmit clock is generated by an internal phase-lock loop which uses CLKIN_PLL as a reference. Note that if this input is used, all the transmit framers must run at the same rate, either 1.544 MHz or 2.048 MHz. This signal could be used for both CHI and parallel system bus.
W29	CHIRXGCLK	I pd	**Receive Global System Clock.** This signal is used for both CHI and parallel system bus. In CHI mode, it is a 2.048 MHz, a 4.096 MHz, a 8.192 MHz, or a 16.384 MHz TDM clock. In parallel system bus mode, it is a 19.44 MHz clock.
Y33	CHIRXGFS	I pd	**Receive System Frame Sync.** This signal is used for both CHI and parallel system bus. In CHI mode, it is an 8 kHz pulse that references the location of time slots in the receive CHI inputs. Its polarity, sampling edge, and offset from time slots in the concentration highways may all be programmed. In parallel system bus mode, it is an 8 kHz reference for time slots within the parallel system bus input highways. In this mode, the frame strobe is a positive pulse with active edge provisioned by a register.
AA34	CHITXGFS	I pd	**Transmit System Frame Sync.** This signal is used for both CHI and parallel system bus. In CHI mode, it is an 8 kHz pulse which references the location of time slots in the transmit CHI outputs. Its polarity, sampling edge, and offset from time slots in the concentration highways may all be programmed. In parallel system bus mode, it is an 8 kHz reference for time slots within the parallel system bus output highways. In this mode, the frame strobe is a positive pulse with active edge provisioned by a register. For version 3.0 devices and later, CHITXGFS also serves as a required 8 kHz frame sync when operating in NSMI slip mode.
Y30	CHITXGCLK	I pd	**Transmit Global System Clock.** This signal is used for both CHI and parallel system bus. In CHI mode, it is a 2.048 MHz, a 4.096 MHz, a 8.192 MHz, or a 16.384 MHz TDM clock. In parallel system bus mode, it is a 19.44 MHz clock.

Table 2-20. Reference Clocks

Pin	Symbol	Type	Name/Description
R1	DS2AISCLK	I pd	**DS2 AIS Clock.** More information can be found in an application note: *Configuring Ultramapper Family of Devices for Ported DS2 Applications.* **VC11 AIS Clock**. A 1.664 MHz clock input. In the VT mapper mode, this clock is used to generate VC11 AIS. The clock is used when VC11 is sent from the LINETXDATA[30:1] outputs. The 1.664 MHz clock is for a VC11 payload. There are 27 bytes per VT1.5 in each STS-1 frame, excluding the VT overhead (1 byte), 26 bytes/125 µs = 1.664 Mbits/s. (VC11 rate is 1.728 Mbits/s.) If used, this input can be provided by a free-running crystal oscillator, or a clocking chip.
U6	E2AISCLK	I pd	**E2 AIS Clock.** More information can be found in an application note: *Configuring Ultramapper Family of Devices for Ported DS2 Applications.* **VC12 AIS Clock**. A 2.240 MHz clock input. In the VT mapper mode, this clock is used to generate VC12 AIS. The clock is used when VC12 is sent from the LINETXDATA[30:1] outputs. The 2.240 MHz clock is for a VC12 payload. There are 36 bytes per VT2.0 in each STS-1 frame, excluding the VT overhead (1 byte), 35 bytes/125 µs = 2.240 Mbits/s. (VC12 rate is 2.304 Mbits/s.) If used, this input can be provided by a free-running crystal oscillator, or a clocking chip.
AP21	E1XCLK	I pd	**E1 X Clock.** This clock signal is used for three purposes: to generate E1 AIS (all 1s), as a reference to the E1 DJA, and as a clock source for the test pattern generator and test pattern monitor. This input may be provided by a 2.048 MHz, a 32.768 MHz, or a 65.536 MHz ± 50 ppm free-running crystal oscillator, or clocking chip. **Note:** For the E1 DJA, an input of 32.768 MHz or 65.536 MHz must be used.
AK20	DS1XCLK	I pd	**DS1 X Clock**. This clock signal is used for three purposes: to generate DS1 AIS (all 1s), as a reference to the DS1 DJA, and as a clock source for the test pattern generator and test pattern monitor. This input may be provided by a 1.544 MHz, a 24.704 MHz, or a 49.408 MHz ± 32 ppm free-running crystal oscillator, or clocking chip. **Note:** For the DS1 DJA, an input of 24.704 MHz or 49.408 MHz must be used.
A21	DS3XCLK	I pd	**DS3 X Clock.** A 44.736 MHz ± 20 ppm clock input for DS3 DJA and TPG. This input may be provided by a 44.736 MHz ± 20 ppm free-running crystal oscillator, or clocking chip.
F18	E3XCLK	I pd	**E3 X Clock.** A 34.368 MHz ± 20 ppm clock input for E3 DJA and TPG. This input may be provided by a 34.368 MHz ± 20 ppm free-running crystal oscillator, or clocking chip.

Table 2-21. Low-Order Path Overhead Access, Transmit Direction

Pin	Symbol	Type	Name/Description
B22	LOPOHCLKIN	I pd	**Low-Order Path Overhead Clock.** 19.44 MHz clock supplied from external circuits that provide the low-order path overhead data.
C21	LOPOHDATAIN	I pd	**Low-Order Path Overhead Data.** The following parts of the low-order (VT) overhead are presented at this pin: communication channel bits (O bits), V5, J2, Z6/N2, Z7, and K4 byte.

Table 2-21. Low-Order Path Overhead Access, Transmit Direction

Pin	Symbol	Type	Name/Description
A22	LOPOHVALIDIN	I pd	**Low-Order Path Overhead Data Input Valid.** This signal is a mask that indicates the location of the overhead bytes in the LOPOHDATAIN.

Table 2-22. Low-Order Path Overhead Access, Receive Direction

Pin	Symbol	Type	Name/Description
F20	LOPOHCLKOUT	O	**Low-Order Path Overhead Clock.** 19.44 MHz clock supplied to external circuits that receive the low-order path overhead data.
B21	LOPOHDATAOUT	O	**Low-Order Path Overhead Data.** Line and path REI and RDI, O-bits, V5, J2, Z6/N2, and Z7/K4 byte.
E20	LOPOHVALIDOUT	O	**Low-Order Path Overhead Data Output Valid.** This signal is a mask that indicates the location of the overhead bytes in the LOPOHDATAOUT.

Table 2-23. Clock Generator

Pin	Symbol	Type	Name/Description
AJ32	CLKIN_PLL	I pd	**Transmit Line Clock Generator Reference Input.** The clock generator is used to derive the transmit line clocks for DS1/E1 synchronized to CLKIN_PLL. The derived clock is used in the DS1/E1 transmit framer sections.
AL33	CG_PLLCLKOUT	O	**Framer PLL Test Mode Output.** Framer PLL clock (1.544 MHz, 2.048 MHz) selected by device register.
AK30, AK32, AG29	MODE[2:0]_PLL	I pd	**Framer PLL Input Clock Mode Select Bits.** The settings of these mode select pins must correspond to the frequency of CLKIN_PLL as shown below.

MODE[2:0]_PLL	CLKIN_PLL	MODE[2:0]_PLL	CLKIN_PLL
000	Reserved	100	16.384 MHz
001	51.840 MHz	101	8.192 MHz
010	26.624 MHz	110	4.096 MHz
011	19.440 MHz	111	2.048 MHz

Table 2-24. Microprocessor Interface

Pin	Symbol	Type	Name/Description
F5	MPCLK	I	**Microprocessor Clock.** This clock is required to properly sample address, data, and control signals from the microprocessor in both asynchronous and synchronous modes of operation.
F6	MPMODE	I	**Microprocessor Mode.** If the microprocessor interface is synchronous, MPMODE should be set to 1. If the microprocessor interface is asynchronous, MPMODE should be set to 0.
C1	CSN	I pu	**Chip Select.** Active-low, high-order address signal. Chip select must be set low at the beginning of any read or write access and returned high at the end of the cycle.
D2	ADSN	I	**Address Strobe.** Active-low address strobe that indicates the beginning of a read or write access. It is a one MPCLK cycle-wide pulse for synchronous mode. In asynchronous mode, it is active for the entire read/write cycle. Address bus signals, ADDR[20:0], are available to the *Ultramapper* when ADSN is low. The address bus should remain valid for the duration of ADSN.
H6	RWN	I	**Read/Write.** RWN is set high during a read cycle, or set low during a write cycle.
E3	DSN	I	**Data Strobe.** For a read cycle, the contents of the internal register will be output on DATA [15:0]; and for a write cycle DATA [15:0] will be clocked into the internal register. To initiate the start of the read/write operation, DSN must be low during the entire read/write cycle. This signal should only be used for asynchronous mode.
K2, M6, L5, H1, J2, J3, G1, L6, H2, H3, K6, F1, J5, J6, G2, E1, F2, H5, D1, F3, E2	ADDR[20:0]	I	**Address [20:0].** ADDR[20] is the most significant bit and ADDR[0] is the least significant bit for addressing all the internal registers during microprocessor access cycles. All addresses are 21-bit word addresses; hence, in a typical application ADDR[0] of the TMXF84622 device would be connected to address bit 1 of a byte addressable system address bus. **Note:** The *Ultramapper* is little-endian, i.e., the least significant byte is stored in the lowest address and the most significant byte is stored in the highest address. Care must be exercised in connection to microprocessors that use big-endian byte ordering.
R6, N1, P3, N2, P5, M1, P6, M2, L1, M3, N6, L2, K1, L3, M5, J1	DATA[15:0]	I/O	**Data [15:0].** 16-bit data bus input for write operations and output for read operations. DATA[15] is the MSB, and DATA[0] is the LSB.
R5, P2	PAR[1:0]	I/O	**Data Parity.** Byte-wide parity bits for data. PAR[1] is the parity for DATA[15:8], and PAR[0] is the parity for DATA[7:0]
P1	DTN	O	**Data Transfer Acknowledge.** The delay associated with DTN going low depends on the *Ultramapper* block being accessed. In asynchronous mode, when ADSN or DSN is deasserted, the deassertion will drive the DTN signal high. When inactive, CSN will drive DTN to be 3-stated. The microprocessor should wait after DTN is deasserted before starting the next operation.
R3, T6	HP_INTN, LP_INTN	O od	**High-Priority and Low-Priority Interrupt.** Active-low. Each of the functional blocks contain their individual low-priority interrupts. High-priority interrupts are generated by TMUX and E13 blocks. Each interrupt is individually maskable. Requires an external 5 kΩ pull-up resistor.
R2	APS_INTN	O od	**Automatic Protection Switch Interrupt.** Active-low. See the TMUX section in the Register Description for specific interrupts. Each interrupt is individually maskable. Requires an external 5 kΩ pull-up resistor.

Table 2-25. Boundary Scan (*IEEE*® 1149.1)

Pin	Symbol	Type	Name/Description
AN22	TCK	I	**Test Clock.** This signal provides timing for boundary scan test operations.
AK21	TDI	I pu	**Test Data In.** Boundary scan test data input signal, sampled on the rising edge of TCK.
AP23	TMS	I pu	**Test Mode Select.** Controls boundary scan test operations. TMS is sampled on the rising edge of TCK.
AJ21	TRST	I pu	**Test Reset (Active-Low).** This signal provides an asynchronous reset for the boundary scan TAP controller.
AN23	TDO	O	**Test Data Out.** Boundary-scan test data output signal is updated on the falling edge of TCK. The TDO output will be high-impedance except when transmitting test data.

Table 2-26. General-Purpose Interface

Pin	Symbol	Type	Name/Description
AP22	RSTN	I pu	**Global Hardware Reset.** Active-low. Initializes all internal registers to their default state. This is an asynchronous reset on the falling edge, but RSTN should be held low for at least 1 µs. RSTN should be held low until both power supplies (1.5 V and 3.3 V) are stabilized upon powerup.
AM21	PMRST	I/O pd	**Performance Monitor Reset.** Resets error counters. When enabled as an input, it is a 1 s square wave that forces an update of PM counters upon the rising edge. When the PMRST is generated internally from the MPU clock, this pin is an output.
AP24	IC3STATEN	I pu	**Output Enable.** When high, output buffers will operate normally. When low, all outputs will be forced to a high-impedance state. IC3STATEN should be held low until both power supplies (1.5 V and 3.3 V) are stabilized upon powerup.
AM23	SCK1	I pd	**Scan Clock 1.** Reserved. Do not connect.
AJ22	SCK2	I pd	**Scan Clock 2.** Reserved. Do not connect.
AN24	SCAN_EN	I pd	**Scan Enable.** Reserved. Do not connect.
AP25	SCANMODE	I pd	**Serial Scan Input for Testing.** Reserved. Do not connect.
AM24	$I_{DD}Q$	I	**IDDQ Input.** This pin must be externally pulled down with a 1 kΩ resistor.

Table 2-27. CDR Interface

Pin	Symbol	Type	Name/Description
AJ15	BYPASS	I pd	**High-Speed CDR Bypass.** Reserved. Do not connect.
AJ14	TSTPHASE	I pd	**Test Phase.** Reserved. Do not connect.
AM15	ECSEL	I pd	**External Clock Select.** Reserved. Do not connect.
AJ16	ETOGGLE	I pd	**External Toggle.** Reserved. Do not connect.
AL17	EXDNUP	I pd	**External Down Up.** Reserved. Do not connect.
AK17	TSTMODE	I pd	**Test Mode.** Reserved. Do not connect.
AM14	TSTSFTLD	I pd	**Test Shift Load.** Reserved. Do not connect.

Table 2-28. Analog Power and Ground Signals

Pin	Symbol	Type	Name/Description
AK12	V_{SSA_CDR1}	—	**CDR1 Ground.** Isolated ground for the internal CDR1.
AJ12	V_{SSA_CDR2}	—	**CDR2 Ground.** Isolated ground for the internal CDR2.
AJ11	V_{SSA_X4PLL}	—	**X4PLL Ground.** Isolated ground for the internal X4PLL.
AL34	V_{SSA_SFPLL}	—	**SFPLL Ground.** Isolated ground for the internal SFPLL.
F19	V_{SSA_DS3PLL}	—	**DS3PLL Ground.** Isolated ground for the internal DS3PLL.
A20	V_{SSA_E3PLL}	—	**E3PLL Ground.** Isolated ground for the internal E3PLL.
AK11	V_{DD15A_CDR1}	—	**CDR1 Power.** 1.5 V power supply for the internal CDR1, which is used by the high-speed receive CDR, the protection receive CDR and the three CDRs associated with the mate interconnect ports. Good engineering practice needs to be applied; refer to the evaluation board schematic.
AJ10	V_{DD15A_CDR2}	—	**CDR2 Power.** 1.5 V power supply for the internal CDR2, which is used by the high-speed receive CDR, the protection receive CDR and the three CDRs associated with the mate interconnect ports. Good engineering practice needs to be applied; refer to the evaluation board schematic.
AK14	V_{DD15A_X4PLL}	—	**X4PLL Power.** 1.5 V power supply for the internal X4PLL, which is used for the transmit protection 1 + 1 port. Good engineering practice needs to be applied; refer to the System Design Guide.
C20	V_{DD15A_DS3PLL}	—	**DS3PLL Power.** 1.5 V power supply for the internal DS3PLL, which is used by the DS3DJA. Good engineering practice needs to be applied; refer to the evaluation board schematic.
B20	V_{DD15A_E3PLL}	—	**E3PLL Power.** 1.5 V power supply for the internal E3PLL, which is used by the E3DJA. Good engineering practice needs to be applied; refer to the System Design Guide.
AK33	V_{DD33A_SFPLL}	—	**SFPLL Power.** 3.3 V power supply for the internal SFPLL, which is used by the CG block. Good engineering practice needs to be applied; refer to the evaluation board schematic.

Table 2-29. Digital Power and Ground Signals

Pin	Symbol	Type	Name/Description
AA7, AA16, AA17, AA18, AA19, AA28, AB7, AB16, AB17, AB18, AB19, AB28, AC7, AC28, AD7, AD28, AE7, AE28, AF7, AF28, AH9, AH10, AH11, AH12, AH13, AH14, AH15, AH16, AH19, AH20, AH21, AH22, AH23, AH24, AH25, AH26, G9, G10, G11, G12, G13, G14, G15, G16, G19, G20, G21, G22, G23, G24, G25, G26, J7, J28, K7, K28, L7, L28, M7, M28, N7, N16, N17, N18, N19, N28, P7, P16, P17, P18, P19, P28, R7, R28, T7, T13, T14, T21, T22, T28, U13, U14, U21, U22, V13, V14, V21, V22,W7, W13, W14, W21, W28, Y7, Y28, W22	V_{DD15}	—	Common power signals for 1.5 V V_{DD}.
A2, A33, AA4, AC31, AD4, AF31, AG4, AG7, AG28, AH8, AH17, AH18, AH27, AJ31, AK4, AL6, AL9, AL12, AL21, AL24, AL27, AL30, AM2, AM33, AN1, AN3, AN32, AN34, AP2, AP33, B1, B3, B32, B34, C2, C33, D5, D8, D11, D14, D17, D20, D23, D26, D29, E31, F4, G8, G17, G18, G27, H7, H28, H31, J4, L31, M4, P31, R4, U7, U28, U31, V28, V4, V7, Y31	V_{DD33}	—	Common power signals for 3.3 V V_{DD}.
A1, A17, A18, A34, AA13, AA14, AA21, AA22, AA31, AB13, AB14, AB21, AB22, AC4, AD31, AF4, AG6, AG31, AJ4, AJ5, AK2, AK3, AK5, AK31, AL2, AL5, AL11, AL20, AL23, AL26, AL29, AL8, AM1, AM3, AM11, AM12, AM32, AN2, AN6, AN9, AN12, AN33, AP1, AP12, AP34, B2, B33, C3, C32, D6, D9, D12, D15, D18, D21, D24, D27, D30, E4, E5, F31, H4, J31, L4, M31, N13, N14, N21, N22, P4, P13, P14, P21, P22, R31, T16, T17, T18, T19, U1, U4, U16, U17, U18, U19, U34, V1, V16, V17, V18, V19, V31, V34, W16, W17, W18, W19, Y4	V_{SS}	—	Common ground signals.

3 Operating Conditions and Reliability

3.1 Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 3-1. Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply Voltage (V_{DD33})	–0.5	4.2	V
Supply Voltage (V_{DD15})	–0.3	2.0	V
Input Voltage: LVCMOS LVDS	 –0.3 –0.3	 5.25 V_{DD33} + 0.3	 V V
Power Dissipation	—	—	mW
Storage Temperature Range	–65	125	°C

3.2 Recommended Operating Conditions

Table 3-2 lists the voltages, along with the tolerances, that are required for proper operation of the TMXF84622 device.

Table 3-2. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
3.3 V Power Supply	V_{DD33}	3.14	3.3	3.47	V
1.5 V Power Supply	V_{DD15}	1.4	1.5	1.6	V
Ground	V_{SS}	—	0.0	—	V
1.0 V: LVDS Reference*	REF10	—	1.0	—	V
1.4 V: LVDS Reference*	REF14	—	1.4	—	V
Ambient Temperature	T_A	–40	—	85	°C

* Internal reference voltage is used if UMPR_LVDS_REF_SEL = 1, or else external voltage is used.

3.3 Handling Precautions

Although electrostatic discharge (ESD) protection circuitry has been designed into this device, proper precautions must be taken to avoid exposure to ESD and electrical overstress (EOS) during all handling, assembly, and test operations. Agere employs both a human-body model (HBM) and a charged-device model (CDM) qualification requirement in order to determine ESD-susceptibility limits and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in each of the models, as defined by JEDEC's JESD22-A114 (HBM) and JESD22-C101 (CDM) standards.

Table 3-3. ESD Tolerance

Device	Minimum Threshold	
	HBM	CDM
TMXF84622	2000 V	500 V

3.4 Thermal Parameters (Definitions and Values)

System and circuit board level performance depends not only on device electrical characteristics, but also on device thermal characteristics. The thermal characteristics frequently determine the limits of circuit board or system performance, and they can be a major cost adder or cost avoidance factor. When the die temperature is kept below 125 °C, temperature-activated failure mechanisms are minimized. The thermal parameters that Agere provides for its packages help the chip and system designer choose the best package for their applications, including allowing the system designer to thermally design and integrate their systems.

It should be noted that all the parameters listed below are affected, to varying degrees, by package design (including paddle size) and choice of materials, the amount of copper in the test board or system board, and system airflow.

Θ_{JA} - Junction to Air Thermal Resistance

Θ_{JA} is a number used to express the thermal performance of a part under JEDEC standard natural convection conditions. Θ_{JA} is calculated using the following formula:

$\Theta_{JA} = (T_J - T_{amb}) / P$; where P = power

Θ_{JMA} - Junction to Moving Air Thermal Resistance

Θ_{JMA} is effectively identical to Θ_{JA} but represents performance of a part mounted on a JEDEC four layer board inside a wind tunnel with forced air convection. Θ_{JMA} is reported at airflows of 200 LFPM and 500 LFPM (linear feet per minute), which roughly correspond to 1 m/s and 2.5 m/s (respectively). Θ_{JMA} is calculated using the following formula:

$\Theta_{JMA} = (T_J - T_{amb}) / P$

Θ_{JC} - Junction to Case Thermal Resistance

Θ_{JC} is the thermal resistance from junction to the top of the case. This number is determined by forcing nearly 100% of the heat generated in the die out the top of the package by lowering the top case temperature. This is done by placing the top of the package in contact with a copper slug kept at room temperature using a liquid refrigeration unit. Θ_{JC} is calculated using the following formula:

$\Theta_{JC} = (T_J - T_C) / P$

Θ_{JB} - Junction to Board Thermal Resistance

Θ_{JB} is the thermal resistance from junction to board. This number is determined by forcing the heat generated in the die out of the package through the leads or balls by lowering the board temperature and insulating the package top. This is done using a special fixture, which keeps the board in contact with a water chilled copper slug around the perimeter of the package while insulating the package top. Θ_{JB} is calculated using the following formula:

$\Theta_{JB} = (T_J - T_B) / P$

Ψ_{JT} - Junction Temperature to Case Temperature

Ψ_{JT} correlates the junction temperature to the case temperature. It is generally used by the customer to infer the junction temperature while the part is operating in their system. It is not considered a true thermal resistance. Ψ_{JT} is calculated using the following formula:

$\Psi_{JT} = (T_J - T_C) / P$

Table 3-4. Thermal Parameter Values

Parameter	Temperature °C/Watt
Θ_{JA}	13
Θ_{JMA} (1 m/s)	9.7
Θ_{JMA} (2.5 m/s)	8.2
Θ_{JC}	2.5
Θ_{JB}	7.8
Ψ_{JT}	1

3.5 Reliability

Product reliability can be calculated as the probability that the product will perform under normal operating conditions for a set period of time. Factors influencing the reliability of a product cover a range of variables, including design and manufacturing. The failure rate of a product is given as the number of units failing per unit time. This failure rate is known as FIT, which is as follows:

1 FIT = 1 failure/1 x 10^9 hours.

Another unit used for failure rate is known as MTBF, which is 1/FIT. Many assumptions are made when calculating the failure rate for a product, such as the average junction temperature and activation energy. The assumptions made for calculating FIT and MTBF are shown in Table 3-5:

Table 3-5. Reliability Data

Junction Temperature	FIT (Per 1 x 10^9 Device Hours)	MTBF	Activation Energy
55 °C	22	4.55 x 10^7 hours	0.7eV

Moisture Sensitivity Level—This is based on IPC/JEDEC test method J-STD-020 (which lists a means of testing and classifying devices for a certain level of moisture sensitivity).

Table 3-6. Moisture Sensitivity Level

Device	Level
TMXF84622	2A
L-TMXF84622 (Pb-free)	3

3.6 Recommended Powerup Sequence

The *Ultramapper* device requires dual power supplies, a 3.3 V supply for the I/O and a 1.5 V supply for the core.

During powerup, RSTN should be held low (holding the device in reset) and IC3STATEN should be held low (3-stating all output buffers). After the 3.3 V and 1.5 V supplies are stable, MPCLK (which affects the device reset) should be applied and must be present for at least two clock cycles before RSTN and IC3STATEN are released. It is then recommended that IC3STATEN be released concurrent with, or after, the release of RSTN. There are no constraints as to which supply (3.3 V or 1.5 V) must come up first, nor does it matter how long it takes the second supply to come up after the first supply.

Additionally, it is recommended that the TRST pin be held low (or pulsed low) upon startup.

3.7 Power Consumption

The power consumption of the device is application dependent since it is not possible to use all the device features simultaneously. The nominal measured values for power per block are shown in Table 3-8.

Table 3-7. Typical Power Consumption by Application

Application	Conditions	Typ 1.5 V Power	Typ 3.3 V Power	Typ Total Power
OC12 to 84 DS1 Cross Connect CHI Loopback	TMUX, three SPEMPRs, three VTMPRSs, three DS1DJAs, three FRMs, and CHI at 8 Mbits/s	1.65 W	0.55 W	2.20 W
OC12 to 84 DS1 Transport Mode	TMUX, three SPEMPRs, three VTMPRSs, three DS1DJAs, and three FRMs	1.60 W	0.50.W	2.10 W
OC12 to 6 DS3 Clear Channel	TMUX, six SPEMPRs, one DS3DJA, and six DS3 I/Os	1.00 W	0.75 W	1.75 W
OC12 to STSPP	High-speed loopback through STSPP and TMUX	0.90 W	0.50 W	1.40 W
OC12 to 84 DS1 Portless Trans-MUX Application, Transport Mode	TMUX, three STS1LTs, five SPEMPRs, three VTMPRs, two M13s, three DS1DJAs, and three FRMs	1.70 W	0.85 W	2.55 W
OC12 to 84 DS1 TransMUX Application, Transport Mode	TMUX, three STS1LTs, three SPEMPRs, three VTMPRs, three M13s, three DS1DJAs, and three FRMs	1.70 W	0.60 W	2.30 W

Table 3-8. Typical Power Consumption Per Block

Typical power by block refers to all instances being used.

Block	Maximum Instance	Typical, Per Single Instance	Unit
TMUX	1	0.120	W
STSPP	1	0.020	W
STSXC	1	0.200	W
MRXC	1	0.050	W
SPEMPR	6	0.009	W
STS1LT	3	0.028	W
VTMPR	3	0.015	W
E13	3	0.013	W
M13	3	0.013	W
TPG/TPM	1	TBD	W
FRM	3	0.195	W
DS1DJA	3	0.026	W
DS3DJA	1	0.050	W
MPU	1	0.420*	W
CDR/PLL	1	0.150	W
LVDS I/O	15	0.020	W
NSMI I/O	3	0.032	W
DS3 I/O	6	0.050	W

* Measured with a 50 MHz MPCLK. With a 25 MHz MPCLK, the typical per single instance value of MPU power is approximately 0.2 W.

Testing has shown that, on the average, approximately 0.35 W can be saved by utilizing the divide by 16 MPU clock power down feature. Please refer to MPU register 0x0019 in the *Ultramapper* Register Description document for further information. Additional MPU clock divisor options are available.

Additional power can be saved by powering down unused LVDS buffers. For details, please see MPU register 0x0026 in the *Ultramapper* Register Description document.

4 Electrical Characteristics

4.1 LVCMOS Interface Specifications

Table 4-1. LVCMOS Input Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Leakage Current	I_I	$V_{SS} < V_{IN} < V_{DD33}$	—	—	1.0*	µA
High-input Voltage	V_{IH}	—	2.0	—	—	V
Low-input Voltage	V_{IL}	—	V_{SS}	—	0.8	V
Input Capacitance	C_I	—	—	—	1.5	pF

* Excludes current due to pull-up or pull-down resistors.

Table 4-2. LVCMOS Output Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage Low	V_{OL}	I_{OL} = max	V_{SS}	—	0.5	V
Output Voltage High	V_{OH}	I_{OL} = max	V_{DD} – 0.5	—	V_{DD}	V
Output Current Low	I_{OL}	—	—	—	6*	mA
Output Current High	I_{OH}	—	—	—	–6*	mA
Output Capacitance	C_O	—	—	3	—	pF
HIZ Output Leakage Current	I_{OZ}	—	—	—	10	µA

* Output current = 10 mA (maximum) for DTN, NSMITXCLK[3:1], and CHITXDATA[1, 3, 4, 5, 6, 10, 11].

Table 4-3. LVCMOS Bidirectional Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Leakage Current	I_L	$V_{SS} < V_{IN} < V_{DD33}$	—	—	11	µA
High-input Voltage	V_{IH}	—	2.0	—	V_{DD33} + 0.3	V
Low-input Voltage	V_{IL}	—	V_{SS}	—	0.8	V
Biput Capacitance	C_{IB}	—	—	5.0	—	pF
Output Voltage Low	V_{OL}	I_{OL} = –6 mA*	—	—	0.5	V
Output Voltage High	V_{OH}	I_{OH} = 6 mA*	2.4	—	—	V
Output Current Low	I_{OL}	—	—	—	6	mA
Output Current High	I_{OH}	—	—	—	–6	mA

* The following bidirectional pins can sink/source 10 mA: NSMIRXCLK[3:1].

4.2 LVDS Interface Characteristics

3.3 V ± 5% V_{DD}, –40 °C to +125 °C junction temperature.

Table 4-4. LVDS Interface dc Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Buffer Parameters						
Input Voltage Range: High (V_{IA} or V_{IB}) Low (V_{IA} or V_{IB})	V_I V_{IH} V_{IL}	$\|V_{GPD}\|$ < 925 mV, dc—1 MHz	 — 0	 — —	 2.4 —	 V V
Input Differential Threshold	V_{IDTH}	dc— 450 MHz	–100	—	100	mV
Input Differential Hysteresis	V_{HYST}	(+V_{IDTH}) – (–V_{IDTH})	—	—	—*	mV
Receiver Differential Input Impedance	R_{IN}	With build-in termination, center-tapped	80	100	120	Ω
Output Buffer Parameters						
Output Voltage: High (V_{OA} or V_{OB}) Low (V_{OA} or V_{OB})	 V_{OH} V_{OL}	 R_{LOAD} = 100 Ω ± 1% R_{LOAD} = 100 Ω ± 1%	 — 0.925	 — —	 1.475 —	 V V
Output Differential Voltage†	$\|V_{OD}\|$	R_{LOAD} = 100 Ω ± 1%	0.25	—	0.45	V
Output Offset Voltage	V_{OS}	R_{LOAD} = 100 Ω ± 1%	1.125	—	1.275	V
Output Impedance, Single Ended	R_O	V_{CM} = 1.0 V and 1.4 V	80	100	120	Ω
R_O Mismatch Between A and B	ΔR_O	V_{CM} = 1.0 V and 1.4 V	—	—	10	%
Change in Differential Voltage Between Complementary States	$\|\Delta V_{OD}\|$	R_{LOAD} = 100 Ω ± 1%	—	—	25	mV
Change in Output Offset Voltage Between Complementary States	ΔV_{OS}	R_{LOAD} = 100 Ω ± 1%	—	—	25	mV
Output Current	I_{SA}, I_{SB}	Driver shorted to V_{SS}	—	—	24	mA
Output Current	I_{SAB}	Drivers shorted together	—	—	12	mA

* The buffer will not produce output transitions when input is open-circuited. When the true and complement inputs are floating, the input buffer will not oscillate.

† 250 mV ≤ $|V_A – V_B|$ ≤ 450 mV

Notes:
The characteristics in the table above apply under the following conditions:
External LVDS reference chosen (UMPR_LVDS_REF_SEL = 0).
REF10 = 1.0 V ±3% and REF14 = 1.4 V ±3%.
Internal LVDS reference chosen (UMPR_LVDS_REF_SEL = 1).
VDD33 supply controlled to within ± 3%.
When UMPR_LVDS_REF_SEL = 1, the internal reference levels are derived using a resistor ladder from VDD33. These levels will vary as much as the VDD33 supply does and are therefore only as accurate as the VDD33. If VDD33 cannot be controlled to within ± 3%, one or more *IEEE* specifications may be violated. While this may not necessarily lead to data errors during transmission, interoperability issues may arise due to specification noncompliance.

5 Timing

5.1 TMUX High-Speed Interface Timing

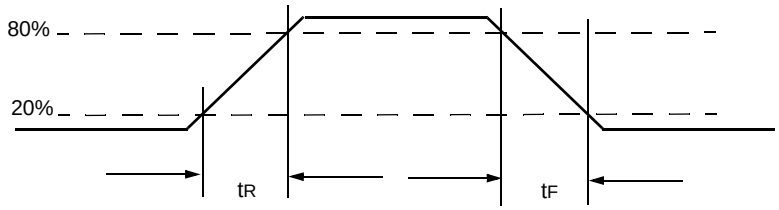


Figure 5-1. TMUX LVDS Signal Rise/Fall Timing

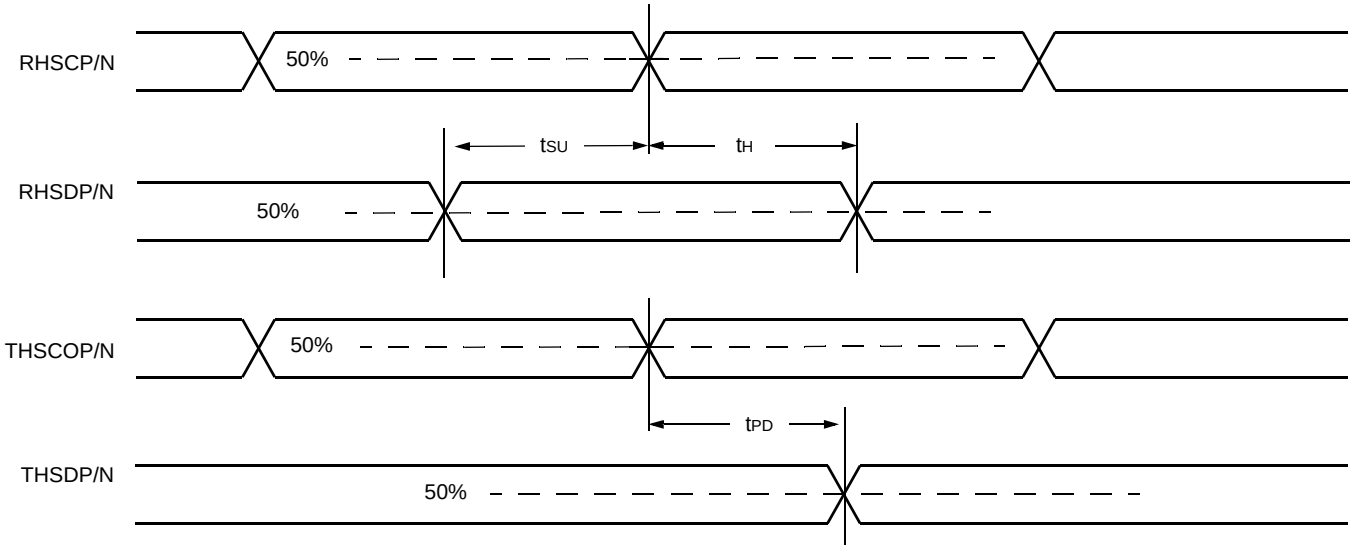


Figure 5-2. TMUX LVDS Clock and Data Timing

Table 5-1. High-Speed Interface Inputs Specifications

Name	Reference	Edge Rising/Falling	Max Rise Time (ns)	Max Fall Time (ns)	Min Setup (ns)	Min Hold (ns)
RHSDP/N (622 MHz)*	Asynchronous	—	0.5	0.5	—	—
RHSDP/N (155 MHz)*	Asynchronous	—	0.5	0.5	—	—
RHSDP/N (155 MHz)	RHSCP/N	R/F	1.0	1.0	2	0

* Input serial data stream should have minimum eye opening of 0.4 UIp-p, and no more than 60 consecutive bits that have no transitional edge within one minute. It must meet 100 ps maximum phase variation limit over a 200 ns interval; this translates to a frequency change of 500 ppm.

Table 5-2. Protection Link Inputs Specifications

Name	Reference	Edge Rising/Falling	Max Rise Time (ns)	Max Fall Time (ns)	Min Setup (ns)	Min Hold (ns)
RPSDP/N (622 MHz)*	Asynchronous	—	0.5	0.5	—	—
RPSDP/N (155 MHz)*	Asynchronous	—	0.5	0.5	—	—
RPSDP/N (155 MHz)	RPSCP/N	R	1.0	1.0	2	0

* Input serial data stream should have minimum eye opening of 0.4 UIp-p, and no more than 60 consecutive bits that have no transitional edge within one minute. It must meet 100 ps maximum phase variation limit over a 200 ns interval; this translates to a frequency change of 500 ppm.

Table 5-3. High-Speed Interface Outputs Specifications

Name	Reference	Edge Rising/Falling	Propagation Delay	
			Min (ns)	Max (ns)
THSDP/N (622.08 MHz or 155.52 MHz)	THSCOP/N	R	0.3	0.8
THSSYNC (MPU_MASTER_SLAVE = 1)	TLSCLK	—	–0.5	0.2

Table 5-4. Protection Link Output Specifications

Name	Reference	Edge Rising/Falling	Propagation Delay	
			Min (ns)	Max (ns)
TPSDP/N (622.08 MHz or 155.52 MHz)	TPSCP/N	R	0.3	0.8

5.2 THSSYNC Characteristics

THSSYNC is an 8 kHz composite frame sync pulse for STS-3 or STS-12. THSSYNC contains J0, J1, and V1-1 information as shown in Figure 5-5. The time delay from any rising edge of a J0 (8 kHz) to the rising edge of the next J0 is 125 µs. The time delay between any two V1-1 (2 kHz) pulses is 500 µs. This is true whether in STS-3 or STS-12 mode.

When MPU_MASTER_SLAVE = 1, then THSSYNC is according to Figure 5-5.

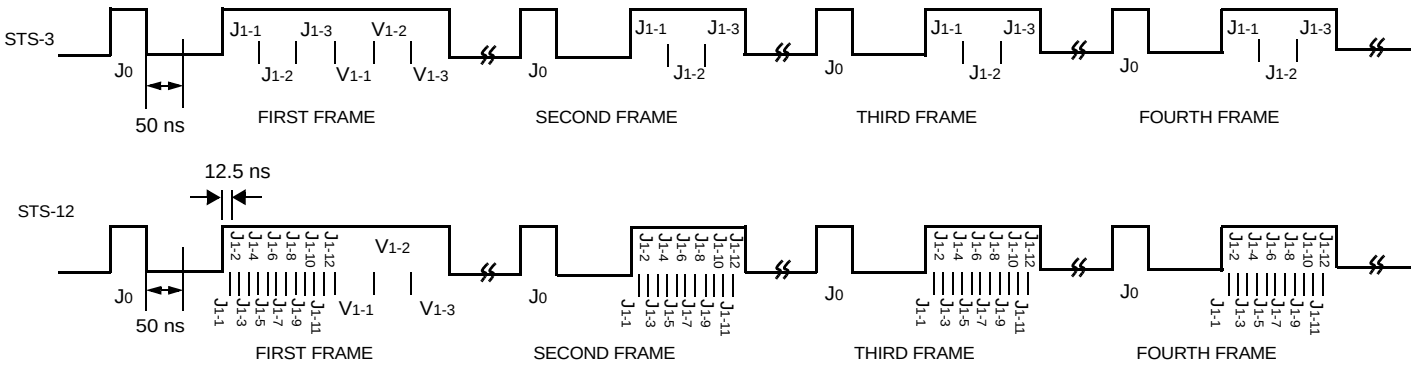


Figure 5-3. THSSYNC Timing Diagram (MPU_MASTER_SLAVE = 1)

When MPU_MASTER_SLAVE = 0, then THSSYNC (supplied from an external source) can be according to Figure 5-4.

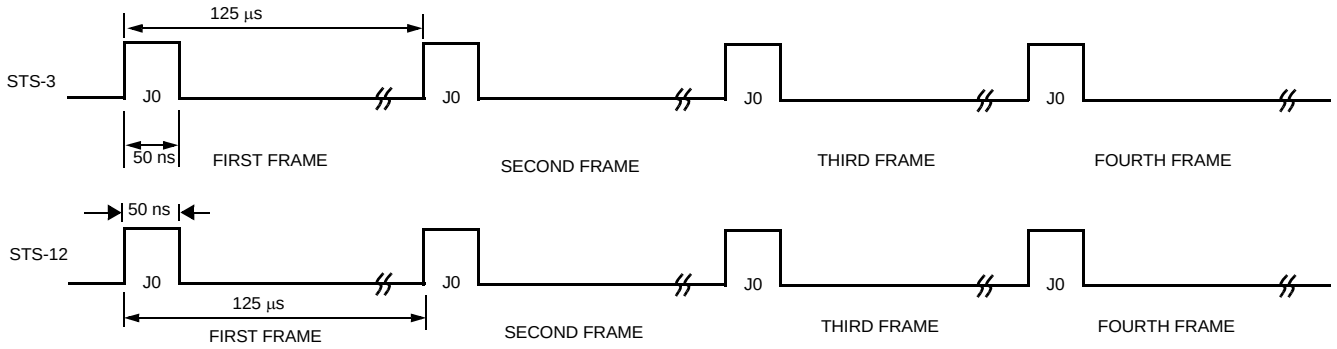


Figure 5-4. THSSYNC Timing Diagram (MPU_MASTER_SLAVE = 0)

When supplied externally, the 8 kHz THSSYNC may have a 50/50 duty cycle since the signal will only be sampled on the rising edge. In this case, THSSYNC should be synchronous to THSC. Although there are no setup/hold specifications for the THSSYNC input with respect to THSC, THSSYNC still needs to be synchronous to the input transmit high-speed clock (THSC). The device looks for the rising edge of THSSYNC to occur regularly in each frame within a window, defined by the setting in TMUX_SYNC_OFFSET[3:0]. A clock derived from THSC samples the incoming frame sync. If THSSYNC is not synchronous to THSC, over time, the rising edge of THSSYNC will fall outside the window causing an STS-N/STM-N level LOF.

However, if the system needs to synchronize VTs, generated from different *Ultramapper*s or other external devices, then THSSYNC needs to look like the waveform representation in Figure 5-5, i.e., THSSYNC must be composed of both the 8 kHz and the 2 kHz sync components (J_0 + V_{1-1}—V_{1-3}); the J_1 portion is not needed.

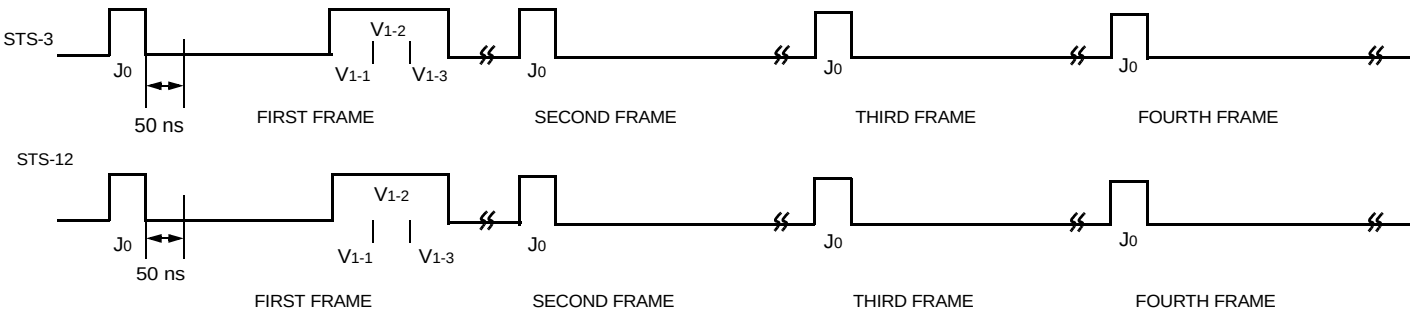
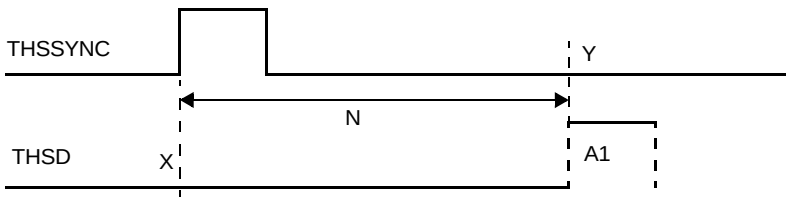


Figure 5-5. THSSYNC Timing Diagram for Synchronized VTs

Figure 5-6 depicts the relationship between the rising edge of the input THSSYNC (when the device is in slave mode) and the beginning of the SONET frame output on THSD. The delay between THSSYNC and the start of the outgoing SONET frame is contributed to internal device delays (pertaining to multiplexing functionality, FIFO, and parallel to serial conversion).



622 Mbits/s mode: N = 80 ± 8 bits. 155 Mbits/s mode: N = 44 ± 8 bits. For the case where TMUX_TLBITCNT, TMUX_TLSTSCNT, TMUX_TLCOLCNT, and TMUX_TLROWCNT, all = 0 (default). Changing these register values will change the location of point X with relation to point Y.

Figure 5-6. Relationship Between THSSYNC and THSD

5.3 STS-3/STM-1 Mate Interconnect Timing

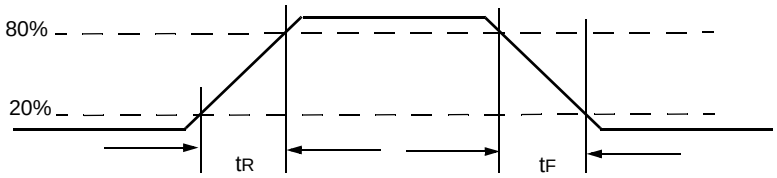


Figure 5-7. STS-3/STM-1 Mate Rise/Fall Timing

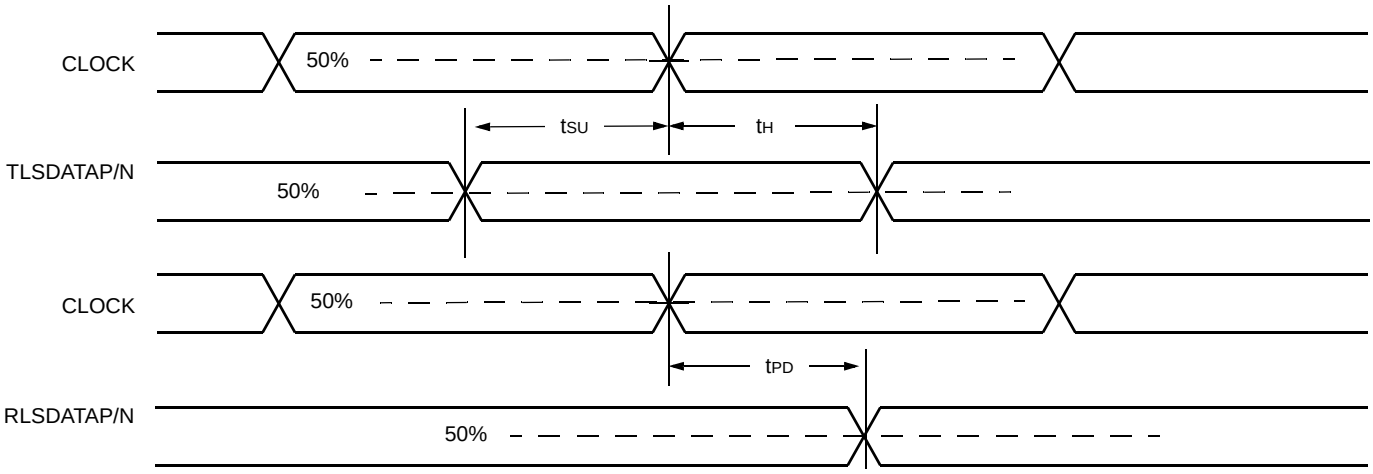


Figure 5-8. STS-3/STM-1 Mate Clock and Data Timing

Table 5-5. STS-3/STM-1 Mate Interconnect Input Specifications

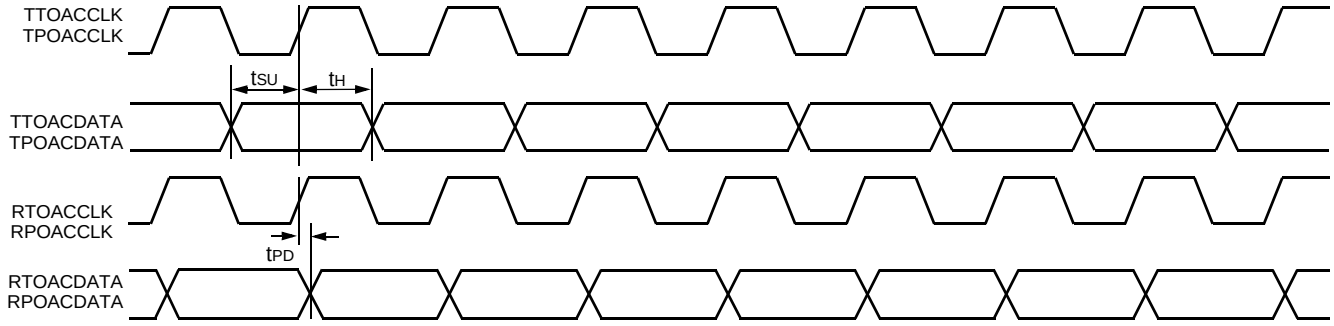
Name	Reference	Edge Rising/Falling	Max Rise Time (ns)	Max Fall Time (ns)	Min Setup (ns)	Min Hold (ns)
TLSDATAP/N[3:1]	Asynchronous	—	—	—	—	—

Table 5-6. STS-3/STM-1 Mate Interconnect Output Specifications

Name	Reference	Edge Rising/Falling	Propagation Delay	
			Min (ns)	Max (ns)
RLSDATAP/N[3:1]	Asynchronous	—	—	—

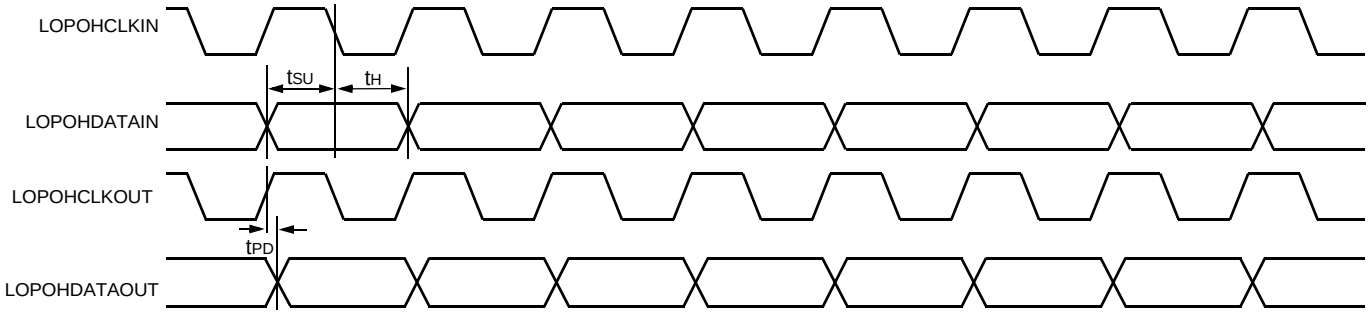
5.4 TOAC, POAC, and LOPOH Timing

The relationships between data, clock, and sync signals are specific to the TOAC and POAC operation mode selected. This is explained in detail in the TOAC/POAC chapter of the *System Design Guide*.



Note: For information pertaining to the output clock duty cycle (in various TOAC/POAC modes of operation), please refer toTable 6-15 and Table 6-16.

Figure 5-9. TOAC, POAC Timing



Note: For all modes, SYNC signals are high during the clock period of the first bit of each frame.

Figure 5-10. LOPOH Timing

Table 5-7. TOAC, POAC, and LOPOH Inputs Specifications

Name	Reference	Edge Rising/Falling	Max Rise Time (ns)	Max Fall Time (ns)	Min Setup (ns)	Min Hold (ns)
TTOACDATA	TTOACCLK (output)	R	10	10	3.5	0
TPOACDATA	TPOACCLK (output)	R	10	10	3.5	0
LOPOHDATAIN and LOPOHVALIDIN	LOPOHCLKIN	F	8	8	5	5

Table 5-8. TOAC, POAC, and LOPOH Outputs Specifications

Name	Reference	Edge Rising (R) Falling (F)	Propagation Delay	
			Min (ns)	Max (ns)
RTOACDATA, RTOACSYNC	RTOACCLK	R	0	3.5
TTOACSYNC	TTOACCLK	R	0	3.5
RPOACDATA, RPOACSYNC	RPOACCLK	F	0	3.5
TPOACSYNC	TPOACCLK	R	0	3.5
LOPOHDATAOUT and LOPOHVALIDOUT	LOPOHCLKOUT	R	0	5

5.5 DS3/E3/STS-1 Timing

Figure 5-11 shows a simplified representation of the DS3/E3/STS-1 I/O.

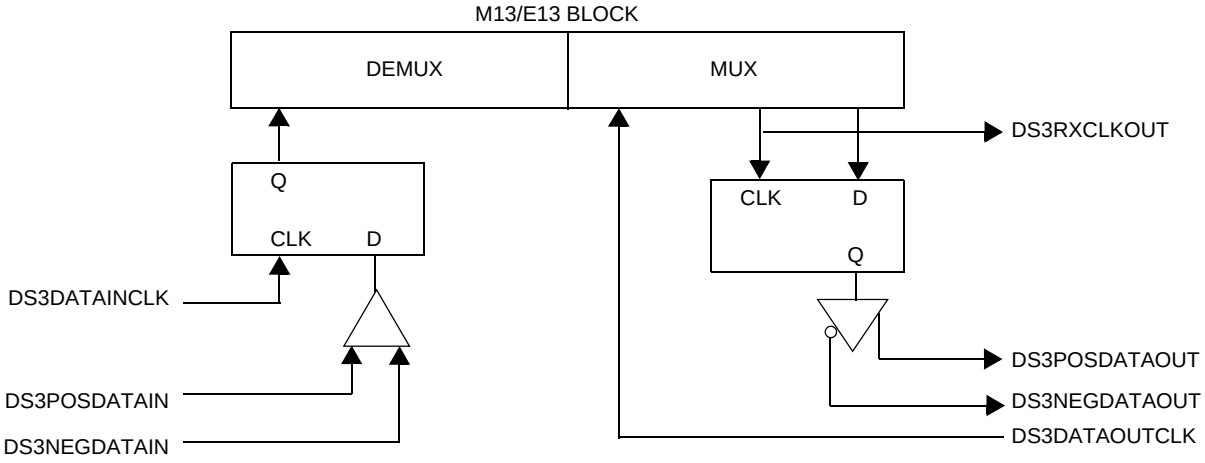


Figure 5-11. DS3/E3 Interface Diagram in M13/E13 Block

Table 5-9. DS3/E3 Inputs Specifications

Name	Reference	Edge Rising/Falling	Max Rise Time (ns)	Max Fall Time (ns)	Min Setup (ns)	Min Hold (ns)
DS3POSDATAIN[6:1] DS3NEGDATAIN[6:1]	DS3DATAINCLK	R/F	5	5	3	3

Table 5-10. STS-1 Inputs Specifications

Name	Reference	Edge Rising/Falling	Max Rise Time (ns)	Max Fall Time (ns)	Min Setup (ns)	Min Hold (ns)
DS3POSDATAIN[6:1] DS3NEGDATAIN[6:1]	DS3DATAINCLK	F	5	5	3	3

Table 5-11. DS3/E3/STS-1 Outputs Specifications

Name	Reference	Edge Rising/Falling	Propagation Delay	
			Min (ns)	Max (ns)
DS3POSDATAOUT[6:1] DS3NEGDATAOUT[6:1]	DS3RXCLKOUT	R/F	0	3

5.6 NSMI Timing

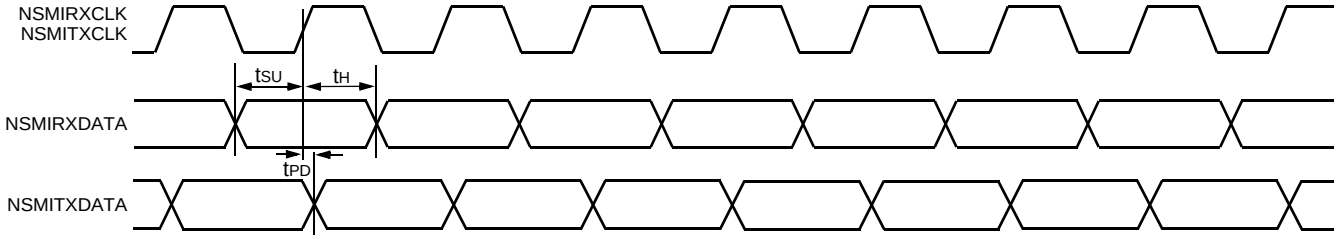
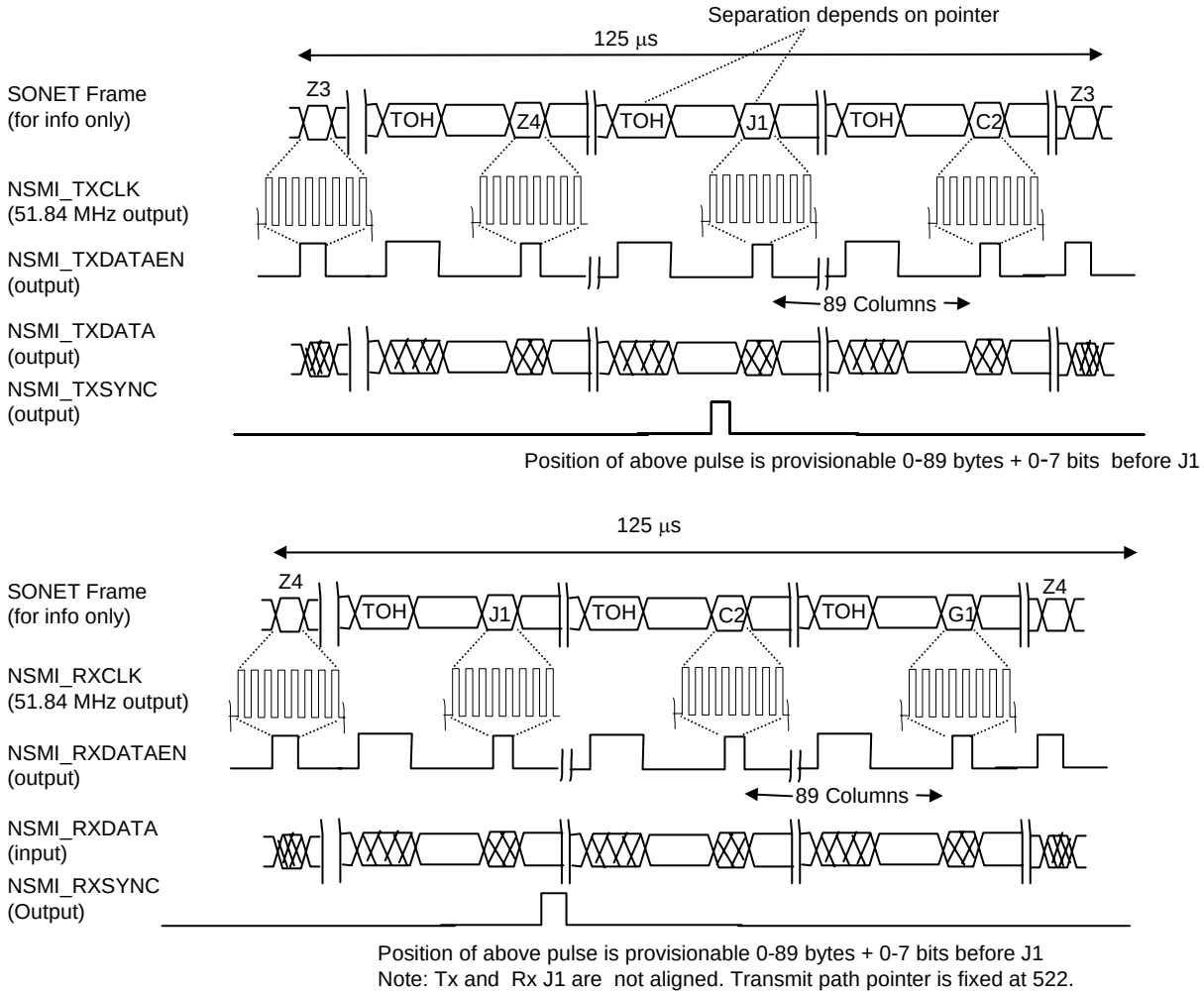


Figure 5-12. NSMI Clock and Data Timing for the STS-1 Mode

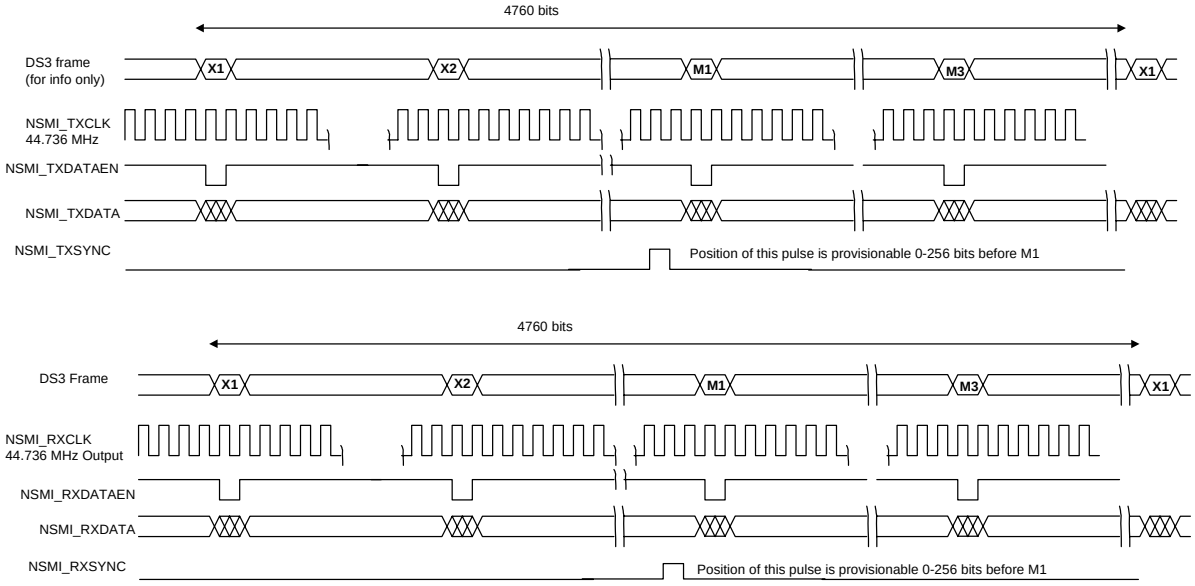


Notes:
Clock from SPEMPR is at 51.84 MHz rate and is not gapped. TXDATAEN is provided to mark the POH time of the SPE.

J1 can occur anywhere in the frame and its position is optionally marked by TXSYNC, which is provisioned to be N columns (bytes) plus M bits earlier in time than J1.

During periods where the POH is present the TXDATAEN signal goes high.

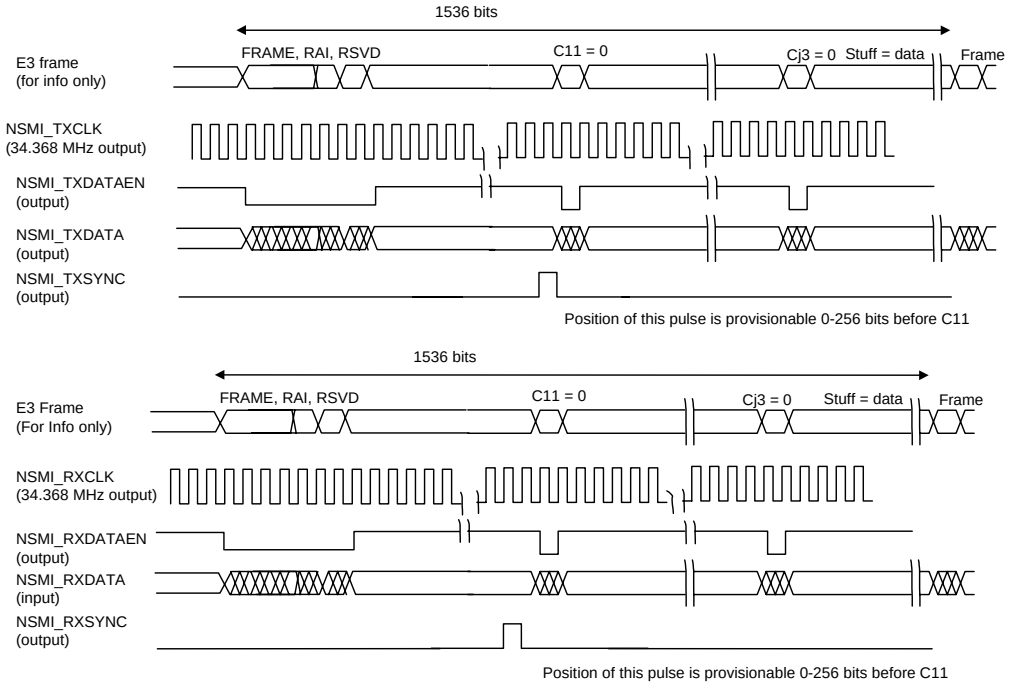
Figure 5-13. NSMI Clock and Data Diagram for SPEMPR NSMI Mode



Notes:
Clock from M13 is at 44.736 MHz rate and is not gapped. TXDATAEN is provided to mark the DS3 frame overhead times.

M1 can occur asynchronously and its position is optionally marked by TXSYNC, which is provisioned to be 0 to 255 bits before the M1 bit. TXDATAEN goes low during DS3 frame overhead bits.

Figure 5-14. NSMI Clock and Data Diagram for M13 NSMI Mode (NSMI <---> M13 <---> DS3 External I/O)

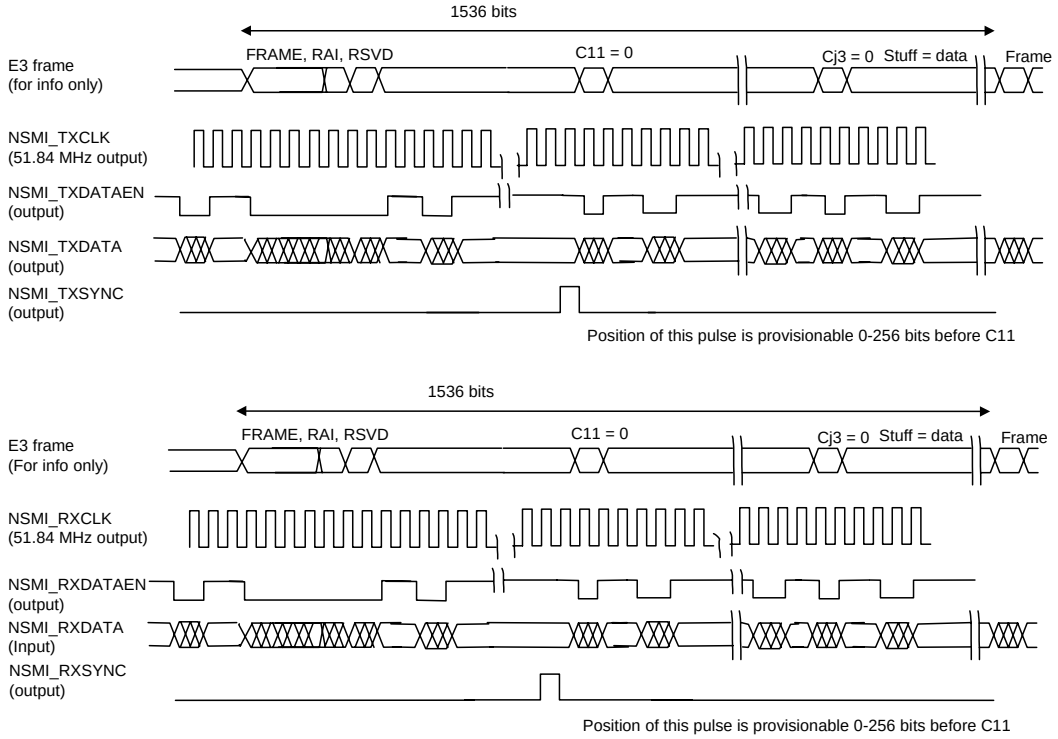


Notes:
Clock from E13 is at 34.368 MHz rate and is not gapped. TXDATAEN is provided to mark the overhead time and control bits time of the E3 frame.

C11's (the first C bit of the first tributary) position is optionally marked by TXSYNC, which is provisioned to be 0 to 255 bits before C11 (bit 385 of the E3 frame).

During periods where the OH is present the TXDATAEN signal goes low. All C bits are zero and the stuff bits are used for data.

Figure 5-15. NSMI Clock and Data Diagram for E13 NSMI Mode 1 (NSMI <---> E13 <---> E3 External I/O

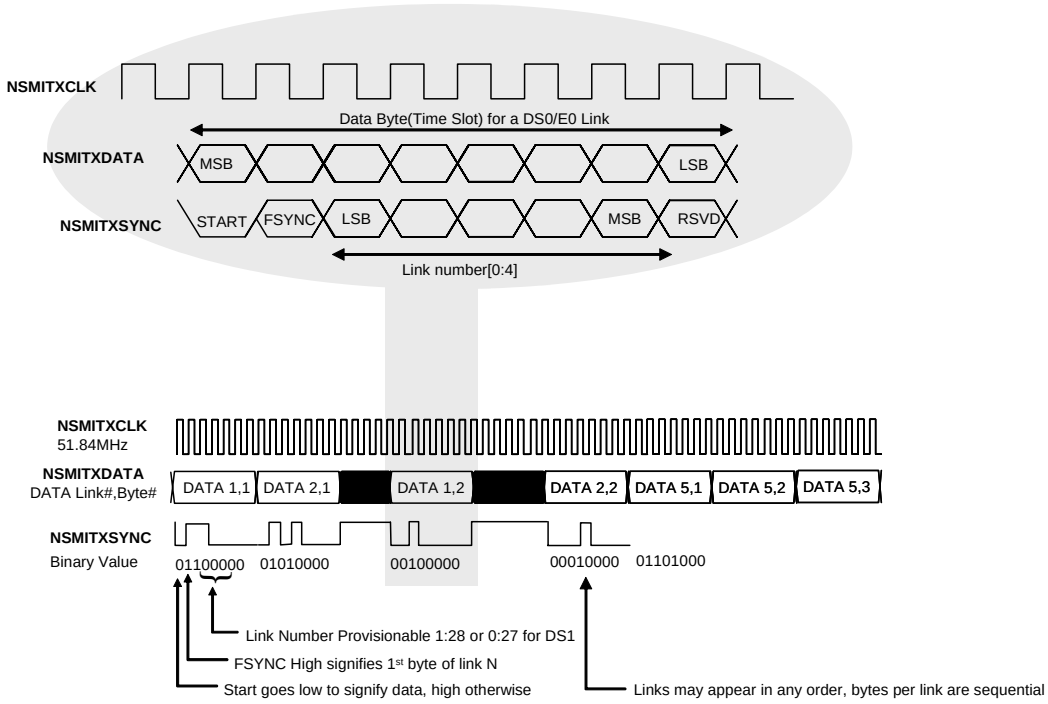


Notes:
Clock from E13 is at 51.84 MHz rate and is not gapped. TXDATAEN is the combination of an internal clock enable and data enable from SPEMPR. TXDATAEN is used to mark the overhead time and control bits time of the E3 frame. Clock enable is used to gap the clock rate to 34.368 MHz.

C11's (the first C bit of the first tributary) position is optionally marked by TXSYNC, which is provisioned to be 0 to 255 bits before C11 (bit 385 of the E3 frame).

During periods where the OH is present the TXDATAEN signal goes low. All C bits are zero and the stuff bits are used for data.

Figure 5-16. NSMI Clock and Data Diagram for E13 NSMI Mode 2 (NSMI <--> E13 <--> SPEMPR <--> STM-N)



Note: The 193rd bit of a DS1 frame is not transmitted on the NSMI but is used to locate the FSYNC position. As a consequence of this, signaling bits are not transported in *Ultramapper* versions 1—2.1. Version 3 devices contain a mode

Figure 5-17. NSMI Clock and Data Diagram for Framer (FRM) NSMI Mode

Table 5-12. NSMI Inputs Specifications

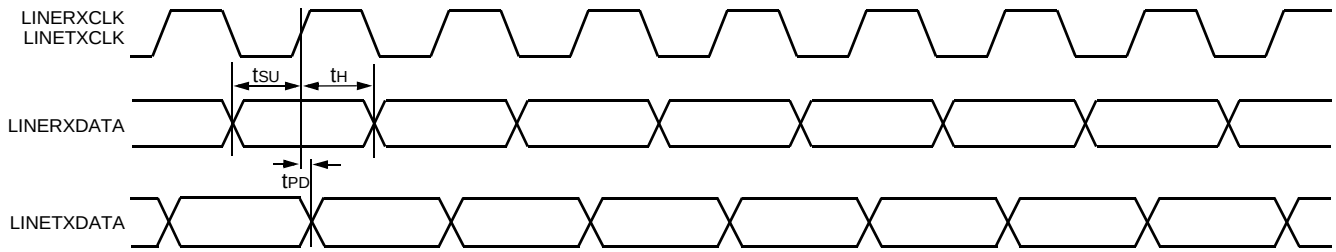
Name	Reference	Edge Rising/Falling	Max Rise Time (ns)	Max Fall Time (ns)	Min Setup (ns)	Min Hold (ns)
NSMIRXDATA[3:1]	NSMIRXCLK	R	3.5	3.5	5	0
NSMIRXSYNC[3:1]	NSMIRXCLK	R	3.5	3.5	5	0
NSMIRXDATA[3:1]*	NSMIRXCLK	R	3.5	3.5	3.5	3
NSMIRXSYNC[3:1]*	NSMIRXCLK	R	3.5	3.5	3.5	3

* Pertinent to DS3 clear channel application, which uses NSMI I/O—this feature is available only in V3.0 devices.

Table 5-13. NSMI Outputs Specifications

Name	Reference	Edge Rising/Falling	Propagation Delay	
			Min (ns)	Max (ns)
NSMITXDATA[3:1]	NSMITXCLK	R	0.5	8.75
NSMITXSYNC[3:1]	NSMITXCLK	R	0.5	8.75
RXDATAEN[3:1]	NSMIRXCLK	R	0.5	8.75
TXDATAEN[3:1]	NSMITXCLK	R	0.5	8.75
NSMIRXSYNC[3:1]	NSMIRXCLK	R	0.5	8.75

5.7 Shared Low-Speed Line Timing



Note: Single rail shown.

Figure 5-18. Shared Low-Speed Line Clock and Data Timing

Table 5-14. Shared Low-Speed Line Timing Input Specifications

Name	Reference	Edge Rising/Falling	Max Rise Time (ns)	Max Fall Time (ns)	Min Setup (ns)	Min Hold (ns)
LINERXDATA[30:1]	LINERXCLK[30:1]	R/F	10*	10*	15	10*

* Alternative specification: the maximum rise and fall times may be increased to 20 ns each if the minimum hold time is increased to 12 ns. The minimum setup time will remain at 15 ns.

Table 5-15. Shared Low-Speed Line Timing Output Specifications

Name	Reference	Edge Rising/Falling	Propagation Delay	
			Min (ns)	Max (ns)
LINETXDATA[30:1]	LINETXCLK[30:1]	R/F	–10	10

5.8 CHI Timing

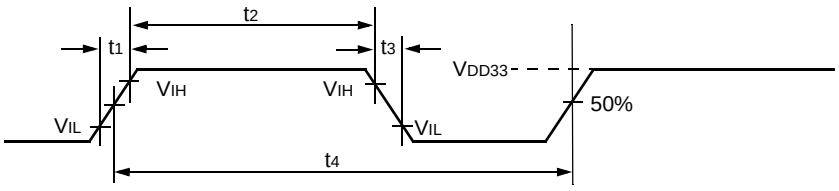
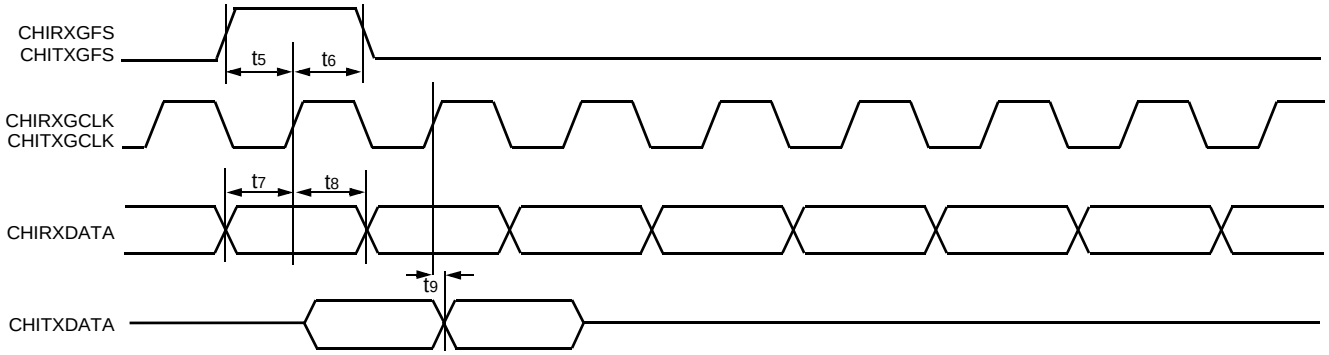


Figure 5-19. CHI Clock Timing

Table 5-16. CHIRXGCLK and CHITXGCLK Timing Specifications

Parameter	Description	Min	Typ	Max	Unit
t1	Rise Time	—	2	7	ns
t2	Width (8.192 MHz)*	48.84	—	73.24	ns
t2	Width (16.384 MHz)*	24.42	—	36.62	ns
t3	Fall Time	—	2	7	ns
t4	Period (8.192 MHz)	—	122.07	—	ns
t4	Period (16.384 MHz)	—	61.03	—	ns

* VIH to VIH or VIL to VIL.

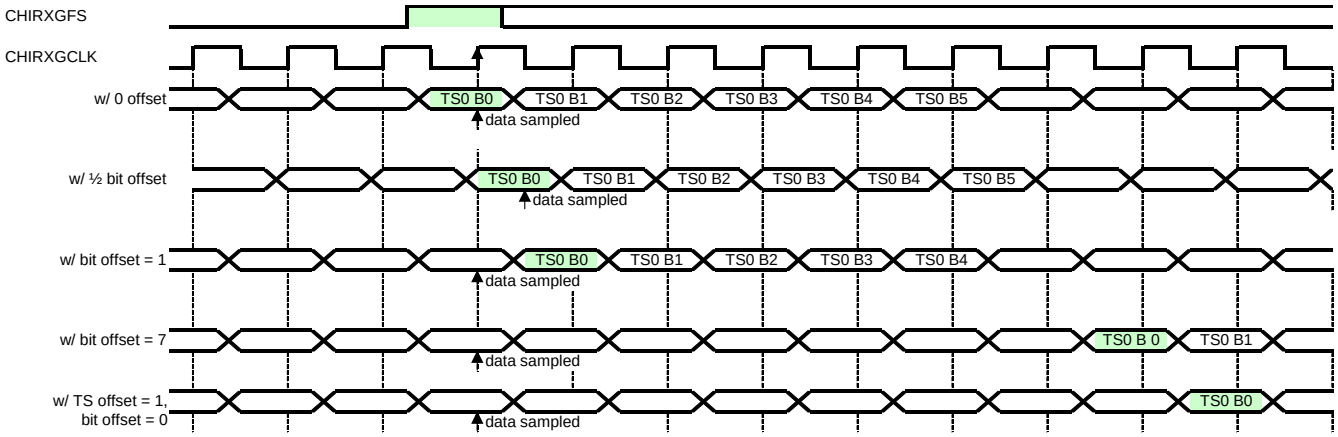


Note: This figure assumes TMXF846221BL-2 is programmed to sample the frame sync signal on the rising edge of the bit clock.

Figure 5-20. CHI Bus Timing

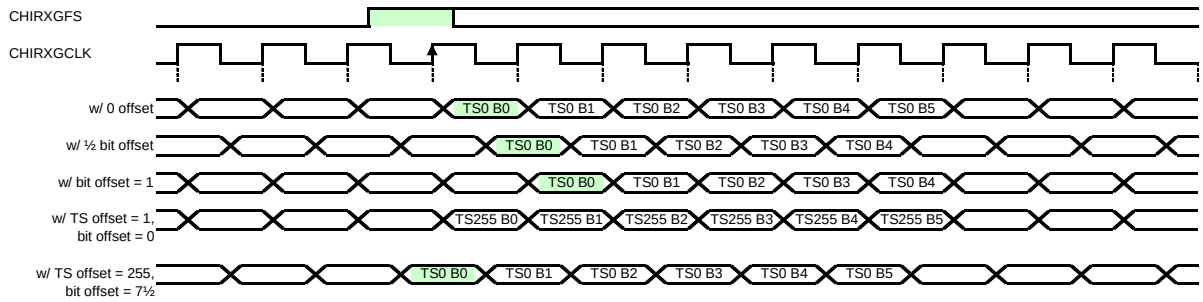
Table 5-17. CHI Interface Timing Specifications

Parameter	Description	Min	Max	Unit
t5	Frame Sync Setup Time to Active CHI Clock Edge	15	—	ns
t6	Frame Sync Hold Time from Active CHI Clock Edge	4	—	ns
t7	CHIRXDATA Setup to Active CHI Clock Edge	15	—	ns
t8	CHIRXDATA Hold Time from Active CHI Clock Edge	4	—	ns
t9	CHITXDATA Propagation Delay from Active CHI Clock Edge	4	30	ns



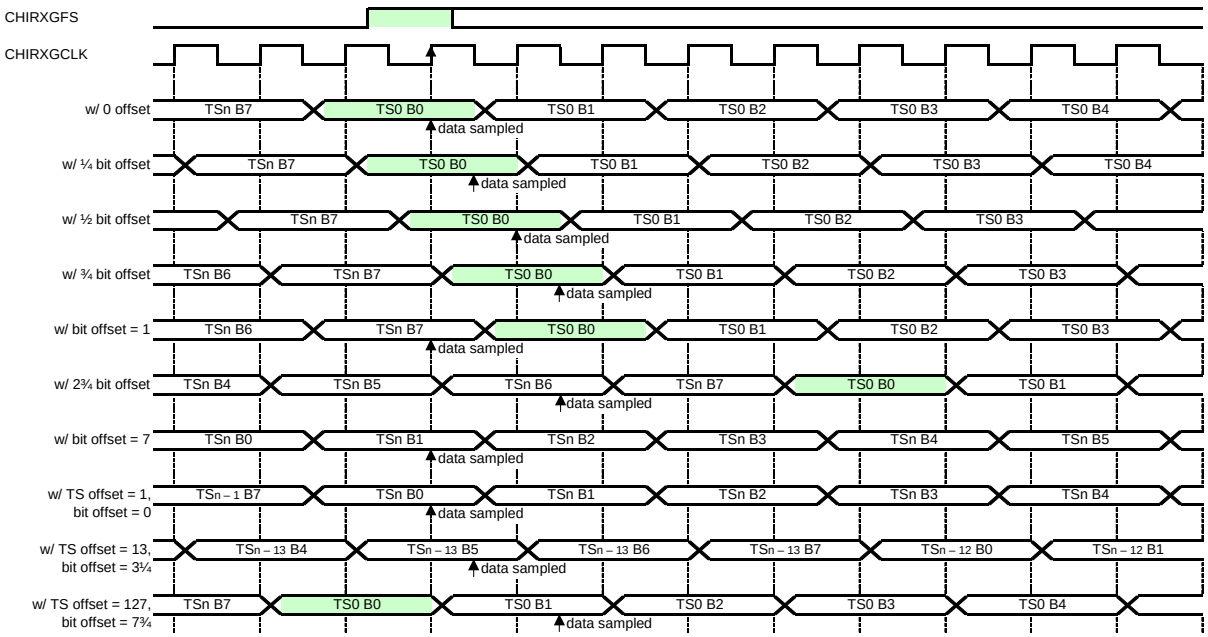
Note: For this timing diagram, it is assumed that the frame sync signal has been programmed to be active-high, and to be sampled by the rising edge of the bit clock.

Figure 5-21. Typical Receive CHI Timing (Non-CMS Mode—FRM_CMS = 0)



Note: For this timing diagram, it is assumed that the frame sync signal has been programmed to be active-high, and to be sampled by the rising edge of the bit clock.

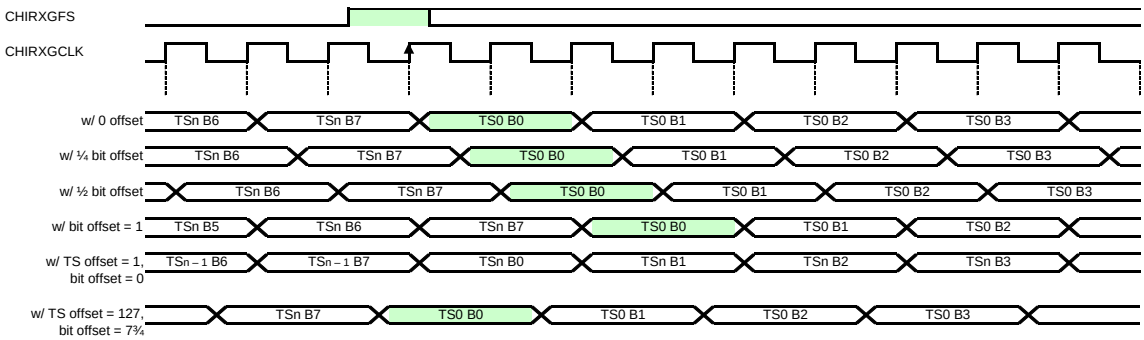
Figure 5-22. Transmit CHI Timing (Non-CMS Mode—FRM_CMS = 0)



Notes:
n = 127 at 16 MHz, n = 63 at 8 MHz, and n = 31 at 4 MHz.

For this timing diagram, it is assumed that the frame sync signal has been programmed to be active-high, and to be sampled by the rising edge of the bit clock.

Figure 5-23. Typical Receive CHI Timing (CMS Mode—FRM_CMS = 1, CHIRX/TXGCLK ≥ 4 MHz)



Note: For this timing diagram, it is assumed that the frame sync signal has been programmed to be active-high, and to be sampled by the rising edge of the bit clock.

Figure 5-24. Transmit CHI Timing (CMS Mode—FRM_CMS = 1, CHIRX/TXGCLK ≥ 4 MHz))

5.9 Parallel System Bus (PSB) Timing

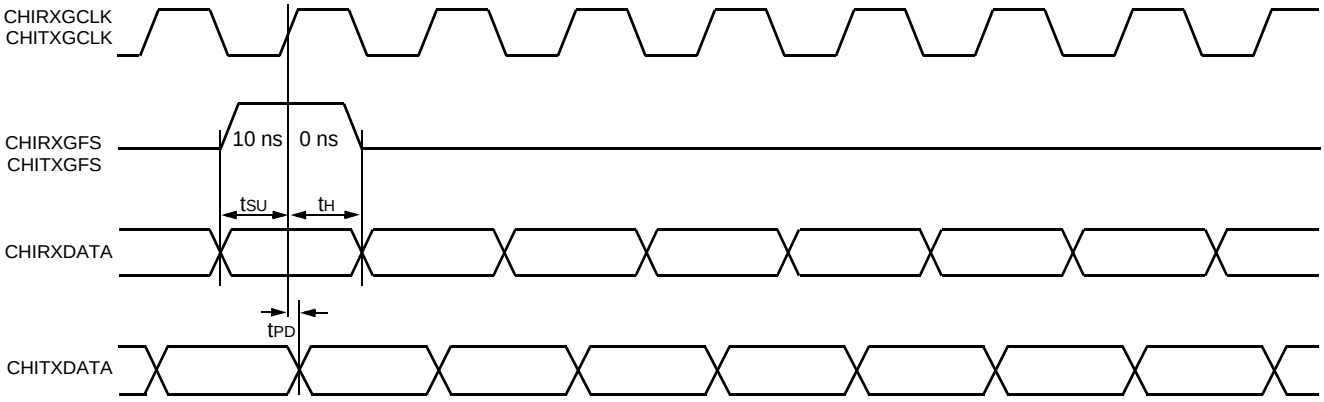


Figure 5-25. PSB Clock and Data Timing

Table 5-18. PSB Inputs Specifications

Name	Reference	Edge Rising/Falling	Max Rise Time (ns)	Max Fall Time (ns)	Min Setup (ns)	Min Hold (ns)
CHIRXDATA[16:1] (PSB mode)	CHIRXGCLK	R/F	10	10	10	0
CHIRXGFS (PSB mode)	CHIRXGCLK	R/F	10	10	10	0
CHITXGFS (PSB mode)	CHITXGCLK	R/F	10	10	10	0

Table 5-19. PSB Output Specifications

Name	Reference	Edge Rising/Falling	Propagation Delay	
			Min (ns)	Max (ns)
CHITXDATA[16:1] (PSB mode)	CHITXGCLK	R/F	4	22

6 Reference Clocks

Table 6-1. High-Speed Interface Input Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
RHSCP/N	6.43	155.52 MHz	20	—	0.4	0.4	Nom	45%—55%
THSCP/N	6.43	155.52 MHz	20	0.01 UIp-p or 64 psp-p or 0.001 UIrms (12 kHz—1.3 MHz)	0.4	0.4	Nom	45%—55%
THSCP/N	1.6	622.08 MHz	20	0.04 UIp-p or 64 psp-p (12 kHz—5 MHz)	0.4 (nom)	0.6 (max)	—	45%—55%

Table 6-2. Protection Link Input Clock Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
RPSCP/N	6.43	155.52 MHz	20	—	0.4	0.4	Nom	45%—55%

Table 6-3. DS3/E3/STS-1 Input Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
DS3DATAOUTCLK[6:1] (DS3)	22.353	44.736 MHz	20	0.05 UIp-p or 1.12 nsp-p (10 kHz—400 kHz)	5	5	Max	40%—60%
DS3DATAINCLK[6:1](DS3)	22.353	44.736 MHz	20	—	3.5	2.5	Max	45%—55%
DS3DATAOUTCLK[6:1](E3)	29.090	34.368 MHz	20	0.03 UIp-p or 0.87 nsp-p (100 kHz—800 kHz)	5	5	Max	40%—60%
DS3DATAINCLK[6:1]](E3)	29.090	34.368 MHz	20	—	3.5	2.5	Max	45%—55%
DS3DATAOUTCLK[6:1](STS-1)	19.290	51.84 MHz	20	0.01 UIp-p or 0.19 nsp-p or 0.001 UIrms (12 kHz—400 kHz)	5	5	Max	40%—60%
DS3DATAINCLK[6:1](STS-1)	19.290	51.84 MHz	20	—	3.5	2.5	Max	45%—55%

Table 6-4. DS1/E1 DJA Input Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
E1XCLK	15.25	65.536 MHz	50	0.1 UIp-p or 1.5 nsp-p (20 kHz—100 kHz)	3.5	3.5	Max	40%—60%
DS1XCLK	20.20	49.408 MHz	32	0.1 UIp-p or 2.0 nsp-p (10 kHz—40 kHz)	3.5	3.5	Max	40%—60%
E1XCLK	30.52	32.768 MHz	50	0.1 UIp-p or 3.0 nsp-p (20 kHz—100 kHz)	3.5	3.5	Max	40%—60%
DS1XCLK	40.40	24.704 MHz	32	0.1 UIp-p or 4.0 nsp-p (10 kHz—40 kHz)	3.5	3.5	Max	40%—60%

Table 6-5. M13/E13 Input Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
DS2AISCLK	158.42	6.312 MHz	30	—	5	5	Max	45%—55%
E2AISCLK	118.37	8.448 MHz	30	—	5	5	Max	45%—55%

Table 6-6. DS3/E3 DJA Input Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
DS3XCLK	22.35	44.736 MHz	20	0.01 UIp-p or 0.22 nsp-p (10 Hz—400 kHz)	3.5	3.5	Max	45%—55%
E3XCLK	29.09	34.368 MHz	20	0.01 UIp-p or 0.29 nsp-p (100 Hz—800 kHz)	3.5	3.5	Max	45%—55%

Table 6-7. LOPOH Input Clock Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
LOPOHCLKIN	51.44	19.44 MHz	—	—	8	8	Max	45%—55%

Table 6-8. Microprocessor Interface Input Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/Max	Duty Cycle
MPCLK (min)	62.5	16 MHz	—	—	4	4	Min	45%—55%
MPCLK (max)*	15.0	66.67 MHz	—	—	4	4	Max	45%—55%

* The following applies to the synchronous microprocessor mode (MPMODE pin = 1): If DTN is used, then the maximum frequency for MPCLK is determined by the processor's setup specification for DTN. MPU maximum bus operating frequency = 1/(MPU DTN setup time + tDTNVPD). For example, an 8 ns setup time would limit MPCLK to 50 MHz for reliable DTN detection.

Table 6-9. Framer PLL Input Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/Max	Duty Cycle
CLKIN_PLL	19.2	51.84 MHz	20	GR-499 and G.823	—	—	—	40%—60%
CHIRXGTCLK (DS1 mode)	647.66	1.544 MHz	32	GR-499	10	10	Max	40%—60%
CHIRXGTCLK (E1 mode)	488.28	2.048 MHz	50	G.823	10	10	Max	40%—60%

Table 6-10. CHI Input Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/Max	Duty Cycle
CHIRXGCLK (CHI mode)	488.28	2.048 MHz	50	—	10	10	Max	40%—60%
CHIRXGCLK (CHI mode)	244.14	4.096 MHz	50	—	10	10	Max	40%—60%
CHIRXGCLK (CHI mode)	122.07	8.192 MHz	50	—	10	10	Max	40%—60%
CHIRXGCLK (CHI mode)	61.035	16.384 MHz	50	—	10	10	Max	40%—60%
CHITXGCLK (CHI mode)	488.28	2.048 MHz	50	—	10	10	Max	40%—60%
CHITXGCLK (CHI mode)	244.14	4.096 MHz	50	—	10	10	Max	40%—60%
CHITXGCLK (CHI mode)	122.07	8.192 MHz	50	—	10	10	Max	40%—60%
CHITXGCLK (CHI mode)	61.035	16.384 MHz	50	—	10	10	Max	40%—60%

Table 6-11. PSB Input Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
CHIRXGCLK (PSB mode)	51.44	19.44 MHz	20	—	10	10	Max	40%—60%
CHITXGCLK (PSB mode)	51.44	19.44 MHz	20	—	10	10	Max	40%—60%

Table 6-12. High-Speed Interface Output Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
THSCOP/N	6.43	155.52 MHz	20	0.1 UIp-p	—	—	—	45%—55%
THSCOP/N	1.6	622 MHz	20	0.1 UIp-p	—	—	—	45%—55%

Table 6-13. Protection Link Output Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
TPSCP/N	6.43	155.52 MHz	20	—	—	—	—	45%—55%
TPSCP/N	1.6	622.08 MHz	20	—	—	—	—	45%—55%

Table 6-14. Line Timing Interface Output Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
RLSCLK	51.44	19.44 MHz	20	—	1.5	1.5	Nom	45%—55%
TLSCLK	51.44	19.44 MHz	20	—	1.5	1.5	Nom	45%—55%

Table 6-15. TOAC Output Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
RTOACCLK (STS1LT; full access)	578	1.728 MHz	—	—	1.5	1.5	Nom	40%—60%
RTOACCLK (TMUX; STS-12 D1-3 mode)	5.2 (µs)	192 kHz	—	—	1.5	1.5	Nom	27%—47%*
RTOACCLK (TMUX; STS-12 D4-12 mode)	1.73 (µs)	576 kHz	—	—	1.5	1.5	Nom	43%—63%*
RTOACCLK (TMUX; STS-12 full access)	48.22	20.736 MHz	—	—	1.5	1.5	Nom	23%—43%*
RTOACCLK (TMUX; STS-3 D1-3 mode)	5.2 (µs)	192 kHz	—	—	1.5	1.5	Nom	48%—68%*
RTOACCLK (TMUX; STS-3 D4-12 mode)	1.73 (µs)	576 kHz	—	—	1.5	1.5	Nom	42%—62%*
RTOACCLK (TMUX; STS-3 full access)	192.9	5.184 MHz	—	—	1.5	1.5	Nom	23%—43%*
TTOACCLK (STS1LT; full access)	578	1.728 MHz	—	—	1.5	1.5	Nom	40%—60%
TTOACCLK (TMUX; STS-12 D1-3 mode)	5.2 (µs)	192 kHz	—	—	1.5	1.5	Nom	27%—47%*
TTOACCLK (TMUX; STS-12 D4-12 mode)	1.73 (µs)	576 kHz	—	—	1.5	1.5	Nom	43%—63%*
TTOACCLK (TMUX; STS-12 full access)	48.22	20.736 MHz	—	—	1.5	1.5	Nom	23%—43%*
TTOACCLK (TMUX-STS-3 D1-3 mode)	5.2 (µs)	192 kHz	—	—	1.5	1.5	Nom	48%—68%*
TTOACCLK (TMUX-STS-3 D4-12 mode)	1.73 (µs)	576 kHz	—	—	1.5	1.5	Nom	42%—62%*
TTOACCLK (TMUX-STS-3 full access)	192.9	5.184 MHz	—	—	1.5	1.5	Nom	23%—43%*

* Positive duty cycle.

Table 6-16. POAC Output Clocks Specifications

Clock Name	Period	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
RPOACCLK (TMUX)	1.73 (µs)	576 kHz	—	—	1.5	1.5	Nom	40%—60%
RPOACCLK (STS1LT)	1.73 (µs)	576 kHz	—	—	1.5	1.5	Nom	40%—60%
RPOACCLK (SPEMPR)	1.73 (µs)	576 kHz	—	—	1.5	1.5	Nom	40%—60%
TPOACCLK (TMUX)	1.73 (µs)	576 kHz	—	—	1.5	1.5	Nom	40%—60%
TPOACCLK (STS1LT)	1.73 (µs)	576 kHz	—	—	1.5	1.5	Nom	40%—60%
TPOACCLK (SPEMPR)	1.73 (µs)	576 kHz	—	—	1.5	1.5	Nom	40%—60%

Table 6-17. DS3/E3/STS-1 Output Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
DS3RXCLKOUT [6:1](DS3)	22.353	44.736 MHz	20	GR-253	1.5	1.5	Nom	45%—55%
DS3RXCLKOUT [6:1](E3)	29.09	34.368 MHz	20	G.783	1.5	1.5	Nom	45%—55%
DS3RXCLKOUT [6:1] (STS-1)	19.29	51.84 MHz	20	GR-253	1.5	1.5	Nom	45%—55%

Table 6-18. LOPOH Output Clock Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
LOPOHCLKOUT	51.44	19.44 MHz	20	—	1.5	1.5	Nom	45%—55%

Table 6-19. NSMI Output Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
RXDATAEN	19.29	51.84 MHz	20	—	1.5	1.5	Nom	45%—55%
NSMITXCLK	19.29	51.84 MHz	20	—	1.5	1.5	Nom	45%—55%

Table 6-20. Framer PLL Output Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
CG_PLLCLKOUT	647.66	1.544 MHz	32	GR-499	—	—	—	45%—55%
CG_PLLCLKOUT	488.28	2.048 MHz	50	G.823	—	—	—	45%—55%

Table 6-21. Shared Low-Speed Receive Line Input/Output Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
LINERXCLK (framer; DS1)	647.66	1.544 MHz	32	—	10	10	Max	45%—55%
LINERXCLK (framer; E1)	488.28	2.048 MHz	50	—	10	10	Max	45%—55%
LINERXCLK (M12)	647.66	1.544 MHz	32	—	10	10	Max	45%—55%
LINERXCLK (E12)	488.28	2.048 MHz	50	—	10	10	Max	45%—55%
LINERXCLK (VTMPR; DS1)	647.66	1.544 MHz	32	—	10	10	Max	45%—55%
LINERXCLK (VTMPR; E1)	488.28	2.048 MHz	50	—	10	10	Max	45%—55%
LINERXCLK (VTMPR; VC11)	600.96	1.664 MHz	20	—	10	10	Max	45%—55%
LINERXCLK (VTMPR; VC12)	446.42	2.24 MHz	20	—	10	10	Max	45%—55%
LINERXCLK (M23)	158.42	6.312 MHz	30	—	10	10	Max	45%—55%

Table 6-21. Shared Low-Speed Receive Line Input/Output Clocks Specifications (continued)

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
LINERXCLK (E23)	118.37	8.448 MHz	30	—	10	10	Max	45%—55%
LINERXCLK (DJA; DS1)	647.66	1.544 MHz	32	—	10	10	Max	45%—55%
LINERXCLK (DJA; E1)	488.28	2.048 MHz	50	—	10	10	Max	45%—55%
LINERXCLK (TPG; DS1)	647.66	1.544 MHz	32	—	10	10	Max	45%—55%
LINERXCLK (TPG; E1)	488.28	2.048 MHz	50	—	10	10	Max	45%—55%

Table 6-22. Shared Low-Speed Transmit Line Input/Output Clocks Specifications

Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
LINETXCLK (framer; DS1)	647.66	1.544 MHz	32	—	1.5	1.5	Nom	45%—55%
LINETXCLK (framer; E1)	488.28	2.048 MHz	50	—	1.5	1.5	Nom	45%—55%
LINETXCLK (M12)	647.66	1.544 MHz	32	—	10	10	Max	45%—55%
LINETXCLK (E12)	488.28	2.048 MHz	50	—	10	10	Max	45%—55%
LINETXCLK (VTMPR; DS1)	647.66	1.544 MHz	32	—	1.5	1.5	Nom	45%—55%
LINETXCLK (VTMPR; E1)	488.28	2.048 MHz	50	—	1.5	1.5	Nom	45%—55%
LINETXCLK (VTMPR; VC11)	600.96	1.664 MHz	20	—	1.5	1.5	Nom	45%—55%
LINETXCLK (VTMPR; VC12)	446.42	2.24 MHz	20	—	1.5	1.5	Nom	45%—55%
LINETXCLK (M23)	158.42	6.312 MHz	30	—	10	10	Max	45%—55%
LINETXCLK (E23)	118.37	8.448 MHz	30	—	10	10	Max	45%—55%
LINETXCLK (DJA; DS1)	647.66	1.544 MHz	32	—	1.5	1.5	Nom	45%—55%
LINETXCLK (DJA; E1)	488.28	2.048 MHz	50	—	1.5	1.5	Nom	45%—55%
LINETXCLK (TPG; DS1)	647.66	1.544 MHz	32	—	1.5	1.5	Nom	45%—55%
LINETXCLK (TPG; E1)	488.28	2.048 MHz	50	—	1.5	1.5	Nom	45%—55%

Table 6-23. NSMI Input/Output Clocks Specifications

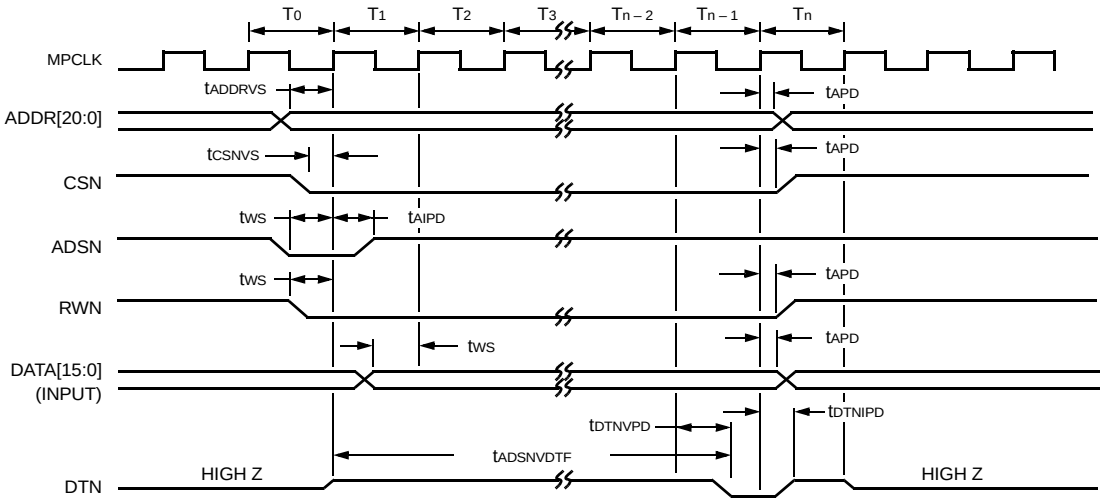
Clock Name	Period (ns)	Frequency	Accuracy (ppm)	Jitter	Rise (ns)	Fall (ns)	Min/ Max	Duty Cycle
NSMIRXCLK (framer)	19.29	51.84 MHz	20	—	3.5	3.5	Max	45%—55%
NSMIRXCLK (STS1LT)	19.29	51.84 MHz	20	—	3.5	3.5	Max	45%—55%
NSMIRXCLK (M13)	22.35	44.736 MHz	20	—	1.5	1.5	Nom	45%—55%
NSMIRXCLK (E13)	29.09	34.368 MHz	20	—	1.5	1.5	Nom	45%—55%
NSMIRXCLK (SPEMPR)	19.29	51.84 MHz	20	—	3.5	3.5	Max	45%—55%

7 Microprocessor Interface Timing

Note: To allow proper operation of the microprocessor interface upon device/board bring up, the recommended powerup sequence (listed in Section 3.6 Recommended Powerup Sequence, on page 37) should be followed. Specifically, to avoid potential bus contention issues, the IC3STATEN pin should be held low during boot up.

7.1 Synchronous Write Mode

The synchronous microprocessor interface mode is selected when MPMODE (pin F6) = 1. In this mode, MPCLK used for the *Ultramapper* is the same as the microprocessor clock. Interface timing for the synchronous mode write cycle is given in Figure 7-1 and in Table 7-1, and for the read cycle in Figure 7-2 and in Table 7-2.



Notes:

MPCLK	Input clock to *Ultramapper* MPU block.
ADDR [20:0]	The address will be available throughout the entire cycle.
CSN (Input)	Chip select is an active-low signal.
ADSN (Input)	Address strobe is active-low. ADSN must be one MPCLK clock period wide.
RWN (Input)	The read (H) write (L) signal is always high except during a write cycle.
DATA[15:0]	Data will be available during cycle T1.
DTN (Output)	Data transfer acknowledge is active-low for one clock and then driven high before entering a high-impedance state. (This is done with an I/O pad using the input as feedback to qualify the 3-state term.) DTN will become 3-stated when CSN is high. Typically, DTN is active for four or five MPCLK cycles after ADSN is low.

Figure 7-1. Microprocessor Interface Synchronous Write Cycle—MPMODE Pin = 1

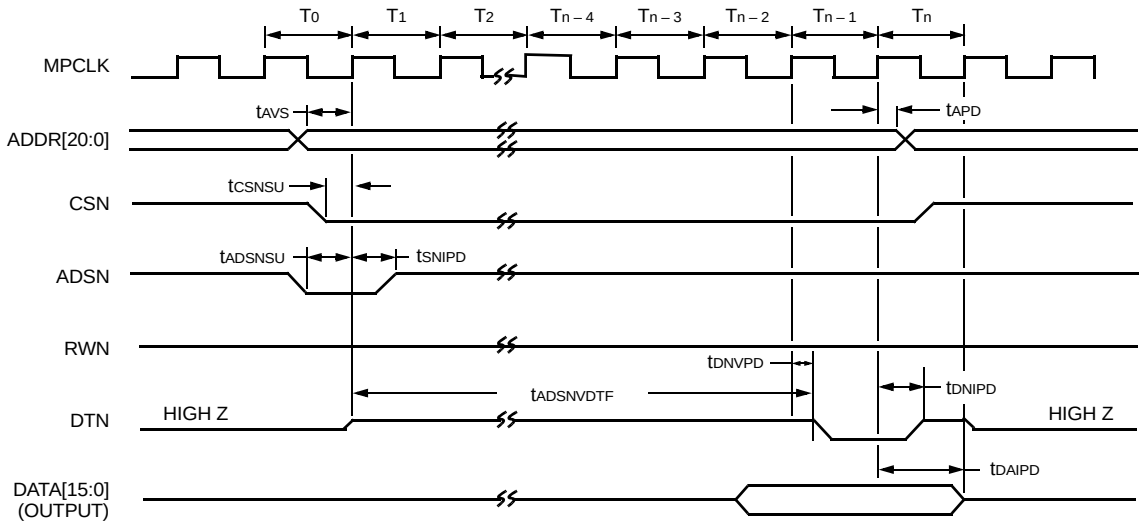
Table 7-1. Microprocessor Interface Synchronous Write Cycle Specifications

Symbol	Parameter	Setup (Min)	Hold (Min)	Delay (Min)	Delay (Max)	Unit
MPCLK	MPCLK 16 MHz Min—66* MHz Max Frequency	—	—	—	—	MHz
tWS	ADSN, RWN, DATA (write) Valid to MPCLK	6.7	—	—	—	ns
tAPD	MPCLK to ADDR, RWN, DATA, CSN (write) Invalid	—	0	—	—	ns
tCSNVS	CSN Valid to MPCLK	6	—	—	—	ns
tADDRVS	ADDR Valid to MPCLK	3.5	—	—	—	ns
tAIPD	MPCLK to ADSN Invalid	—	0	—	—	ns
tDTNVPD	MPCLK to DTN Valid	—	—	2.5	12	ns
tDTNIPD	MPCLK to DTN Invalid	—	—	2.5	12	ns
TADSNVDTF	ADSN Valid to DTN Falling	—	—	—	—†	ns

* If DTN is used, then the maximum frequency for MPCLK is determined by the processor's setup specification for DTN. MPU maximum bus operating frequency = 1/(MPU DTN setup time + tDTNVPD). For example, an 8 ns setup time would limit MPCLK to 50 MHz for reliable DTN detection.

† DTN fall is variable, depending on the block selected for access and in some cases the state of the SONET frame. This interval is typically in the 100 ns to 200 ns range, but can be several hundred ns. It should never exceed 35 MPCLK cycles. Certain registers in the VTMPR block have a very long acknowledge cycle (in the order of 32 MPCLK cycles). The reason for this is that those registers can also be accessed by the VTMPR lower-order path overhead interface as part of SONET overhead termination functions. Therefore the user must insert long enough delay or use the DTN signal to read/write these registers correctly. Additionally, if the high-speed CDR is used, during initialization, enough time must be provided to allow the CDR to stabilize. If the CDR has not stabilized, it may take much longer than 35 MPCLK cycles for accesses to certain VTMPR registers (DTN return times on the order of several μs). It is recommended that the user wait at least 10 ms after the CDR has been reset before attempting to access any VTMPR registers. CDR provisioning is accomplished via the UMPR_CLCR register. In addition to the above, the VT_RDY bit must be set before attempting any VTMPR register accesses.

7.2 Synchronous Read Mode



Notes:

MPCLK Input clock to *Ultramapper* MPU block.

ADDR [20:0] The address will be available throughout the entire cycle, and must be stable before ADSN turns high.

CSN (Input) Chip select is an active-low signal.

ADSN (Input) Address strobe is active-low. ADSN must be one MPCLK clock period wide.

RWN (Input) The read (H) write (L) signal is always high during the read cycle.

DTN (Output) Data transfer acknowledge on the host bus interface is initiated on T6. This signal is active for one clock, and then driven high before entering a high-impedance state. (This is done with an I/O pad using the input as feedback to qualify the 3-state term.) DTN will become 3-stated when CSN is high. Typically, DTN is active four or five MPCLK cycles after ADSN is low.

DATA [15:0] Read data is stable in Tn – 1. The data is guaranteed to be stable no later than the time at which DTN becomes active.

Figure 7-2. Microprocessor Interface Synchronous Read Cycle—MPMODE Pin = 1

Table 7-2. Microprocessor Interface Synchronous Read Cycle Specifications

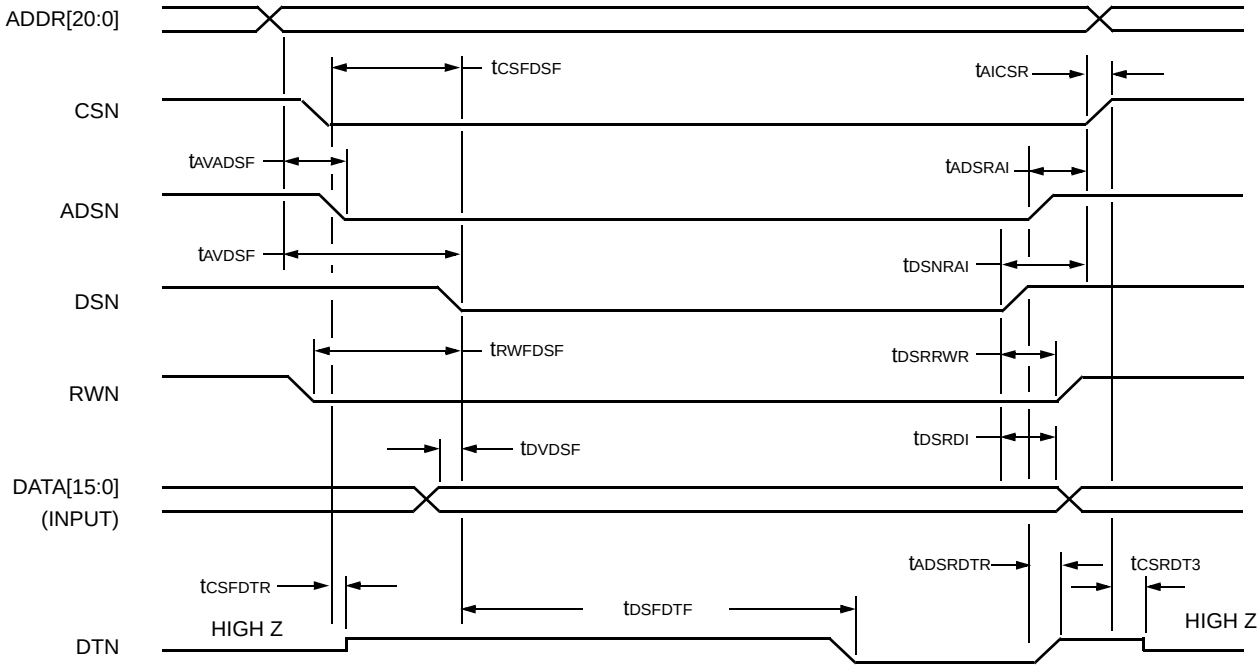
Symbol	Parameter	Setup (Min)	Hold (Min)	Delay (Min)	Delay (Max)	Unit
MPCLK	MPCLK 16 MHz Min—66* MHz Max Frequency	—	—	—	—	MHz
tAVS	ADDR Valid to MPCLK	3.5	—	—	—	ns
tAPD	MPCLK to ADDR Invalid	—	0	—	—	ns
tCSNSU	CSN Active to MPCLK	6	—	—	—	ns
tADSNSU	ADSN Valid to MPCLK	6	—	—	—	ns
tSNIPD	MPCLK to ADSN Inactive	—	0	—	—	ns
tDNVPD	MPCLK to DTN Valid	—	—	2.5	12	ns
tDNIPD	MPCLK to DTN Invalid	—	—	2.5	12	ns
tDAIPD	MPCLK to DATA 3-State	—	—	3.5	15	ns
tADSNVDTF	ADSN Valid to DTN Falling	—	—	—	—†	ns

* If DTN is used, then the maximum frequency for MPCLK is determined by the processor's setup specification for DTN. MPU maximum bus operating frequency = 1/(MPU DTN setup time + tDNVPD). For example, an 8 ns setup time would limit MPCLK to 50 MHz for reliable DTN detection.

† DTN fall is variable, depending on the block selected for access and in some cases the state of the SONET frame. This interval is typically in the 100 ns to 200 ns range, but can be several hundred ns. It should never exceed 35 MPCLK cycles. Certain registers in the VTMPR block have a very long acknowledge cycle (in the order of 32 MPCLK cycles). The reason for this is that those registers can also be accessed by the VTMPR lower-order path overhead interface as part of SONET overhead termination functions. Therefore the user must insert long enough delay or use the DTN signal to read/write these registers correctly. Additionally, if the high-speed CDR is used, during initialization, enough time must be provided to allow the CDR to stabilize. If the CDR has not stabilized, it may take much longer than 35 MPCLK cycles for accesses to certain VTMPR registers (DTN return times on the order of several µs). It is recommended that the user wait at least 10 ms after the CDR has been reset before attempting to access any VTMPR registers. CDR provisioning is accomplished via the UMPR_CLCR register. In addition to the above, the VT_RDY bit must be set before attempting any VTMPR register accesses.

7.3 Asynchronous Write Mode

The asynchronous microprocessor interface mode is selected when MPMODE (pin F6) = 0. Interface timing for the asynchronous mode write cycle is given in Figure 7-3 and in Table 7-3, and for the read cycle in Figure 7-4 and in Table 7-4. Although this is an asynchronous interface, an MPCLK is still required. This clock can be different (asynchronous) from the MPU clock. Internal to the chip, RWN, ADSN, and DSN will be sampled by MPCLK.



Notes:

ADDR [20:0]	Address is asynchronously passed from the host bus to the internal bus. The address will be available throughout the entire cycle. ADDR must be held constant while ADSN and DSN are valid (low).
CSN (Input)	Chip select is an active-low signal. CSN must be held low (active) until ADSN and DSN are deasserted.
ADSN (Input)	Address strobe is active-low. ADSN must be stable for the entire period. ADSN and CSN may be connected and driven from the same source.
DSN (Input)	Data strobe is active-low.
DATA [15:0]	Write data is asynchronously passed from the host bus to the internal bus. Data will be available throughout the entire cycle. DATA must be held constant while DSN is valid (low).
RWN (Input)	The read/write signal should be high for a read cycle and low for a write cycle. It should always be held high, except during a write cycle. RWN must be held low (write) until DSN is deasserted (high).
DTN (Output)	Data transfer acknowledge (active-low). DTN is driven out of 3-state to inactive-high on the assertion of CSN. When the internal transaction is complete, DTN goes active-low. DTN is then driven high again when either ADSN or DSN is deasserted. DTN will become 3-stated when CSN is high. DTN fall is variable, depending on the block selected for access and in some cases the state of the SONET frame. This interval is typically in the 100 ns to 200 ns range, but can be several hundred ns. In lab measurements, it has never exceeded 1000 ns.

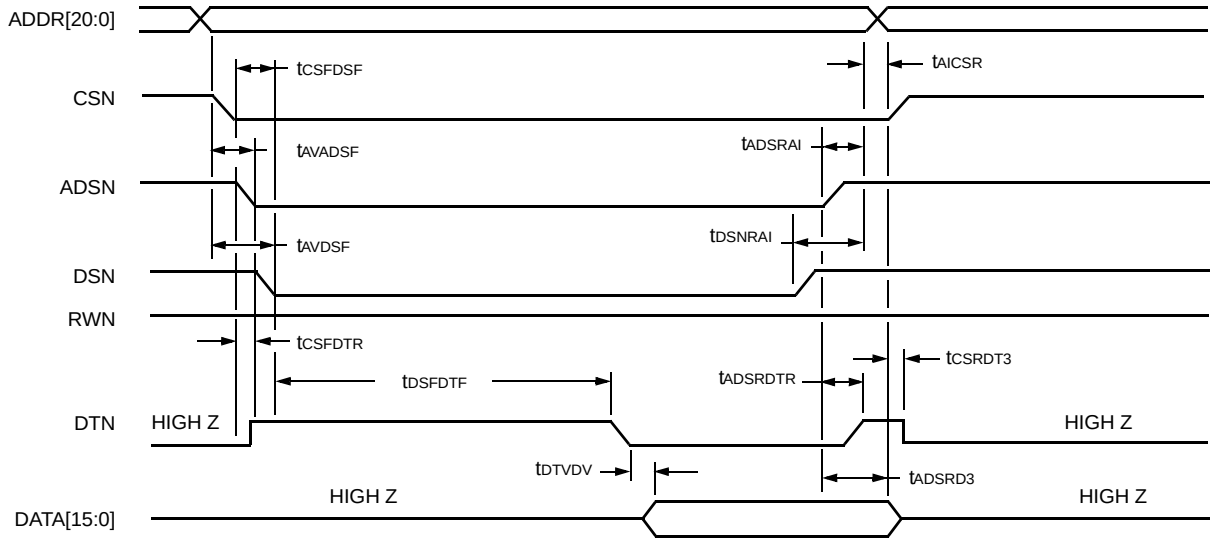
Figure 7-3. Microprocessor Interface Asynchronous Write Cycle—MPMODE Pin = 0

Table 7-3. Microprocessor Interface Asynchronous Write Cycle Specifications

Symbol	Parameter	Setup (Min)	Hold (Min)	Delay (Min)	Delay (Max)	Unit
MPCLK	MPCLK 16 MHz Min—66 MHz Max Frequency	—	—	—	—	MHz
t_{CSFDSF}	CSN Fall Setup and Hold to DSN Fall	0	—	—	—	ns
t_{AICSR}	CSN Rise to ADDR Invalid	—	0	—	—	ns
t_{AVADSF}	ADDR Valid Setup and Hold to ADSN Fall	1.0	—	—	—	ns
t_{ADSRAI}	ADSN Rise to ADDR Invalid	—	1.42	—	—	ns
t_{AVDSF}	ADDR Valid Setup and Hold to DSN Fall	0	—	—	—	ns
t_{DSNRAI}	DSN Rise to ADDR Invalid	—	0	—	—	ns
t_{RWFDSF}	RWN Fall Setup and Hold to DSN Fall	0	—	—	—	ns
t_{DSRRWR}	DSN Rise to RWN Rise	—	0	—	—	ns
t_{DVDSF}	DATA Valid Setup and Hold to DSN Fall	0	—	—	—	ns
t_{DSRDI}	DSN Rise to DATA Invalid	—	0	—	—	ns
t_{CSFDTR}	CSN Fall to DTN Rise	—	—	5.2	16.0	ns
t_{DSFDTF}	DSN Fall to DTN Fall	—	0	—	*	ns
$t_{ADSRDTR}$	ADSN or DSN Rise to DTN Rise	—	—	2.9	13.3	ns
t_{CSRDT3}	CSN Rise to DTN 3-State	—	—	2.9	13	ns

* Certain registers in the VTMPR block have a very long acknowledge cycle (in the order of 32 MPCLK cycles). The reason for this is that those registers can also be accessed by the VTMPR lower order path overhead interface as part of SONET overhead termination functions. Therefore, the user must insert a long enough delay or use the DTN signal to read/write these registers correctly. Additionally, if the high-speed CDR is used, during initialization, enough time must be provided to allow the CDR to stabilize. If the CDR has not stabilized, it may take much longer than 35 MPCLK cycles for accesses to certain VTMPR registers (DTN return times on the order of several µs). It is recommended that the user wait at least 10 ms after the CDR has been reset before attempting to access any VTMPR registers. CDR provisioning is accomplished via the UMPR_CLCR register. In addition to the above, the VT_RDY bit must be set before attempting any VTMPR register accesses.

7.4 Asynchronous Read Mode



Notes:

ADDR [20:0]	Address is asynchronously passed from the host bus to the internal bus. The address will be available throughout the entire cycle.
CSN (Input)	Chip select is an active-low signal.
ADSN (Input)	Address strobe is active-low.
DSN (Input)	Data strobe is active-low.
RWN (Input)	The read (H) write (L) signal is always high during a read cycle.
DTN (Output)	Data transfer acknowledge (active-low). DTN is driven out of 3-state to inactive-high on the assertion of CSN. When the internal transaction is complete, DTN goes active-low. DTN is then driven high again when either ADSN or DSN is deasserted. DTN will become 3-stated when CSN is high.
DATA [15:0]	16-bit data bus.

Figure 7-4. Microprocessor Interface Asynchronous Read Cycle—MPMODE Pin = 0

Table 7-4. Microprocessor Interface Asynchronous Read Cycle Specifications

Symbol	Parameter	Setup (Min)	Hold (Min)	Delay (Min)	Delay (Max)	Unit
MPCLK	MPCLK 16 MHz Min—66 MHz Max Frequency	—	—	—	—	MHz
t_{CSFDSF}	CSN Fall Setup and Hold to DSN Fall	0	—*	—	—	ns
t_{AICSR}	CSN Rise to ADDR Invalid	—	0	—	—	ns
t_{AVADSF}	ADDR Valid Setup and Hold to ADSN Fall	1.0	—†	—	—	ns
t_{ADSRAI}	ADSN Rise to ADDR Invalid	—	1.42	—	—	ns
t_{AVDSF}	ADDR Valid Setup and Hold to DSN Fall	0	—†	—	—	ns
t_{DSNRAI}	DSN Rise to ADDR Invalid	—	0	—	—	ns
t_{CSFDTR}	CSN Fall to DTN Rise	—	—	5.2	16.0	ns
t_{DSFDTF}	DSN Fall to DTN Fall	—	0	—	—‡	ns
$t_{ADSRDTR}$	ADSN or DSN Rise to DTN Rise	—	—	2.9	13.3	ns
t_{CSRDT3}	CSN Rise to DTN 3-State	—	—	2.9	13.0	ns
t_{DTVDV}	DTN Valid to DATA Valid	—	—	—	0	ns
t_{ADSRD3}	ADSN Rise to DATA 3-State	—	—	2.9	14 + MPCLK§	ns

* CSN must be held low (active) until ADSN and DSN are deasserted.

† ADDR must be held constant while ADSN and DSN are valid (low).

‡ DTN fall is variable, depending on the block selected for access and in some cases, the state of the SONET frame. This interval is typically in the 100 ns to 200 ns range, but can be several hundred ns. It should never exceed 35 MPCLK cycles. Certain registers in the VTMPR block have a very long acknowledge cycle (in the order of 32 MPCLK cycles). The reason for this is that those registers can also be accessed by the VTMPR lower-order path overhead interface as part of SONET overhead termination functions. Therefore the user must insert long enough delay or use the DTN signal to read/write these registers correctly. Additionally, if the high-speed CDR is used, during initialization, enough time must be provided to allow the CDR to stabilize. If the CDR has not stabilized, it may take much longer than 35 MPCLK cycles for accesses to certain VTMPR registers (DTN return times on the order of several μs). It is recommended that the user wait at least 10 ms after the CDR has been reset before attempting to access any VTMPR registers. CDR provisioning is accomplished via the UMPR_CLCR register. In addition to the above, the VT_RDY bit must be set before attempting any VTMPR register accesses.

§ DATA[15:0] is enabled by a retimed version of the ADSN.

8 Other Timing

This interface may be used as either synchronous or asynchronous mode.

Table 8-1. General-Purpose Inputs Specifications

Name	Reference	Edge Rising/Falling	Rise Time (ns)	Fall Time (ns)	Setup (ns)	Hold (ns)
RSTN	Async	—	—	—	—	—
PMRST	Async	—	—	—	—	—
TDI and TMS	TCLK	R	5	5	19.5	6.4

Table 8-2. Miscellaneous Output Specifications

Name	Reference	Edge Rising/Falling	Propagation Delay	
			Min (ns)	Max (ns)
RHSFSYNCN	Asynchronous	—	—	—

Table 8-3. General-Purpose Output Specifications

Name	Reference	Edge Rising/Falling	Propagation Delay	
			Min (ns)	Max (ns)
TDO	TCLK	F	12.5	45

9 Hardware Design File References

(IBIS, Spice, BSDL, etc.) Available upon request.

10 700-Pin PBGAM1T Diagrams

* 2 oz option

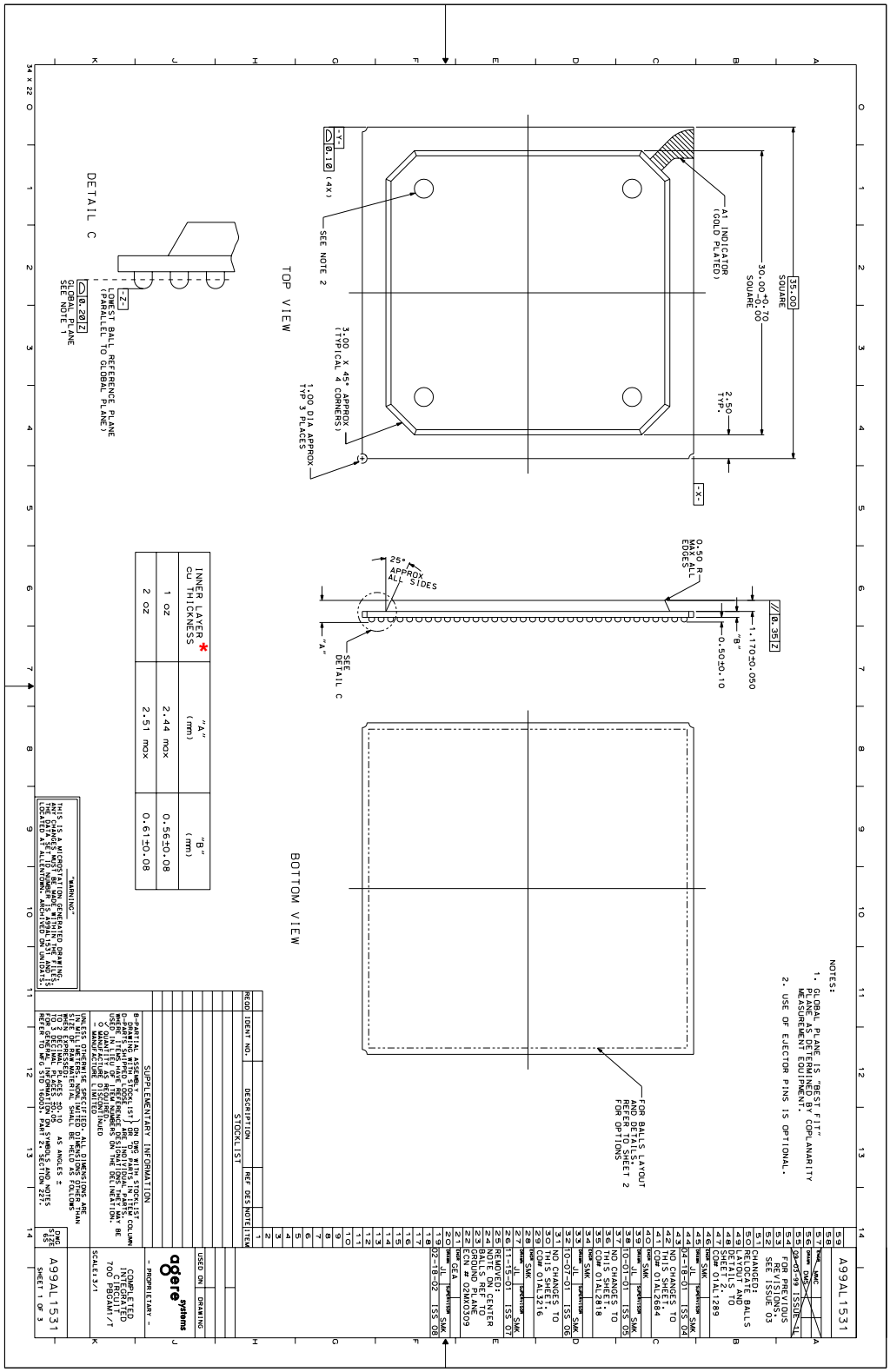


Figure 10-1. 700-Pin PBGAM1T Physical Dimension

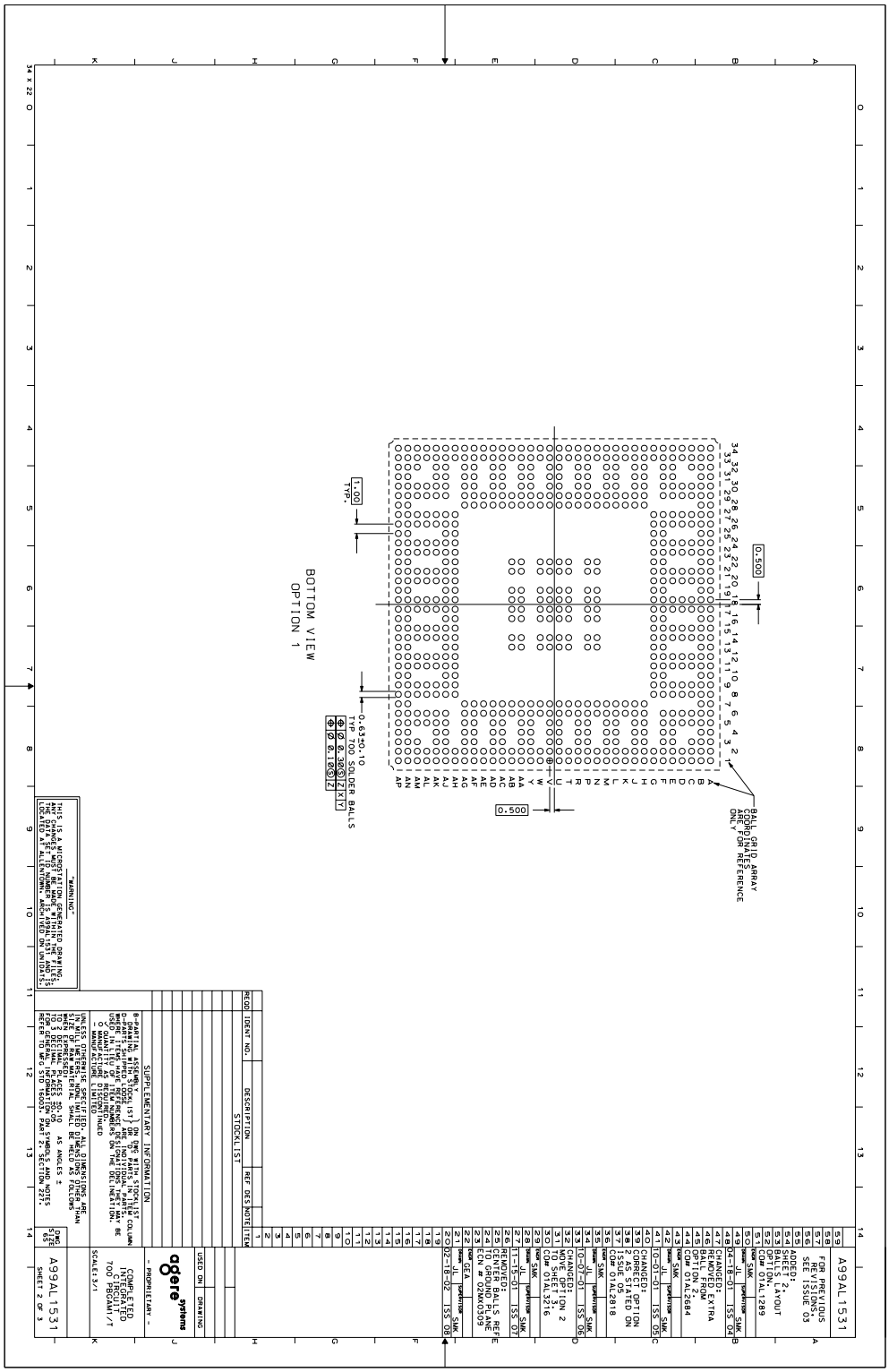


Figure 10-2. Bottom View of 700-Pin PBGAM1T Balls Location

11 Ordering Information

Table 11-1. Ordering Information

Device	Package	Comcode
TMXF846221BL-21	700-pin PBGAM1T	700054129
TMXF846221BL-3	700-pin PBGAM1T	700052305
L-TMXF846221BL-3*	700-pin PBGAM1T	700077978

* Pb-free/RoHS

12 Glossary

AIS	Alarm indication signal
AMI	Alternate mark inversion
APS	Automatic protection switch
ASM	Associated signaling mode
BER	Bit error rate
BLSR	Bidirectional line switched ring
BOM	Bit-oriented message
BPV	Bipolar violation
B8ZS	Bipolar 8 zero substitution
CCI	Common channel signaling
CDR	Clock and data recovery
CHI	Concentrated highway interface
CMI	Coded mark inversion
CRC	Cyclic redundancy check
CRV	Coding rule violation
DACS	Digital access cross connects
DJA	Digital jitter attenuation
ESF	Extended superframe
EXZ	Excessive zeros
FCS	Frame check sequence
FDL	Facility data link
FEAC	Far-end alarm and control
FEBE	Far-end block error
HDB3	High-density bipolar of order three
HDLC	High-level data link control
LIU	Line interface unit
LOC	Loss of clock
LOF	Loss of frame
LOS	Loss of signal
LOPOH	Low-order path overhead
MCDR	Mate clock and data recovery
MRXC	Multirate cross connect
NSMI	Network serial multiplexed interface
OOF	Out of frame
PBGA	Plastic ball grid array
POAC	Path overhead access channel
PRBS	Pseudorandom bit sequence
PRM	Performance report message
QRSS	Quasirandom signal source
RAI	Remote alarm indicator
RDI	Remote defect indication
REI	Remote error indication
SDH	Synchronous digital hierarchy
SEF	Severely errored frame
TCM	Tandem connection monitoring
TOAC	Transport overhead access channels
UDT	Unstructured data transport

13 Change History

13.1 Changes to this Document Since Revision 9

On page 31, deleted STS1LT from the description.

On page 39, added two rows to Table 4-3.

Starting on page 55, updated the duty cycle in all tables in Section 6.

Other changes that were made to this document are listed in Table 13-1.

Table 13-1. Document Changes

Change	Change	Change	Change	Change	Change	Change	Change
page 37	page 43	page 50	page 60	page 62	page 68	page 69	page 70

13.2 Navigating Through an *Adobe Acrobat* ® Document

If the reader displays this document in *Acrobat Reader*, clicking on any blue entry in the text will bring the reader to that reference point.

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