

# LMX9814, LMX9820, and LMX5251: Crystal Tuning Guide

National Semiconductor  
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## 1.0 Scope

The RF local oscillator and internal digital clocks for the National Semiconductor® LMX9814 WPAN module, LMX9820 Serial Port module, and LMX5251 CMOS Radio chip are derived from the reference clock at the CLK+ input. This reference may either come from an external clock or a dedicated crystal oscillator. The crystal oscillator connections require an Xtal and two grounded capacitors. This document describes how to set up the crystal driver circuit.

## 2.0 Xtal Mode

The LMX9814, LMX9820, and LMX5251 each contain a crystal driver circuit. This circuit operates with an external crystal and capacitors to form an oscillator. (See Figure 2-1.)

The crystal appears inductive near its resonant frequency. It forms a resonant circuit with its load capacitors. The resonant frequency may be trimmed with the crystal load capacitance.

### 2.1 LOAD CAPACITANCE

For resonance at the correct frequency, the crystal should be loaded with its specified load capacitance, which is the value of capacitance used in conjunction with the crystal unit. Load capacitance is a parameter specified by the crystal, typically expressed in pF. The crystal circuit shown in Figure 2-2 is composed of:

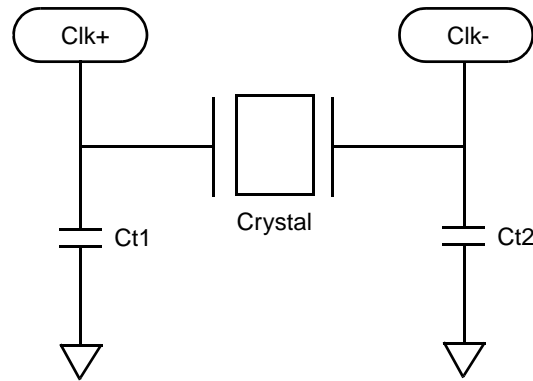
- C1 (motional capacitance)
- R1 (motional resistance)
- L1 (motional inductance)
- C0 (static or shunt capacitance)

The LMX9814, LMX9820, and LMX5251 provide some of the load with internal capacitors  $C_{int}$ . The remainder must come from the external capacitors labeled Ct1 and Ct2 as shown in Figure 2-1. Ct1 and Ct2 should have the same the value for best noise performance. Crystal load capacitance ( $C_L$ ) is calculated as the following:

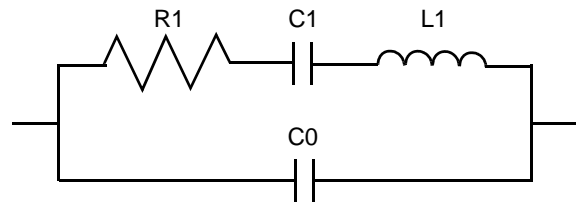
$$C_L = C_{int} + Ct1 // Ct2$$

The  $C_L$  above does not include the crystal internal self-capacitance C0 as shown in Figure 2-2, so the total capacitance is:

$$C_{total} = C_L + C0$$



**Figure 2-1. LMX5251 Crystal Recommended Circuit**



**Figure 2-2. Crystal Equivalent Circuit**

## 3.0 Crystal Pullability

Pullability is another important parameter for a crystal, which is the change in frequency of a crystal with units of ppm/pF, either from the natural resonant frequency to a load resonant frequency, or from one load resonant frequency to another. The frequency can be pulled in a parallel resonant circuit by changing the value of load capacitance. A decrease in load capacitance causes an increase in frequency, and an increase in load capacitance causes a decrease in frequency.

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## 4.0 Frequency Tuning

Frequency Tuning is achieved by adjusting the crystal load capacitance with external capacitors. It is a Bluetooth requirement that the frequency is always within  $\pm 20$  ppm. So a crystal with an aging and temperature drift specification of better than  $\pm 20$  ppm is required. Here is an example:

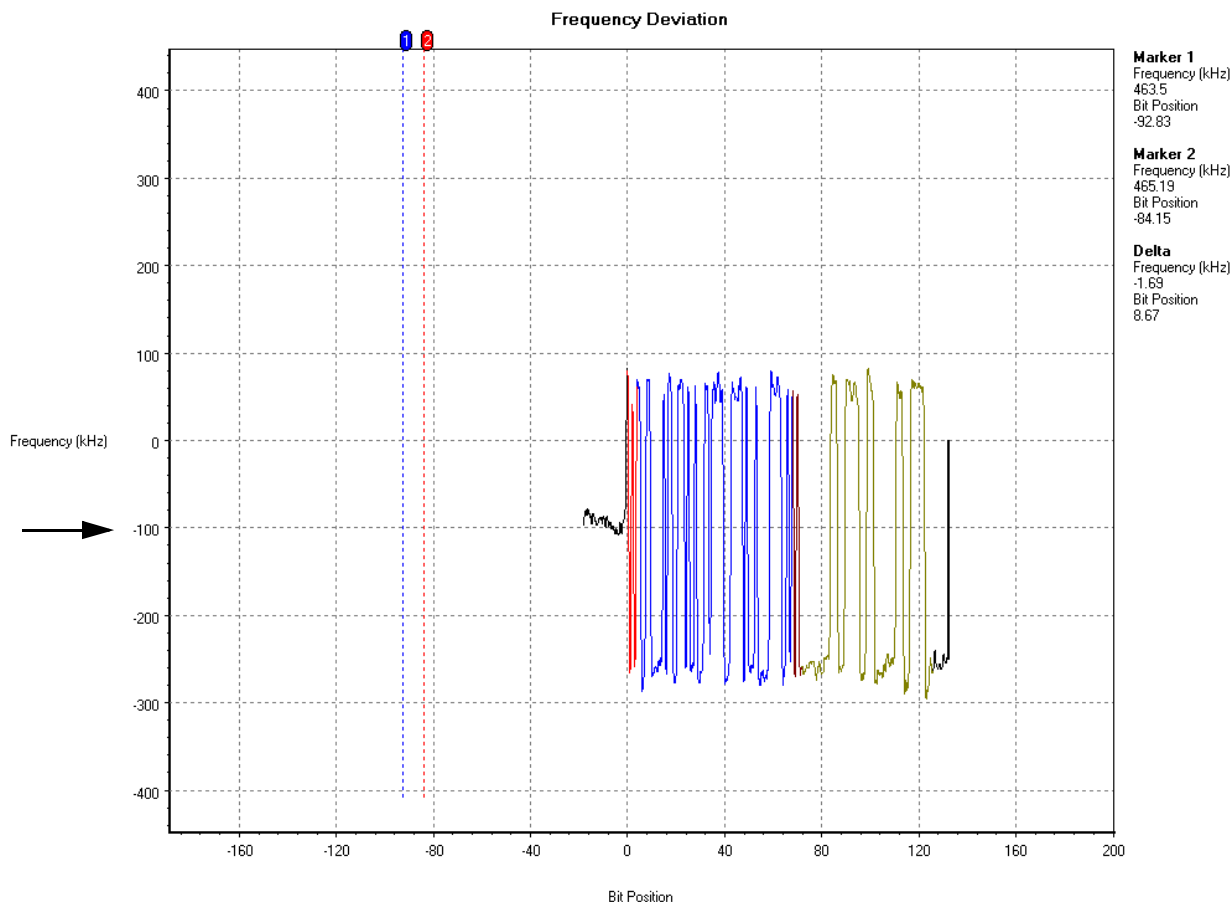
The VXE4-1055 is a 12 MHz SMT crystal from Vite. National is using this crystal with the LMX5251, LMX9814, and LMX9820. Table 4-1 shows the specification of VXE4-1055.

Since the internal capacitance of the crystal circuit is 4-5 pF and the load capacitance is 9 pF, 10 pF is a good starting point for Ct1 and Ct2. The 2480 MHz RF frequency offset is then tested. Figure 4-1 shows the RF frequency offset test results.

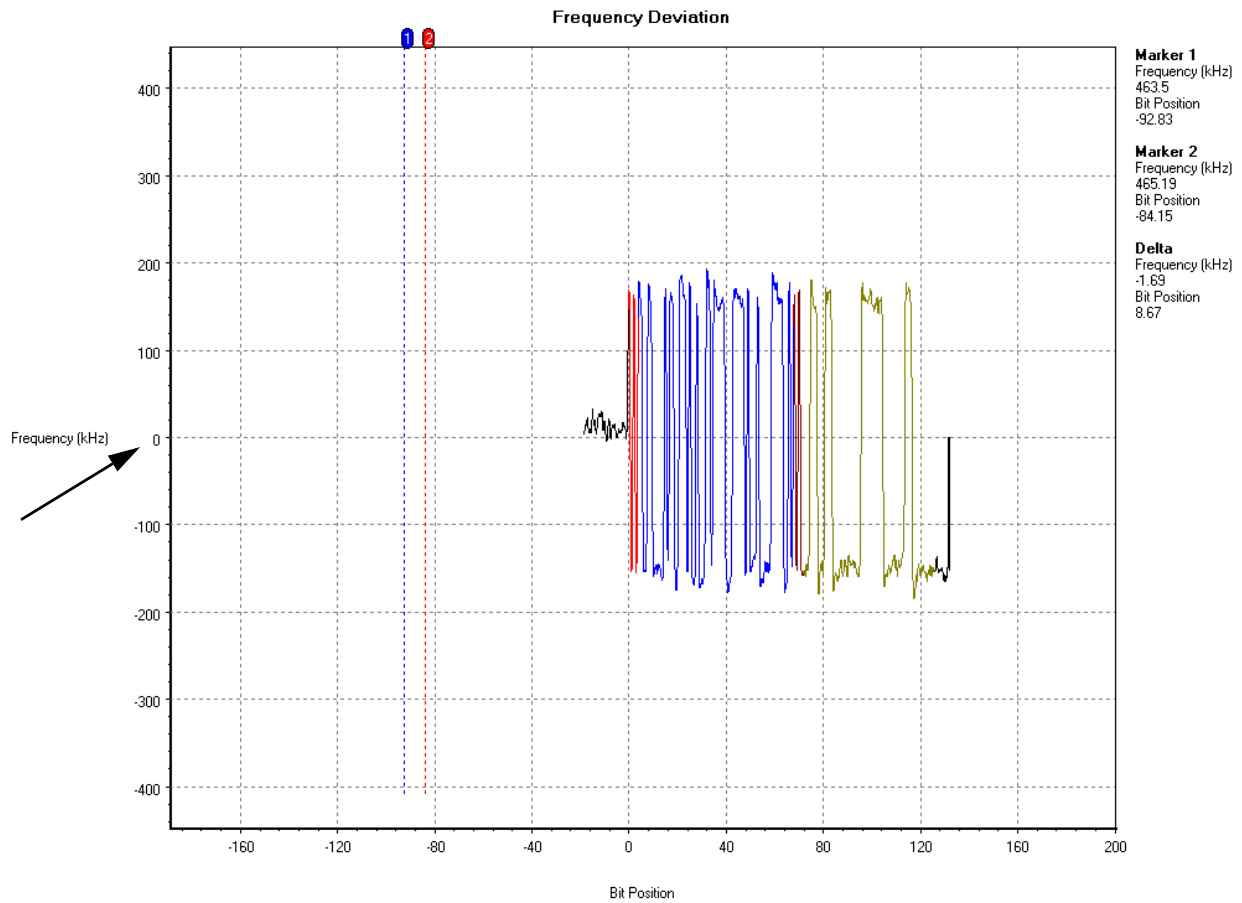
Figure 4-1 shows the results are 100 kHz off the center frequency, which is  $-4$  ppm. The pullability of the crystal is 24 ppm/pF, so the load capacitance must be decreased by about 0.2 pF. By changing Ct1 or Ct2 to 9 pF, the total load capacitance is increased by 0.26 pF. Figure 4-2 shows the frequency offset test results. The frequency offset is now zero with Ct1 = 9 pF, Ct2 = 10 pF.

**Table 4-1. VXE4-1055-12M000**

Specification	Value
Package	6x3.5x1.1 mm tall 4 pads
Frequency	12.000 MHz
Mode	Fundamental
Stability	$\pm 18$ ppm at $-20$ to $+70^\circ\text{C}$ (inclusive of all conditions)
Load Capacitance	9 pF
ESR	40 $\Omega$ max, 20 $\Omega$ typ
Shunt Capacitance	7 pF max
Drive Level	10 to 100 $\mu\text{W}$
Pullability	24 ppm/pF min
Storage Temperature	$-40$ to $+85^\circ\text{C}$



**Figure 4-1. Frequency Offset with 10 pF Capacitors**



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**Figure 4-2. Frequency Offset with 9 pF//10 pF Capacitors**

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