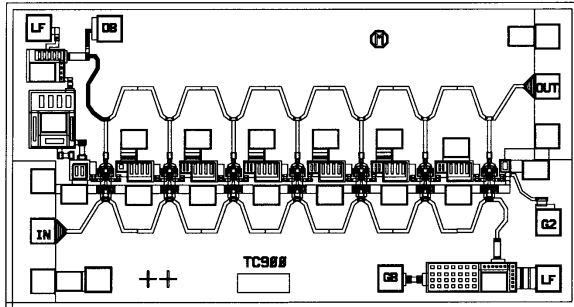


Avago HMMC-5025

2–50 GHz Distributed Amplifier



Data Sheet



Chip Size:	1720 x 920 μm (67.7 x 36.2 mils)
Chip Size Tolerance:	$\pm 10 \mu\text{m}$ (± 0.4 mils)
Chip Thickness:	$127 \pm 15 \mu\text{m}$ (5.0 ± 0.6 mils)
Pad Dimensions:	$80 \times 80 \mu\text{m}$ (3.2×3.2 mils)

Description

The HMMC-5025 was designed as a generic wide band distributed amplifier, covering the frequency span 2–50 GHz. It consists of seven stages. Each stage is made up of two cascoded FETs with gate peripheries of 48 μm per FET. Both input and output ports were designed to provide 50 Ohm terminations. Bonding pads are provided in the layout to allow amplifier operation at frequencies lower than 2 GHz by means of external circuit components.

The amplifier is biased with a single positive drain supply (V_{DD}) and a single negative gate supply (V_{G1}). A second gate connection is provided for external gain control applications.

Features

- **Frequency range:**
2–50 GHz
- **Small signal gain:**
8.5 dB
- **P_{-1dB} @ 40 GHz:**
12 dBm
- **Noise figure:**
5 dB @ 2–35 GHz
7 dB @ 35–50 GHz
- **Return loss:**
In/Out: < -10 dB
- **30 dB gain control**

Absolute Maximum Ratings^[1]

Symbol	Parameters/Conditions	Units	Min.	Max.
V_{DD}	Positive Drain Voltage	V		7.0
I_{DD}	Total Drain Current	mA		170
V_{G1}	First Gate Voltage	V	-3.5	0
V_{G2}	Second Gate Voltage	V	-3.0	+3.0
P_{DC}	DC Power Dissipation	watts		1.2
P_{in}	CW Input Power	dBm		20
T_{ch}	Operating Channel Temp.	$^{\circ}\text{C}$		150
T_{case}	Operating Case Temperature	$^{\circ}\text{C}$	-55	
T_{stg}	Storage Temperature	$^{\circ}\text{C}$	-65	+165
T_{max}	Max. Assembly Temp. (for 60 seconds max.)	$^{\circ}\text{C}$		300

Notes:

1. Operation in excess of any one of these conditions may result in permanent damage to this device. $T_A = 25^{\circ}\text{C}$ except for T_{ch} , T_{stg} , and T_{max} .

HMMC-5025 DC Specifications/Physical Properties^[1]

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
I_{DSS}	Saturated Drain Current ($V_{DD} = 5.0\text{ V}$, $V_{G1} = 0\text{ V}$, $V_{G2} = \text{open circuit}$)	mA	130	150	170
V_p	First Gate Pinch-off Voltage ($V_{DD} = 5.0\text{ V}$, $I_{DD} = 15\text{ mA}$, $V_{G2} = \text{open circuit}$)	V	-1.7		-0.5
V_{G2}	Second Gate Self-Bias Voltage ($V_{DD} = 5.0\text{ V}$, $I_{DD} = 75\text{ mA}$)	V		2	
$I_{DSOFF}(V_{G1})$	First Gate Pinch-off Current ($V_{DD} = 5.0\text{ V}$, $V_{G1} = -3.5\text{ V}$, $V_{G2} = \text{open circuit}$)	mA		6	10
$I_{DSOFF}(V_{G2})$	Second Gate Pinch-off Current ($V_{DD} = 5.0\text{ V}$, $I_{DD} = 75\text{ mA}$, $V_{G2} = -2.5\text{ V}$)	mA		10	
θ_{ch-bs}	Thermal Resistance ($T_{backside} = 25^\circ\text{C}$)	$^\circ\text{C}/\text{W}$		63	

Note:

1. Measured in wafer form with $T_{chuck} = 25^\circ\text{C}$. (Except θ_{ch-bs} .)

Electrical Specifications^[1], $V_{DD} = 5.0\text{ V}$, $I_{DD}(Q) = 75\text{ mA}$, $Z_{in} = Z_o = 50\Omega$

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
BW	Guaranteed Bandwidth ^[2]	GHz	2		50
S_{21}	Small Signal Gain	dB	7.0	8.5	
ΔS_{21}	Small Signal Gain Flatness	dB		± 0.75	± 1.5
RL_{in}	Input Return Loss	dB	10	15	
RL_{out}	Output Return Loss	dB	10	15	
S_{12}	Reverse Isolation	dB	20	30	
P_{-1dB}	Output Power @ 1dB Gain Compression @ 40 GHz	dBm		12	
P_{sat}	Saturated Output Power @ 40 GHz	dBm		16	
H_2	Second Harmonic Power Level ($2 < f_o < 26$) $P_o(f_o) = 10\text{ dBm}$	dBc		-35	
H_3	Third Harmonic Power Level ($2 < f_o < 20$) $P_o(f_o) = 10\text{ dBm}$	dBc		-25	
NF	Noise Figure (2 – 35 GHz) Noise Figure (35 – 50 GHz)	dB		5.0 7.0	

Notes:

1. Small-signal data measured in wafer form with $T_{chuck} = 25^\circ\text{C}$. Harmonic data measured on individual devices mounted in a microcircuit package at $T_A = 25^\circ\text{C}$.
2. Performance may be extended to lower frequencies through the use of appropriate off-chip circuitry.

Application

The HMMC-5025 traveling wave amplifier is designed for use as a general purpose wideband power stage in communication systems, and microwave instrumentation, and optical systems. It is ideally suited for broadband applications requiring a flat gain response and excellent port matches over a 2 to 50 GHz frequency range. Dynamic gain control and low-frequency extension capabilities are designed into these devices.

Biasing and Operation

The recommended bias conditions for best performance for the HMMC-5025 are $V_{DD} = 5.0V$, $I_{DD} = 75\text{ mA}$. To achieve these drain current levels, V_{G1} is typically biased between $-0.2V$ and $-0.6V$. No other bias supplies or connections to the device are required for 2 to 50 GHz operation. The gate voltage (V_{G1})

should be applied prior to the drain voltage (V_{DD}) during power up and removed after the drain voltage during power down.

The HMMC-5025 is a DC coupled amplifier. External coupling capacitors are needed on RF_{IN} and RF_{OUT} ports. The drain bias pad is connected to RF and must be decoupled to the lowest operating frequency.

The auxiliary gate and drain contacts are provided when performance below 1 GHz is required. Connect external capacitors to ground to maintain input and output VSWR at low frequencies (see Additional References). Do not apply bias to these pads.

The second gate (V_{G2}) can be used to obtain 30 dB (typical) dynamic gain control. For normal operation, no external bias is required on this contact.

Assembly Techniques

GaAs MMICs are ESD sensitive. ESD preventive measures must be employed in all aspects of storage, handling, and assembly. MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability.

Avago application note #54, "GaAs MMIC ESD, Die Attach and Bonding Guidelines" provides basic information on these subjects.

Additional References:

AN #1053, "Designing with HMMC-5021, -5022, -5026, and -5027 GaAs MMIC Amplifiers."

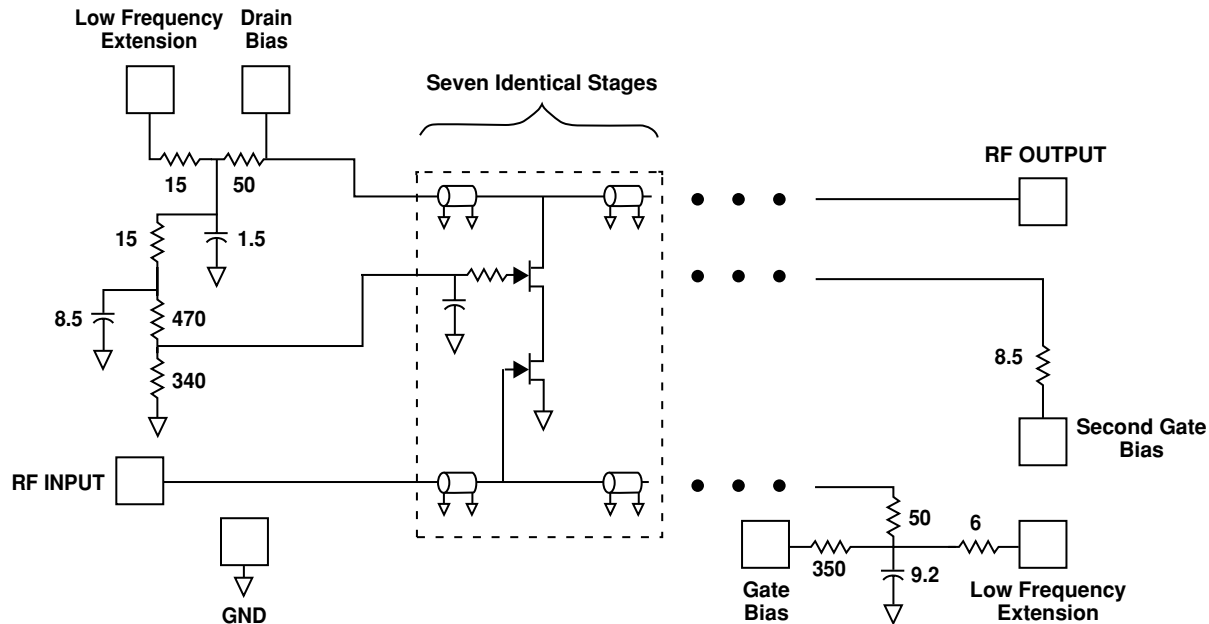


Figure 1. HMMC-5025 Schematic.

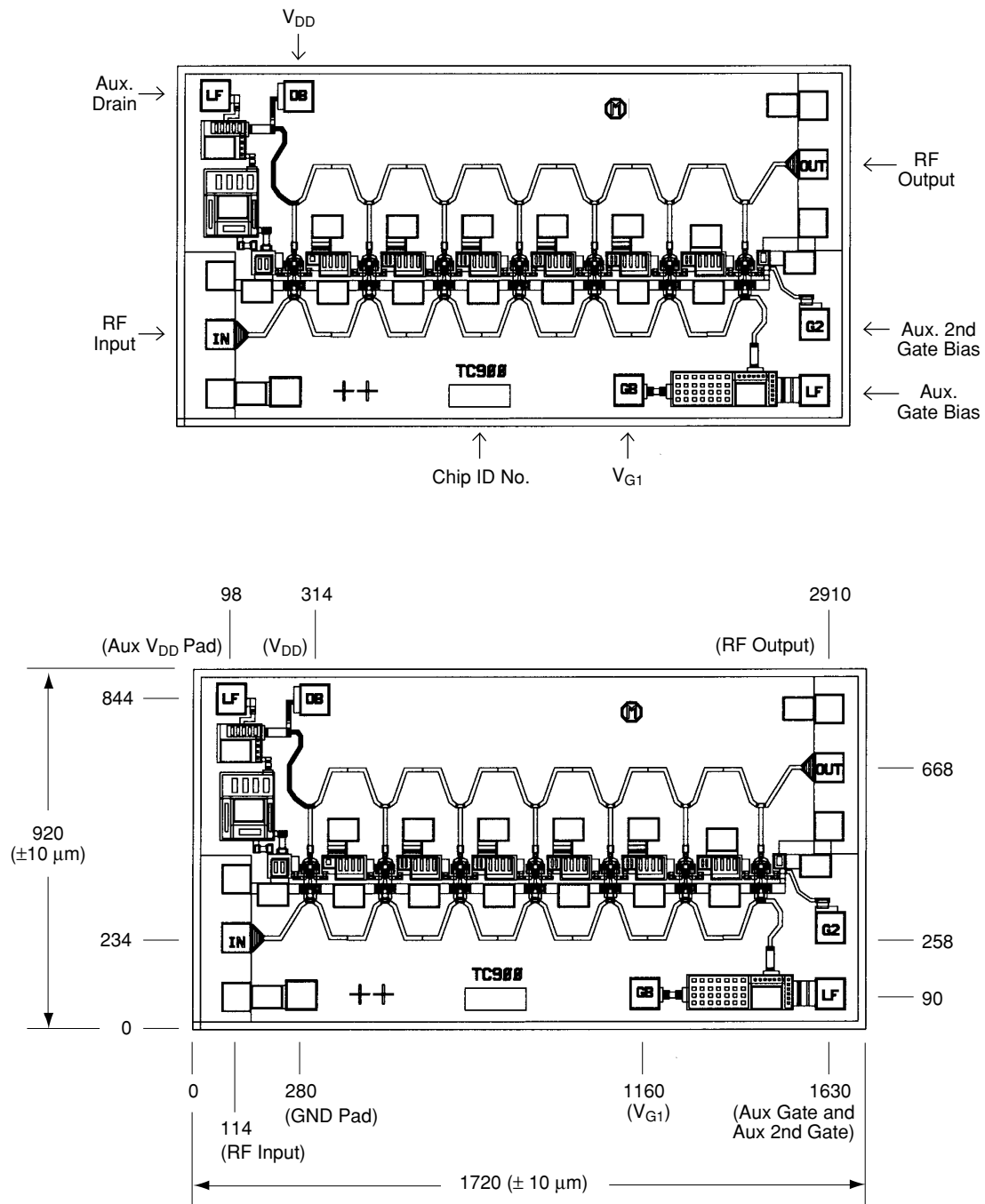


Figure 2. HMMC-5025 Bond Pad Locations.

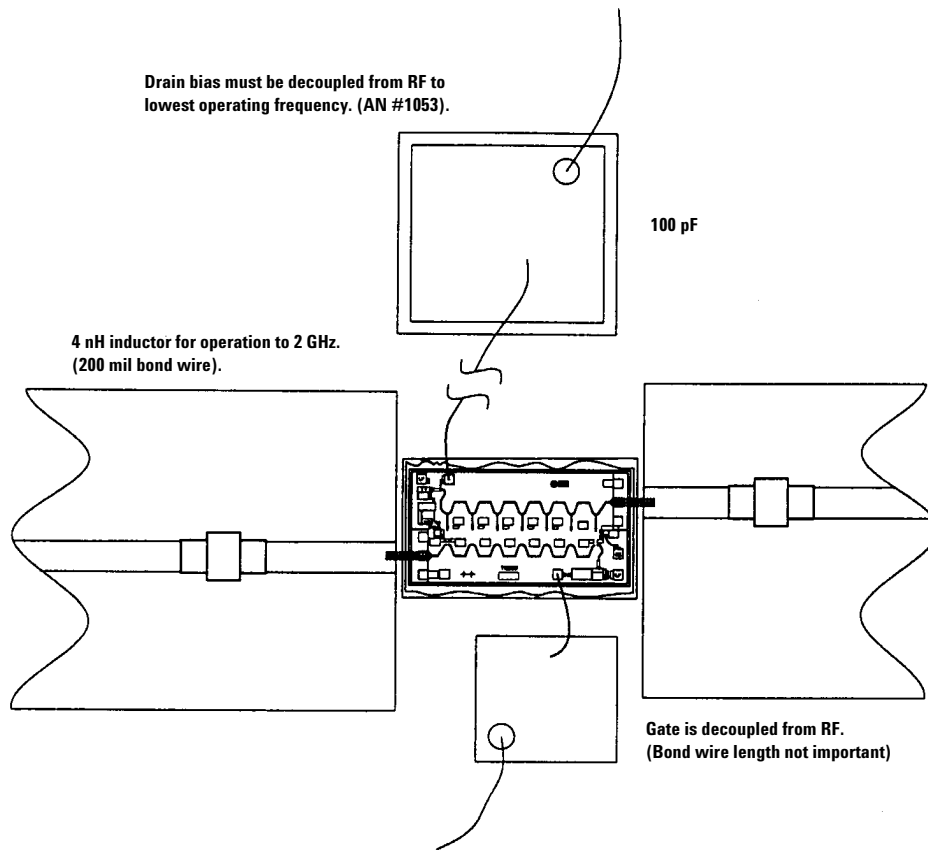


Figure 3. HMMC-5025 Assembly Diagram.

HMMC-5025 Typical Performance

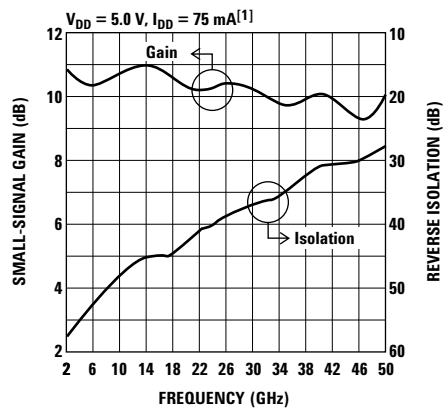


Figure 4. Typical Gain and Reverse Isolation vs. Frequency.

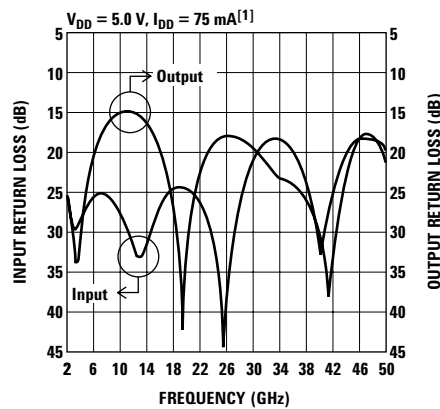


Figure 5. Typical Input and Output Return Loss vs. Frequency.

Note:

1. Data obtained from on-wafer measurements. $T_{\text{chuck}} = 25^\circ\text{C}$.

HMMC-5025 Typical Scattering Parameters⁽¹⁾,
 (T_{chuck} = 25°C, V_{DD} = 5.0 V, I_{DD} = 75 mA, Z_{in} = Z_o = 50 Ω)

Freq. GHz	S ₁₁			S ₁₂			S ₂₁			S ₂₂		
	dB	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang
2	-24.6	0.059	-150.2	-52.0	0.0025	-110.2	8.5	2.660	147.8	-26.1	0.049	-64.0
3	-29.7	0.033	147.5	-49.1	0.0035	-130.2	8.4	2.630	139.6	-33.8	0.020	-23.6
4	-28.9	0.036	89.0	-47.1	0.0044	-146.4	8.4	2.630	129.8	-30.1	0.031	43.9
5	-27.0	0.045	56.2	-45.5	0.0053	-161.6	8.4	2.629	119.5	-24.6	0.059	55.9
6	-25.8	0.052	32.6	-44.2	0.0061	-176.8	8.4	2.643	108.9	-20.8	0.091	52.1
7	-25.2	0.055	12.7	-43.3	0.0068	169.3	8.5	2.668	98.1	-18.4	0.121	43.8
8	-25.4	0.054	-6.3	-42.6	0.0074	155.6	8.6	2.705	86.9	-16.7	0.147	33.4
9	-26.0	0.050	-25.3	-42.1	0.0078	143.8	8.8	2.743	75.5	-15.6	0.166	22.3
10	-27.4	0.043	-46.3	-41.7	0.0083	132.1	8.9	2.787	63.7	-15.0	0.178	10.7
11	-29.4	0.034	-70.4	-41.4	0.0085	121.9	9.0	2.823	51.6	-14.8	0.182	-0.9
12	-31.7	0.026	-102.9	-40.9	0.0090	112.3	9.1	2.853	39.3	-14.9	0.179	-12.6
13	-33.0	0.022	-145.8	-40.7	0.0093	104.5	9.2	2.874	26.9	-15.4	0.169	-24.2
14	-31.4	0.027	168.6	-40.3	0.0097	95.4	9.2	2.891	14.3	-16.3	0.153	-35.7
15	-29.1	0.035	136.8	-39.7	0.0104	88.5	9.2	2.891	1.8	-17.6	0.131	-47.3
16	-27.0	0.045	113.4	-39.0	0.0112	80.5	9.2	2.884	-10.8	-19.5	0.106	-59.3
17	-25.4	0.053	95.4	-38.4	0.0120	71.9	9.2	2.870	-23.3	-22.2	0.077	-72.0
18	-24.5	0.060	77.9	-37.7	0.0131	62.9	9.1	2.853	-35.7	-26.7	0.046	-86.1
19	-24.1	0.062	62.1	-37.1	0.0140	53.8	9.1	2.836	-48.1	-35.6	0.017	-114.9
20	-24.4	0.061	48.2	-36.3	0.0153	44.3	9.0	2.819	-60.3	-35.3	0.017	107.2
21	-25.0	0.056	37.0	-35.3	0.0172	32.7	9.0	2.806	-72.6	-27.0	0.045	80.0
22	-25.6	0.052	22.6	-35.1	0.0176	19.5	8.9	2.798	-84.7	-23.2	0.069	66.2
23	-27.7	0.041	7.2	-34.7	0.0184	8.9	8.9	2.796	-97.1	-21.0	0.089	54.9
24	-30.9	0.028	-8.2	-34.4	0.0191	-2.8	8.9	2.789	-109.5	-19.4	0.107	44.2
25	-38.4	0.012	-39.5	-34.3	0.0194	-14.7	8.9	2.789	-121.9	-18.6	0.118	33.6
26	-40.1	0.010	-169.3	-33.9	0.0202	-25.3	8.9	2.789	-134.5	-18.2	0.124	24.2
27	-30.9	0.029	156.0	-33.7	0.0206	-37.0	8.9	2.794	-147.2	-18.2	0.124	15.5
28	-26.0	0.050	138.6	-33.7	0.0206	-48.5	8.9	2.795	-160.1	-18.4	0.120	7.7
29	-23.1	0.070	122.8	-33.4	0.0213	-58.3	8.9	2.787	-173.1	-18.8	0.115	2.1
30	-21.0	0.089	110.2	-33.3	0.0216	-71.3	8.9	2.780	174.0	-19.6	0.105	-3.4
31	-19.8	0.102	95.3	-32.9	0.0228	-81.1	8.9	2.772	160.9	-20.5	0.095	-7.5
32	-18.9	0.114	82.3	-32.5	0.0236	-93.6	8.8	2.768	147.8	-21.3	0.086	-9.1
33	-18.6	0.117	70.4	-32.3	0.0244	-105.4	8.8	2.762	134.5	-22.4	0.076	-6.4
34	-18.5	0.118	58.6	-32.3	0.0244	-120.3	8.8	2.752	121.2	-23.0	0.071	-4.7
35	-19.0	0.112	46.2	-31.9	0.0254	-132.8	8.8	2.747	107.8	-23.5	0.067	-3.5
36	-20.0	0.100	35.6	-31.6	0.0264	-146.2	8.8	2.741	94.4	-23.7	0.066	-2.5
37	-21.5	0.084	26.4	-31.5	0.0266	-161.5	8.7	2.735	80.7	-24.4	0.060	-4.3
38	-24.0	0.063	18.8	-31.5	0.0267	-175.1	8.7	2.728	67.0	-25.4	0.054	-8.9
39	-27.6	0.042	18.9	-31.5	0.0266	171.1	8.7	2.723	53.0	-27.1	0.044	-11.8
40	-32.9	0.023	46.7	-31.4	0.0270	157.6	8.7	2.711	39.0	-30.4	0.030	-9.1
41	-30.3	0.031	99.2	-31.2	0.0276	140.9	8.6	2.703	24.8	-38.1	0.012	18.9
42	-25.5	0.053	107.1	-31.0	0.0282	125.0	8.6	2.695	10.5	-32.6	0.023	93.1
43	-22.2	0.078	102.7	-31.4	0.0270	115.6	8.6	2.689	-4.0	-26.2	0.049	94.9
44	-20.1	0.099	94.4	-31.1	0.0280	101.4	8.6	2.679	-18.1	-22.4	0.076	86.4
45	-19.0	0.112	85.3	-31.3	0.0272	87.2	8.5	2.672	-33.4	-20.2	0.098	75.3
46	-18.6	0.117	76.5	-30.5	0.0297	72.1	8.5	2.676	-48.5	-18.8	0.115	61.6
47	-18.3	0.121	69.8	-30.6	0.0297	49.9	8.6	2.686	-64.0	-18.0	0.126	48.2
48	-18.8	0.115	62.5	-30.7	0.0293	37.8	8.6	2.689	-79.8	-18.3	0.122	28.8
49	-19.3	0.108	59.9	-30.5	0.0300	20.0	8.6	2.691	-96.1	-19.5	0.106	6.1
50	-20.3	0.096	58.9	-30.3	0.0307	2.7	8.6	2.677	-293.0	-21.7	0.082	-22.7

Note:

1. Data obtained from on-wafer measurements.

HMMC-5025 Typical Performance

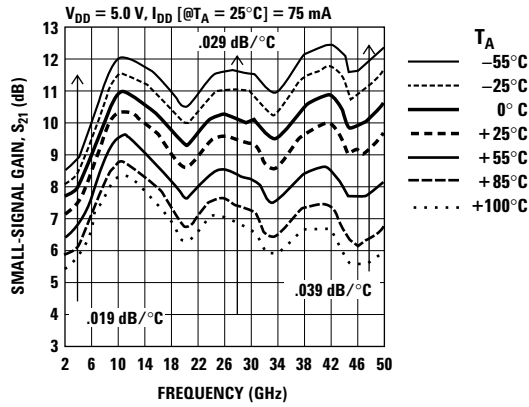


Figure 6. Typical Small-Signal Gain vs. Temperature.

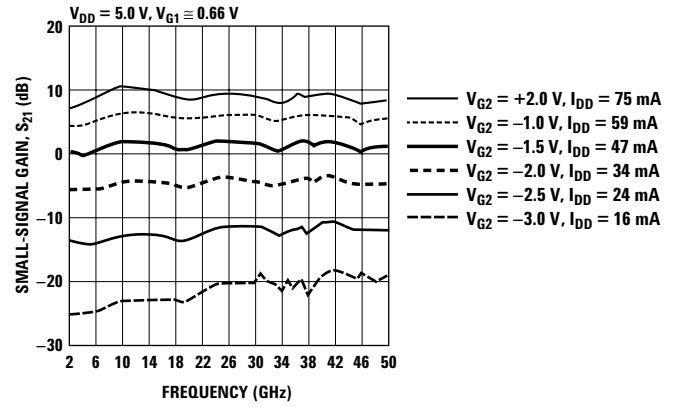


Figure 7. Typical Gain vs. Second Gate Control Voltage.

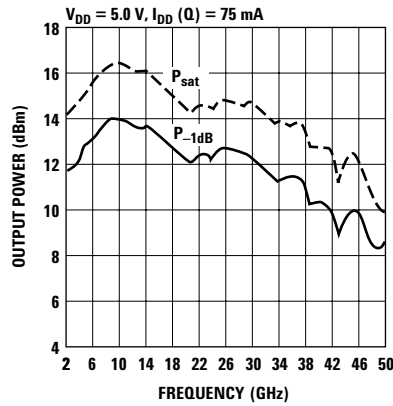


Figure 8. Typical 1 dB Gain Compression and Saturated Output Power vs. Frequency.

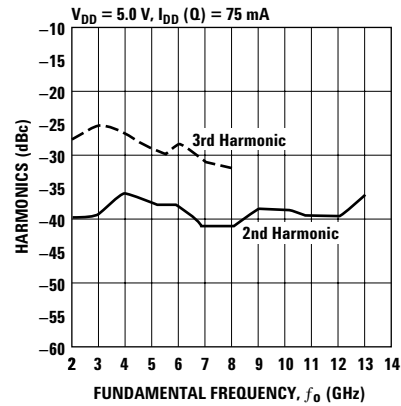


Figure 9. Typical Second and Third Harmonics vs. Fundamental Frequency at $P_{OUT} = 10$ dBm.

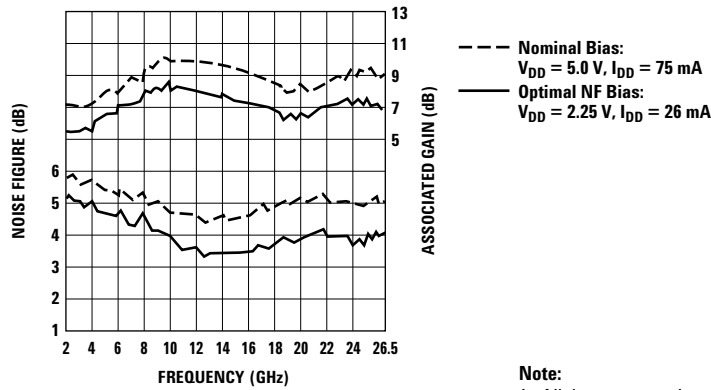


Figure 10. Typical Noise Figure Performance.

Note:

1. All data measured on individual devices mounted in an HP83040 Series Modular Microcircuit Package @ $T_A = 25^\circ\text{C}$ (except where noted).

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications. In this data sheet the term *typical* refers to the 50th percentile performance. For additional information contact your local Avago Technologies' sales representative.

For product information and a complete list of distributors, please go to our web site:

www.avagotech.com

Avago, Avago Technologies, and the A logo are trademarks of Avago Technologies, Limited in the United States and other countries.

Data subject to change. Copyright © 2006 Avago Technologies, Limited. All rights reserved.

Obsoletes 5965-5446E

5988-2546EN March 12, 2007

