PRODUCT BRIEF

GANGES

STS-192 SONET/SDH FRAMER AND POS/ATM MAPPER

Features

- Supports full duplex mapping of ATM cells or packets for a single STS-192c/AU-4-64c, four STS-48c/AU-4-16c or sixteen STS-12c/AU-4-4c SONET/SDH payloads.
- Supports a single STS-192/STM-64 or quad STS-48/STM-16 line interfaces on the line side and on the protection port. Each STS-48/STM-16 can support a concatenated payload or can be channelized down to STS-12c/AU-4-4c.
- Terminates and generates SONET/SDH section, line, & path layers on the line side and APS port, with transport/section E1, E2, F1 and DCC overhead interfaces in both transmit and receive directions.
- Supports independent loop timing when in quad STS-48/STM-16 mode.
- Supports protection switching (APS) between two Ganges devices or between two fiber optics modules
- Provides an Optical Internetworking Forum (OIF) SFI-4 compliant 622.08 MHz, 16-bit bus LVDS interface on the line side in both the TX and RX directions.
- Provides a 64-bit, 200 MHz FlexBus 4 system interface that supports the transfer of either packets or ATM cells.
- Support mixed ATM and POS data termination, configurable on a per-tributary basis
- 16-bit synchronous microprocessor interface for configuration, control, and status monitoring.
- Packaged in a 624-pin CBGA.
- Implemented in .18 micron, 1.8V and 2.5V technology.

General Description

The Ganges IC is a highly integrated VLSI device that provides full duplex mapping of Packets or ATM cells into SONET/SDH payloads at rates up to 9.95Gb/s.

Ganges provides full section and line overhead processing for either a single STS-192/STM-64, or four STS-48/STM-16. It supports framing, scrambling and descrambling, alarm signal insertion and detection, and bit interleaved parity (B1/B2) processing. It also provides path overhead processing for STS-192c/AU-4-64c, STS-48c/AU-4-16c or STS-12c/AU-4-4c SONET/SDH payloads and includes bit interleaved parity (B3) processing.

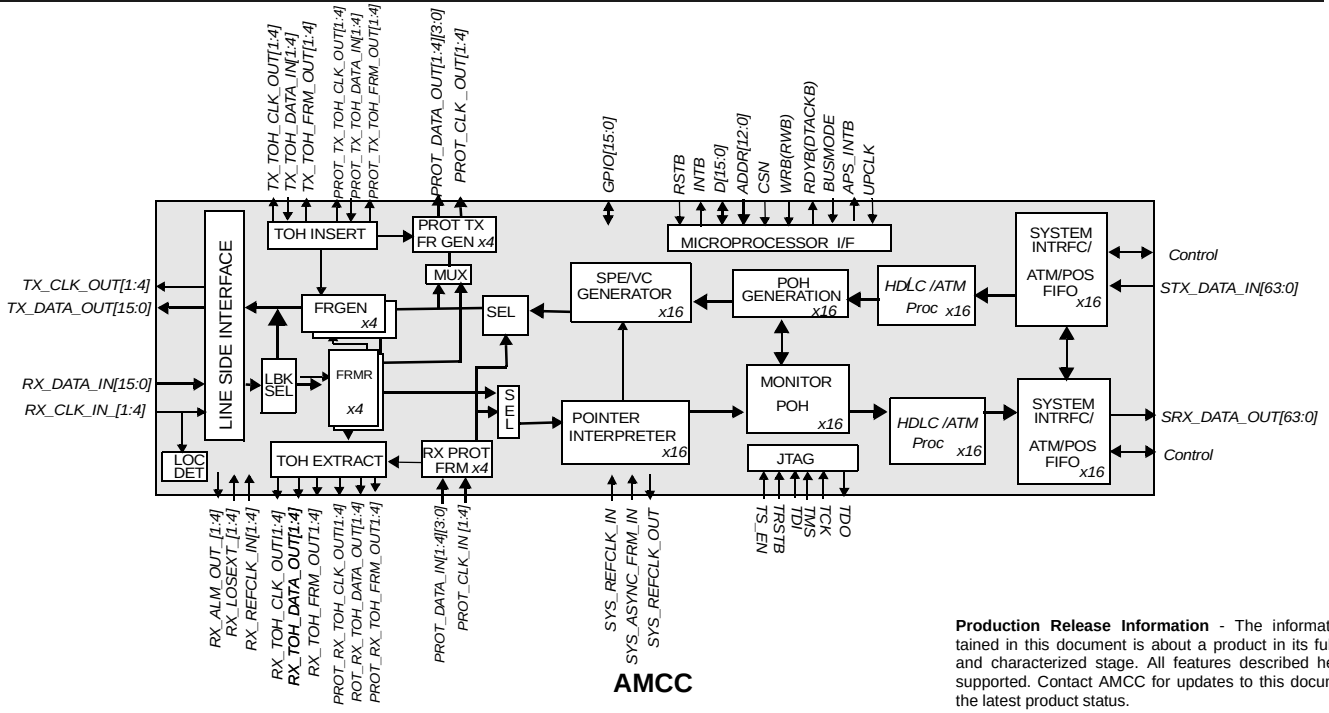
The automatic protection switching (APS) port of the Ganges supports generation and termination of SONET/SDH section and line, as well as TOH insertion and extraction. This allows inter-device protection switching between two Ganges devices or intra-device protection between two fiber optics modules.

The Ganges is SONET/SDH standards compliant with Bellcore GR-253, ITU G.707, and ANSI T1.105 -1995.

Applications

- Core ATM switches and IP Routers (POS)
- ATM, POS and Frame Relay line cards in Edge and Metro Switches
- Direct Mapping of any traffic type in SONET/SDH STS-192/STM-64 and STS-48/STM-16 payloads

S19202 Block Diagram



AMCC

Production Release Information - The information contained in this document is about a product in its fully tested and characterized stage. All features described herein are supported. Contact AMCC for updates to this document and the latest product status.

STS-192 POS/ATM SONET/SDH MAPPER ***PRODUCT BRIEF***

Overview and Applications

SONET Processing

The S19202CBI30 supports either a single STS-192/STM-64, or four STS-48/STM-16 SONET/SDH on its primary line interface as well as on its APS port. It provides full duplex mapping of ATM cells or packets for STS-192c/AU-4-64c, STS-48c/AU-4-16c, and/or STS-12c/AU-4-4c SONET/SDH payloads.

A TOH/SOH interface provides direct add/drop capability for E1, E2, F1, and both Section and Line DCC channels.

On the transmit side the S19202CBI30 generates section, line, and path overhead. It performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and generates section, line and path Bit Interleaved Parity (B1/B2/B3) for far-end performance monitoring.

On the receive side the S19202CBI30 processes section, line, and path overhead. It performs framing (A1, A2), descrambling, alarm detection, pointer interpretation, bit interleaved parity monitoring (B1/B2/B3), and error count accumulation for performance monitoring.

The APS interface is a mirror image of the primary line interface that also operates either as a single STS-192/ or as four STS-48/STM-16 SONET/SDH Line. This includes TOH add/drop as well section and line monitoring. This APS port can directly interface to a fiber optics module or to the APS port of a mate S19202CBI30.

ATM Processing

When configured for ATM cell processing, the S19202CBI30's ATM processor(s) will perform all necessary cell processing as defined by ATM UNI3.1 and ITU-T I.432.1 and I.432.2.

HDLC Processing

When configured for POS mode, the S19202CBI30's HDLC processor(s) provide the insertion of HDLC framed packets into the STS SPE(s)/STM VC(s). The S19202CBI30 performs HDLC processing as defined by IETF RFCs 1661, 1662 and 2615. This includes optional Address/Control field insertion and removal, Frame Check Sequence (FCS) generation and check, transparency processing, HDLC frame delineation and optional X43+1 scrambling and de-scrambling.

The HDLC processor(s) are also compatible with Frame Relay Forum's FRF.14 specification.

Line-side Interface

On the main line-side and the APS port, the S19202CBI30 supports a 16-bit parallel LVDS interface, operating at 622MHz that is compliant with the OIF SFI-4 recommendation and designed to interface to AMCC's S3091/92 and S3097/98 OC-192 physical layer devices.

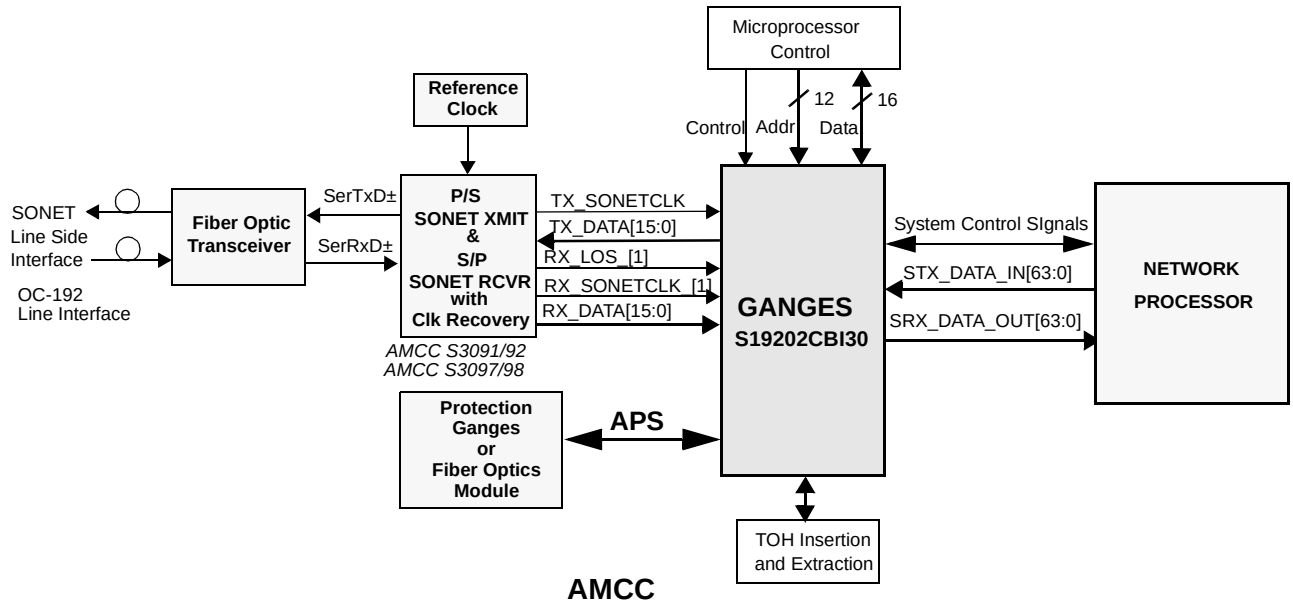
For quad STS-48/STM-16 operation, the S19202CBI30 supports four 4-bit, 622 MHz, line interfaces and is designed to interface to AMCC's S3455 OC-48 physical layer device.

System Interface

The S19202CBI30 IC provides a 64-bit, 200MHz, FlexBus 4™ system interface for the transport of either packets or ATM cells. The S19202CBI30 also includes a clear channel mode that enables the direct mapping of system payload from the system interface into Synchronous Payload Envelope.

The FlexBus 4 interface complies with the OIF SPI-4 specification.

TYPICAL APPLICATION: Ganges in a STS-192/AU-4-64 application with APS



AMCC

200 Minuteman Road, Andover, MA 01810 Ph: (978) 247-8000 Fax: (978) 623-0024