



FAST CMOS OCTAL REGISTERED TRANSCEIVER

IDT29FCT2052AT/CT

FEATURES:

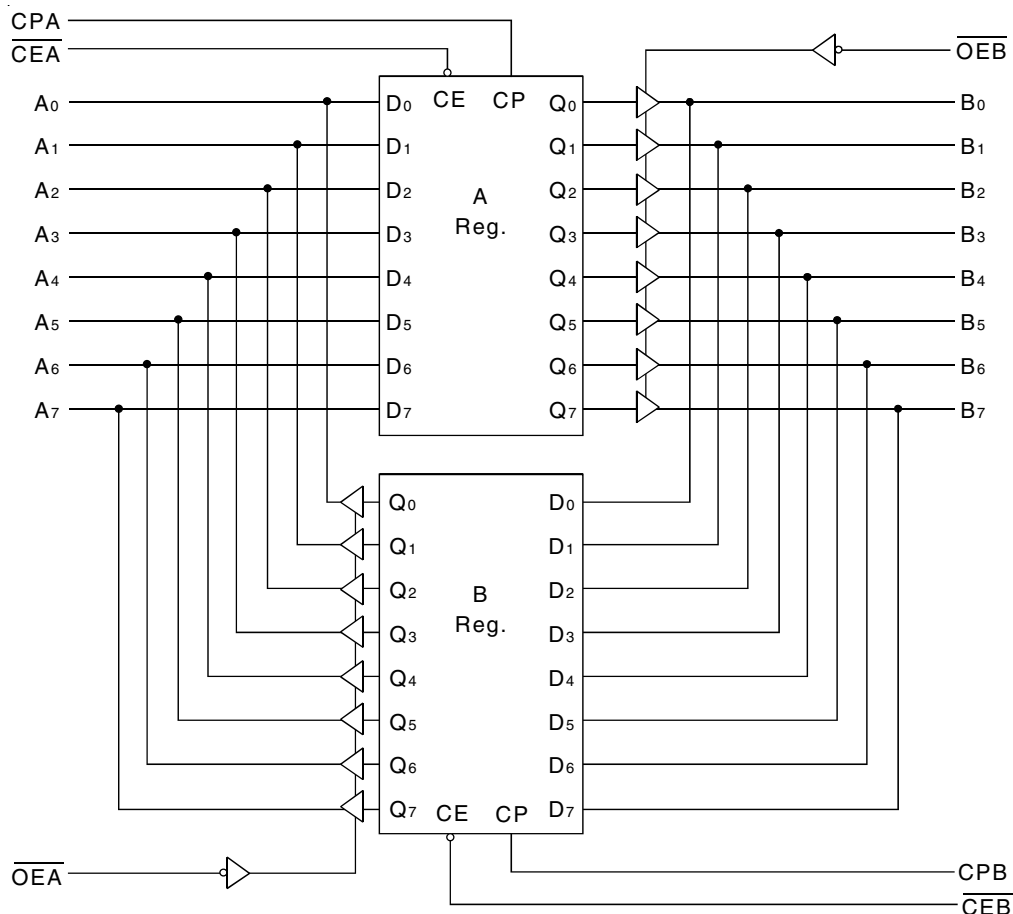
- A and C grades
- Low input and output leakage $\leq 1\mu\text{A}$ (max.)
- CMOS power levels
- True TTL input and output compatibility:
 - $V_{OH} = 3.3V$ (typ.)
 - $V_{OL} = 0.3V$ (typ.)
- High Drive outputs (-15mA IOH, 48mA IOL)
- Meets or exceeds JEDEC standard 18 specifications
- Power off disable outputs permit "live insertion"
- Available in SOIC and QSOP packages

DESCRIPTION:

The IDT29FCT2052T is an 8-bit registered transceiver built using an advanced dual metal CMOS technology. Two 8-bit back-to-back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and 3-state output enable signals are provided for each register. Both A outputs and B outputs are guaranteed to sink 64mA.

The IDT29FCT2052T has balanced drive outputs with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times-reducing the need for external series terminating resistors. The IDT29FCT2052T is a plug-in replacement for the IDT29FCT52T.

FUNCTIONAL BLOCK DIAGRAM

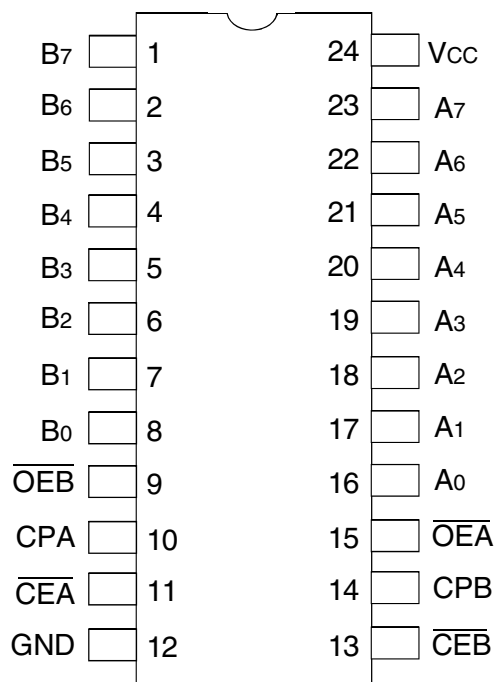


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INDUSTRIAL TEMPERATURE RANGE

FEBRUARY 2006

PIN CONFIGURATION



SOIC/ QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to VCC+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-60 to +120	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed VCC by +0.5V unless otherwise noted.
- Inputs and VCC terminals only.
- Output and I/O terminals only.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

NOTE:

- This parameter is measured at characterization but not tested.

REGISTER FUNCTION TABLE⁽¹⁾

(Applies to A or B Register)

Inputs			Internal	Function
D	CP	CĒ	Q	
X	X	H	NC	Hold Data
L	↑	L	L	Load Data
H	↑	L	H	

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
NC = No Change
↑ = LOW-to-HIGH Transition

OUTPUT CONTROL⁽¹⁾

OĒ	Internal Q	Y-Outputs	Function
H	X	Z	Disable Outputs
L	L	L	Enable Outputs
L	H	H	

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance

PIN DESCRIPTION

Name	I/O	Description
A0-7	I/O	Eight bidirectional lines carrying the A Register inputs or B Register outputs
B0-7	I/O	Eight bidirectional lines carrying the B Register inputs or A Register outputs
CPA	I	Clock for the A Register. When \overline{CEA} is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal.
\overline{CEA}	I	Clock Enable for the A Register. When \overline{CEA} is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal. When \overline{CEA} is HIGH, the A Register holds its contents, regardless of CPA signal transitions.
\overline{OEB}	I	Output Enable for the A Register. When \overline{OEB} is LOW, the A Register outputs are enabled onto the B0-7 lines. When \overline{OEB} is HIGH, the B0-7 outputs are in the high-impedance state.
CPB	I	Clock for the B Register. When \overline{CEB} is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal.
\overline{CEB}	I	Clock Enable for the B Register. When \overline{CEB} is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal. When \overline{CEB} is HIGH, the B Register holds its contents, regardless of CPB signal transitions.
\overline{OEA}	I	Output Enable for the B Register. When \overline{OEA} is LOW, the B Register outputs are enabled onto the A0-7 lines. When \overline{OEA} is HIGH, the A0-7 outputs are in the high-impedance state.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V
I_{IH}	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ $V_I = 2.7\text{V}$	—	—	± 1	μA
I_{IL}	Input LOW Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ $V_I = 0.5\text{V}$	—	—	± 1	μA
I_{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁴⁾	$V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$ $V_I = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}			—	—	± 1	
I_I	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$	—	—	± 1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$	—	-0.7	-1.2	V
V_H	Input Hysteresis	—	—	200	—	mV
I_{CC}	Quiescent Power Supply Current	$V_{CC} = 3\text{V}$ $V_{IN} = \text{GND or } V_{CC}$	—	0.01	1	μA

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit
I_{ODL}	Output LOW Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_{OUT} = 1.5\text{V}^{(3)}$	16	48	—	mA
I_{ODH}	Output HIGH Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_{OUT} = 1.5\text{V}^{(3)}$	-16	-48	—	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -15\text{mA}$	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 12\text{mA}$	—	0.3	0.5	V

NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^\circ\text{C}$ ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^\circ\text{C}$.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open \overline{OE}_A or $\overline{OE}_B = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle \overline{OE}_A or $\overline{OE}_B = \text{GND}$ One Bit Toggling at $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.6	2.2	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	1.1	4.2	
		$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle \overline{OE}_A or $\overline{OE}_B = \text{GND}$ Eight Bits Toggling at $f_i = 2.5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	1.5	4 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	3.8	13 ⁽⁵⁾	

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.

3. Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND.

4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.

5. Values for these conditions are examples of ΔI_{CC} formula. These limits are guaranteed but not tested.

6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$

$I_{CC} = \text{Quiescent Current}$

$\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$

$D_H = \text{Duty Cycle for TTL Inputs High}$

$N_T = \text{Number of TTL Inputs at } D_H$

$I_{CCD} = \text{Dynamic Current caused by an Input Transition Pair (HLH or LHL)}$

$f_{CP} = \text{Output Frequency}$

$f_i = \text{Output Frequency}$

$N_i = \text{Number of Outputs at } f_i$

All currents are in milliamps and all frequencies are in megahertz.

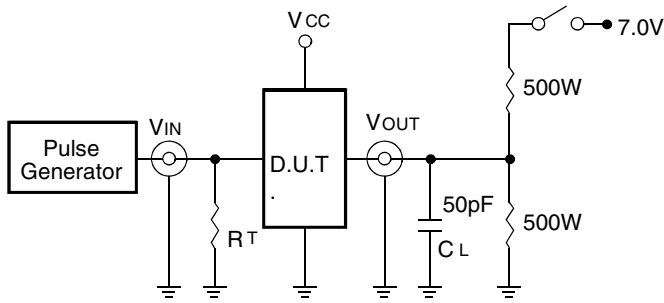
SWITCHING CHARACTERISTICS OVER OPERATING RANGE⁽¹⁾

Symbol	Parameter	Condition ⁽¹⁾	29FCT2052AT		29FCT2052CT		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH}	Propagation Delay	CL = 50pF RL = 500Ω	2	10	2	6.3	ns
t _{PHL}	CPA, CPB to An, Bn						
t _{PZH}	Output Enable Time		1.5	10.5	1.5	7	ns
t _{PZL}	$\overline{OE}A$ or $\overline{OE}B$ to An, Bn						
t _{PHZ}	Output Disable Time		1.5	10	1.5	6.5	ns
t _{PLZ}	$\overline{OE}A$ or $\overline{OE}B$ to An, Bn						
t _{SU}	Set-up Time, HIGH or LOW An, Bn to CPA, CPB		2.5	—	2.5	—	ns
t _H	Hold Time, HIGH or LOW An, Bn to CPA, CPB		2	—	1.5	—	ns
t _{SU}	Set-up Time, HIGH or LOW $\overline{CE}A$, $\overline{CE}B$ to CPA, CPB		3	—	3	—	ns
t _H	Hold Time, HIGH or LOW $\overline{CE}A$, $\overline{CE}B$ to CPA, CPB	2	—	2	—	ns	
t _w	Clock Pulse Width HIGH or LOW ⁽³⁾	3	—	3	—	ns	

NOTES:

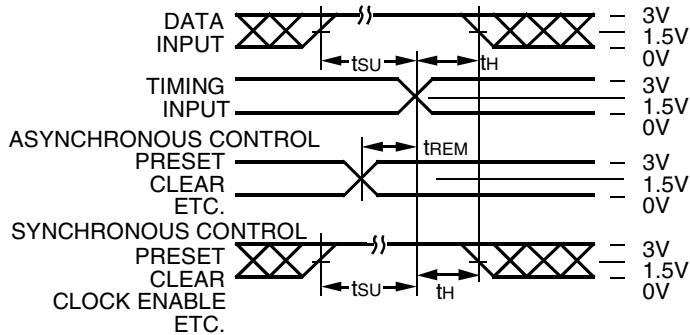
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS



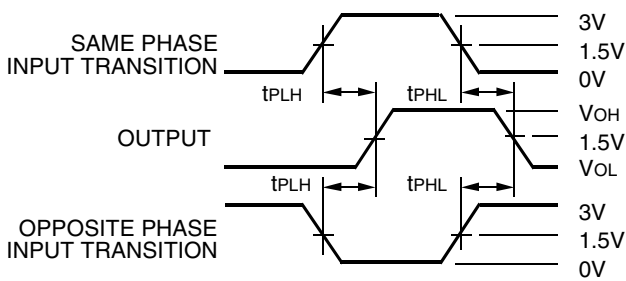
Octal Link

Test Circuits for All Outputs



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Set-Up, Hold, and Release Times



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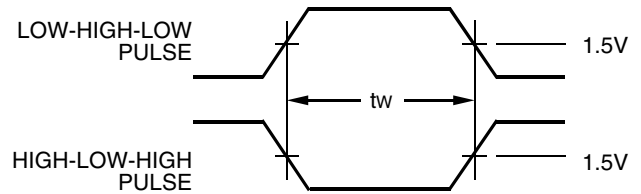
Propagation Delay

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

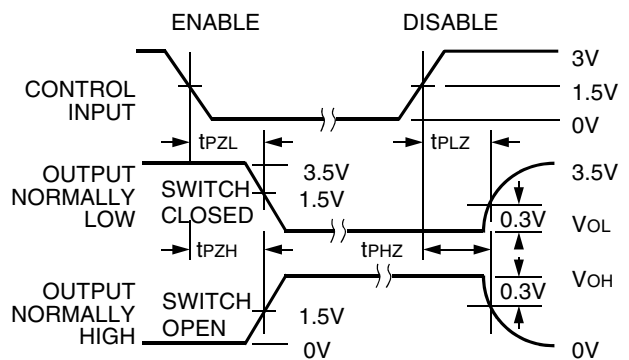
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

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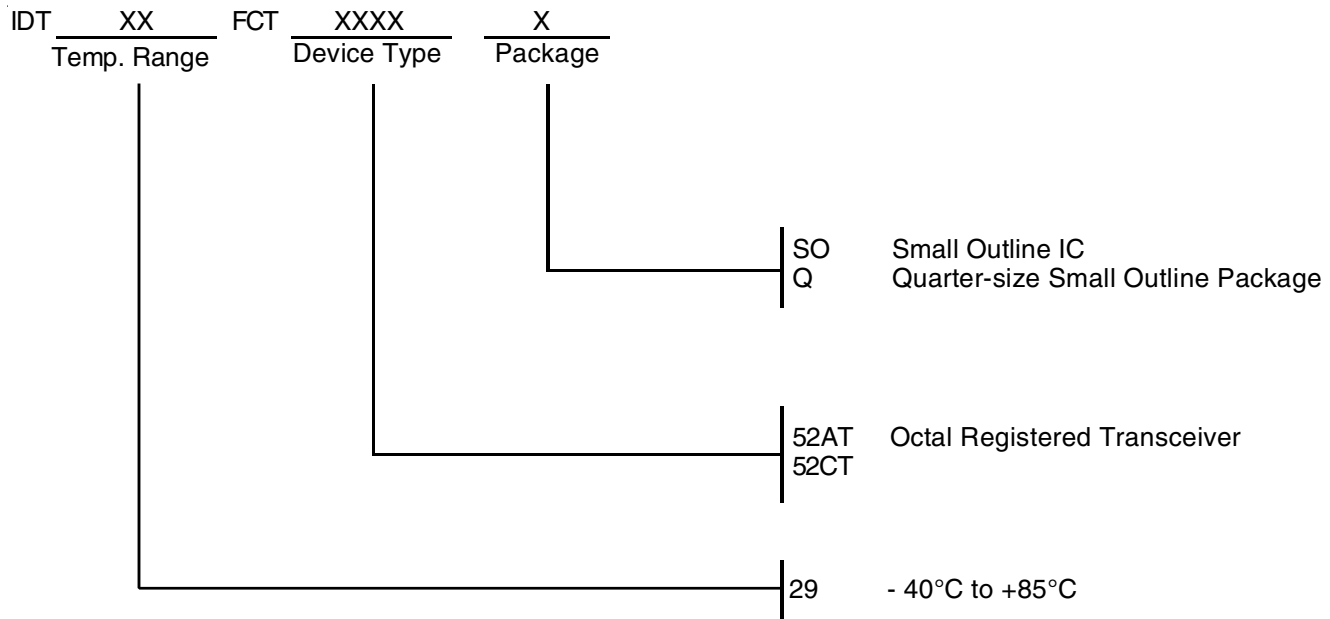
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Enable and Disable Times

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tr ≤ 2.5ns; tr ≤ 2.5ns.

ORDERING INFORMATION



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