

# 700MHz, DIFFERENTIAL-TO-3.3V LVPECL ZERO DELAY CLOCK GENERATOR

# ICS8735-21

## General Description

The ICS8735-21 is a highly versatile 1:1 Differential-to-3.3V LVPECL clock generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The CLK, nCLK pair can accept most standard differential input levels. The ICS8735-21 has a fully integrated PLL and can be configured as zero delay buffer, multiplier or divider, and has an output frequency range of 31.25MHz to 700MHz. The reference divider, feedback divider and output divider are each programmable, thereby allowing for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8. The external feedback allows the device to achieve “zero delay” between the input clock and the output clocks. The PLL\_SEL pin can be used to bypass the PLL for system test and debug purposes. In bypass mode, the reference clock is routed around the PLL and into the internal output dividers.



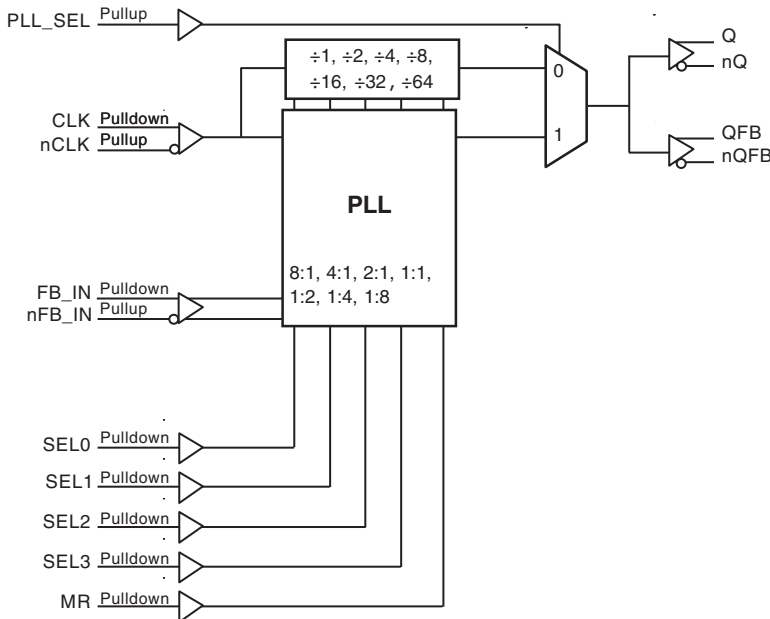
## Features

- One differential 3.3V LVPECL output pair  
One differential feedback output pair
- Differential CLK/nCLK input pair
- CLK/nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSSL, SSTL
- Output frequency range: 31.25MHz to 700MHz
- Input frequency range: 31.25MHz to 700MHz
- VCO range: 250MHz to 700MHz
- External feedback for “zero delay” clock regeneration with configurable frequencies
- Programmable dividers allow for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8
- Cycle-to-cycle jitter: 25ps (maximum)
- Static phase offset: 50ps ± 100ps
- Full 3.3V supply voltage
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

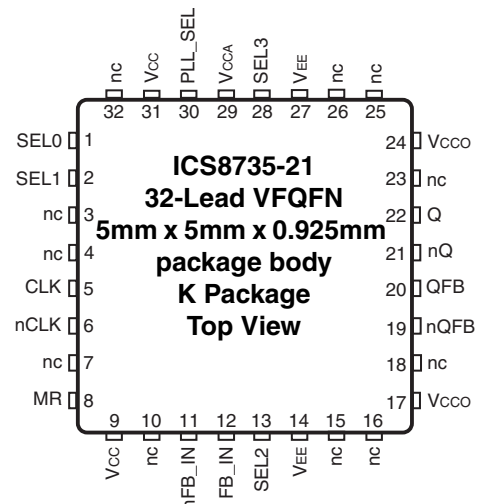
## Pin Assignments

CLK	1	20	nc
nCLK	2	19	SEL1
MR	3	18	SEL0
Vcc	4	17	Vcc
nFB_IN	5	16	PLL_SEL
FB_IN	6	15	Vcca
SEL2	7	14	SEL3
VEE	8	13	Vcco
nQFB	9	12	Q
QFB	10	11	nQ

## Block Diagram



**ICS8735-21**  
**20-Lead SOIC**  
**7.5mm x 12.8mm x 2.3mm package body**  
**M Package**  
**Top View**



**Table 1. Pin Descriptions**

Name	Type		Description
CLK	Input	Pulldown	Non-inverting differential clock input.
nCLK	Input	Pullup	Inverting differential clock input.
nFB_IN	Input	Pullup	Inverting differential feedback input to phase detector for regenerating clocks with "zero delay."
FB_IN	Input	Pulldown	Non-inverted differential feedback input to phase detector for regenerating clocks with "zero delay."
MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true output Q to go low and the inverted output nQ to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTTL interface levels.
SEL0, SEL1, SEL2, SEL3	Input	Pulldown	Determines output divider values in Table 3. LVCMOS / LVTTTL interface levels.
PLL_SEL	Input	Pullup	PLL select. Selects between the PLL and reference clock as the input to the dividers. When LOW, selects reference clock. When HIGH, selects PLL. LVCMOS/LVTTTL interface levels.
nQ, Q	Output		Differential output pair. LVPECL interface levels.
nQFB, QFB	Output		Differential feedback output pair. LVPECL interface levels.
V <sub>EE</sub>	Power		Negative supply pin.
V <sub>CC</sub>	Power		Core supply pins.
V <sub>CCA</sub>	Power		Analog supply pin.
V <sub>CCO</sub>	Power		Output supply pin.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

## Function Tables

Table 3A. Control Input Function Table

Inputs					Outputs PLL_SEL = 1 PLL Enable Mode
SEL3	SEL2	SEL1	SEL0	Reference Frequency Range (MHz)*	Q/nQ, QFB/nQFB
0	0	0	0	250 - 700	÷1
0	0	0	1	125 - 350	÷1
0	0	1	0	62.5 - 175	÷1
0	0	1	1	31.25 - 87.5	÷1
0	1	0	0	250 - 700	÷2
0	1	0	1	125 - 350	÷2
0	1	1	0	62.5 - 175	÷2
0	1	1	1	250 - 700	÷4
1	0	0	0	125 - 350	÷4
1	0	0	1	250 - 700	÷8
1	0	1	0	125 - 350	x2
1	0	1	1	62.5 - 175	x2
1	1	0	0	31.25 - 87.5	x2
1	1	0	1	62.5 - 175	x4
1	1	1	0	31.25 - 87.5	x4
1	1	1	1	31.25 - 87.5	x8

\*NOTE: VCO frequency range for all configurations above is 250MHz to 700MHz.

Table 3B. PLL Bypass Function Table

Inputs				Outputs PLL_SEL = 0 PLL Bypass Mode
SEL3	SEL2	SEL1	SEL0	Q/nQ, QFB/nQFB
0z	0	0	0	÷4
0	0	0	1	÷4
0	0	1	0	÷4
0	0	1	1	÷8
0	1	0	0	÷8
0	1	0	1	÷8
0	1	1	0	÷16
0	1	1	1	÷16
1	0	0	0	÷32
1	0	0	1	÷64
1	0	1	0	÷2
1	0	1	1	÷2
1	1	0	0	÷4
1	1	0	1	÷1
1	1	1	0	÷2
1	1	1	1	÷1

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{CC}$	4.6V
Inputs, $V_I$	-0.5V to $V_{CC} + 0.5V$
Outputs, $I_O$ Continuous Current Surge Current	50mA 100mA
Package Thermal Impedance, $\theta_{JA}$ 20 Lead SOIC 32 Lead VFQFN	46.2°C/W (0 lfpm) 37.0°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{CCA}$	Analog Supply Voltage		3.135	3.3	3.465	V
$V_{CCO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{EE}$	Power Supply Current				150	mA
$I_{CCA}$	Analog Supply Current				15	mA

**Table 4B. LVCMOS/LVTTL DC Characteristics,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage		-0.3		0.8	V
$I_{IH}$	Input High Current	SEL[0:3], MR	$V_{CC} = V_{IN} = 3.465V$		150	$\mu A$
		PLL_SEL	$V_{CC} = V_{IN} = 3.465V$		5	$\mu A$
$I_{IL}$	Input Low Current	SEL[0:3], MR	$V_{CC} = 3.465V, V_{IN} = 0V$	-5		$\mu A$
		PLL_SEL	$V_{CC} = 3.465V, V_{IN} = 0V$	-150		$\mu A$

**Table 4C. Differential DC Characteristics,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	CLK, FB_IN	$V_{CC} = V_{IN} = 3.465V$		150	$\mu A$
		nCLK, nFB_IN	$V_{CC} = V_{IN} = 3.465V$		5	$\mu A$
$I_{IL}$	Input Low Current	CLK, FB_IN	$V_{CC} = 3.465V$ , $V_{IN} = 0V$	-5		$\mu A$
		nCLK, nFB_IN	$V_{CC} = 3.465V$ , $V_{IN} = 0V$	-150		$\mu A$
$V_{PP}$	Peak-to-Peak Voltage; NOTE 1		0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2		$V_{EE} + 0.5$		$V_{CC} - 0.85$	V

NOTE 1:  $V_{IL}$  should not be less than -0.3V.NOTE 2: Common mode input voltage is defined as  $V_{IH}$ .**Table 4D. LVPECL DC Characteristics,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CCO} - 1.4$		$V_{CCO} - 0.9$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CCO} - 2.0$		$V_{CCO} - 1.7$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CCO} - 2V$ .**Table 5. Input Frequency Characteristics,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{IN}$	Input Frequency	CLK, nCLK	PLL_SEL = 1	31.25	700	MHz
			PLL_SEL = 0		700	MHz

## AC Electrical Characteristics

**Table 6. AC Characteristics,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				700	MHz
$t_{PD}$	Propagation Delay; NOTE 1	PLL_SEL = 0V, $f \leq 700MHz$	3.0		4.2	ns
$tsk(o)$	Output Skew; NOTE 2, 3	PLL_SEL = 0V			20	ps
$tsk(\emptyset)$	Static Phase Offset; NOTE 3, 4	PLL_SEL = 3.3V	-50	50	150	ps
$f_{jit}(cc)$	Cycle-to-Cycle Jitter; NOTE 3, 5				25	ps
$f_{jit}(\theta)$	Phase Jitter; NOTE 3, 5, 6				$\pm 50$	ps
$t_L$	PLL Lock Time				1	ms
$t_R / t_F$	Output Rise/Fall Time; NOTE 7	20% to 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle		47		53	%

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

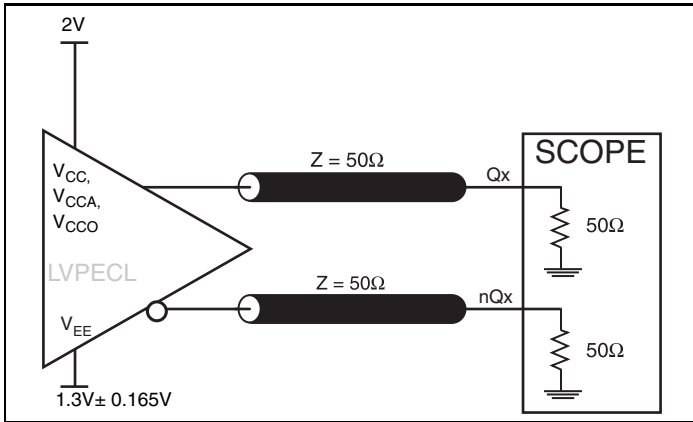
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: Defined as the time difference between the input reference clock and the averaged feedback input signal across all conditions, when the PLL is locked and the input reference frequency is stable.

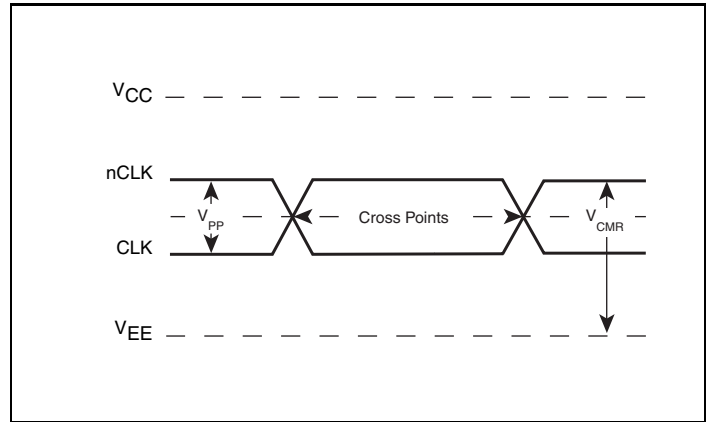
NOTE 5: Characterized at VCO frequency of 622MHz.

NOTE 6: Phase jitter is dependent on the input source used.

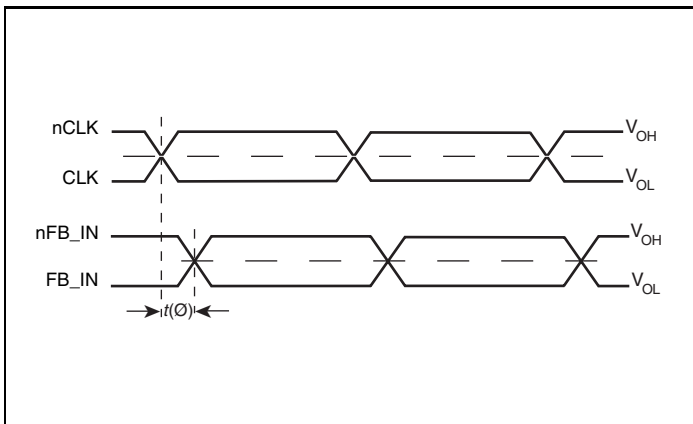
### Parameter Measurement Information



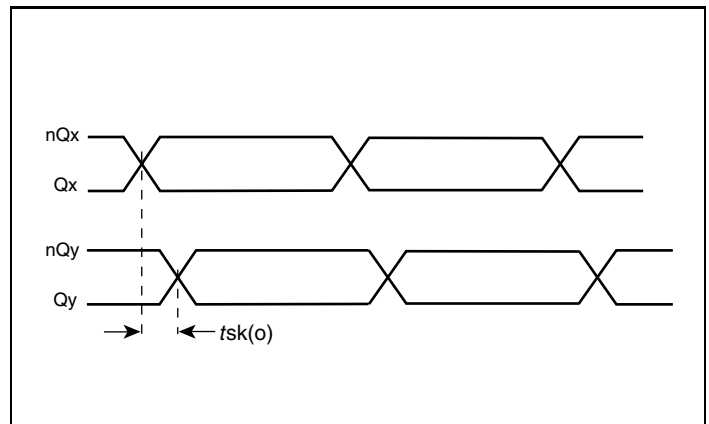
3.3V Output Load AC Test Circuit



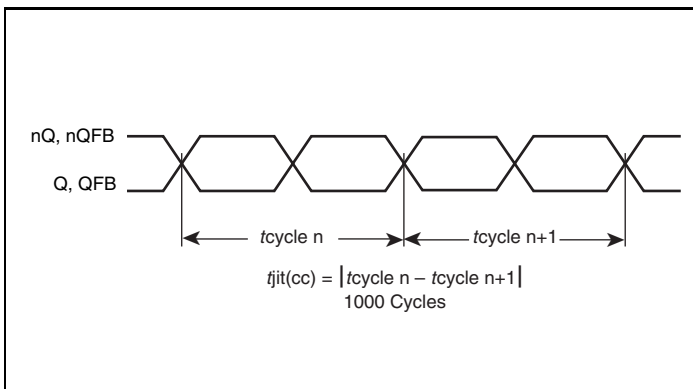
Differential Input Level



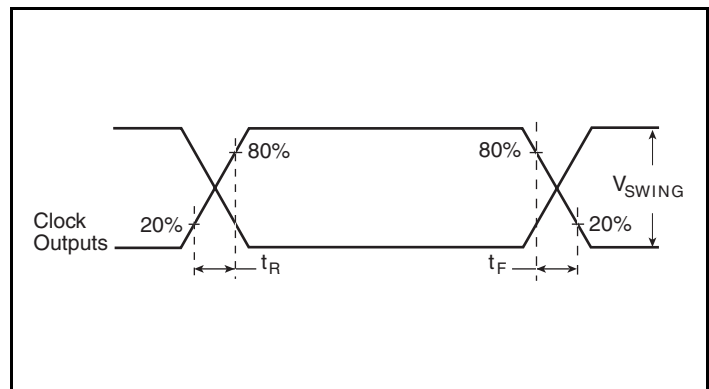
Phase Jitter and Static Phase Offset



Output Skew



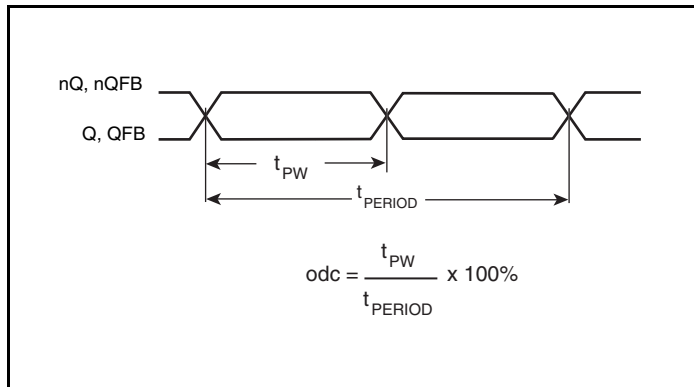
Cycle-to-Cycle Jitter



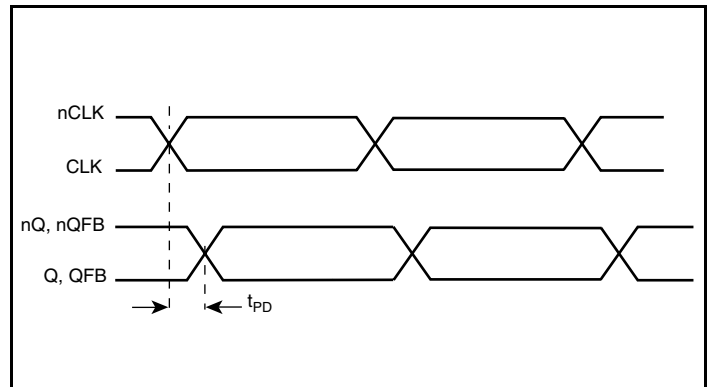
Output Rise/Fall Time



## Parameter Measurement Information, continued



Output Duty Cycle/Pulse Width/Period



Propagation Delay

## Application Information

### Recommendations for Unused Input and Output Pins

#### Inputs:

##### LVC MOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

##### CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

##### FB\_IN/nFB\_IN Inputs

For applications not requiring the use of the differential input, both FB\_IN and nFB\_IN can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from FB\_IN to ground.

#### Outputs:

##### LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

## Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS8735-21 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{CC}$ ,  $V_{CCA}$  and  $V_{CCO}$  should be individually connected to the power supply plane through vias, and  $0.01\mu\text{F}$  bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic  $V_{CC}$  pin and also shows that  $V_{CCA}$  requires that an additional  $10\Omega$  resistor along with a  $10\mu\text{F}$  bypass capacitor be connected to the  $V_{CCA}$  pin. The  $10\Omega$  resistor can also be replaced by a ferrite bead.

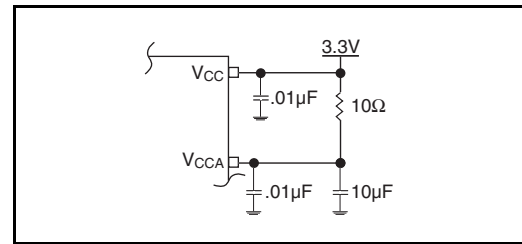


Figure 1. Power Supply Filtering

## Wiring the Differential Input to Accept Single Ended Levels

*Figure 2* shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{CC}/2$  is generated by the bias resistors  $R1$ ,  $R2$  and  $C1$ . This bias circuit should be located as close as possible to the input pin. The ratio of  $R1$  and  $R2$  might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only  $2.5\text{V}$  and  $V_{CC} = 3.3\text{V}$ ,  $V_{REF}$  should be  $1.25\text{V}$  and  $R2/R1 = 0.609$ .

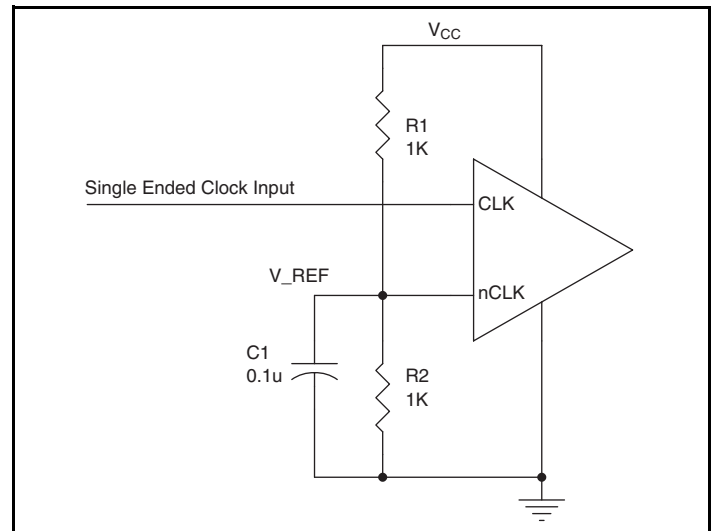
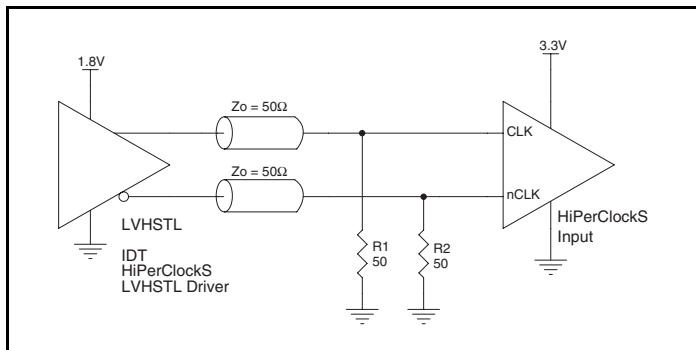


Figure 2. Single-Ended Signal Driving Differential Input

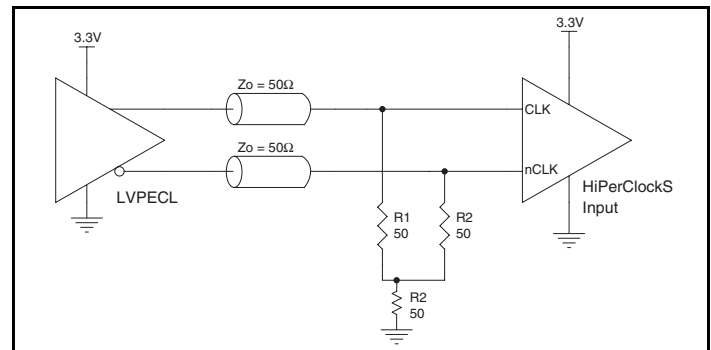
### Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 3A to 3F show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver

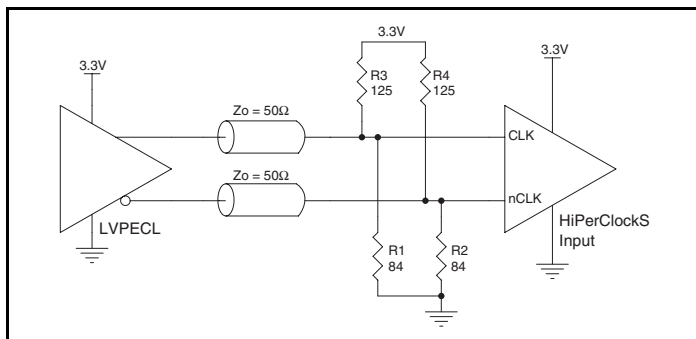
component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



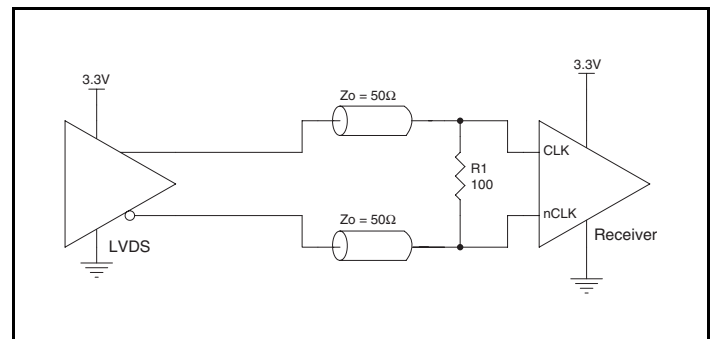
**Figure 3A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver**



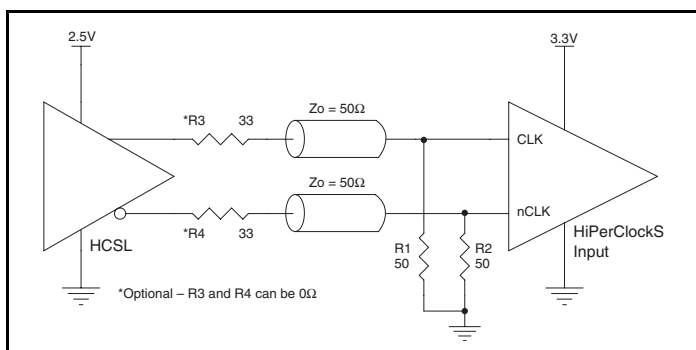
**Figure 3B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



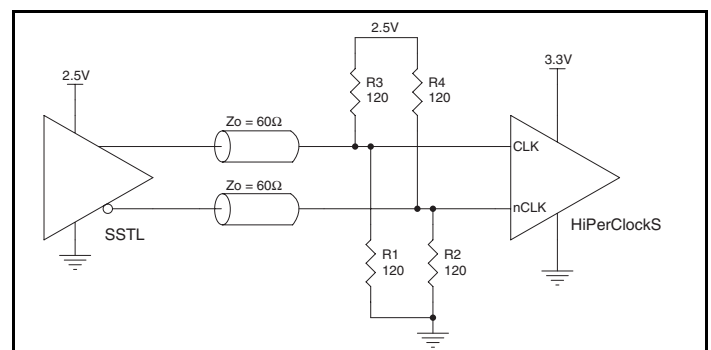
**Figure 3C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



**Figure 3D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver**



**Figure 3E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver**



**Figure 3F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver**

## Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive  $50\Omega$

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

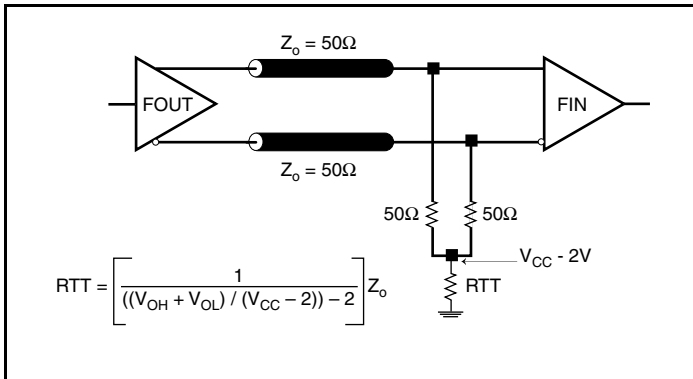


Figure 4A. 3.3V LVPECL Output Termination

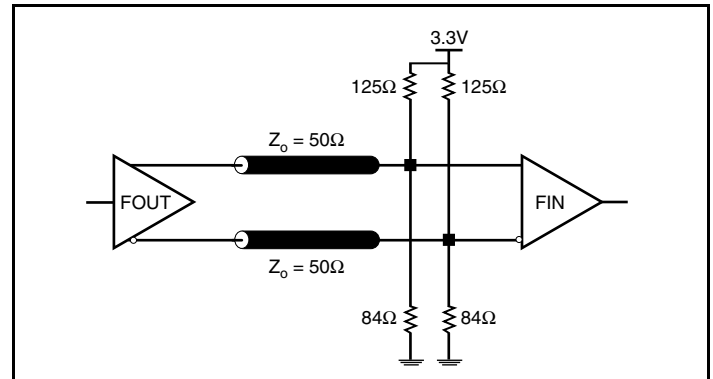


Figure 4B. 3.3V LVPECL Output Termination

### Schematic Example

Figure 5 shows a schematic example of the ICS8735-21. In this example, the input is driven by an HCSL driver. The zero delay buffer is configured to operate at 155.52MHz input and 77.75MHz output. The logic control pins are configured as follows:

SEL [3:0] = 0101; PLL\_SEL = 1

The decoupling capacitors should be physically located near the power pin. For ICS8735-21.

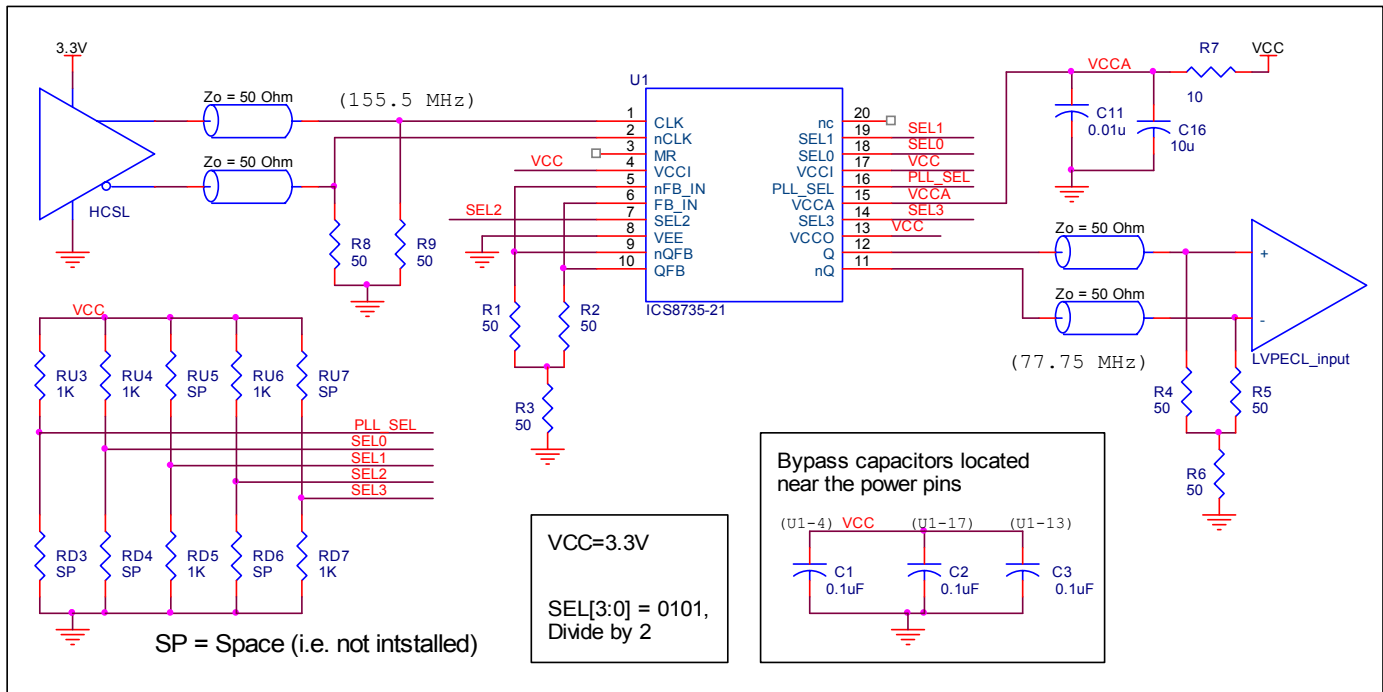


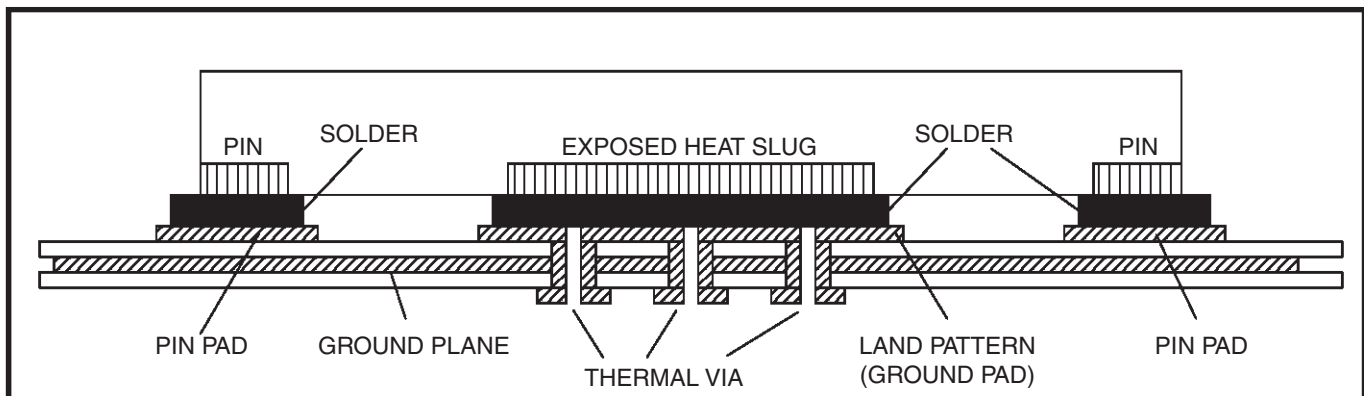
Figure 5. ICS8735-21 LVPECL Buffer Schematic Example

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are

application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor's Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.



**Figure 6. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**

## Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8735-21. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS8735-21 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{CC\_MAX} = 3.465V * 150mA = 519.8mW$
- Power (outputs)<sub>MAX</sub> = **30mW/Loaded output pair**  
If all outputs are loaded, the total power is  $2 * 30mW = 60mW$

**Total Power**<sub>MAX</sub> = (3.465V, with all outputs switching) =  $519.8mW + 60mW = 579.8mW$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 83.2°C/W per Table 7A below.

Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ\text{C} + 0.580W * 83.2^\circ\text{C/W} = 118.3^\circ\text{C}. \text{ This is well below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

**Table 7A. Thermal Resistance  $\theta_{JA}$  for 20 Lead SOIC, Forced Convection**

$\theta_{JA}$ vs. Air Flow			
Linear Feet per Minute	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	83.2°C/W	65.7°C/W	57.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

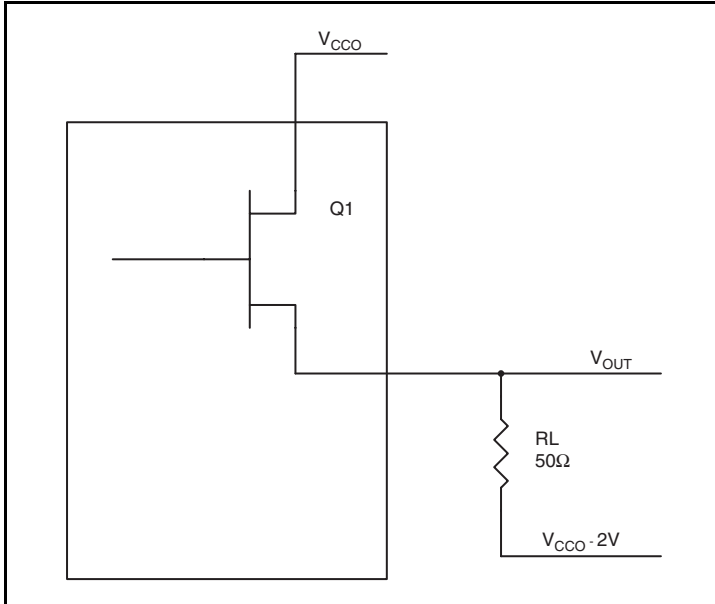
**Table 7B. Thermal Resistance  $\theta_{JA}$  for 32 Lead VFQFN, Forced Convection**

$\theta_{JA}$ by Velocity			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 7*.



**Figure 7. LVPECL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CCO} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CCO\_MAX} - 0.9V$   
( $V_{CCO\_MAX} - V_{OH\_MAX}$ ) = **0.9V**
- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CCO\_MAX} - 1.7V$   
( $V_{CCO\_MAX} - V_{OL\_MAX}$ ) = **1.7V**

$Pd\_H$  is power dissipation when the output drives high.

$Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$$

$$\text{Total Power Dissipation per output pair} = Pd\_H + Pd\_L = \mathbf{30mW}$$



## Reliability Information

Table 8A.  $\theta_{JA}$  vs. Air Flow Table for a 20 Lead TSSOP

$\theta_{JA}$ vs. Air Flow			
Linear Feet per Minute	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	83.2°C/W	65.7°C/W	57.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Table 8B.  $\theta_{JA}$  vs. Air Flow Table for a 32 Lead VFQFN, Forced Convection

$\theta_{JA}$ by Velocity			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

## Transistor Count

The transistor count for ICS8735-21 is: 2969

## Package Outline and Package Dimensions

Package Outline - M Suffix for 20 Lead SOIC

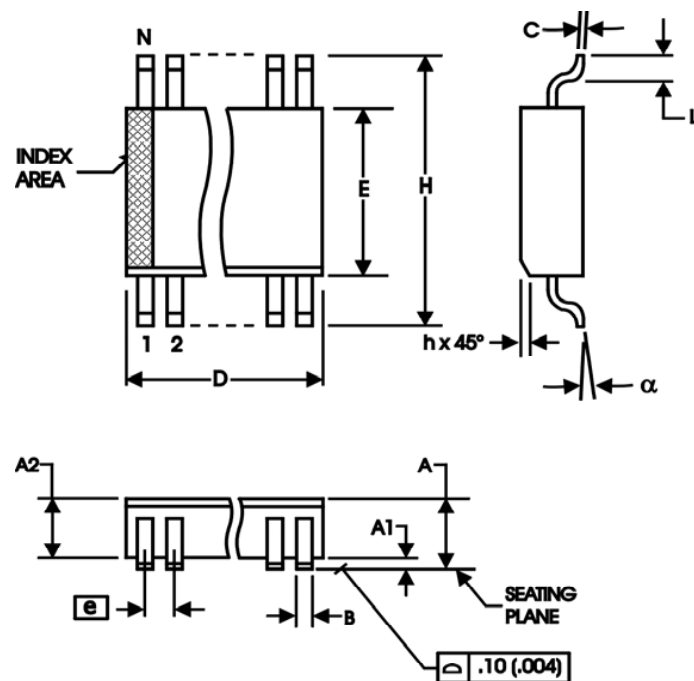
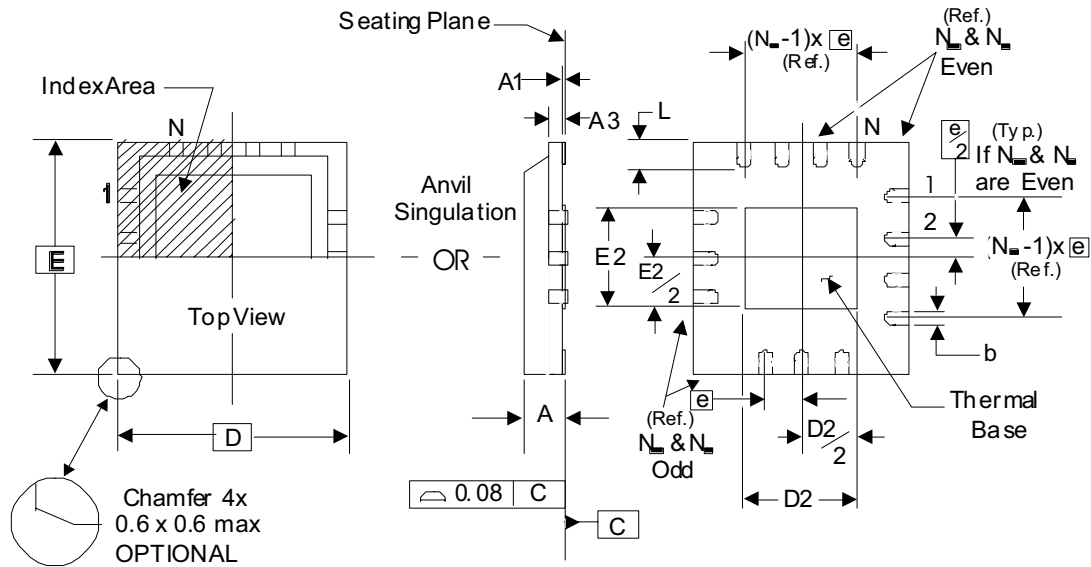


Table 9A. Package Dimensions for 20 Lead SOIC

300 Millimeters All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	20	
A		2.65
A1	0.10	
A2	2.05	2.55
B	0.33	0.51
C	0.18	0.32
D	12.60	13.00
E	7.40	7.60
e	1.27 Basic	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
$\alpha$	0°	7°

Reference Document: JEDEC Publication 95, MS-013, MS-119

## Package Outline - K Suffix for 32 Lead VFQFN



The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 9B below.

Table 9B. Package Dimensions for 32 Lead VFQFN

JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters			
Symbol	Minimum	Nominal	Maximum
$N$		32	
$A$	0.80		1.00
$A1$	0		0.05
$A3$		0.25 Ref.	
$b$	0.18	0.25	0.30
$N_D$ & $N_E$		8	
$D$ & $E$		5.00 Basic	
$D2$ & $E2$	3.0		3.3
$e$		0.50 Basic	
$L$	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

## Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8735AM-21	ICS8735AM-21	20 Lead SOIC	Tube	0°C to 70°C
8735AM-21T	ICS8735AM-21	20 Lead SOIC	1000 Tape & Reel	0°C to 70°C
8735AM-21LF	ICS8735AM-21LF	"Lead-Free" 20 Lead SOIC	Tube	0°C to 70°C
8735AM-21LFT	ICS8735AM-21LF	"Lead-Free" 20 Lead SOIC	1000 Tape & Reel	0°C to 70°C
8735AK-21LF	ICS8735A21L	"Lead-Free" 32 Lead VFQFN	Tray	0°C to 70°C
8735AK-21LFT	ICS8735A21L	"Lead-Free" 32 Lead VFQFN	2500 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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ICS8735-21

700MHZ, DIFFERENTIAL-TO-3.3V LVPECL ZERO DELAY CLOCK GENERATOR

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