

LVDS Transmitter 24-Bit Color Flat Panel Display (FPD) Link

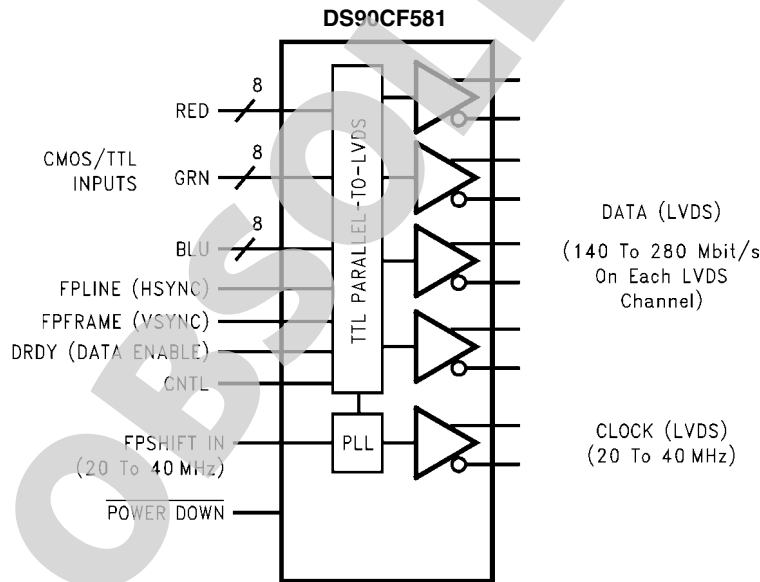
General Description

The DS90CF581 transmitter converts 28 bits of CMOS/TTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. At a transmit clock frequency of 40 MHz, 24 bits of RGB data and 4 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY, CNTL) are transmitted at a rate of 280 Mbps per LVDS data channel. Using a 40 MHz clock, the data throughput is 140 Megabytes per second. This transmitter is intended to interface to any of the FPD Link receivers. The chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

Features

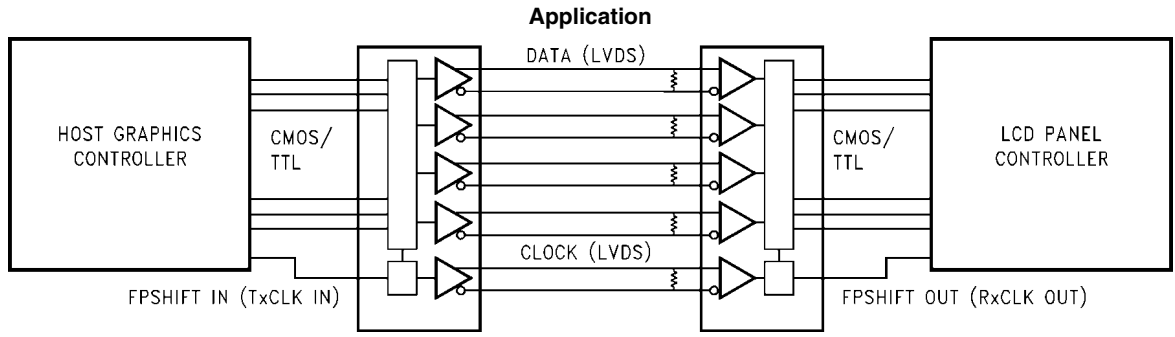
- Up to 140 Megabyte/sec Bandwidth
- Narrow bus reduces cable size and cost
- 290 mV swing LVDS devices for low EMI
- Low power CMOS design
- Power-down mode
- PLL requires no external components
- Low profile 56-lead TSSOP package
- Falling edge data strobe
- Compatible with TIA/EIA-644 LVDS standard

Block Diagrams



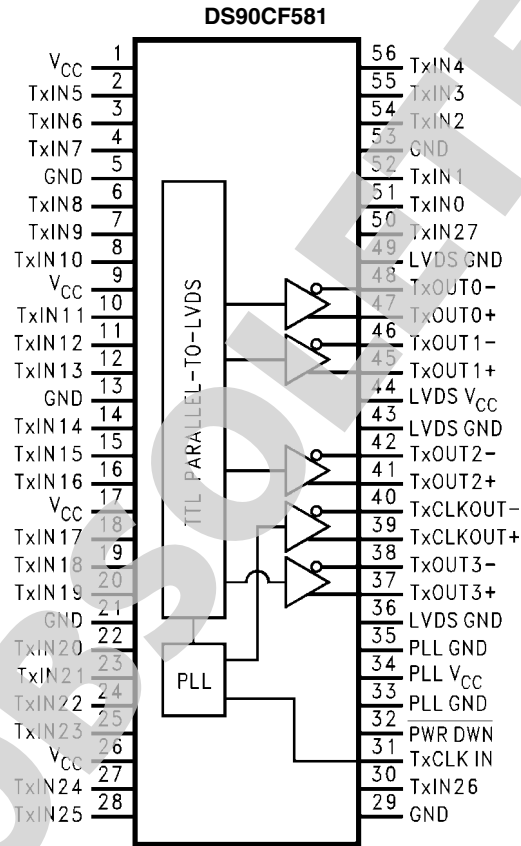
Order Number DS90CF581MTD
See NS Package Number MTD56

1248628



1248602

Connection Diagram



1248603

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.3 to +6V
CMOS/TTL Input Voltage	-0.3 to ($V_{CC} + 0.3V$)
LVDS Driver Output Voltage	-0.3 to ($V_{CC} + 0.3V$)
LVDS Output Short Circuit Duration	continuous
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	+260°C
Maximum Package Power Dissipation @ +25°C	
MTD56 (TSSOP) Package:	

DS90CF581	1.63W
Derate Package:	
DS90CF581	12.5 mW/°C above +25°C
This device does not meet 2000V ESD rating. <small>(Note 4)</small>	

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Free				
Air Temperature (T_A)	-10	+25	+70	°C
Receiver Input Range	0		2.4	V
Supply Noise Voltage (V_{CC})			100	mV _{P-P}

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
CMOS/TTL DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V	
V_{IL}	Low Level Input Voltage		GND		0.8	V	
V_{CL}	Input Clamp Voltage	$I_{CL} = -18\text{ mA}$		-0.79	-1.5	V	
I_{IN}	Input Current	$V_{IN} = V_{CC}, \text{GND}, 2.5V \text{ or } 0.4V$		±5.1	±10	µA	
LVDS DRIVER DC SPECIFICATIONS							
V_{OD}	Differential Output Voltage	$R_L = 100\Omega$	250	290	450	mV	
ΔV_{OD}	Change in V_{OD} between Complimentary Output States				35	mV	
V_{OS}	Offset Voltage <small>(Note 5)</small>		1.1	1.25	1.375	V	
ΔV_{OS}	Change in V_{OS} between Complimentary Output States				35	mV	
V_{OH}	High Level Output Voltage			1.3	1.6	V	
V_{OL}	Low Level Output Voltage		0.9	1.01		V	
I_{OS}	Output Short Circuit Current	$V_{OUT} = 0V, R_L = 100\Omega$		-2.9	-5	mA	
I_{OZ}	Output TRI-STATE® Current	Power Down = 0V, $V_{OUT} = 0V \text{ or } V_{CC}$		±1	±10	µA	
TRANSMITTER SUPPLY CURRENT							
I_{CCTW}	Transmitter Supply Current, Worst Case	$R_L = 100\Omega, C_L = 5\text{ pF},$ Worst Case Pattern <small>(Figure 1, Figure 3)</small>	$f = 32.5\text{ MHz}$		34	51	mA
			$f = 37.5\text{ MHz}$		36	53	mA
I_{CCTG}	Transmitter Supply Current, 16 Grayscale	$R_L = 100\Omega, C_L = 5\text{ pF},$ Grayscale Pattern <small>(Figure 2, Figure 3)</small>	$f = 32.5\text{ MHz}$		27	47	mA
			$f = 37.5\text{ MHz}$		28	48	mA
I_{CCTZ}	Transmitter Supply Current, Power Down	Power Down = Low		1	25	µA	

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for $V_{CC} = 5.0V$ and $T_A = +25^{\circ}C$.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Note 4: ESD Rating: HBM (1.5 k Ω , 100 pF)

PLL $V_{CC} \geq 1000V$

All other pins $\geq 2000V$

EIAJ (0 Ω , 200 pF) $\geq 150V$

Note 5: V_{OS} previously referred as V_{CM} .

Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units	
LLHT	LVDS Low-to-High Transition Time (<i>Figure 3</i>)		0.75	1.5	ns	
LHLT	LVDS High-to-Low Transition Time (<i>Figure 3</i>)		0.75	1.5	ns	
TCIT	TxCLK IN Transition Time (<i>Figure 4</i>)			8	ns	
TCCS	TxOUT Channel-to-Channel Skew (<i>Note 6</i>) (<i>Figure 5</i>)			350	ps	
TPPos0	Transmitter Output Pulse Position for Bit 0 (<i>Figure 11</i>)	f = 20 MHz	-200	150	350	ps
TPPos1	Transmitter Output Pulse Position for Bit 1		6.3	7.2	7.5	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		12.8	13.6	14.6	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		20	20.8	21.5	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		27.2	28	28.5	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		34.5	35.2	35.6	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		42.2	42.6	42.9	ns
TPPos0	Transmitter Output Pulse Position for Bit 0 (<i>Figure 11</i>)	f = 40 MHz	-100	100	300	ps
TPPos1	Transmitter Output Pulse Position for Bit 1		2.9	3.3	3.9	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		6.1	6.6	7.1	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		9.7	10.2	10.7	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		13	13.5	14.1	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		17	17.4	17.8	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		20.3	20.8	21.4	ns
TCIP	TxCLK IN Period (<i>Figure 6</i>)	25	T	50	ns	
TCIH	TxCLK IN High Time (<i>Figure 6</i>)	0.35T	0.5T	0.65T	ns	
TCIL	TxCLK IN Low Time (<i>Figure 6</i>)	0.35T	0.5T	0.65T	ns	
TSTC	TxIN Setup to TxCLK IN (<i>Figure 6</i>)	f = 20 MHz	14		ns	
		f = 40 MHz	8		ns	
THTC	TxIN Hold to TxCLK IN (<i>Figure 6</i>)	2.5	2		ns	
TCCD	TxCLK IN to TxCLK OUT Delay @ 25°C, $V_{CC} = 5.0V$ (<i>Figure 7</i>)	5		9.7	ns	
TPLLS	Transmitter Phase Lock Loop Set (<i>Figure 8</i>)			10	ms	
TPDD	Transmitter Powerdown Delay (<i>Figure 10</i>)			100	ns	

Note 6: This limit based on bench characterization.

AC Timing Diagrams

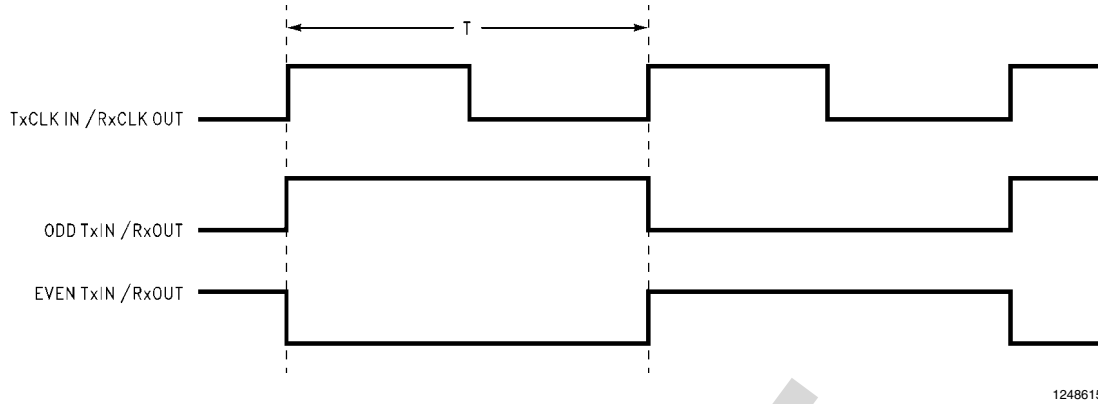
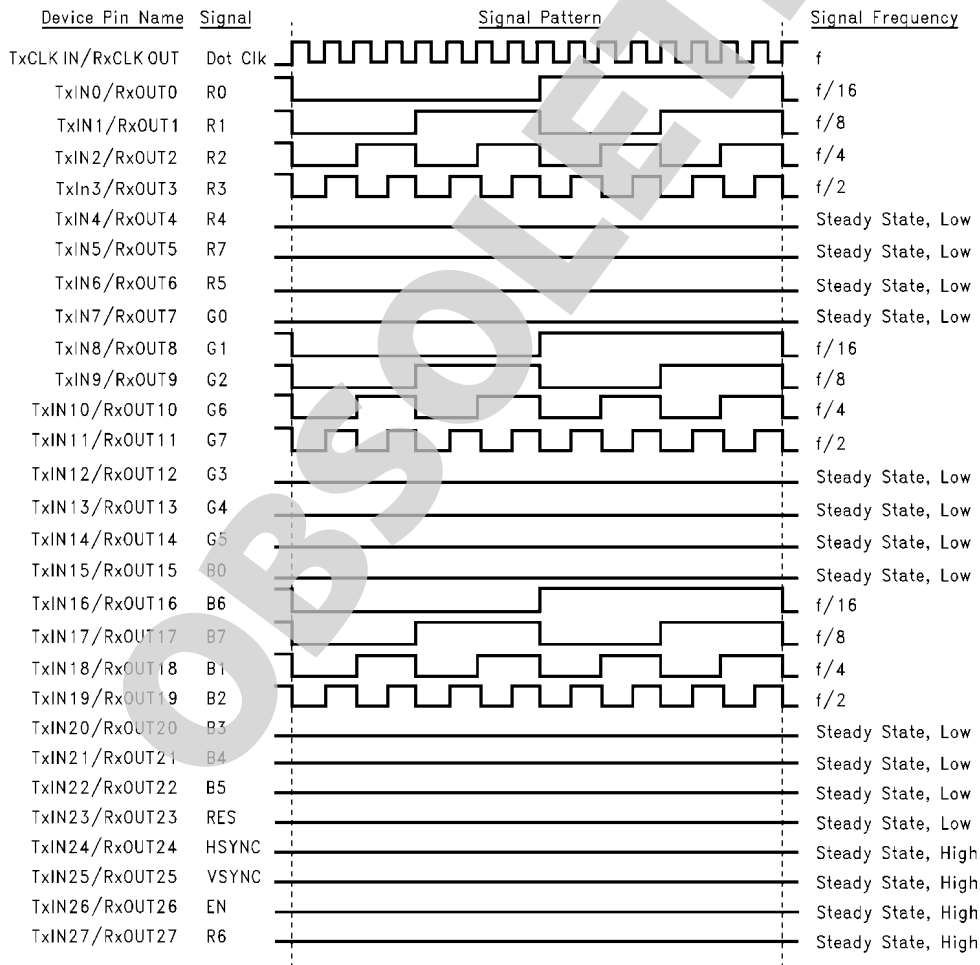


FIGURE 1. "WORST CASE" Test Pattern



1248616

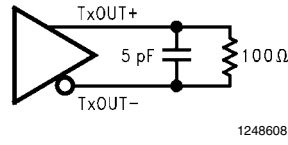
Note 7: The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

Note 8: The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

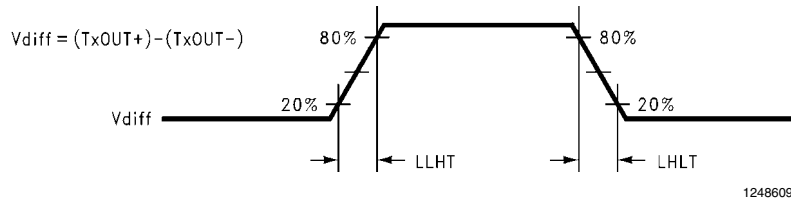
Note 9: Figure 1 and Figure 2 show a falling edge data strobe (TxCLK IN/RxCLK OUT).

Note 10: Recommended pin to signal mapping. Customer may choose to define differently.

FIGURE 2. "16 GRAYSCALE" Test Pattern (Note 7, Note 8, Note 9, Note 10)

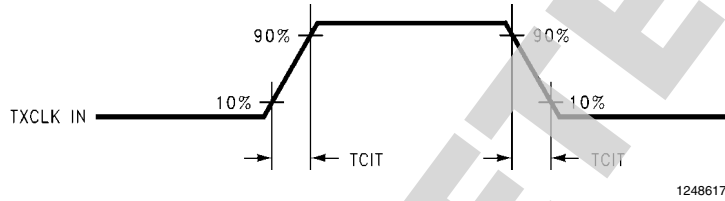


1248608



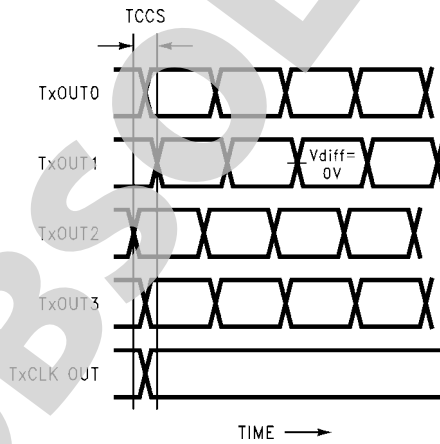
1248609

FIGURE 3. DS90CF581 (Transmitter) LVDS Output Load and Transition Timing



1248617

FIGURE 4. DS90CF581 (Transmitter) Input Clock Transition Time



1248618

Note 11: Measurements at $V_{diff} = 0V$

Note 12: TCCS measured between earliest and latest initial LVDS edges.

Note 13: TxCLK OUT Differential High→Low Edge for DS90CF581

TxCLK OUT Differential Low→High Edge for DS90CR581

FIGURE 5. DS90CF581 (Transmitter) Channel-to-Channel Skew

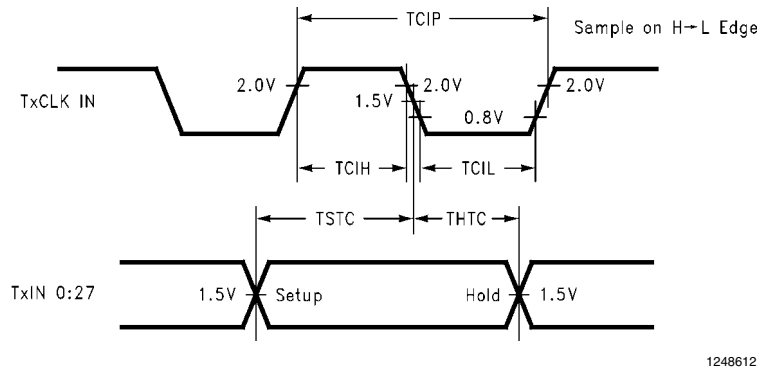


FIGURE 6. DS90CF581 (Transmitter) Setup/hold and High/Low Times

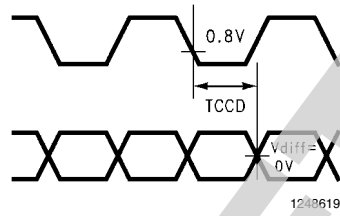


FIGURE 7. DS90CF581 (Transmitter) Clock In to Clock Out Delay

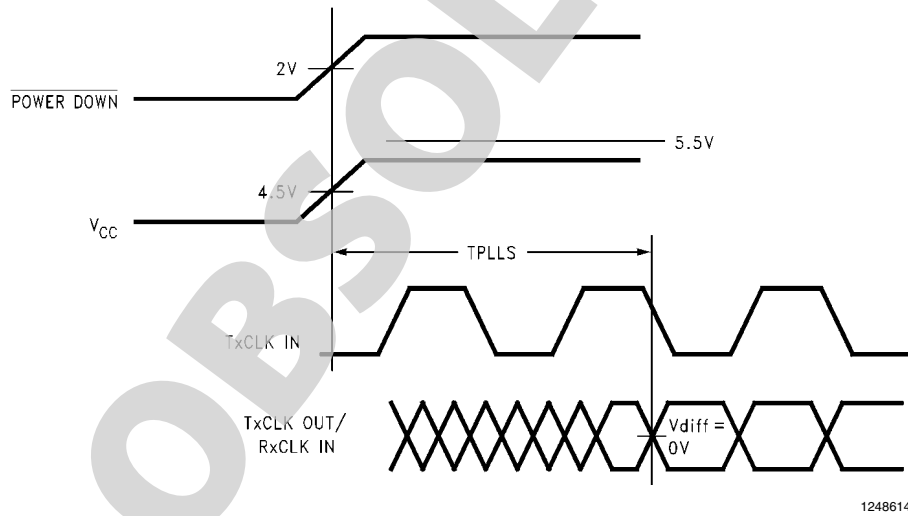
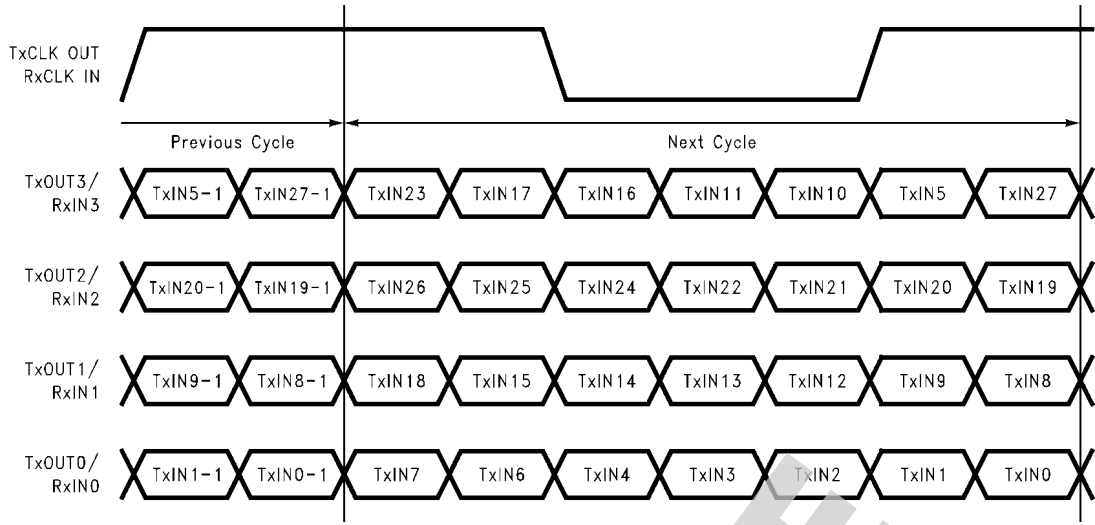
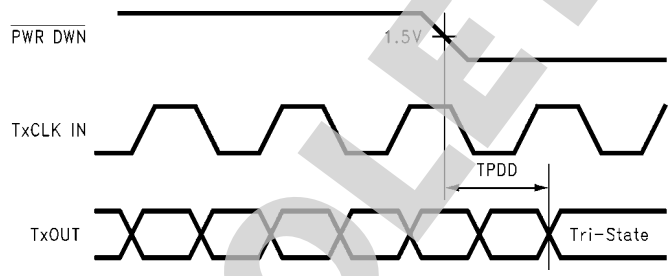


FIGURE 8. DS90CF581 (Transmitter) Phase Lock Loop Set Time



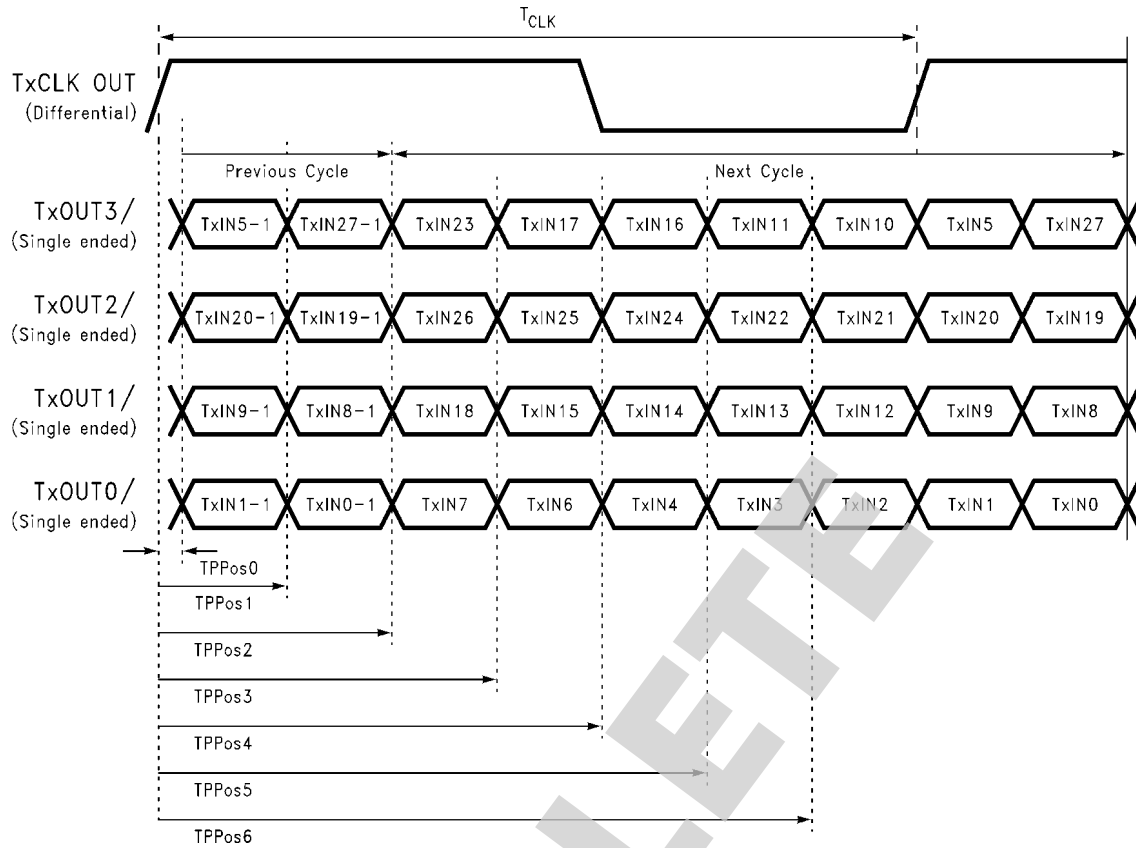
1248623

FIGURE 9. 28 Parallel TTL Data Inputs Mapped to LVDS Outputs (DS90CF581)



1248624

FIGURE 10. Transmitter Powerdown Delay



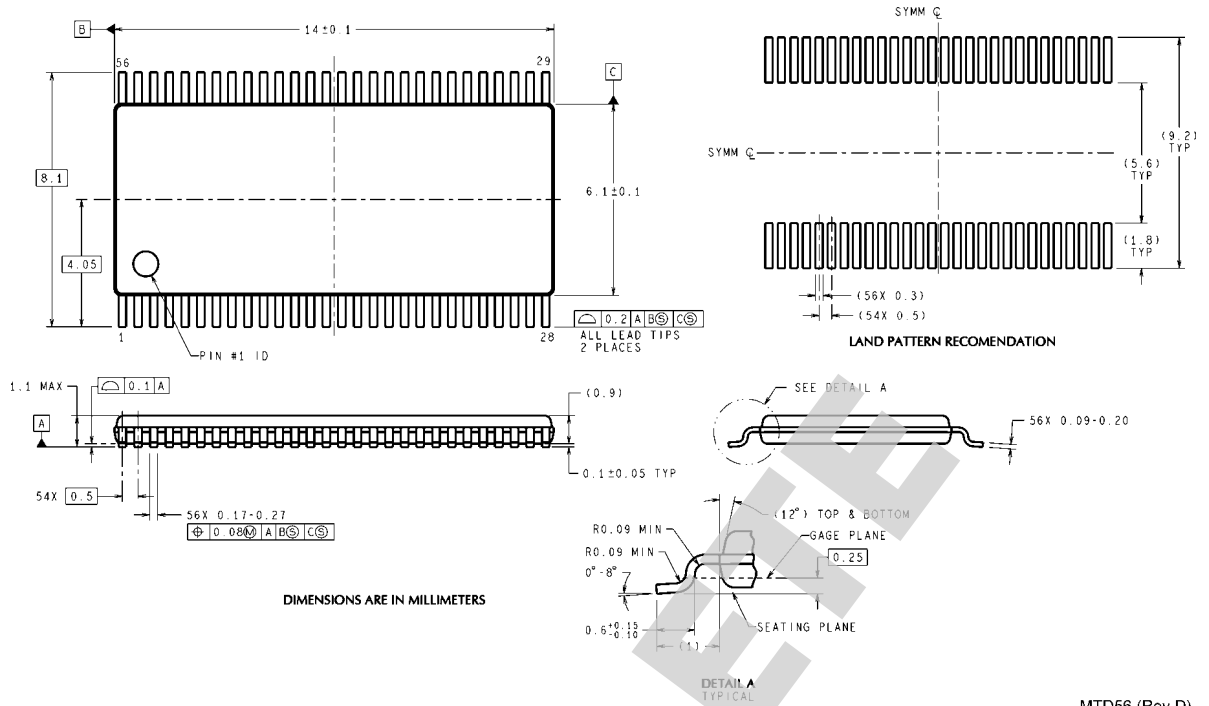
1248626

FIGURE 11. Transmitter LVDS Output Pulse Position Measurement

DS90CF581 Pin Descriptions — FPD Link Transmitter

Pin Name	I/O	No	Description
TxIN	I	28	TTL level input. This includes: 3 Red, 8 Green, 8 Blue, and 4 control lines (FPLINE, FPFRAME, DRDY, CNTL). (Also referred to as HSYNC, VSYNC and DATA ENABLE)
TxOUT+	O	4	Positive LVDS differential data output
TxOUT-	O	4	Negative LVDS differential data output
FPSHIFT IN	I	1	TTL level clock input. The falling edge acts as data strobe.
TxCLK OUT+	O	1	Positive LVDS differential clock output
TxCLK OUT-	O	1	Negative LVDS differential clock output
PWR DOWN	I	1	TTL level input. Assertion (low input) TRI-STATE the outputs, ensuring low current at power down.
V _{CC}	I	4	Power supply pins for TTL inputs
GND	I	5	Ground pins for TTL inputs
PLL V _{CC}	I	1	Power supply pin for PLL
PLL GND	I	2	Ground pins for PLL
LVDS V _{CC}	I	1	Power supply pin for LVDS outputs
LVDS GND	I	3	Ground pins for LVDS outputs

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Molded Thin Shrink Small Outline Package, JEDEC
Order Number DS90CF581MTD
NS Package Number MTD56

MTD56 (Rev D)

Notes

DS90CF581

OBSOLETE

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH® Tools	www.national.com/webench
Audio	www.national.com/audio	App Notes	www.national.com/appnotes
Clock and Timing	www.national.com/timing	Reference Designs	www.national.com/refdesigns
Data Converters	www.national.com/adc	Samples	www.national.com/samples
Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards
LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/lido	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Solutions	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempensors	SolarMagic™	www.national.com/solarmagic
Wireless (PLL/VCO)	www.national.com/wireless	PowerWise® Design University	www.national.com/training

THE CONTENTS OF THIS DOCUMENT ARE PROVIDED IN CONNECTION WITH NATIONAL SEMICONDUCTOR CORPORATION ("NATIONAL") PRODUCTS. NATIONAL MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE ACCURACY OR COMPLETENESS OF THE CONTENTS OF THIS PUBLICATION AND RESERVES THE RIGHT TO MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE. NO LICENSE, WHETHER EXPRESS, IMPLIED, ARISING BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT.

TESTING AND OTHER QUALITY CONTROLS ARE USED TO THE EXTENT NATIONAL DEEMS NECESSARY TO SUPPORT NATIONAL'S PRODUCT WARRANTY. EXCEPT WHERE MANDATED BY GOVERNMENT REQUIREMENTS, TESTING OF ALL PARAMETERS OF EACH PRODUCT IS NOT NECESSARILY PERFORMED. NATIONAL ASSUMES NO LIABILITY FOR APPLICATIONS ASSISTANCE OR BUYER PRODUCT DESIGN. BUYERS ARE RESPONSIBLE FOR THEIR PRODUCTS AND APPLICATIONS USING NATIONAL COMPONENTS. PRIOR TO USING OR DISTRIBUTING ANY PRODUCTS THAT INCLUDE NATIONAL COMPONENTS, BUYERS SHOULD PROVIDE ADEQUATE DESIGN, TESTING AND OPERATING SAFEGUARDS.

EXCEPT AS PROVIDED IN NATIONAL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, NATIONAL ASSUMES NO LIABILITY WHATSOEVER, AND NATIONAL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO THE SALE AND/OR USE OF NATIONAL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

LIFE SUPPORT POLICY


NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

National Semiconductor and the National Semiconductor logo are registered trademarks of National Semiconductor Corporation. All other brand or product names may be trademarks or registered trademarks of their respective holders.

Copyright© 2009 National Semiconductor Corporation

For the most current product information visit us at www.national.com


National Semiconductor
Americas Technical
Support Center
 Email: support@nsc.com
 Tel: 1-800-272-9959

National Semiconductor Europe
Technical Support Center
 Email: europe.support@nsc.com

National Semiconductor Asia
Pacific Technical Support Center
 Email: ap.support@nsc.com

National Semiconductor Japan
Technical Support Center
 Email: jpn.feedback@nsc.com