Winbond Electronics Corp.

100 MHZ 3-DIMM SDRAM BUFFER

1. GENERAL DESCRIPTION

The W83178S is a 13 outputs SDRAM clock buffer for 3-DIMMs models incorporate with W83196S-14 which is the clock synthesizer especially for the 100 MHz models such as Intel BX chipsets. (Refer the datasheet fo Winbond W83196S-14)

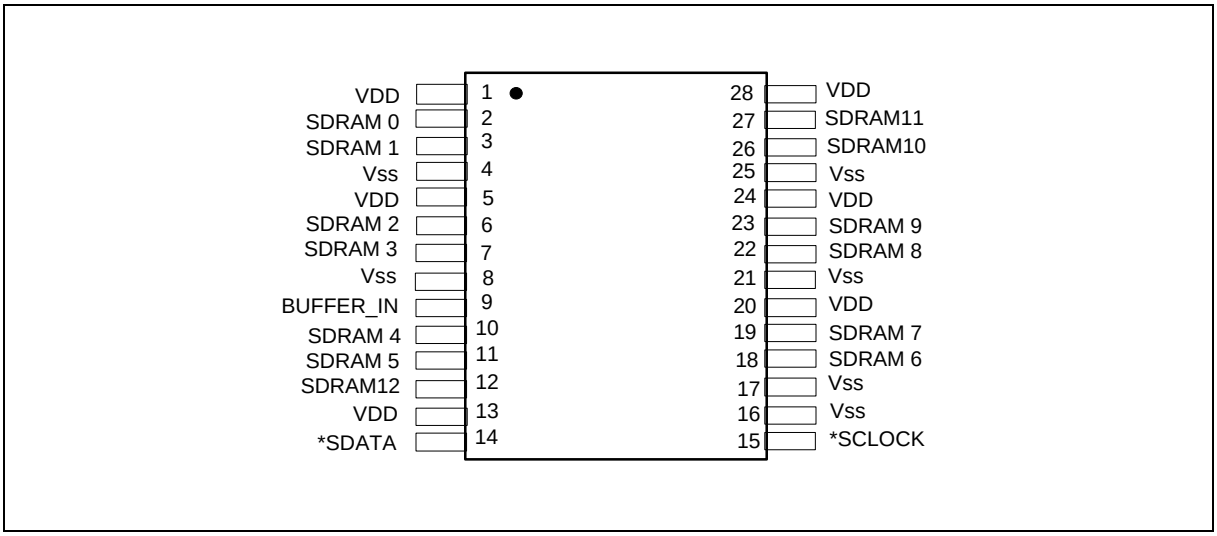
The W83178S receives the clock from chipset by the Buffer_In pin and provides almost zero-delay (less than 4 nS propagation delay) SDRAM buffer outputs for the 13 SDRAM clocks which are synchronous with the CPU clock outputs priovided by W83196S-14. The clock skew between any two clock outputs is less than 250 pS and the output buffer impedance is about 15 ohms.

The W83178S also provides I^2C serial bus interface to program the registers to enable or disable each SDRAM clock outputs.

2. FEATURES

- Supports Intel Pentium II CPUs for BX chipset
- 13 SDRAM clocks for 3-DIMMs
- Clock skew less than 250 pS
- Almost none delay Buffer-in controlling SDRAM clocks(<4 nS propagation delay)
- I^2C 2-wire serial interface
- Programmable registers to enable/stop each output
- Incorporate with W83196S-14
- Packaged in 28-pin SOP

3. PIN CONFIGURATION



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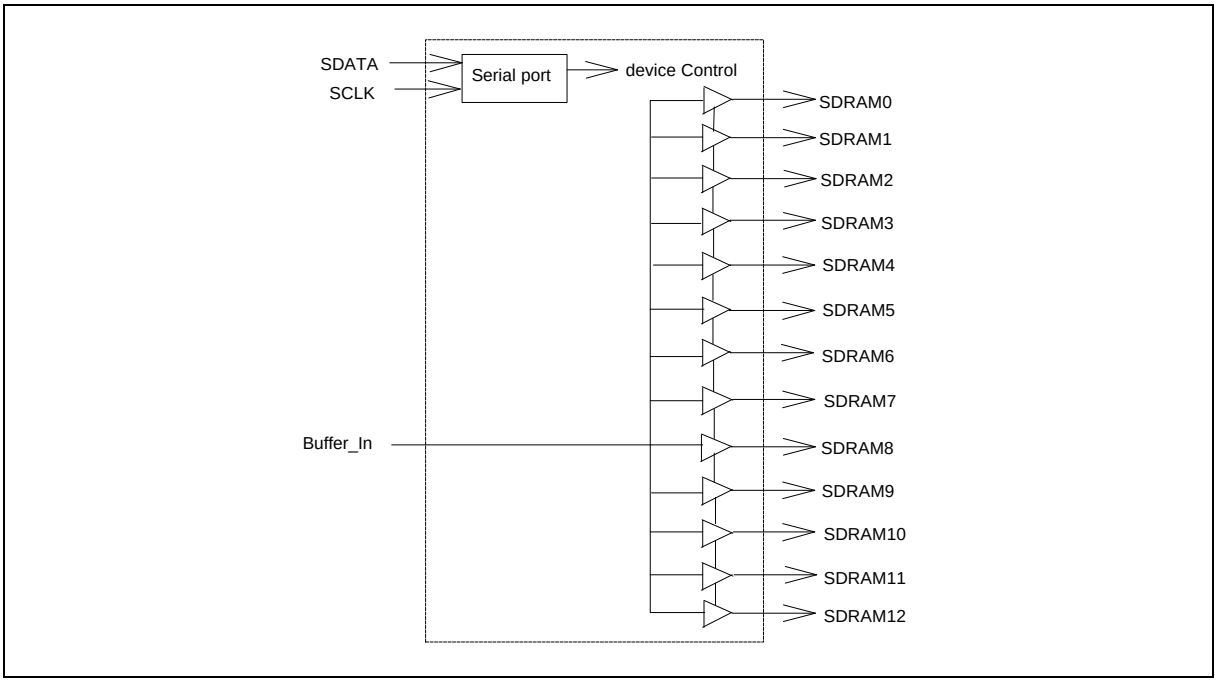
4. BLOCK DIAGRAM



5. PIN DESCRIPTION

IN - Input

OUT - Output

I/O - Bi-directional Pin

* - Internal 250K Ω pull-up

SYMBOL	PIN	I/O	FUNCTION
SDRAM [0:12]	2, 3, 6, 7, 10, 11, 12, 18, 19, 22, 23, 26, 27	O	SDRAM clock outputs which have the same frequency as CPU clocks.
*SDATA	14	I/O	Serial data of I^2C 2-wire control interface
*SDCLK	15	IN	Serial clock of I^2C 2-wire control interface
BUFFER_IN	9	IN	Clock Input from the chipset
V_{DD}	1, 5, 13, 20, 24, 28	-	Power supply
Vss	4, 8, 16, 17, 21, 25	-	Circuit ground

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6. FUNCTIONAL DESCRIPTION

6.1 2-Wire I²C Control Interface

The clock generator is a slave I2C component which can be read back the data stored in the latches for verification. All proceeding bytes must be sent to change one of the control bytes. The 2-wire control interface allows each clock output individually enabled or disabled. On power up, the W83178S initializes with default register settings, and then it's optional to use the 2-wire control interface.

The SDATA signal only changes when the SDCLK signal is low, and is stable when SDCLK is high during normal data transfer. There are only two exceptions. One is a high-to-low transition on SDATA while SDCLK is high used to indicate the beginning of a data transfer cycle. The other is a low-to-high transition on SDATA while SDCLK is high used to indicate the end of a data transfer cycle. Data is always sent as complete 8-bit bytes followed by an acknowledge generated.

Byte writing starts with a start condition followed by 7-bit slave address and [1101 0010], command code checking [0000 0000], and byte count checking. After successful reception of each byte, an acknowledge (low) on the SDATA wire will be generated by the clock chip. Controller can start to write to internal I2C registers after the string of data. The sequence order is as follows:

Bytes sequence order for I²C controller:

Clock Address A(6:0) & R/W	**Ack**	**8 bits dummy Command code**	**Ack**	**8 bits dummy Byte count**	**Ack**	**Byte0,1,2... until Stop**

Set R/W to 1 when read back the data sequence is as follows:

Clock Address A(6:0) & R/W	**Ack**	**Byte 0**	**Ack**	**Byte 1**	**Ack**	**Byte2, 3, 4... until Stop**

6.2 Serial Control Registers

The Pin column lists the affected pin number and the @PowerUp column gives the state at true power up. Registers are set to the values shown only on true power up. "Command Code" byte and "Byte Count" byte must be sent following the acknowledge of the Address Byte. Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledge. After that, the below described sequence (Register 0, Register 1, Register 2, ...) will be valid and acknowledged.

6.2.1 Register 0: (1 = Active, 0 = Inactive)

BIT	@POWERUP	PIN	DESCRIPTION
7	1	11	SDRAM5 (Active/Inactive)
6	1	10	SDRAM4 (Active/Inactive)
5	-	-	Reserved
4	-	-	Reserved
3	1	7	SDRAM3 (Active/Inactive)
2	1	6	SDRAM2 (Active/Inactive)
1	1	3	SDRAM1 (Active/Inactive)
0	1	2	SDRAM0 (Active/Inactive)

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6.2.2 Register 1: (1 = Active, 0 = Inactive)

BIT	@POWERUP	PIN	DESCRIPTION
7	1	27	SDRAM11 (Active/Inactive)
6	1	28	SDRAM10 (Active/Inactive)
5	1	23	SDRAM9 (Active/Inactive)
4	1	22	SDRAM8 (Active/Inactive)
3	1	-	Reserved
2	1	-	Reserved
1	1	19	SDRAM7 (Active/Inactive)
0	1	18	SDRAM6 (Active/Inactive)

6.2.3 Register 2: (1 = Active, 0 = Inactive)

BIT	@POWERUP	PIN	DESCRIPTION
7	x	-	Reserved
6	1	12	SDRAM12 (Active/Inactive)
5	x	-	Reserved
4	x	-	Reserved
3	x	-	Reserved
2	x	-	Reserved
1	x	-	Reserved
0	x	-	Reserved

7.0 SPECIFICATIONS

7.1 Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or V_{DD}).

PARAMETER	SYMBOL	RATING
Voltage on any pin with respect to GND	V_{DD}, V_{IN}	-0.5V to +7.0V
Storage Temperature	T_{STG}	-65° C to +150° C
Ambient Temperature	T_B	-55° C to +125° C
Operating Temperature	T_A	0° C to +70° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

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7.2 AC Characteristics

V_{DD} = 3.3V ±5 % , T_A = 0° C to +70° C, Test load = 30 pF

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Input Frequency	FIN	0		150	MHz	
Output Rise Time	TR	1.5		4.0	V/nS	Measured from 0.4V to 2.4V
Output Fall Time	TF	1.5		4.0	V/nS	Measured from 0.4V to 2.4V
Output Skew, Rising Edges	TSR			250	pS	
Output Skew, Falling Edges	TSF			250	pS	
Output Enable Time	TEN	1.0		8.0	nS	
Output Disable Time	TDIS	1.0		8.0	nS	
Rising Edge Propagation Delay	TPR	1.0		<4.0	nS	
Falling Edge Propagation Delay	TPF	1.0		<4.0	nS	
Duty Cycle	TD	45		55	%	Measure at 1.5V
AC Output Impedance	ZO		15		Ω	

7.3 DC Characteristics

V_{DD} = 3.3V ±5 %, T_A = 0° C to +70° C

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Input Low Voltage	VIL	Vss -03		0.8	V_{dc}	
Input High Voltage	VIH	2.0		VDD +0.5	V_{dc}	
Input Leakage Current, BUFFER_IN	IIL	-5		+5	µA	
Input Leakage Current	IIL	-20		+5	µA	
Output Low Voltage	VOL			50	mV_{dc}	IOL = 1 mA
Output High Voltage	VOH	3.1			V_{dc}	IOH = -1 mA
Output Low Current	IOL	65	100	160	mA	VOL = 1.5V
Output High Current	IOH	70	110	185	mA	VOH = 1.5V
Input Pin Capacitance	CIN			5	pF	
Output Pin Capacitance	COUT			6	pF	
Input Pin Inductance	LIN			7	nH	

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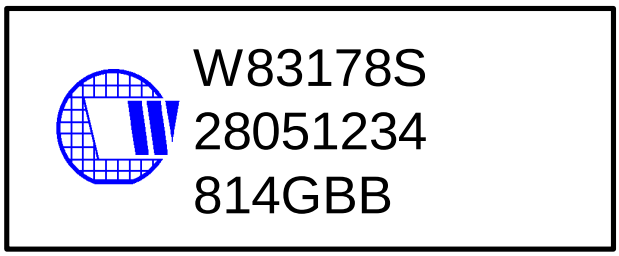
8. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83178S	28-pin SOP	Commercial, 0° C to +70° C

9. HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83178S

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 814 G B B

814: packages made in '98, week 14

G: assembly house ID; A means ASE, S means SPIL, G means GR

BB: IC revision

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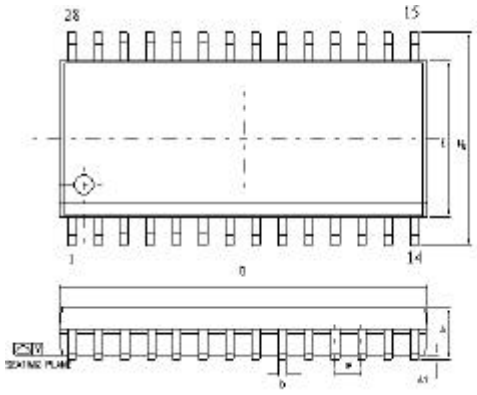
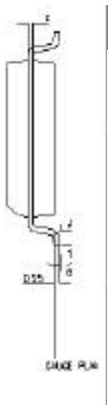
10. PACKAGE DIMENSIONS

28-pin SOP





Control demensions are in milmeters .

SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	2.35	2.65	0.093	0.104
A1	0.10	0.30	0.004	0.012
b	0.33	0.51	0.013	0.020
c	0.23	0.32	0.009	0.013
E	7.40	7.60	0.291	0.299
D	17.70	18.10	0.697	0.713
e	1.27 BSC		0.050 BSC	
H_E	10.00	10.65	0.394	0.419
Y	———	0.10	———	0.004
L	0.40	1.27	0.016	0.050
θ	0	8	0	8

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