

## Features

- Very high speed: 55 ns
- Temperature ranges
  - Industrial: -40°C to +85°C
  - Automotive-E: -40°C to +125°C
- Pin compatible with CY62137V
- Ultra low active power
  - Typical active current: 1.5 mA at f = 1 MHz
  - Typical active current: 7 mA at f = f<sub>MAX</sub> (55 ns speed)
- Low and ultra low standby power
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Available in Pb-free and non Pb-free 48-ball FBGA package

## Functional Description

The CY62137CV30/33 and CY62137CV are high-performance CMOS static RAMs organized as 128K words by 16 bits. These devices feature advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life (MoBL) in portable applications such as cellular telephones. These devices also have an automatic power down feature that significantly reduces power consumption by 80 percent when

addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99 percent when deselected; Chip Enable ( $\overline{CE}$ ) HIGH or both Byte Low Enable (BLE) and Byte High Enable (BHE) are HIGH. The input and output pins (IO<sub>0</sub> through IO<sub>15</sub>) are placed in a high-impedance state in the following conditions:

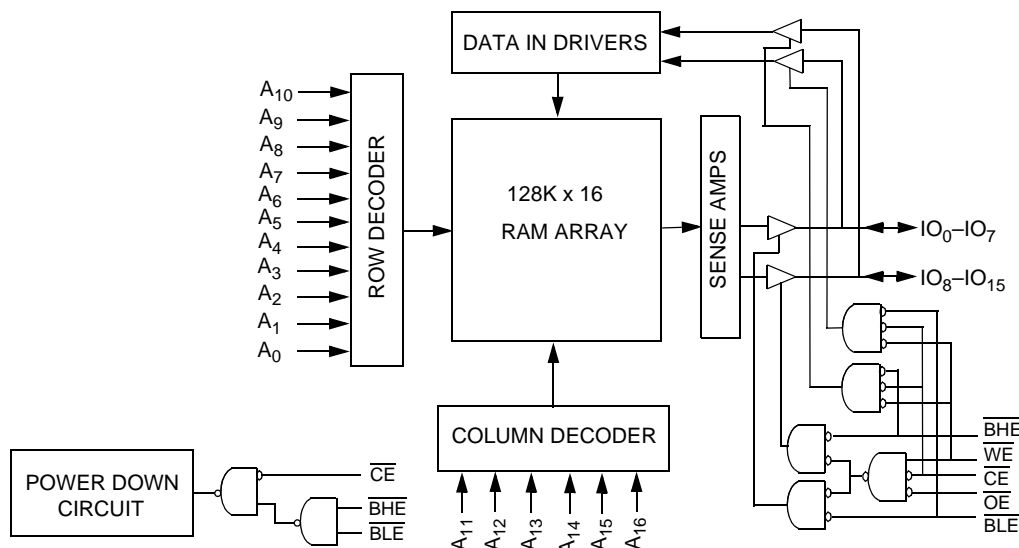
- Deselected ( $\overline{CE}$  HIGH)
- Outputs are disabled ( $\overline{OE}$  HIGH)
- Both BHE and BLE are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH)
- Write operation is active ( $\overline{CE}$  LOW and Write Enable ( $\overline{WE}$ ) LOW)

Write to the device by taking  $\overline{CE}$  and  $\overline{WE}$  inputs LOW. If  $\overline{BLE}$  is LOW, then data from the IO pins (IO<sub>0</sub> through IO<sub>7</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>). If BHE is LOW, then data from the IO pins (IO<sub>8</sub> through IO<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>).

Read from the device by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW, while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If BLE is LOW, then data from the memory location specified by the address pins appear on IO<sub>0</sub> to IO<sub>7</sub>. If BHE is LOW, then data from memory appears on IO<sub>8</sub> to IO<sub>15</sub>. See the "Truth Table" on page 10 for a complete description of read and write modes.

For best practice recommendations, refer to the Cypress application note AN1064, *SRAM System Guidelines*.

## Logic Block Diagram

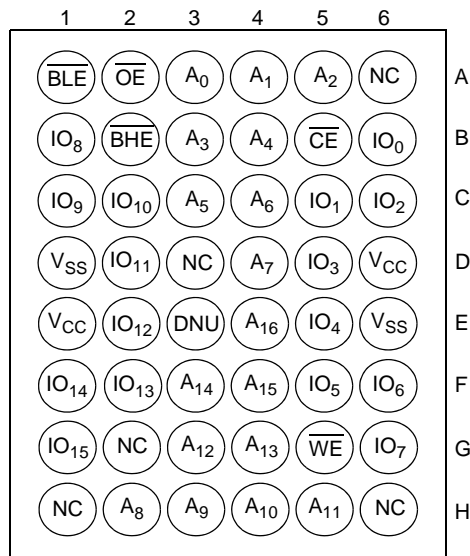


## Product Portfolio

Product	Range	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
						Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
		f = 1 MHz		f = f <sub>MAX</sub>							
		Min	Typ <sup>[1]</sup>	Max		Typ <sup>[1]</sup>	Max	Typ <sup>[1]</sup>	Max	Typ <sup>[1]</sup>	Max
CY62137CV30LL	Industrial	2.7	3.0	3.3	55	1.5	3	7	15	2	10
					70	1.5	3	5.5	12		
CY62137CV30LL	Automotive	2.7	3.0	3.3	70	1.5	3	5.5	15	2	15
CY62137CV33LL	Industrial	3.0	3.3	3.6	55	1.5	3	7	15	5	15
CY62137CVSL	Industrial	2.9	3.3	3.6	70	1.5	3	5.5	12	1	5

## Pin Configuration

Figure 1. 48-Ball FBGA Pinout [2, 3]



### Notes

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(TYP)</sub>, T<sub>A</sub> = 25°C.
2. NC pins are not connected on the die.
3. To ensure proper operation, leave floating E3 (DNU) pin or tie to V<sub>SS</sub>.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... -65°C to + 150°C

Ambient Temperature with Power Applied ..... -55°C to + 125°C

Supply Voltage to Ground Potential..... - 0.5V to  $V_{CC(Max)}$  + 0.5V

DC Voltage Applied to Outputs in High-Z State <sup>[4]</sup>..... -0.5V to  $V_{CC}$  + 0.3V

DC Input Voltage <sup>[4]</sup>..... -0.5V to  $V_{CC}$  + 0.3V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V (MIL-STD-883, Method 3015)

Latch up Current ..... > 200 m

## Operating Range

Device	Range	Ambient Temperature	V <sub>CC</sub>
CY62137CV30	Industrial	-40°C to +85°C	2.7V to 3.3V
CY62137CV33			3.0V to 3.6V
CY62137CV			2.9V to 3.6V
CY62137CV30	Automotive	-40°C to +125°C	2.7V to 3.3V

## Electrical Characteristics

Over the operating range

Parameter	Description	Test Conditions	CY62137CV30-55			CY62137CV30-70			Unit	
			Min	Typ <sup>[1]</sup>	Max	Min	Typ <sup>[1]</sup>	Max		
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -1.0 mA	2.4			2.4			V	
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA			0.4			0.4	V	
V <sub>IH</sub>	Input HIGH Voltage		2.2		V <sub>CC</sub> +0.3	2.2		V <sub>CC</sub> +0.3	V	
V <sub>IL</sub>	Input LOW Voltage		-0.3		0.8	-0.3		0.8	V	
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	Ind'l	-1	+1	-1		+1	μA	
			Auto			-2		+2		
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , output disabled	Ind'l	-1	+1	-1		+1	μA	
			Auto			-2		+2		
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	V <sub>CC</sub> = V <sub>CC(Max)</sub> I <sub>OUT</sub> = 0 mA CMOS levels	Ind'l	7	15		5.5	12	mA
				Auto				5.5	15	
		f = 1 MHz	Ind'l	1.5	3		1.5	3		
			Auto				1.5	3		
I <sub>SB1</sub>	Automatic CE Power Down Current – CMOS Inputs	CE ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V f = f <sub>MAX</sub> (address and data only), f = 0 (OE, WE, BHE, and BLE),	Ind'l	2	10		2	10	μA	
			Auto				2	15		
I <sub>SB2</sub>	Automatic CE Power Down Current – CMOS Inputs	CE ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0, V <sub>CC</sub> = 3.3V	Ind'l	2	10		2	10	μA	
			Auto				2	15		

### Note

4. V<sub>IL(Min)</sub> = -2.0V for pulse durations less than 20 ns.

## Electrical Characteristics (Continued)

Over the operating range

Parameter	Description	Test Conditions		CY62137CV33-55			CY62137CV-70			Unit
				Min	Typ <sup>[1]</sup>	Max	Min	Typ <sup>[1]</sup>	Max	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -1.0 mA	V <sub>CC</sub> = 3.0V	2.4			2.4			V
			V <sub>CC</sub> = 2.9V				2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA	V <sub>CC</sub> = 3.0V			0.4			0.4	V
			V <sub>CC</sub> = 2.9V						0.4	V
V <sub>IH</sub>	Input HIGH Voltage			2.2		V <sub>CC</sub> + 0.3	2.2		V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage			-0.3		0.8	-0.3		0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		-1		+1	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , output disabled		-1		+1	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub> f = 1 MHz	V <sub>CC</sub> = V <sub>CC(Max)</sub> I <sub>OUT</sub> = 0 mA CMOS levels		7	15		5.5	12	mA
					1.5	3		1.5	3	
I <sub>SB1</sub>	Automatic CE Power Down Current – CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ $f = f_{MAX}$ (address and data only), $f = 0$ ( $\overline{OE}$ , $\overline{WE}$ , $\overline{BHE}$ , and $\overline{BLE}$ ),			5	15		5	15	μA
I <sub>SB2</sub>	Automatic CE Power Down Current – CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = 0$ , V <sub>CC</sub> = 3.6V		LL		5	15			μA
				SL					1	

## Capacitance

Tested initially and after any design or process changes that may affect these parameters

Parameter	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz,	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = V <sub>CC(TYP)</sub>		

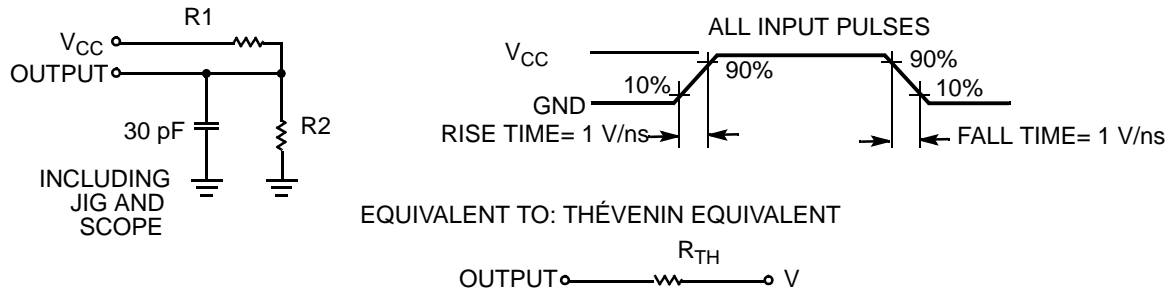
## Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters

Parameter	Description	Test Conditions	FBGA	Unit
θ <sub>JA</sub>	Thermal Resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two layer printed circuit board	55	°C/W
θ <sub>JC</sub>	Thermal Resistance (junction to case)		16	°C/W

## AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveform



Parameters	3.0V	3.3V	Unit
R1	1105	1216	Ω
R2	1550	1374	Ω
R <sub>TH</sub>	645	645	Ω
V <sub>TH</sub>	1.75	1.75	V

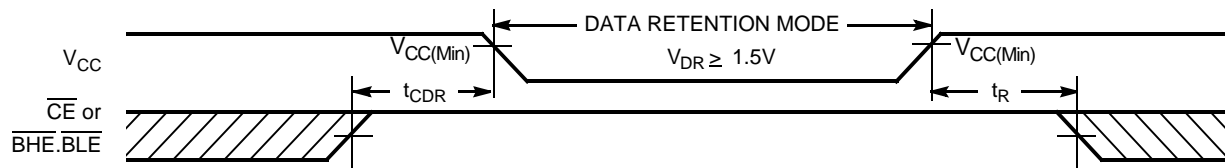
## Data Retention Characteristics

Over the operating range

Parameter	Description	Conditions		Min	Typ <sup>[1]</sup>	Max	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention			1.5			V
I <sub>CCDR</sub>	Data Retention Current	V <sub>CC</sub> = 1.5V, CE ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V	LL Ind'l Auto SL Ind'l		1	6 8 4	μA
t <sub>CDR</sub> <sup>[5]</sup>	Chip Deselect to Data Retention Time			0			ns
t <sub>R</sub> <sup>[6]</sup>	Operation Recovery Time			t <sub>RC</sub>			ns

## Data Retention Waveform

Figure 3. Data Retention Waveform<sup>[7]</sup>



### Notes

5. Tested initially and after any design or process changes that may affect these parameters.
6. Full device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(Min)</sub> > 100 μs or stable at V<sub>CC(Min)</sub> > 100 μs.
7. BHE, BLE is the AND of BHE and BLE. Deselect the chip by either disabling chip enable signals or by disabling  $\overline{\text{BHE}}$  and  $\overline{\text{BLE}}$ .

## Switching Characteristics

 Over the operating range <sup>[8]</sup>

Parameter	Description	55 ns		70 ns		Unit
		Min	Max	Min	Max	
<b>Read Cycle</b>						
t <sub>RC</sub>	Read Cycle Time	55		70		ns
t <sub>AA</sub>	Address to Data Valid		55		70	ns
t <sub>OHA</sub>	Data Hold From Address Change	10		10		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		55		70	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		25		35	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low-Z <sup>[9]</sup>	5		5		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High-Z <sup>[9, 10]</sup>		20		25	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low-Z <sup>[9]</sup>	10		10		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High-Z <sup>[9, 10]</sup>		20		25	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power Up	0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power Down		55		70	ns
t <sub>DBE</sub>	$\overline{BLE}/\overline{BHE}$ LOW to Data Valid		55		70	ns
t <sub>LZBE</sub>	$\overline{BLE}/\overline{BHE}$ LOW to Low-Z <sup>[9, 11]</sup>	5		5		ns
t <sub>HZBE</sub>	$\overline{BLE}/\overline{BHE}$ HIGH to High-Z <sup>[9, 10]</sup>		20		25	ns
<b>Write Cycle <sup>[12]</sup></b>						
t <sub>WC</sub>	Write Cycle Time	55		70		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	45		60		ns
t <sub>AW</sub>	Address Setup to Write End	45		60		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Setup to Write Start	0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	40		45		ns
t <sub>BW</sub>	$\overline{BLE}/\overline{BHE}$ LOW to Write End	50		60		ns
t <sub>SD</sub>	Data Setup to Write End	25		30		ns
t <sub>HD</sub>	Data Hold From Write End	0		0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High-Z <sup>[9, 10]</sup>		20		25	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low-Z <sup>[9]</sup>	10		10		ns

### Notes

8. Test conditions assume signal transition time of 5 ns or less, timing reference levels of  $V_{CC(Typ)}/2$ , input pulse levels of 0 to  $V_{CC(Typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  and 30 pF load capacitance.
9. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZBE</sub> is less than t<sub>LZBE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
10. t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZBE</sub>, and t<sub>HZWE</sub> transitions are measured when the output enters a high-impedance state.
11. If both byte enables are toggled together, this value is 10 ns.
12. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$ , and/or  $\overline{BLE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing are referenced to the edge of the signal that terminates the write.

## Switching Waveforms

Figure 4. Read Cycle 1: Address Transition Controlled [13, 14]

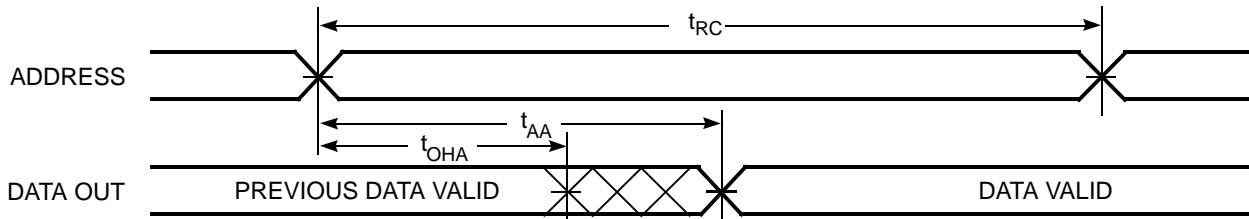
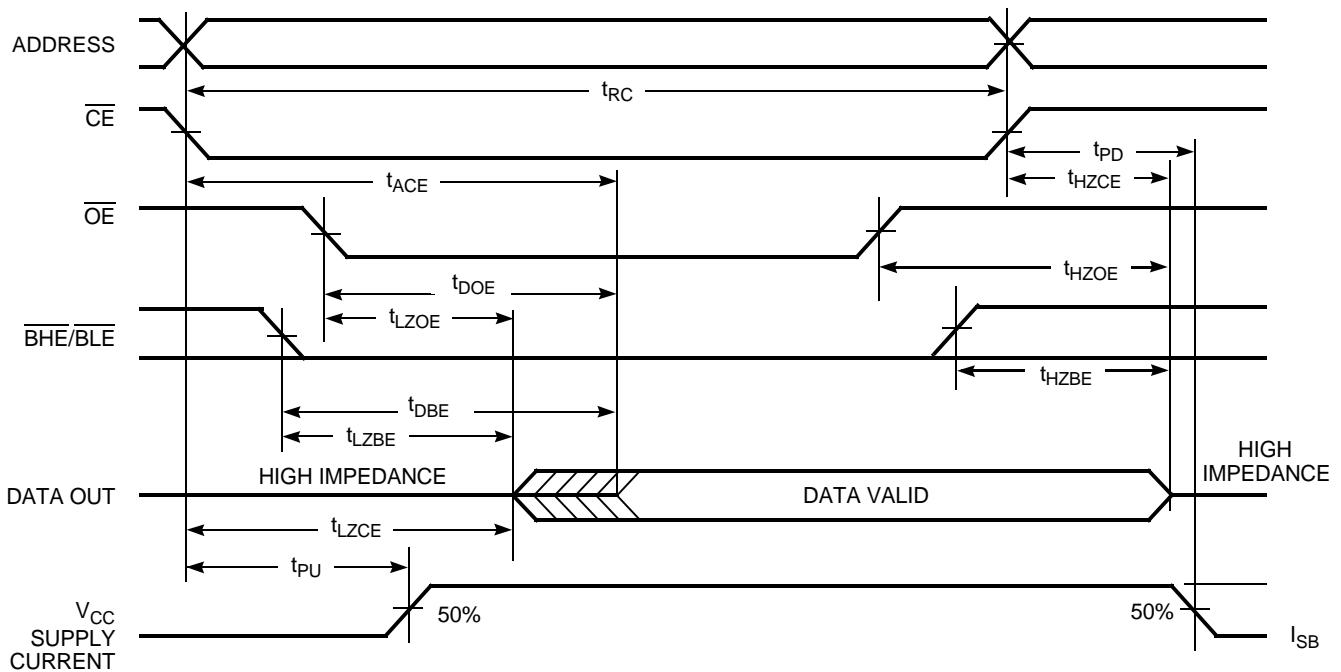


Figure 5. Read Cycle 2:  $\overline{OE}$  Controlled [14, 15]



### Notes

13. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ .
14.  $\overline{WE}$  is HIGH for read cycle.
15. Address valid before or similar to  $\overline{CE}$  and  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW.

Switching Waveforms (continued)

Figure 6. Write Cycle 1:  $\overline{WE}$  Controlled [12, 16, 17]

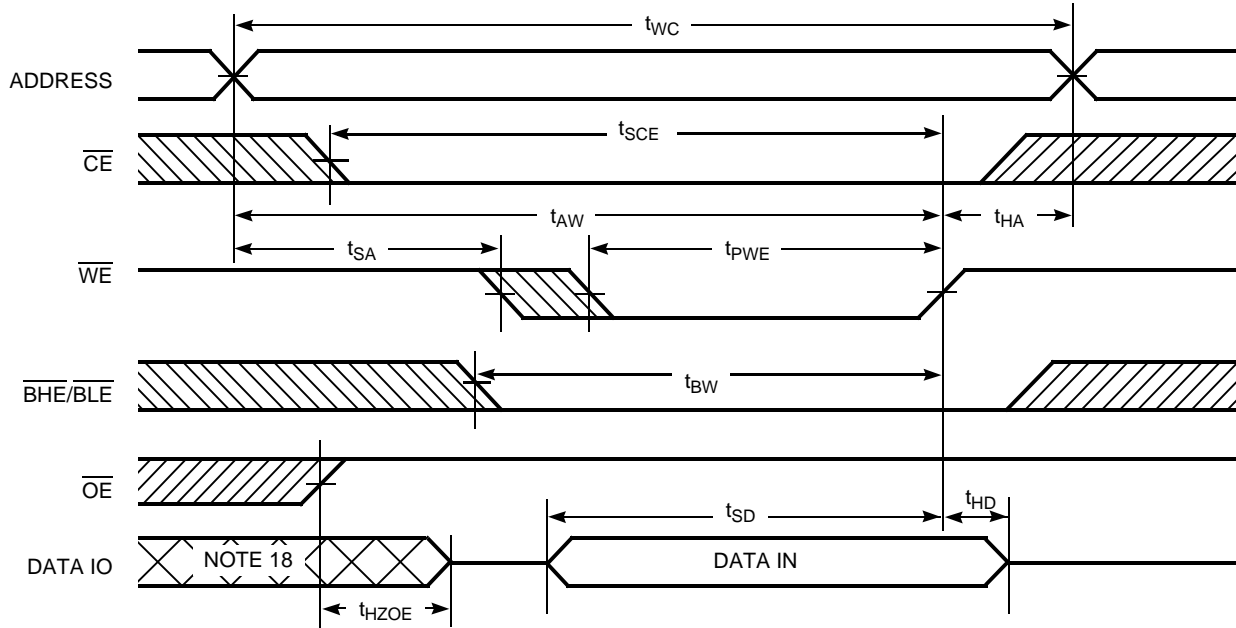
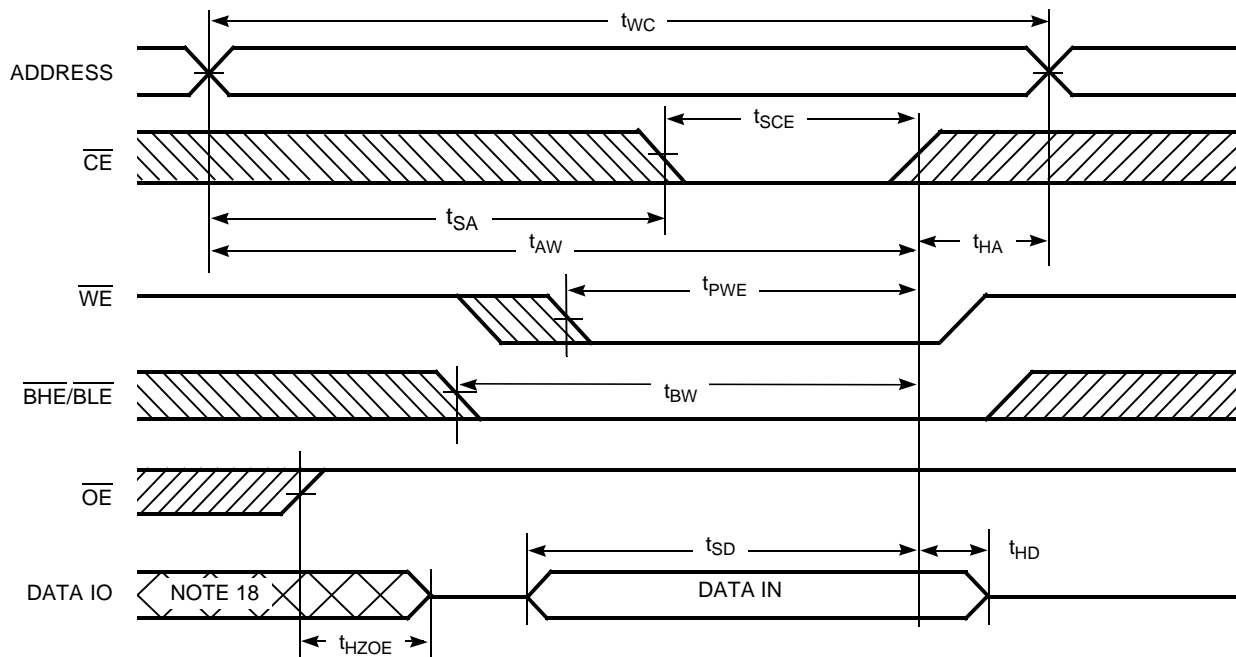


Figure 7. Write Cycle 2:  $\overline{CE}$  Controlled [12, 16, 17]



Notes

- 16. Data IO is high impedance if  $\overline{OE} = V_{IH}$ .
- 17. If  $\overline{CE}$  goes HIGH simultaneously with  $WE = V_{IH}$ , the output remains in a high-impedance state.
- 18. During this period, the IOs are in an output state. Do not apply input signals.



Switching Waveforms (continued)

Figure 8. Write Cycle 3:  $\overline{WE}$  Controlled,  $\overline{OE}$  LOW [17]

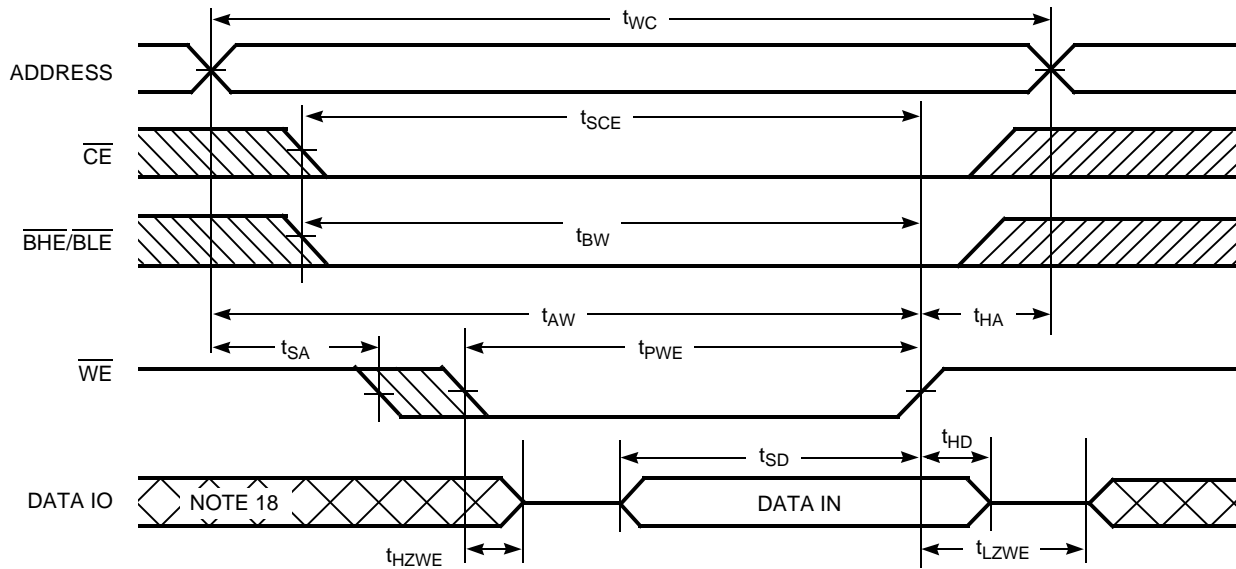
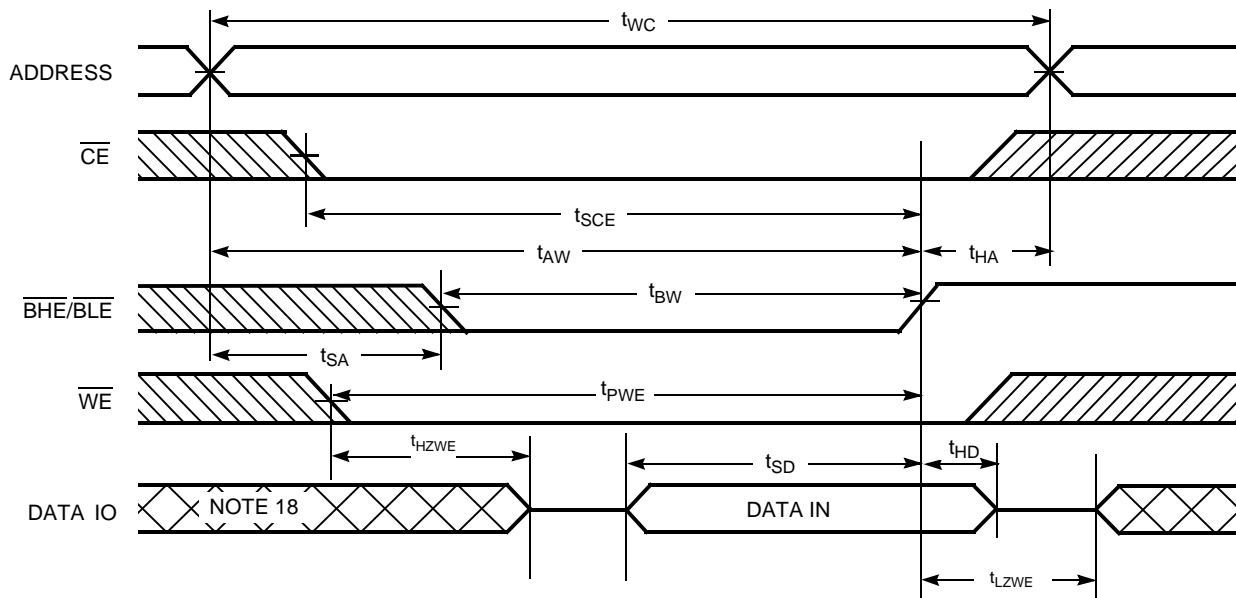


Figure 9. Write Cycle 4:  $\overline{BHE/BLE}$  Controlled,  $\overline{OE}$  LOW [17]



### Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs or Outputs	Mode	Power
H	X	X	X	X	High-Z	Deselect or Power Down	Standby ( $I_{SB}$ )
X	X	X	H	H	High-Z	Deselect or Power Down	Standby ( $I_{SB}$ )
L	H	L	L	L	Data Out ( $IO_0$ – $IO_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	L	H	L	Data Out ( $IO_0$ – $IO_7$ ); $IO_8$ – $IO_{15}$ in High-Z	Read	Active ( $I_{CC}$ )
L	H	L	L	H	Data Out ( $IO_8$ – $IO_{15}$ ); $IO_0$ – $IO_7$ in High-Z	Read	Active ( $I_{CC}$ )
L	H	H	L	L	High-Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	L	High-Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	L	H	High-Z	Output Disabled	Active ( $I_{CC}$ )
L	L	X	L	L	Data In ( $IO_0$ – $IO_{15}$ )	Write	Active ( $I_{CC}$ )
L	L	X	H	L	Data In ( $IO_0$ – $IO_7$ ); $IO_8$ – $IO_{15}$ in High-Z	Write	Active ( $I_{CC}$ )
L	L	X	L	H	Data In ( $IO_8$ – $IO_{15}$ ); $IO_0$ – $IO_7$ in High-Z	Write	Active ( $I_{CC}$ )

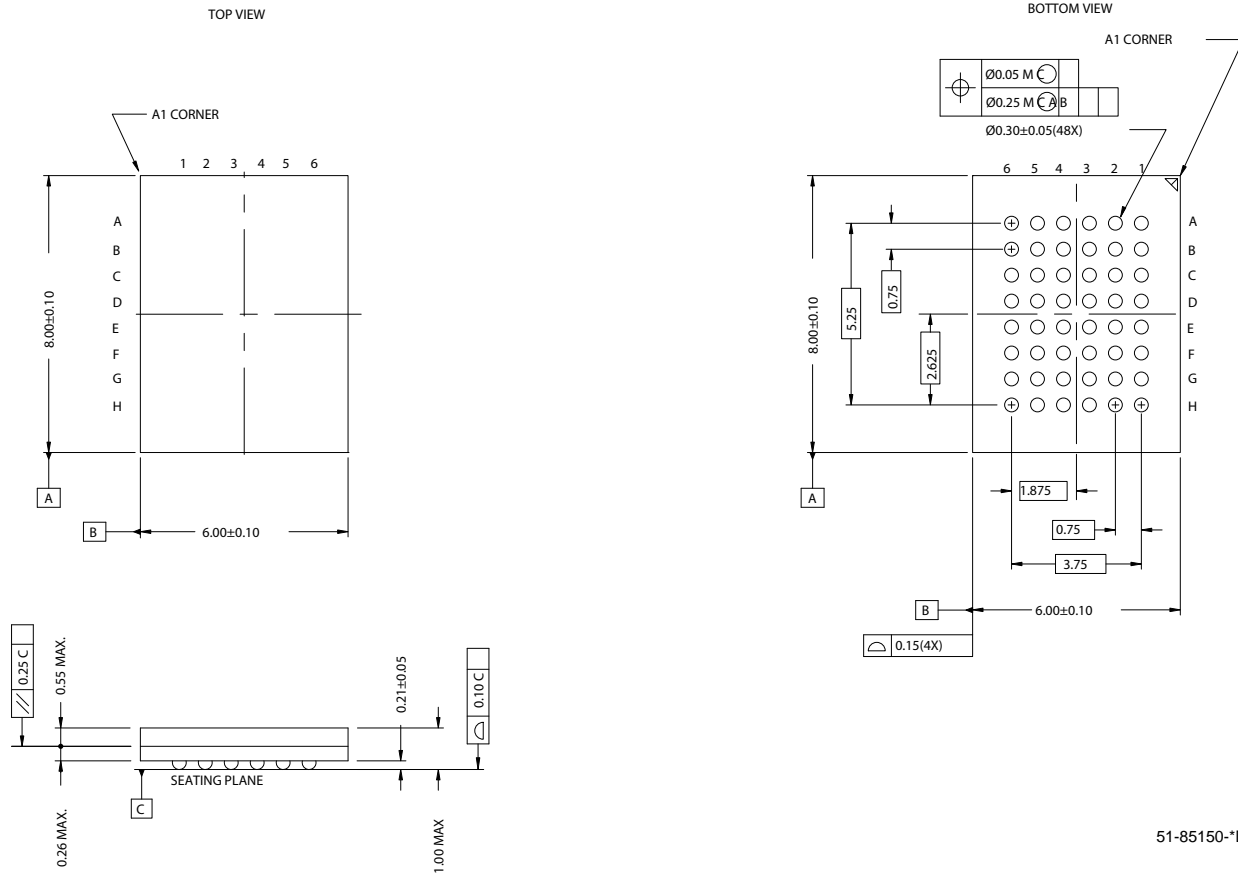
### Ordering Information

Contact your local Cypress sales representative for availability of these parts

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62137CV30LL-55BVI	51-85150	48-ball FBGA (6 x 8 x 1 mm)	Industrial
	CY62137CV30LL-55BVXI		48-ball FBGA (6 x 8 x 1 mm), Pb-free	
	CY62137CV33LL-55BVI		48-ball FBGA (6 x 8 x 1 mm)	
70	CY62137CV30LL-70BAI	51-85096	48-ball FBGA (7 x 7 x 1.2 mm)	Industrial
	CY62137CV30LL-70BVI	51-85150	48-ball FBGA (6 x 8 x 1 mm)	
	CY62137CVSL-70BAI	51-85096	48-ball FBGA (7 x 7 x 1.2 mm)	
	CY62137CVSL-70BAXI		48-ball FBGA (7 x 7 x 1.2 mm), Pb-free	
	CY62137CV30LL-70BAE	51-85096	48-ball FBGA (7 x 7 x 1.2 mm)	Automotive
	CY62137CV30LL-70BVE	51-85150	48-ball FBGA (6 x 8 x 1 mm)	
	CY62137CV30LL-70BVXE		48-ball FBGA (6 x 8 x 1 mm), Pb-free	

## Package Diagrams

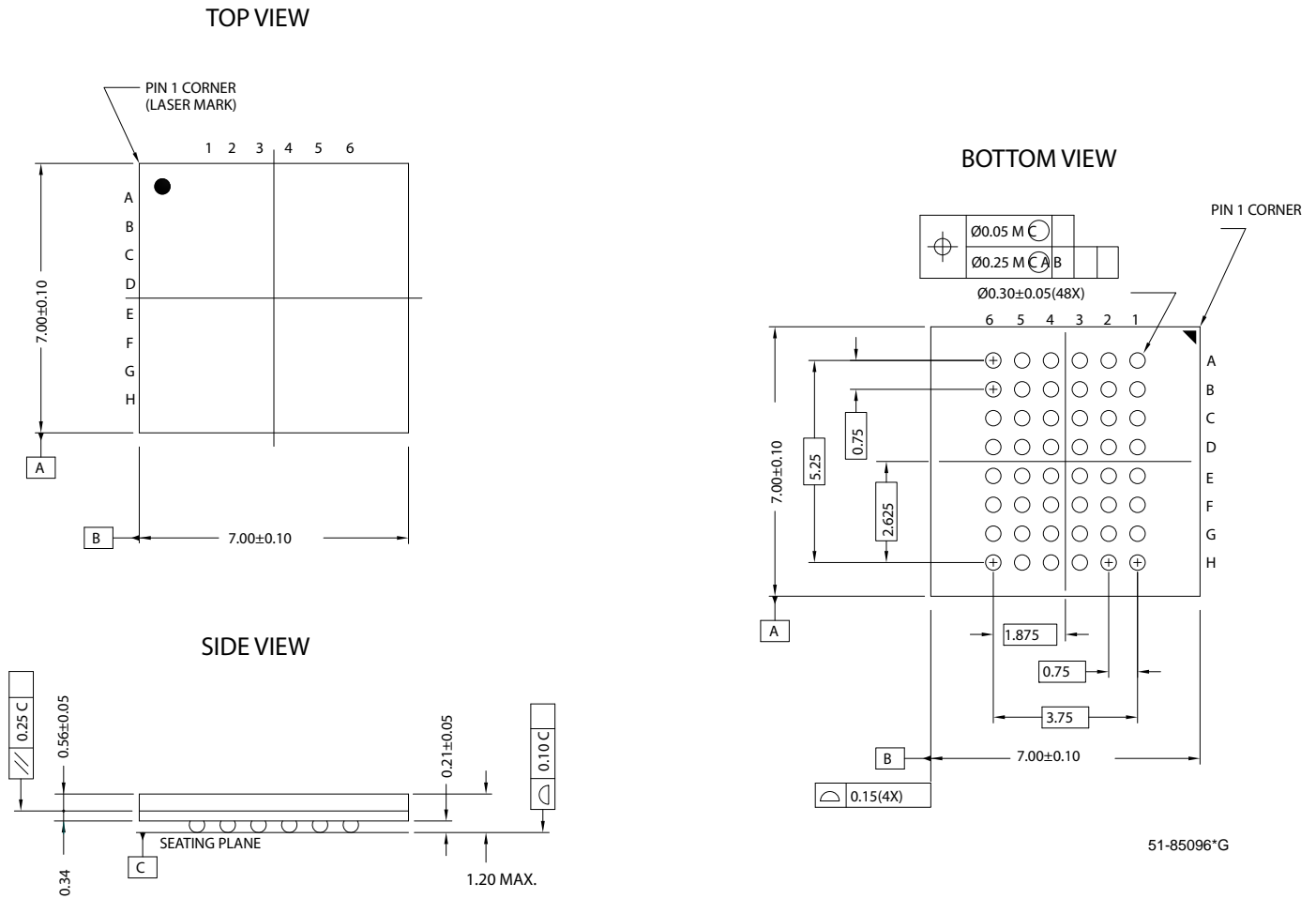
Figure 10. 48-Ball FBGA (6 x 8 x 1 mm)



51-85150-D

**Package Diagrams** (continued)

**Figure 11. 48-Ball FBGA (7 x 7 x 1.2 mm)**



## Document History Page

Document Title: CY62137CV30/33 MoBL® and CY62137CV MoBL 2-Mbit (128K x 16) Static RAM Document Number: 38-05201				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	112393	02/19/02	GAV	New Data Sheet (advance information)
*A	114015	04/25/02	JUI	Added BV package diagram Changed from Advance Information to Preliminary
*B	117064	07/12/02	MGN	Changed from Preliminary to Final
*C	118122	09/10/02	MGN	Added new part number: CY62137CV with wider voltage (2.7V – 3.6V) Added new SL power bin for new part number For T <sub>AA</sub> = 55 ns, improved t <sub>PWE</sub> min from 45 ns to 40 ns For T <sub>AA</sub> = 70 ns, improved t <sub>PWE</sub> min from 50 ns to 45 ns For T <sub>AA</sub> = 70 ns, improved t <sub>LZWE</sub> min from 5 ns to 10 ns
*D	118761	09/23/02	MGN	Improved Typ I <sub>CC</sub> spec to 7 mA (for 55 ns) and 5.5 mA (for 70 ns) Improved Max I <sub>CC</sub> spec to 15 mA (for 55 ns) and 12 mA (for 70 ns) For T <sub>AA</sub> = 55 ns, improved t <sub>LZWE</sub> min from 5 ns to 10 ns Changed upper spec for Supply Voltage to Ground Potential to V <sub>CC(Max)</sub> + 0.5V Changed upper spec. for DC Voltage Applied to Outputs in High-Z State and DC Input Voltage to V <sub>CC</sub> + 0.3V
*E	343877	See ECN	PCI	Added Automotive Information in Operating Range, DC, and Ordering Information Table
*F	419237	See ECN	ZSD	Changed the address of Cypress Semiconductor Corporation on Page 1 from “3901 North First Street” to “198 Champion Court” Updated the ordering information table and replaced the Package name column with Package diagram
*G	486789	See ECN	VKN	Removed part number CY62137CV25 from the product offering Updated the ordering information table
*H	1665045	See ECN	VKN/SFV	Changed V <sub>CC</sub> range for CY7C62137CV from 2.7–3.6V to 2.9–3.6V

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