21554 PCI-to-PCI Non-Transparent Bridge Evaluation Board

User's Guide

January 2001

Order Number: 273475-001

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Introduction 1

This document describes the 21554 PCI-to-PCI nontransparent Bridge Evaluation Board (referred to as the DE1B55401).

1.1 Overview

The DE1B55401 is a PCI expansion board that is used to evaluate the operation of the 21554 when used as a gateway to an intelligent subsystem. The subsystem can use a variety of PCI devices and local processors. The DE1B55401 can be used to perform the following functions:

- Develop initialization code to configure the 21554 and associated logic and devices on the local PCI bus as a intelligent controller
- Evaluate the operation of the 21554 with a variety of PCI devices configured in an intelligent subsystem.
- Build and evaluate a system using synchronous and asynchronous clocking
- Testing of features such as:
  - — I^2O* transactions
  - — Power management features
  - — Vital Product Data (VPD) support

1.2 Features

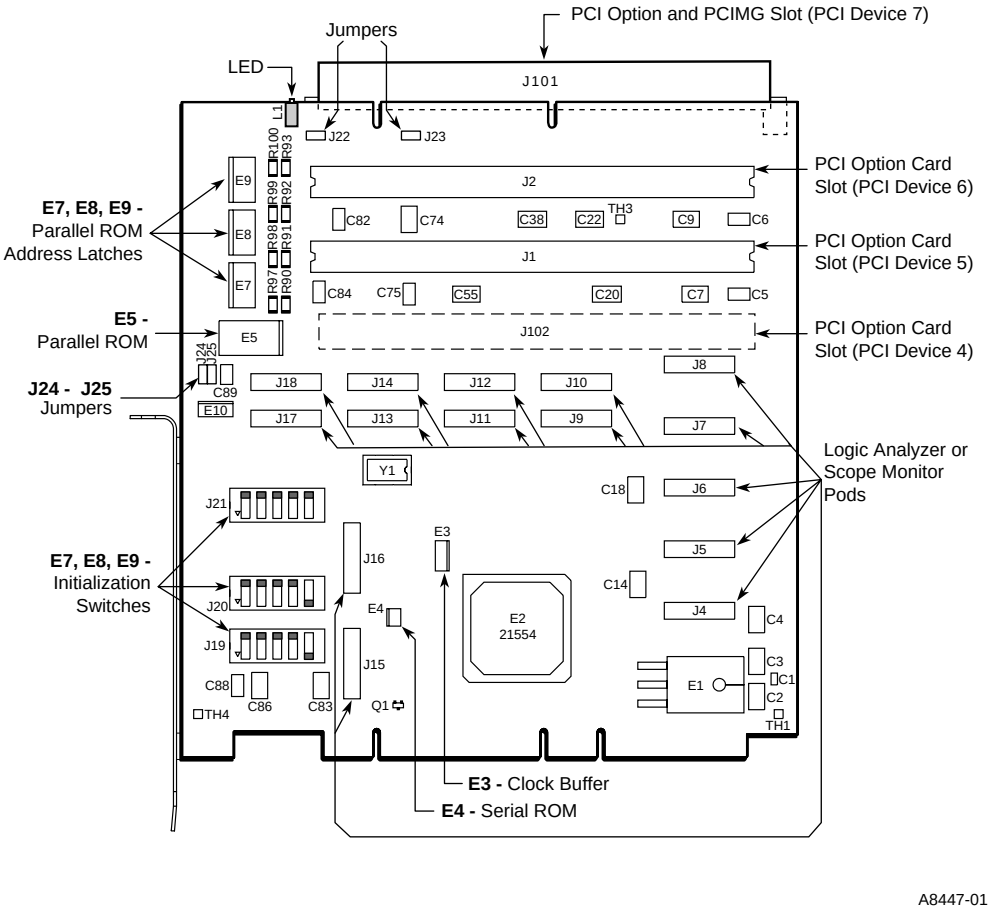
The DE1B55401 has the following features:

- Complies fully with the protocol and electrical standards of Revision 2.2 of the PCI Local Bus Specification.
- Includes a 21554 “nontransparent” PCI-to-PCI Bridge that provides bridging between two processor domains.
- Includes a host PCI interface that plugs into any 5V PCI option card slot.
- Provides four local bus 5V PCI bus option card slots. One slot may be used as a local processor or system slot.
- Support, products, and documentation.

1.3 Major Components

Figure 1-1 shows the major components on the DE1B55401.

Figure 1-1. Major Components



1.3.1 Local or Secondary Bus Connectors

J1, J2, J101, and J102 are the local PCI option slots. The top slot (J101) is also capable of becoming the local processor with the insertion of a PICMG Single Board Computer. It is the PCI portion of the PCI-ISA card edge connector. All connectors are 64-bit. See Section 1.8, “Local Bus Slot Numbering and IDSEL Mapping” on page 1-12.

1.3.2 Test Point Pods

The DE1B55401's 64 test points are presented in 16-pin pods, which are header type connectors. Each pod contains eight (8) individual test point pairs. There are 15 pods on the board. The pods are arranged on the board in three groups:

- The J4, J5, J6, J7, and J8 pods are the PCI 64-bit extension signals.
- The J9, J10, J11, J12, J13, J14, J17, and J18 pods are the control, address and data, and clock signals for the secondary PCI bus.
- The J15 and J16 pods are the parallel ROM data and address lines.

1.3.3 Jumpers

- J22, J23, J24, and J25 can have mechanical jumpers installed. They control ROM and socket enabling. See Section 1.5.
- Zero-ohm resistors must me soldered on or off the board to configure the clock and clamping options. See Section 1.6 and Section 1.7.

1.3.4 Switch Packs

J19, J20, and J21 control the options at power up, the direction of the REQ# and GNT# lines, and the on-board parallel ROM functions. See Section 1.4, Chapter 2, and Chapter 3.

1.3.5 Devices

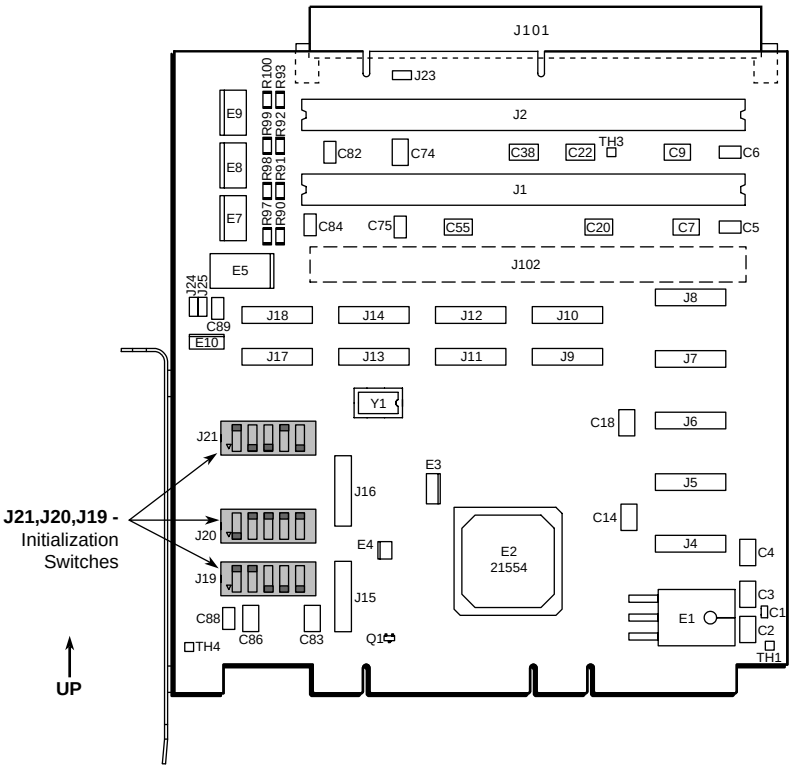
- E1 is a voltage regulator which generates 3.3V **s_vio**. See Section 1.7.
- E2 is the 21554 PCI-to-PCI Bridge IC.
- E3 is a clock buffer IC.
- E4 is the serial ROM.
- E5 is the parallel ROM and E7, E8, and E9 are address latches for the parallel ROM.
- E6 is an empty external ROM socket that is mounted the reverse side of the board behind the address latches. This socket can be used to attach a ROM emulator.
- Y1 is a 33.333 MHz crystal oscillator that can be used for an independent local clock signal.
- L1 is a LED indicator that shows the LOO bit (LED On or Off bit) which is switched through software. This LED can light if jumper J22 is installed.

1.4 Switch Settings

There are three 5-switch switch packs on the DE1B55401. Each switch is single-pole, double throw. The switche packs are in dual-in-line (DIP) packages designated J19, J20, and J21. The switches are identified as SW1 through SW5.

Figure 1-2 shows the locations of the switches and Table 1-1 is a high level description of their operation. Further details on the operation of these switches can be found in Section 3.

Figure 1-2. Switches



A8448-01

Table 1-1 describes operation of the switches. The switches should be set before powering up the system.

- The up position means switch points toward the local sockets.
- Down means the switch points toward the card edge.

Table 1-1. DIP Switch Operation

Switch Pack	Switch	Description	Reference
J19	SW1	Arbiter Control	Table 2-2
	SW3-4	Controls **pr_cs** for MDE operation	
	SW5	Controls Local Clock Divide	
J20	SW-1	Controls **pr_ad2** for SROM operation	Table 2-1, Table 3-4
	SW-2	Controls **pr_ad3** for lockout bit control	
	SW-3	Controls **pr_ad4** For Synchronous/Asynchronous clocking	Table 3-5
	SW-4	Controls **pr_ad5** for **s_clko** operation	
	SW-5	Controls **pr_ad6** for Central function selection	Table 3-3
J21	SW1-5	Controls the REQ/GNT lines for Arbiter control	Table 3-3 and Table 3-4

1.5 Stake-Pin Jumpers

In addition to clock selection and routing the DE1B55401 provides stake-pin jumpers for selecting special features. The jumpers can be used for debugging and for evaluating the special features. Table 1-2 shows the configuration jumpers and the jumper function.

Table 1-2. Jumper Connections

Jumpers	Function
J22	When installed, it enable **l_stat** pull-up resistor for Hot-Swap Functionality testing and enables operation of LED1.
J23	When installed, **s_ad<24>** is IDSEL when J101 is a PCI Option slot. When not installed, pin A26 is GNT2 from the local processor.
J24	Enables **pr_cs** control of the flash ROM's **CE.** See Table 2-2 on page 2-3.
J25	Enables **pr_cs** control of the socket ROM's **CE.**

1.6 Clock Configuration

Figure 1-3 shows the location of the zero-ohm jumper resistors that control the clock and clamping voltages.

Note: The signals **p_clk** and **s_clk_o** are not wired to scope pod positions for improved signal integrity. Table 1-3 gives the configuration for viewing these signals, if needed.

Figure 1-3. Zero-Ohm Resistor Jumpers

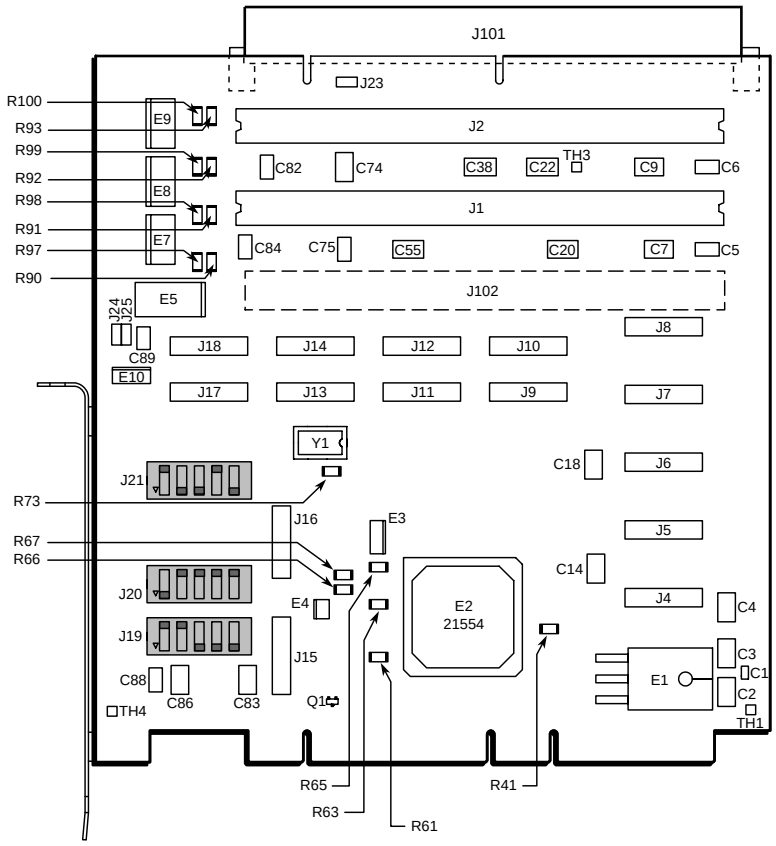


Table 1-3 shows the connections required to allow observation of these signals at scope pod connector pins and shows the resistors and jumpers needed to configure the clocks.

Table 1-3. Clock Configuration Jumpers

Function	Installed	Removed
Connects **p_clk** to test pod J18 pin 9.	R61[a]	R61
21554 **s_clk_o** as local clock.	R65, R66	R67, R73
Output of clock buffer as **s_clk_i.**	R66	R67
System slot drives **s_clk_i** on the 21554.	R67	R66
Use Oscillator as asynchronous local clock.	R73	R65, R67
System slot provides the local clock.	R90, R91, R92, R93	R97, R98, R99, 100
Clock buffer provides the local clock.	R97, R98, R99, R100	R90, R91, R92, R93

a. Install for test purposes only. Remove for normal operation.

1.7 Clamping Voltage

Table 1-4 shows the configuration of resistor jumpers needed for a specific **s_ vio** voltage. These jumper resistors designate the secondary bus as a 3.3V or a 5V PCI device. A mix of 3.3 and 5 V cards is not allowed. Figure 1-3 shows the location of the resistor jumpers.

Table 1-4. Voltage Clamp[a]

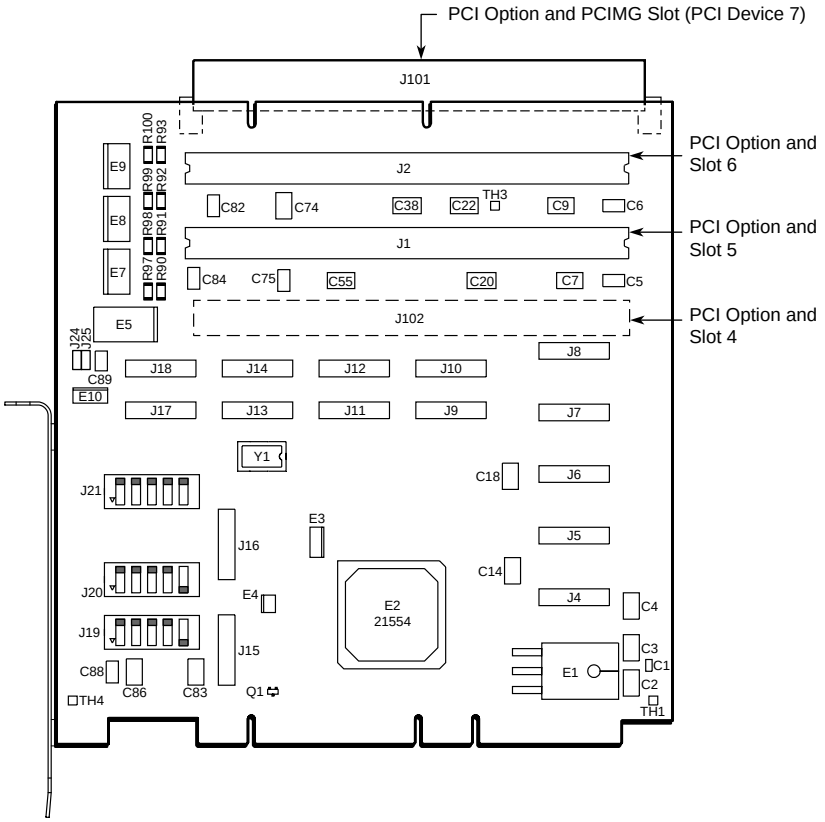
Clamping Voltage	Installed	Removed
3.3V **s_vio**	R41	R63
5V **s_vio**	R63	R41

a. Only one jumper resistor (R95 or R97) may be installed at a time. Installing both or no jumper resistors is not allowed.

1.8 Local Bus Slot Numbering and IDSEL Mapping

Figure 1-4 shows that the PCI local bus option card slots are mapped to PCI device numbers 4,5,6 and 7. The local bus lines **s_ad<24>** and **s_ad<31:28>** are used as local IDSEL lines.

Figure 1-4. Local PCI Slot Numbering



1.9 Interrupt Routing

Table 1-5 shows the ORing of interrupts. 12 interrupts are connected to the secondary bus PCI slots but four (4) are driven to the card edge.

The 12 incoming interrupts must be combined in accordance with the *PCI-to-PCI Bridge Architecture Specification*.

Table 1-5. Interrupt O-Ring

Device Number	Interrupt Pin on Device	Interrupt Pin on Board Connector
4 (Optional slot J102)	INTA#	INTB#
	INTB#	INTC#
	INTC#	INTD#
	INTD#	INTA#
5 (Slot J1)	INTA#	INTC#
	INTB#	INTD#
	INTC#	INTA#
	INTD#	INTB#
6 (Slot J2)	INTA#	INTD#
	INTB#	INTA#
	INTC#	INTB#
	INTD#	INTC#
7 (PICMG slot J101)	INTA#	INTA#
	INTB#	INTB#
	INTC#	INTC#
	INTD#	INTD#

1.10 Typical Configurations

Figure 1-5 shows the DE1B55401 with one local bus option card.

Figure 1-5. One Local Bus Option Card

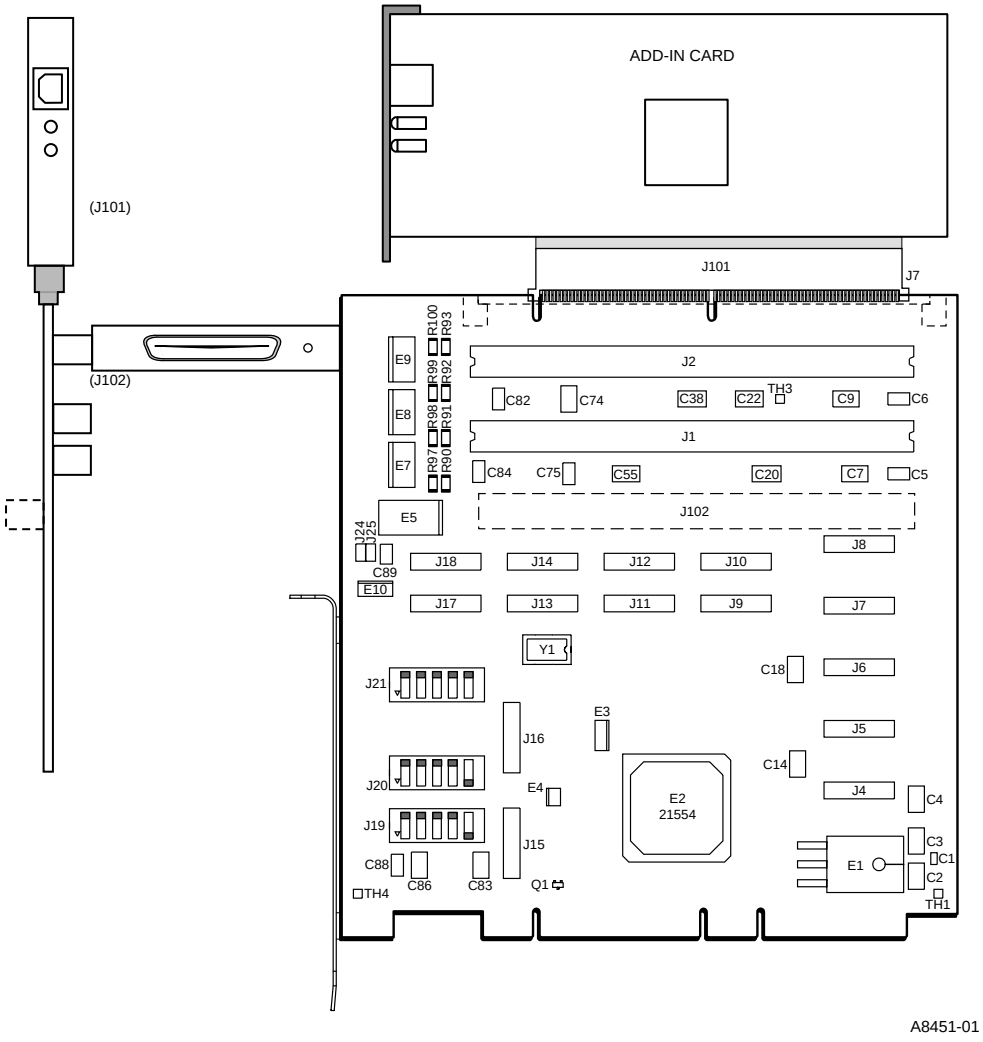
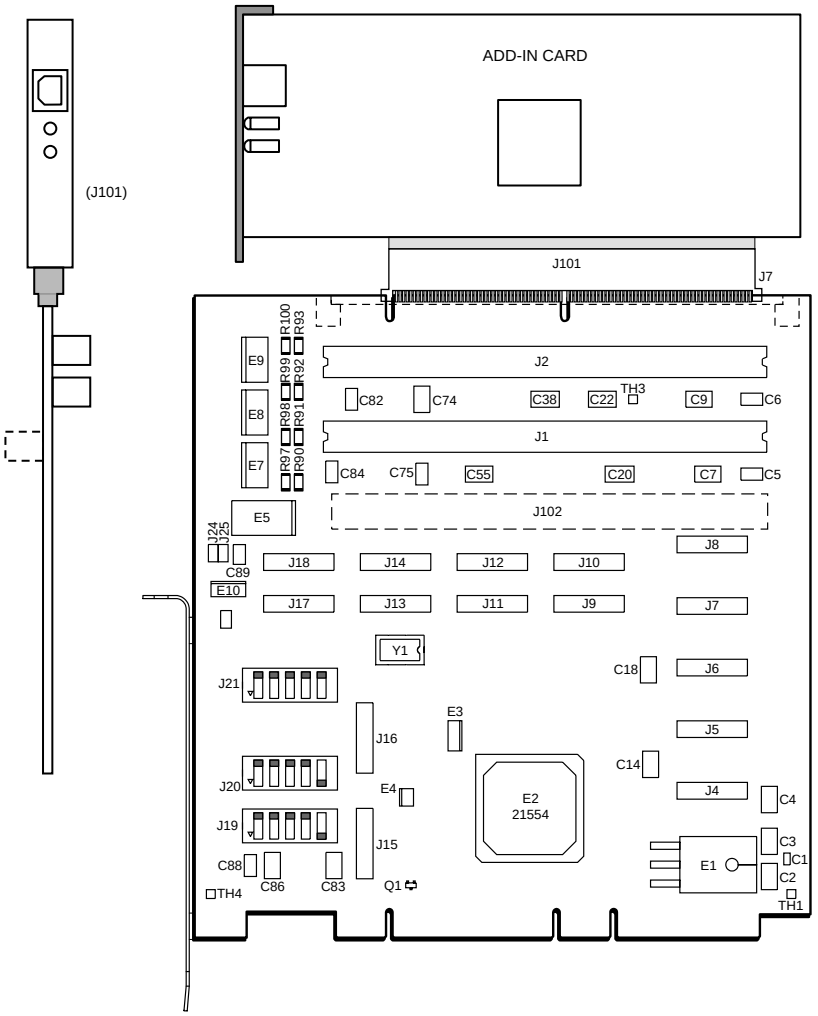


Figure 1-6 shows the DE1B55401 with two local bus option cards.

Note: The option card can be either 32-bit or 64-bit.

Figure 1-6. Two Local Bus Option Cards



Operation and Installation 2

This chapter provides information about the DE1B55401 specifications, hardware, and software requirements. It also describes how to install the DE1B55401.

2.1 Specifications

The physical and power specifications for the DE1B55401 are:

Dimensions:

- Height: 20.2 cm (8.0 in)
- Width: 17.8 cm (7.0 in)

Power Requirements:

- DC amps @ 5 V: 2 A (maximum)
- On Board 3.3volt regulator for **s_vio** and Vdd 5A (Maximum)

2.2 Hardware Requirements

The following equipment is required to use the DE1B55401:

- A computer system equipped with a PCI option slots.
- A PCI expansion slot on the motherboard that is equipped for the 5-V PCI environment
- PCI option cards used to create the local subsystem
- An optional local processor to control the subsystem

The local processor can be used out of the any PCI slots. The top PCI slot is configurable as a PICMG CPU slot.

2.3 Software Requirements

The DE1B55401 is shipped with the SROM and parallel ROM programmed during module test. One version of test pattern in the parallel ROM will print the 21554 banner to the screen during system boot.

The DE1B55401 kit provides DOS utilities that can be used to configure program the serial and parallel ROM. The diskette included in the DE1B55401 kit contains:

- DOS utility PVIEW.EXE to read all PCI configuration space registers.
- CDEBUG, a version of DOS DEBUG that reads memory locations directly.
- DOS4GW.EXE is a DOS32 extender. It must be in the same directory when running the utilities.
- DBFLASH.EXE an executable utility for erasing and updating the flash ROM memory.
- MSKROM.EXE an executable utility for programming the SROM.
- The software diskettes are standard 3.5 inch floppy disks. Follow the installation procedure printed on the inside of the shipping package.

2.3.1 SROM Programming

To program the SROM on the DE1B55401, use the MKSROM.EXE utility. Use a text editor to create an ASCII data file.

MSKSROM file.dat

Where:	MSKROM	Executes the MSKROM utility.
	file.dat	Specifies the file to load into the SROM.

To program a blank SROM:

1. Change SW1 and SW2 to "down" during initialization of the system.
2. After the system initializes, switch SW1 to "up".
3. Use MKSROM.EXE utility, For example:
   mksrom.exe sromfile.dat
4. Set SW2 to "up" position and reboot system.

Table 2-1. Switch Operation for SROM Programming

Switch Pack	Switch	Switch Down	Switch Up	Description
J20	SW1	Serial ROM Output Disabled	Serial ROM Output Enabled	The initialization is read from the SROM pr_ad<2>:sr_do
	SW2	No lockout (debug)	Lockout (normal operation)	Controls the primary lockout bit Reset Value on pr_ad<3>

2.3.2 Flash ROM Programming

Dbflash.exe is an MSDOS based program that allows the flash ROM attached to the 21554 to be erased and updated with new images. When dbflash.exe is run on a system that has a 21554 installed on the PCI bus, the program scans all the PCI buses looking for the 21554 component. When found, the program identifies the 21554 PCI location and starts the update process that was selected on the command line.

2.3.2.1 Board Setup

Table 2-2 and Table 2-3 give the DE1B55401 switch configuration for using the DBFLASH.EXE utility.

Table 2-2. Switch Configuration for FLASH Programming

Switch Pack	Switch	Switch Down	Switch Up[a]	Description
J19	SW3	ROM Socket **pr_cs**	Program and access memory using DBFLASH.EXE.	Enables DBFLASH access to the ROM Socket or to the flash memory. See Figure 1-1 on page 1-6.

a. Default setting.

Table 2-3. Jumper for FLASH Programming

Jumper	Flash CE ROM Control
J24	When installed, enable **pr_cs** control of the ROM CE . When removed, disable **pr_cs** control of CE ROM.

2.3.2.2 Running DbFlash.exe

Make sure both DBFLASH.EXE and DOS4GW.EXE are in same directory or environment path. Dbflash.exe takes parameters to tell it what to do. A typical flash programming update will require the user to specify the flash block to update and the new image to use.

Dbflash /b0 NewRomImage.bin

This example will flash image 'NewRomImage.bin' into block 0 of 21554 expansion ROM. During the next boot of the PC, the BIOS will find this image in the ROM and if it has a PCI compliant Expansion ROM header the image will be loaded and executed by the system BIOS during POST. For more information on how this works, read the *PCI Local Bus Specification, V2.1* (or newer).

Table 2-4. DBFLASH.EXE Command Summary

Command	Description	Comments
Dbflash /e	Erase entire flash ROM contents	Will erase all blocks
Dbflash /bx image.bin	Program block x with image.bin	If image larger than 1 block, program will continue into the next block until entire image is loaded.

Note: Any other application software is the responsibility of the user.

2.4 DE1B55401 Installation Procedure

Figure 1-1 Illustrates the DE1B55401 and shows the location of components referred to in this section.

Install the DE1B55401 as follows:

1. Power down the host system that will contain the DE1B55401.
2. Consider the unique mounting problems of the DE1B55401 in the target system:

   If necessary, the motherboard and associated support devices may need to be set up on a bench top to allow access to the DE1B55401 for test purposes.
3. Before applying power:
   a. Verify the DIP switch settings for J19, J20, and J21.
   b. Insert the card edge of the DE1B55401 into a PCI slot.
   c. Insert a 5V or universal option PCI card into any or each of the four local bus option-card slots. Section 1.10 shows examples of typical PCI configurations.
4. Power up the system.
5. Verify auto-configuration of the 21554 and of any devices that are plugged in as follows:
   a. If the on-board ROM is preloaded the 21554 banner will be present.
   b. Verify that system BIOS or firmware detects and configures the 21554.
   c. To verify the loading of the SROM, run the MKSROM utility without an SROM file as an input. See Section 2.3.1, “SROM Programming” on page 2-2.
6. PCI bus data, address, and control signals are monitored by connecting a logic analyzer to connectors the test pods. See Appendix A.

Optional Configurations 3

3.1 PICMG Configuration

This chapter describes how to configure the DE1B55401 for a Single Board Computer (SBC) with a PCI interface as defined be the PICMG PCI-ISA interface specification. The DE1B55401can support an intelligent subsystem on the local bus. The intelligent subsystem is architecture independent. The 21554 can interface to the PCI interface of any intelligent subsystem. The J101 connector has the capability of accepting an intelligent controller.

Table 3-1 details the jumper options necessary for this mode of operation.

Table 3-1. PICMG Stake Pin Jumper

Jumper	Function
J23	When installed, use **s_ad<24>** as IDSEL when J101 is a PCI Option slot. When removed[a], pin A26 becomes GNT2 from local processor. Correct routing of **s_idsel** for Slot J101.

a. Factory default.

To operate a controller on the local bus the clocks have to be routed accordingly. Table 3-2 identifies the series of zero ohm resistors that must be configured to implement the system slot as the clock source.

Table 3-2. PICMG Options Jumpers

Function	Installed	Removed
System slot drives **s_clk_i** on the 21554	R67	R66, R65
System slot provides local clock	R90,R91,R92,R93	R97, R98, R99, R100

3.2 Central Function and Arbiter Control

Table 3-3 specifies how to configure the DE1B55401 as an external or central arbitrator. When an intelligent subsystem is on the local bus, the DE1B55401 can operate using an external arbiter agent or the 21554 Central Function mode internal arbitration logic.

Table 3-3. Central Function and Arbiter Control

Switch Pack	Switch	Switch Down	Switch Up	Description
J20	SW5	Enable 21554 arbiter	System slot J101 is the Central Function	Central Function Mode **pr_ad<6>**
J21	SW1	Disable 21554 arbiter	System slot J101 is the external arbiter.	Arbiter Function **pr_ad<7>**

Table 3-4 shows the configuration of switch pack switches for system arbitration with PICMG operation.

Table 3-4. REQ# and GNT# Selection

Switch Pack	Switch[a]	Request/ Grant	Switch Down System slot (J102) as arbiter	Switch Up 21554 as arbiter
J21	SW2	req#1	REQ1 from PICMG slot	REQ1 from 21554
	SW3	gnt#1	GNT1 from PICMG slot	GNT1 from 21554
	SW4	req#2	REQ2 from PICMG slot	REQ2 from 21554
	SW5	gnt#2	GNT2 from PICMG slot	GNT2 from 21554
J20	SW1	req#3	REQ2 from PICMG slot	REQ2 from 21554
	SW2	gnt#3	GNT2 from PICMG slot	GNT2 from 21554

a. All switches must be either up or down for correct operation.

3.3 Asynchronous Clocking

The local bus can be configured for synchronous or asynchronous operations. If the PICMG slot is the source of the clocks, the resistor strapping options must be followed as mentioned in Section 3.1. In addition to this, switch bank J20 SW3 needs to indicate asynchronous clocking mode and **s_clk_o** needs to be disabled from the 21554. Table 3-5 lists these switches and their operations in more detail.

Table 3-5. Synchronous or Asynchronous Clock Control

Switch Pack	Switch	Switch Down	Switch Up	Description
J20	SW3	Synchronous host and local clock domains	Asynchronous host and local clock domains	Synchronous/ Asynchronous Operation **pr_ad<4>**
	SW4	Disable 21554 **s_clk_o**	Enable 21554 **s_clk_o**	**s_clk_o pr_ad<5>**

Signal and Default Information A

A.1 Test Pod Pin Outs

Test points are accessible through board mounted Header type connectors, which are referred to as pods. The following tables give the schematic name of the signal that can be found at each pod pin. All even numbered pod pins are grounded. All odd numbered pod pins connect to a unique signal that is documented on the *21554 Bridge Reference Design* Schematic.

Table A-1 associates the pod pin numbers to the secondary bus control signals and address and data lines. See Figure 1-1 for the location of this connector.

Table A-1. Secondary Bus Test Pods

Secondary Bus Control Signals				
Pod Pin[a] Number	**J9**	**J17**	**J13**	**J8**
1	$\overline{\text{S\_FRAME}}$	$\overline{\text{S\_REQ3}}$	$\overline{\text{S\_CBE3}}$	$\overline{\text{S\_CBE4}}$
3	$\overline{\text{S\_IRDY}}$	$\overline{\text{S\_GNTC3}}$	$\overline{\text{S\_CBE2}}$	$\overline{\text{S\_CBE5}}$
5	$\overline{\text{S\_TRDY}}$	$\overline{\text{S\_REQ2}}$	$\overline{\text{S\_CBE1}}$	$\overline{\text{S\_CBE6}}$
7	$\overline{\text{S\_DEVSEL}}$	$\overline{\text{S\_GNTC2}}$	$\overline{\text{S\_CBE0}}$	$\overline{\text{S\_CBE7}}$
9	$\overline{\text{S\_STOP}}$	$\overline{\text{S\_REQ1}}$	$\overline{\text{P\_GNT}}$	$\overline{\text{S\_ACK64}}$
11	$\overline{\text{S\_PERR}}$	$\overline{\text{S\_GNTC1}}$	$\overline{\text{P\_REQ}}$	$\overline{\text{S\_REQ64}}$
13	$\overline{\text{S\_SERR}}$	$\overline{\text{S\_REQ0}}$	(no connection)	S_PAR64
15	S_PARR	$\overline{\text{S\_GNTC0}}$	(no connection)	(no connection)
Secondary Address and Data Pods				
Pod Pin[a] Number	**J10 S_AD<0:7>**	**J12 S_AD<8:15>**	**J11 S_AD<16:23>**	**J14 S_AD<24:31>**
1	S_AD7	S_AD15	S_AD23	S_AD31
3	S_AD6	S_AD14	S_AD22	S_AD30
5	S_A5	S_AD13	S_AD21	S_AD29
7	S_AD4	S_AD12	S_AD20	S_AD28
9	S_AD3	S_AD11	S_AD19	S_AD27
11	S_AD2	S_AD10	S_AD18	S_AD26
13	S_AD1	S_AD9	S_AD17	S_AD25
15	S_AD0	S_AD8	S_AD16	S_AD24

a. All even numbered pod pins are wired to earth ground.

Table A-2 associates the pod pin numbers to the extended secondary bus address and data lines. See Figure 1-1 on page 1-6 for the location of these connector.

Table A-2. Extended Secondary Address and Data Pods

Pod Pin[a] Number	J4 S_AD<32:39>	J5 S_AD<40:47>	J6 S_AD<48:55>	J7 S_AD<56:63>
1	S_AD39	S_AD47	S_AD55	S_AD63
3	S_AD38	S_AD46	S_AD54	S_AD62
5	S_AD37	S_AD45	S_AD53	S_AD61
7	S_AD36	S_AD44	S_AD52	S_AD60
9	S_AD35	S_AD43	S_AD51	S_AD59
11	S_AD34	S_AD42	S_AD50	S_AD58
13	S_AD33	S_AD41	S_AD49	S_AD57
15	S_AD32	S_AD40	S_AD48	S_AD56

a. All even numbered pod pins are wired to earth ground.

Table A-3 associates the pod pin numbers to the parallel ROM control signals and associates the pod pin numbers to the clock control signals. See Figure 1-1 on page 1-6 for the location of this connector.

Table A-3. Parallel ROM and Clock Control Pods

Pod Pin[a] Number	J15 Parallel ROM	J18 Clock Signal
1	DB_SRC5	S_CLK0_A
3	$\overline{\text{S\_RST}}$	S_CLK0_D
5	$\overline{\text{PR\_WR}}$	S_CLK0_C
7	$\overline{\text{PR\_RD}}$	CLKB
9	$\overline{\text{PR\_CS}}$	P_PCLK
11	$\overline{\text{PR\_ALE}}$	(no connection)
13	$\overline{\text{PR\_CLK}}$	(no connection)
15	$\overline{\text{P\_MGGEN}}$	(no connection)

a. All even numbered pod pins are wired to earth ground.

A.2 Factory Default Switch and Jumper Configuration

The DEB55401 is configured at the factory for normal or typical operation.

- Table A-4 gives the factory configuration for the stake-pin jumpers.

Table A-4. Stake-Pin Jumpers

Jumper	Factory Installed or Not installed
J22	Not Installed
J23	Installed
J24	Installed
J25	Not Installed

- Table A-5 gives the factory configuration for the switch pack switches.

Table A-5. Switch Pack Factory Defaults

Switch	Factory Configured to Up or Down[a]
J21	All switches are up. (SW1 through SW5)
J20	SW1, SW2, SW3, and SW4 are up
	SW5 is down
J19	All switches are up. (SW1 through SW5)

a. The up position leaves the switch lever pointing towards the local option sockets.

- Table A-6 gives the factory configuration of the zero-ohm resistor jumpers.

Table A-6. Resistor Jumper Factory Defaults

Resistor Jumper	In/Out	Resistor Jumper	In/Out
R65	In	R66	In
R67	Out	R73	Out
R90	Out	R91	Out
R92	Out	R93	Out
R97	In	R98	In
R99	In	R100	In
R41[a]	Out	R63	In

a. Voltage clamp jumpers are set for 5V