

## Features

- Temperature ranges
  - Commercial: 0°C to 70°C
  - Industrial/Automotive -A: -40°C to 85°C
  - Automotive-E: -40°C to 125°C
- High Speed
  - $t_{AA} = 10 \text{ ns}$
- Low Active Power
  - 324 mW (max)
- 2.0V Data Retention
- Automatic Power Down when Deselected
- TTL-compatible Inputs and Outputs
- Easy Memory Expansion with  $\overline{CE}$  and  $\overline{OE}$  features

## Functional Description

The CY7C1049CV33 is a high performance CMOS Static RAM organized as 524,288 words by eight bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{CE}$ ), an active LOW Output Enable ( $\overline{OE}$ ), and three-state drivers. Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{18}$ ).

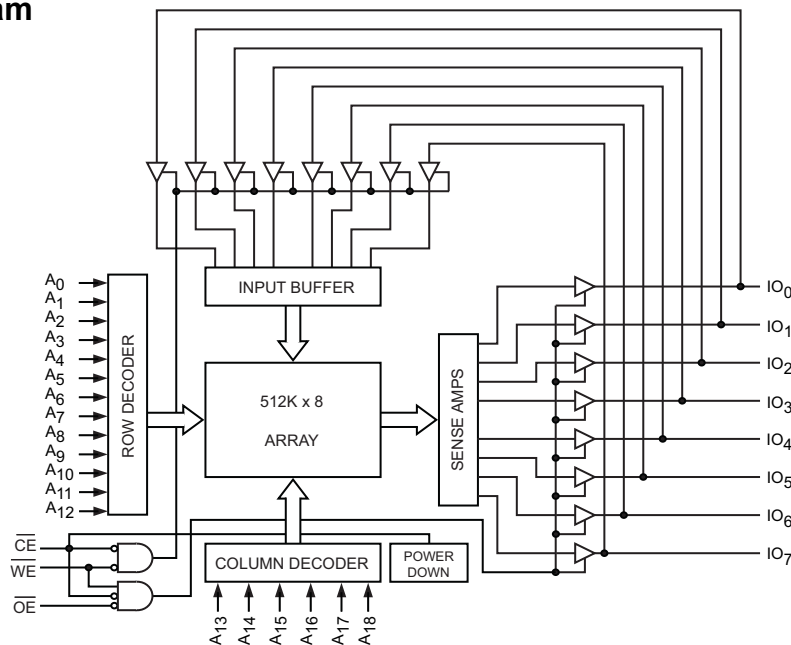
Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

The eight input and output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

The CY7C1049CV33 is available in standard 400-mil-wide 36-pin SOJ package and 44-pin TSOP II package with center power and ground (revolutionary) pinout.

For best practice recommendations, refer to the Cypress application note [AN1064, SRAM System Guidelines](#).

## Logic Block Diagram



## Contents

<b>Features</b> .....	<b>1</b>	<b>AC Switching Characteristics</b> .....	<b>7</b>
<b>Functional Description</b> .....	<b>1</b>	<b>Switching Waveforms</b> .....	<b>8</b>
<b>Logic Block Diagram</b> .....	<b>1</b>	<b>Truth Table</b> .....	<b>9</b>
<b>Contents</b> .....	<b>2</b>	<b>Ordering Information</b> .....	<b>9</b>
<b>Pin Configuration</b> .....	<b>3</b>	<b>Package Diagrams</b> .....	<b>10</b>
<b>Selection Guide</b> .....	<b>3</b>	<b>Document History Page</b> .....	<b>11</b>
<b>Pin Definitions</b> .....	<b>4</b>	<b>Sales, Solutions, and Legal Information</b> .....	<b>12</b>
<b>Maximum Ratings</b> .....	<b>5</b>	Worldwide Sales and Design Support.....	12
<b>Operating Range</b> .....	<b>5</b>	Products .....	12
<b>Electrical Characteristics</b> .....	<b>5</b>	PSoC Solutions .....	12
<b>Capacitance</b> .....	<b>5</b>		
<b>Thermal Resistance</b> .....	<b>5</b>		

Pin Configuration

Figure 1. 36-Pin SOJ (Top View)

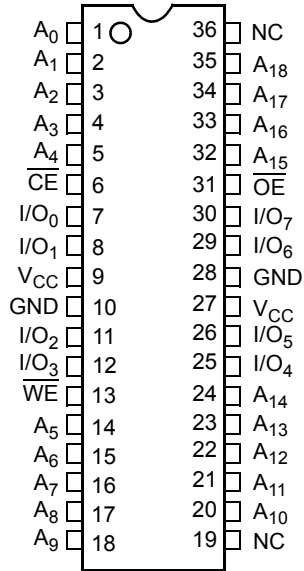
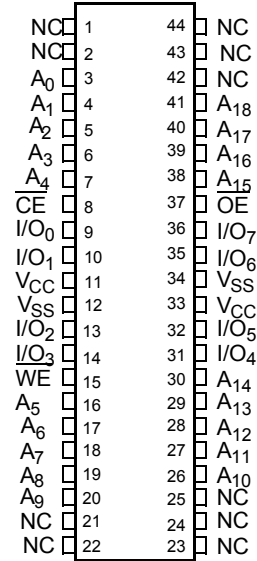


Figure 2. 44-Pin TSOP II (Top View)



Selection Guide

Description		-10	-12	-15	Unit
Maximum Access Time		10	12	15	ns
Maximum Operating Current	Commercial	90	85	-	mA
	Industrial/Automotive-A	100	95	-	mA
	Automotive-E	-	-	95	mA
Maximum CMOS Standby Current	Commercial/Industrial/ Automotive-A	10	10	-	mA
	Automotive-E	-	-	15	mA

**Pin Definitions**

Pin Name	36-SOJ Pin Number	44 TSOP-II Pin Number	I/O Type	Description
A <sub>0</sub> -A <sub>18</sub>	1-5,14-18, 20-24,32-35	3-7,16-20, 26-30,38-41	Input	<b>Address inputs used to select one of the address locations.</b>
I/O <sub>0</sub> -I/O <sub>7</sub>	7,8,11,12,25, 26,29,30	9,10,13,14, 31,32,35,36	Input/Output	<b>Bidirectional data I/O lines.</b> Used as input or output lines depending on operation
NC <sup>[1]</sup>	19,36	1,2,21,22,23,24, 25,42,43, 44	No Connect	<b>No connects.</b> This pin is not connected to the die
$\overline{\text{WE}}$	13	15	Input/Control	<b>Write Enable input, active LOW.</b> When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted.
$\overline{\text{CE}}$	6	8	Input/Control	<b>Chip Enable input, active LOW.</b> When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{\text{OE}}$	31	37	Input/Control	<b>Output Enable, active LOW.</b> Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins.
V <sub>SS</sub> , GND	10,28	12,34	Ground	<b>Ground for the device.</b> Should be connected to ground of the system.
V <sub>CC</sub>	9,27	11,33	Power Supply	<b>Power supply inputs to the device.</b>

**Note**

1. NC pins are not connected on the die.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied ..... -55°C to +125°C

Supply Voltage on V<sub>CC</sub> to Relative GND<sup>[2]</sup> -0.5V to +4.6VDC

Voltage Applied to Outputs in High-Z State<sup>[2]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

Input Voltage<sup>[2]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

Current into Outputs (LOW) ..... 20 mA

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial/ Automotive-A	-40°C to +85°C	
Automotive-E	-40°C to +125°C	

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-10		-12		-15		Unit	
			Min	Max	Min	Max	Min	Max		
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min.; I <sub>OH</sub> = -4.0 mA	2.4		2.4		2.4		V	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min.; I <sub>OL</sub> = 8.0 mA		0.4		0.4		0.4	V	
V <sub>IH</sub>	Input HIGH Voltage		2.0	V <sub>CC</sub> + 0.3	2.0	V <sub>CC</sub> + 0.3	2.0	V <sub>CC</sub> + 0.3	V	
V <sub>IL</sub>	Input LOW Voltage <sup>[2]</sup>		-0.3	0.8	-0.3	0.8	-0.3	0.8	V	
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	Com'l/Ind'l/ Auto-A	-1	+1	-1	+1			μA
								-20	+20	
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	Com'l		90		85			mA
				Ind'l/Auto-A		100		95		
					Auto-E					
I <sub>SB1</sub>	Automatic CE Power Down Current —TTL Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>IH</sub> ; V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>	Com'l/Ind'l/ Auto-A		40		40			mA
				Auto-E					45	
I <sub>SB2</sub>	Automatic CE Power Down Current —CMOS Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0	Com'l/Ind'l/ Auto-A		10		10			mA
				Auto-E					15	

## Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 3.3V	8	pF
C <sub>OUT</sub>	I/O Capacitance		8	pF

## Thermal Resistance

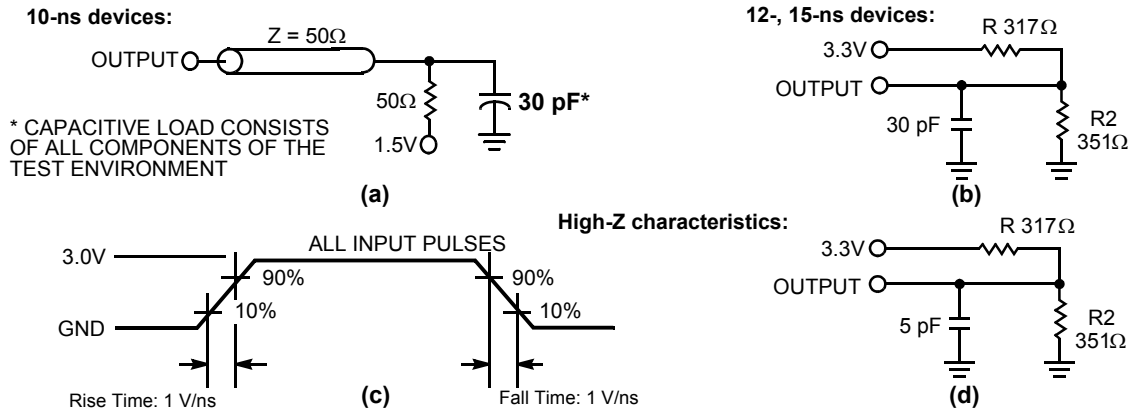
Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	36-Pin SOJ	44-TSOP-II	Unit
Θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	46.51	41.66	°C/W
Θ <sub>JC</sub>	Thermal Resistance (Junction to Case)		18.8	10.56	°C/W

### Notes

- V<sub>IL</sub> (min) = -2.0V and V<sub>IH</sub>(max) = V<sub>CC</sub> + 0.5V for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

Figure 3. AC Test Loads and Waveforms [3]



**Note**

4. AC characteristics (except High-Z) for 10 ns parts are tested using the load conditions shown in Figure (a). All other speeds are tested using the Thevenin load shown in Figure (b). High-Z characteristics are tested for all speeds using the test load shown in Figure (d).

## AC Switching Characteristics

Over the Operating Range <sup>[5]</sup>

Parameter	Description	-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	
<b>Read Cycle</b>								
$t_{\text{power}}^{[6]}$	$V_{\text{CC}}$ (typical) to the first access	100		100		100		$\mu\text{s}$
$t_{\text{RC}}$	Read Cycle Time	10		12		15		ns
$t_{\text{AA}}$	Address to Data Valid		10		12		15	ns
$t_{\text{OHA}}$	Data Hold from Address Change	3		3			3	ns
$t_{\text{ACE}}$	$\overline{\text{CE}}$ LOW to Data Valid		10		12		15	ns
$t_{\text{DOE}}$	$\overline{\text{OE}}$ LOW to Data Valid		5		6		7	ns
$t_{\text{LZOE}}$	$\overline{\text{OE}}$ LOW to Low-Z	0		0		0		ns
$t_{\text{HZOE}}$	$\overline{\text{OE}}$ HIGH to High-Z <sup>[7, 8]</sup>		5		6		7	ns
$t_{\text{LZCE}}$	$\overline{\text{CE}}$ LOW to Low-Z <sup>[8]</sup>	3		3		3		ns
$t_{\text{HZCE}}$	$\overline{\text{CE}}$ HIGH to High-Z <sup>[7, 8]</sup>		5		6		7	ns
$t_{\text{PU}}$	$\overline{\text{CE}}$ LOW to Power Up	0		0		0		ns
$t_{\text{PD}}$	$\overline{\text{CE}}$ HIGH to Power Down		10		12		15	ns
<b>Write Cycle</b> <sup>[9, 10]</sup>								
$t_{\text{WC}}$	Write Cycle Time	10		12		15		ns
$t_{\text{SCE}}$	$\overline{\text{CE}}$ LOW to Write End	7		8		10		ns
$t_{\text{AW}}$	Address Setup to Write End	7		8		10		ns
$t_{\text{HA}}$	Address Hold from Write End	0		0		0		ns
$t_{\text{SA}}$	Address Setup to Write Start	0		0		0		ns
$t_{\text{PWE}}$	$\overline{\text{WE}}$ Pulse Width	7		8		10		ns
$t_{\text{SD}}$	Data Setup to Write End	5		6		7		ns
$t_{\text{HD}}$	Data Hold from Write End	0		0		0		ns
$t_{\text{LZWE}}$	$\overline{\text{WE}}$ HIGH to Low-Z <sup>[8]</sup>	3		3		3		ns
$t_{\text{HZWE}}$	$\overline{\text{WE}}$ LOW to High-Z <sup>[7, 8]</sup>		5		6		7	ns

### Notes

5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
6.  $t_{\text{POWER}}$  gives the minimum amount of time that the power supply should be at stable, typical  $V_{\text{CC}}$  values until the first memory access can be performed.
7.  $t_{\text{HZOE}}$ ,  $t_{\text{HZCE}}$ , and  $t_{\text{HZWE}}$  are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
8. At any given temperature and voltage condition,  $t_{\text{HZCE}}$  is less than  $t_{\text{LZCE}}$ ,  $t_{\text{HZOE}}$  is less than  $t_{\text{LZOE}}$ , and  $t_{\text{HZWE}}$  is less than  $t_{\text{LZWE}}$  for any given device.
9. The internal Write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  LOW, and  $\overline{\text{WE}}$  LOW.  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  must be LOW to initiate a Write, and the transition of either of these signals can terminate the Write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the Write.
10. The minimum Write cycle time for Write Cycle No. 3 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) is the sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

### Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [11, 12]

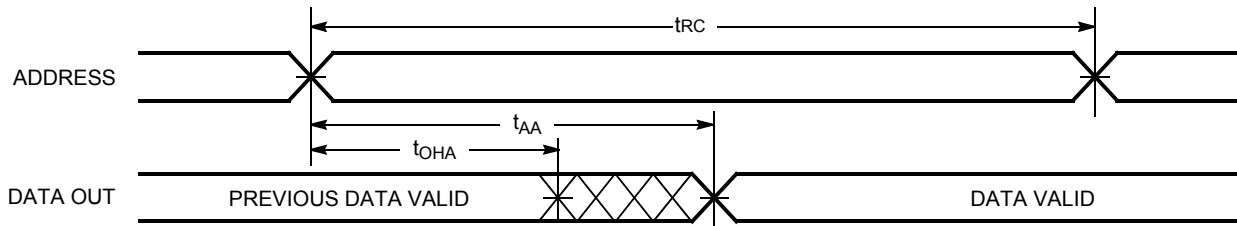


Figure 5. Read Cycle No. 2 ( $\overline{OE}$  Controlled) [12, 13]

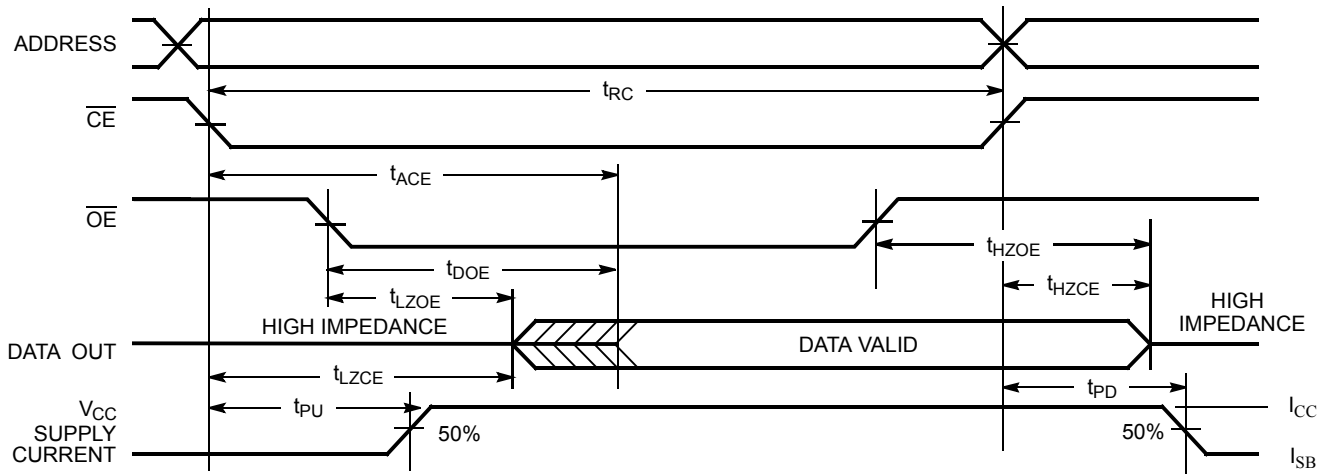
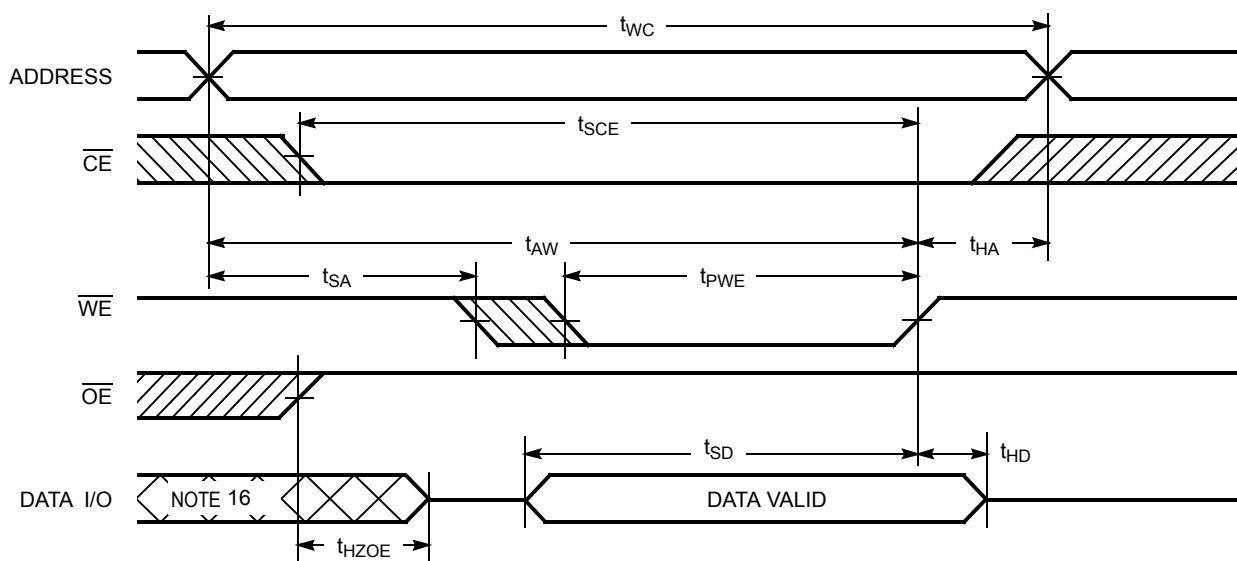


Figure 6. Write Cycle No. 1 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write) [14, 15]



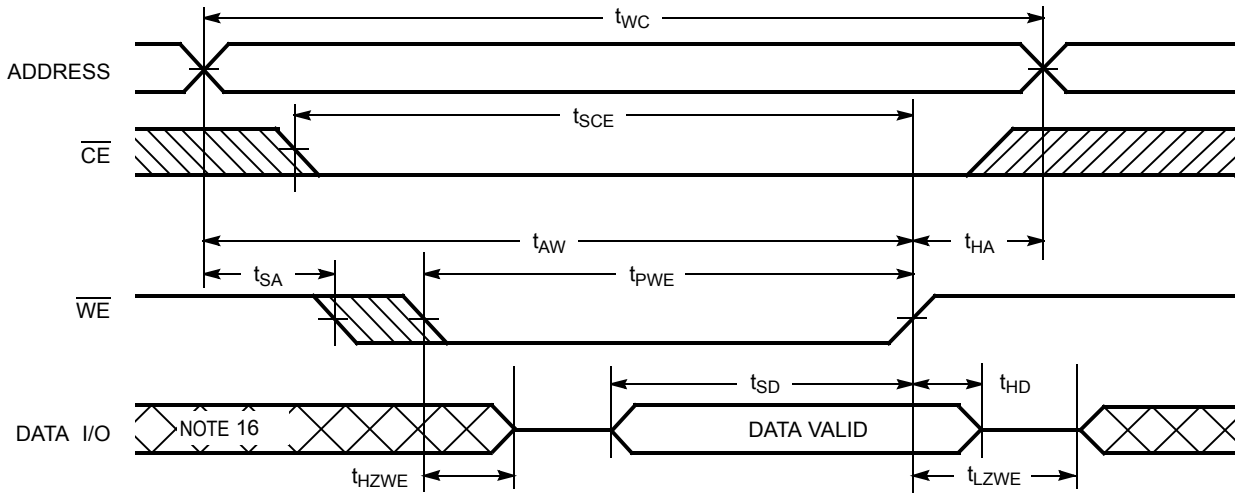
**Notes**

- 11. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
- 12. WE is HIGH for read cycles.
- 13. Address valid before or similar to  $\overline{CE}$  transition LOW.
- 14. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 15. If CE goes HIGH simultaneously with WE HIGH, the output remains in high impedance state.
- 16. During this period, the I/Os are in output state. Do not apply input signals.



Switching Waveforms (continued)

Figure 7. Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [15]



Truth Table

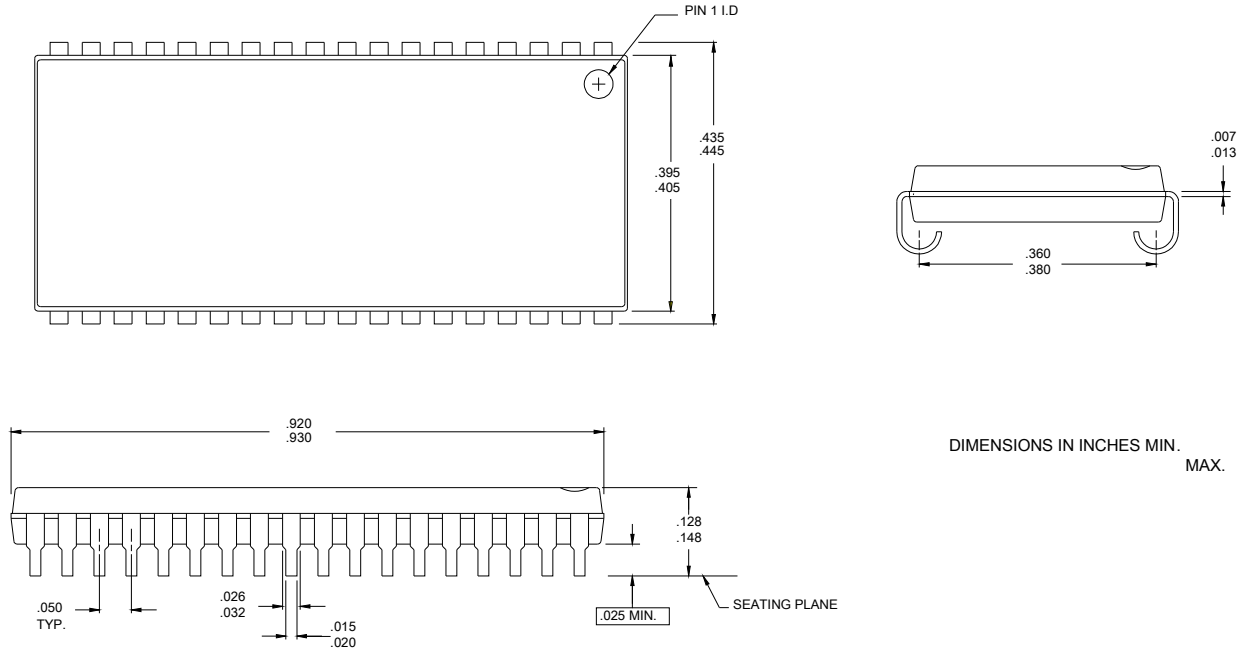
CE	OE	WE	I/O <sub>0</sub> -I/O <sub>7</sub>	Mode	Power
H	X	X	High-Z	Power Down	Standby ( $I_{SB}$ )
L	L	H	Data Out	Read	Active ( $I_{CC}$ )
L	X	L	Data In	Write	Active ( $I_{CC}$ )
L	H	H	High-Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1049CV33-10VXC	51-85090	36-Pin (400-Mil) Molded SOJ (Pb-Free)	Commercial
	CY7C1049CV33-10VXA	51-85090	36-Pin (400-Mil) Molded SOJ (Pb-Free)	Automotive-A
12	CY7C1049CV33-12ZSXA	51-85087	44-Pin TSOP II (Pb-Free)	Automotive-A
15	CY7C1049CV33-15VXE	51-85090	36-Pin (400-Mil) Molded SOJ (Pb-Free)	Automotive-E
	CY7C1049CV33-15ZSXE	51-85087	44-Pin TSOP II (Pb-Free)	

Package Diagrams

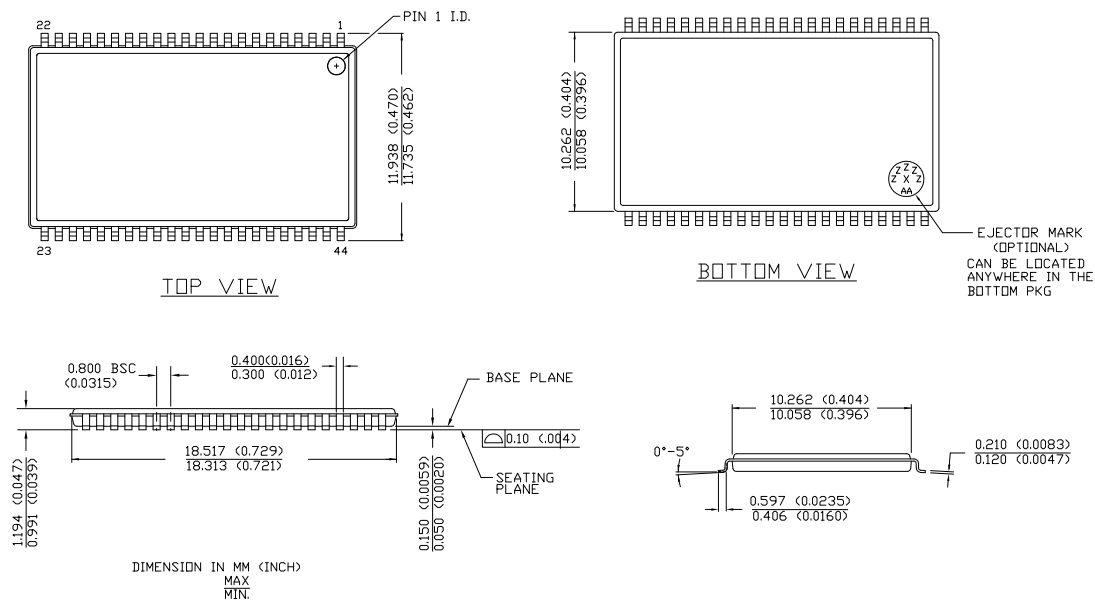
Figure 8. 36-Pin (400-Mil) Molded SOJ V36, 51-85090



51-85090 \*D

Figure 9. 44-Pin TSOP II, 51-85087

44 Lead TSOP TYPE II – STANDARD



51-85087 \*C

Document History Page

Document Title: CY7C1049CV33 4-Mbit (512K X 8) Static RAM				
Document Number: 38-05006				
Rev.	ECN	Orig. of Change	Submission Date	Description of Change
**	112569	HGK	03/06/02	New data sheet
*A	114091	DFP	04/25/02	Changed Tpower unit from ns to μs
*B	116479	CEA	09/16/02	Add applications foot note to data sheet, page 1.
*C	262949	RKF	See ECN	Added Automotive-E Specs Added Θ <sub>JA</sub> and Θ <sub>JC</sub> values on Page #3.
*D	300091	RKF	See ECN	Added -20-ns Speed bin
*E	344595	SYT	See ECN	Added Pb-Free package on page #8 Removed shading for CY7C1049CV33-15ZSX in the ordering Information on page 9
*F	2615344	VKN/PYRS	12/03/08	Added Automotive-A information Removed 8 ns and 20 ns speed bins, Changed t <sub>POWER</sub> spec from 1 μs to 100 μs, Updated Ordering Information table.
*G	2841563	NXR/	01/07/2010	Added CY7C1049CV33-10VXA to Ordering Info table.
*H	2898958	AJU	03/25/10	Removed inactive parts from the ordering informaiton table. Updated package diagrams.

© Cypress Semiconductor Corporation, 2002-2010. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

### Products

Automotive	<a href="http://cypress.com/go/automotive">cypress.com/go/automotive</a>
Clocks & Buffers	<a href="http://cypress.com/go/clocks">cypress.com/go/clocks</a>
Interface	<a href="http://cypress.com/go/interface">cypress.com/go/interface</a>
Lighting & Power Control	<a href="http://cypress.com/go/powerpsoc">cypress.com/go/powerpsoc</a> <a href="http://cypress.com/go/plc">cypress.com/go/plc</a>
Memory	<a href="http://cypress.com/go/memory">cypress.com/go/memory</a>
Optical & Image Sensing	<a href="http://cypress.com/go/image">cypress.com/go/image</a>
PSoC	<a href="http://cypress.com/go/psoc">cypress.com/go/psoc</a>
Touch Sensing	<a href="http://cypress.com/go/touch">cypress.com/go/touch</a>
USB Controllers	<a href="http://cypress.com/go/USB">cypress.com/go/USB</a>
Wireless/RF	<a href="http://cypress.com/go/wireless">cypress.com/go/wireless</a>

### PSoC Solutions

[psoc.cypress.com/solutions](http://psoc.cypress.com/solutions)  
PSoC 1 | PSoC 3 | PSoC 5

---

© Cypress Semiconductor Corporation, 2002-2010. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.