

# 256K x 16 Static RAM

## Features

- High speed
  - $t_{AA} = 12 \text{ ns}$
- Low active power
  - 1540 mW (max.)
- Low CMOS standby power (L version)
  - 2.75 mW (max.)
- 2.0V Data Retention (400  $\mu\text{W}$  at 2.0V retention)
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  features

## Functional Description

The CY7C1041B is a high-performance CMOS static RAM organized as 262,144 words by 16 bits.

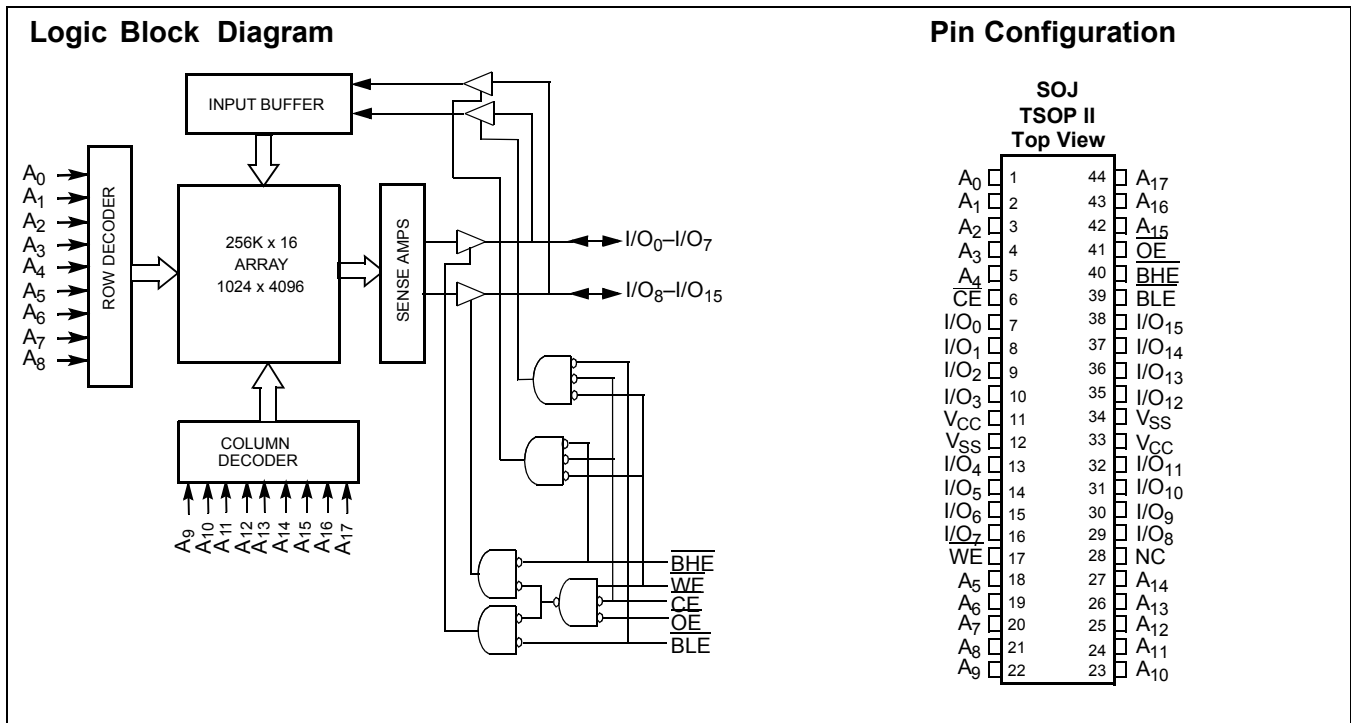
Writing to the device is accomplished by taking Chip Enable (CE) and Write Enable (WE) inputs LOW. If Byte Low Enable

(BLE) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>17</sub>). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>17</sub>).

Reading from the device is accomplished by taking Chip Enable (CE) and Output Enable ( $\overline{\text{OE}}$ ) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O<sub>8</sub> to I/O<sub>15</sub>. See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state when the device is deselected ( $\overline{\text{CE}}$  HIGH), the outputs are disabled ( $\overline{\text{OE}}$  HIGH), the BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation (CE LOW, and WE LOW).

The CY7C1041B is available in a standard 44-pin 400-mil-wide body width SOJ and 44-pin TSOP II package with center power and ground (revolutionary) pinout.



**Selection Guide**

		7C1041B-12	7C1041B-15	7C1041B-17	7C1041B-20	7C1041B-25	Unit
Maximum Access Time		12	15	17	20	25	ns
Maximum Operating Current	Com'l	200	190	180	170	160	mA
	Ind'l	220	210	200	190	180	
Maximum CMOS Standby Current	Com'l	3	3	3	3	3	mA
	Com'l	L	-	0.5	0.5	0.5	
	Ind'l	-	6	6	6	6	

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied ..... -55°C to +125°C

Supply Voltage on V<sub>CC</sub> to Relative GND<sup>[1]</sup> .... -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

DC Input Voltage<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

Current into Outputs (LOW) ..... 20 mA

**Operating Range**

Range	Ambient Temperature <sup>[2]</sup>	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 0.5
Industrial	-40°C to +85°C	

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	7C1041B-12		7C1041B-15		7C1041B-17		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.5	2.2	V <sub>CC</sub> + 0.5	2.2	V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Input LOW Voltage <sup>[1]</sup>		-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	-1	+1	-1	+1	mA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output Disabled	-1	+1	-1	+1	-1	+1	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	Com'l		200	190	180		mA
			Ind'l		220	210	200		
I <sub>SB1</sub>	Automatic CE Power-Down Current —TTL Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>IH</sub> V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		40		40		40	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current —CMOS Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0	Com'l		3	3	3		mA
			Com'l		L	-	0.5	0.5	
			Ind'l		-	6	6		

**Notes:**

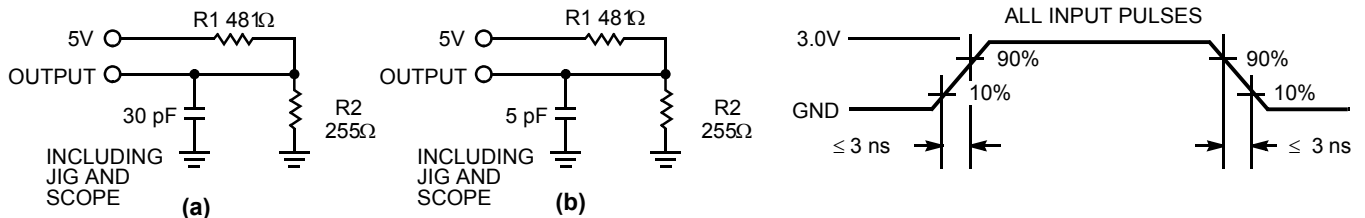
- V<sub>IL</sub> (min.) = -2.0V for pulse durations of less than 20 ns.
- T<sub>A</sub> is the case temperature.

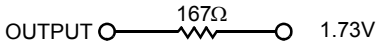
**Electrical Characteristics** Over the Operating Range (continued)

Parameter	Description	Test Conditions	7C1041B-20		7C1041B-25		Unit
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.5	2.2	V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Input LOW Voltage <sup>[1]</sup>		-0.5	0.8	-0.5	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	-1	+1	mA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output Disabled	-1	+1	-1	+1	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	Com'l	170		160	mA
			Ind'l	190		180	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current — TTL Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>IH</sub> V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		40		40	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current — CMOS Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0	Com'l	3		3	mA
			Com'l   L	0.5		0.5	mA
			Ind'l	6		6	mA

**Capacitance<sup>[3]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	8	pF
C <sub>OUT</sub>	I/O Capacitance		8	pF

**AC Test Loads and Waveforms**


Equivalent to: THÉVENIN EQUIVALENT  


**Note:**

3. Tested initially and after any design or process changes that may affect these parameters.

**Switching Characteristics<sup>[4]</sup> Over the Operating Range**

Parameter	Description	7C1041B-12		7C1041B-15		7C1041B-17		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>								
$t_{power}$	$V_{CC}$ (typical) to the First Access <sup>[5]</sup>	1		1		1		$\mu$ s
$t_{RC}$	Read Cycle Time	12		15		17		ns
$t_{AA}$	Address to Data Valid		12		15		17	ns
$t_{OHA}$	Data Hold from Address Change	3		3		3		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		12		15		17	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		6		7		7	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z	0		0		0		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[6, 7]</sup>		6		7		7	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[7]</sup>	3		3		3		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup>		6		7		7	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down		12		15		17	ns
$t_{DBE}$	Byte Enable to Data Valid		6		7		7	ns
$t_{LZBE}$	Byte Enable to Low Z	0		0		0		ns
$t_{HZBE}$	Byte Disable to High Z		6		7		7	ns
<b>Write Cycle<sup>[8, 9]</sup></b>								
$t_{WC}$	Write Cycle Time	12		15		17		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	10		12		14		ns
$t_{AW}$	Address Set-Up to Write End	10		12		14		ns
$t_{HA}$	Address Hold from Write End	0		0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	10		12		14		ns
$t_{SD}$	Data Set-Up to Write End	7		8		8		ns
$t_{HD}$	Data Hold from Write End	0		0		0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[7]</sup>	3		3		3		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[6, 7]</sup>		6		7		7	ns
$t_{BW}$	Byte Enable to End of Write	10		12		12		ns

**Notes:**

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- This part has a voltage regulator which steps down the voltage from 5V to 3.3V internally.  $t_{power}$  time has to be provided initially before a read/write operation is started.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW, and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle no. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

**Switching Characteristics<sup>[4]</sup> Over the Operating Range (continued)**

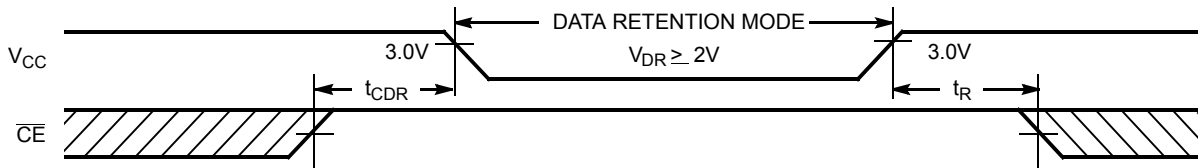
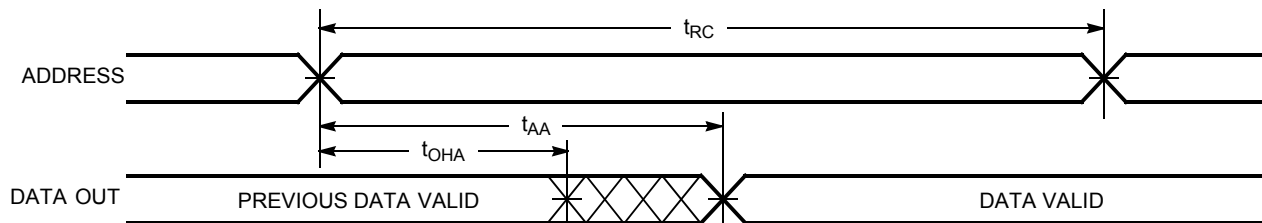
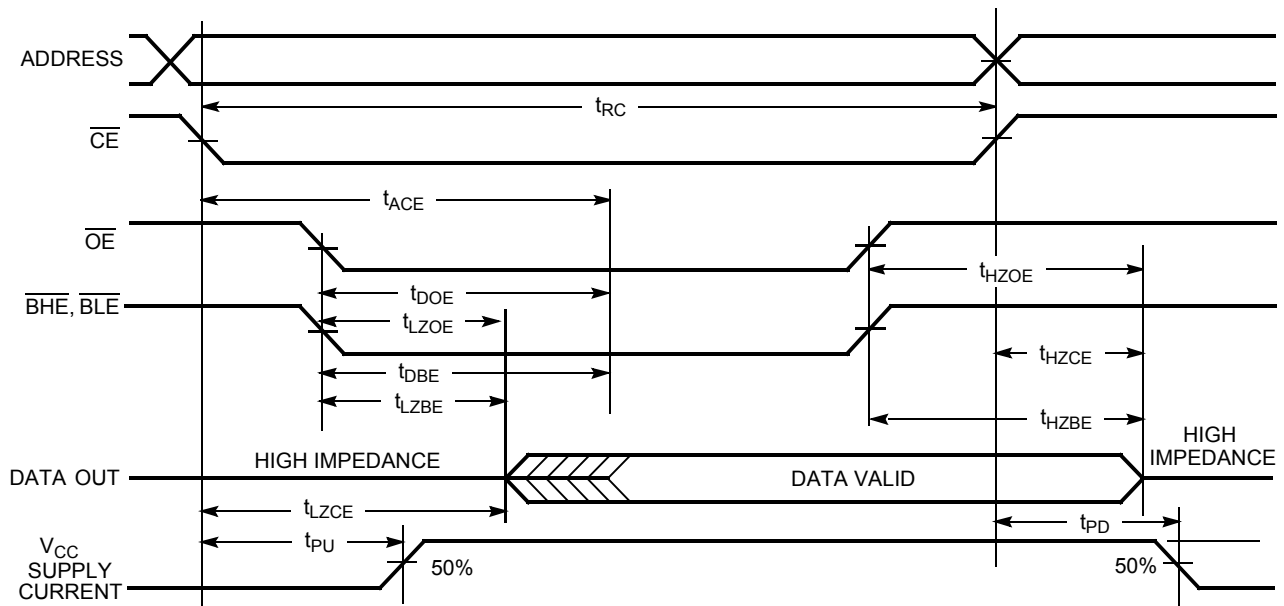
Parameter	Description	7C1041B-20		7C1041B-25		Unit
		Min.	Max.	Min.	Max.	
<b>Read Cycle</b>						
$t_{power}$	$V_{CC}$ (typical) to the First Access <sup>[5]</sup>	1		1		$\mu$ s
$t_{RC}$	Read Cycle Time	20		25		ns
$t_{AA}$	Address to Data Valid		20		25	ns
$t_{OHA}$	Data Hold from Address Change	3		5		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		20		25	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		8		10	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z	0		0		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[6, 7]</sup>		8		10	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[7]</sup>	3		5		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup>		8		10	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0		0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down		20		25	ns
$t_{DBE}$	Byte Enable to Data Valid		8		10	ns
$t_{LZBE}$	Byte Enable to Low Z	0		0		ns
$t_{HZBE}$	Byte Disable to High Z		8		10	ns
<b>WRITE CYCLE<sup>[8, 9]</sup></b>						
$t_{WC}$	Write Cycle Time	20		25		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	13		15		ns
$t_{AW}$	Address Set-Up to Write End	13		15		ns
$t_{HA}$	Address Hold from Write End	0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	13		15		ns
$t_{SD}$	Data Set-Up to Write End	9		10		ns
$t_{HD}$	Data Hold from Write End	0		0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[7]</sup>	3		5		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[6, 7]</sup>		8		10	ns
$t_{EW}$	Byte Enable to End of Write	13		15		ns

**Data Retention Characteristics Over the Operating Range (L version only)**

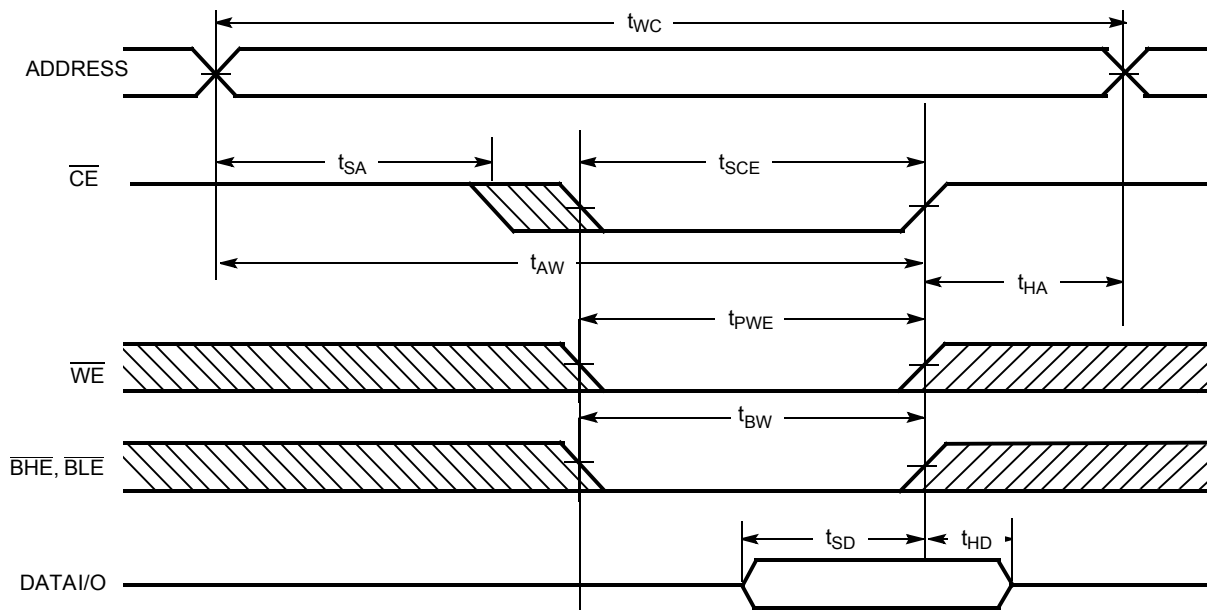
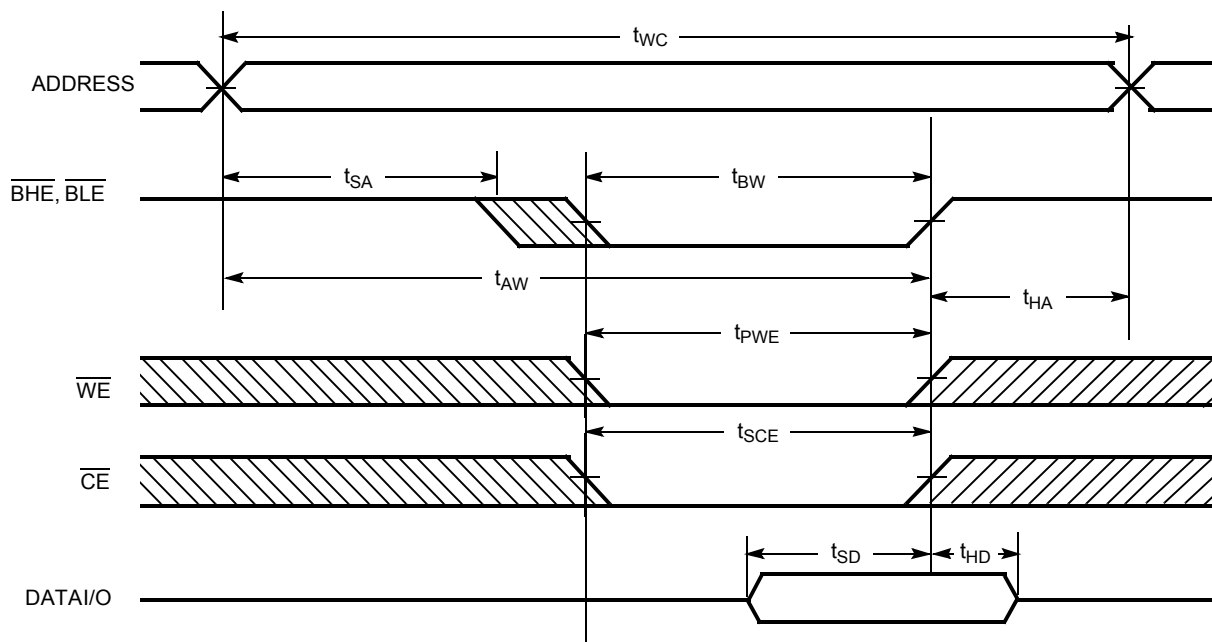
Parameter	Description			Conditions <sup>[11]</sup>	Min.	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention				2.0		V
$I_{CCDR}$	Data Retention Current	Com'l	L	$V_{CC} = V_{DR} = 3.0V$ , $CE \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		200	mA
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time				0		ns
$t_R^{[10]}$	Operation Recovery Time				$t_{RC}$		ns

**Notes:**

10.  $t_r \leq 3$  ns for the -12 and -15 speeds.  $t_r \leq 5$  ns for the -20 and slower speeds.  
 11. No input may exceed  $V_{CC} + 0.5V$ .

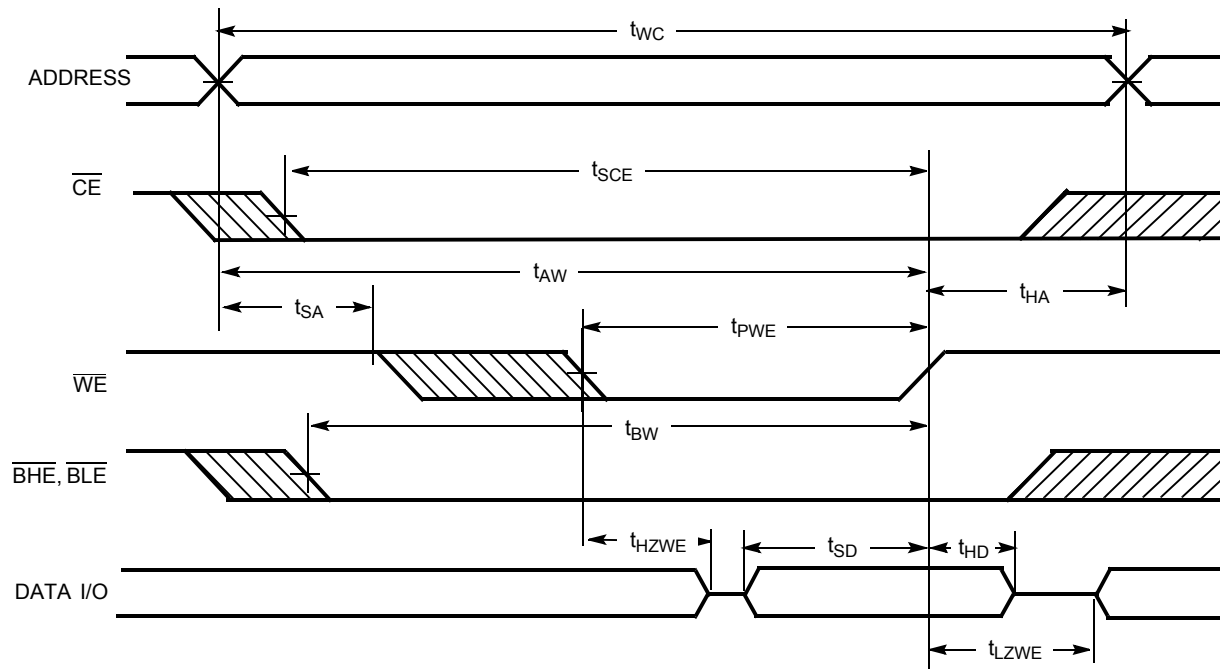
**Data Retention Waveform**

**Switching Waveforms**
**Read Cycle No. 1<sup>[12, 13]</sup>**

**Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[13, 14]</sup>**

**Notes:**

12. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$ , and/or  $\overline{BLE}$  =  $V_{IL}$ .
13. WE is HIGH for read cycle.
14. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)<sup>[15, 16]</sup>**

**Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)**

**Notes:**

15. Data I/O is high impedance if  $\overline{\text{OE}}$  or  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = V_{IH}$ .
16. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.

**Switching Waveforms** (continued)

**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)**

**Truth Table**

CE	OE	WE	BLE	BHE	I/O <sub>0</sub> -I/O <sub>7</sub>	I/O <sub>8</sub> -I/O <sub>15</sub>	Mode	Power
H	X	X	X	X	High Z	High Z	Power Down	Standby ( $I_{SB}$ )
L	L	H	L	L	Data Out	Data Out	Read All bits	Active ( $I_{CC}$ )
L	L	H	L	H	Data Out	High Z	Read Lower bits only	Active ( $I_{CC}$ )
L	L	H	H	L	High Z	Data Out	Read Upper bits only	Active ( $I_{CC}$ )
L	X	L	L	L	Data In	Data In	Write All bits	Active ( $I_{CC}$ )
L	X	L	L	H	Data In	High Z	Write Lower bits only	Active ( $I_{CC}$ )
L	X	L	H	L	High Z	Data In	Write Upper bits only	Active ( $I_{CC}$ )
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

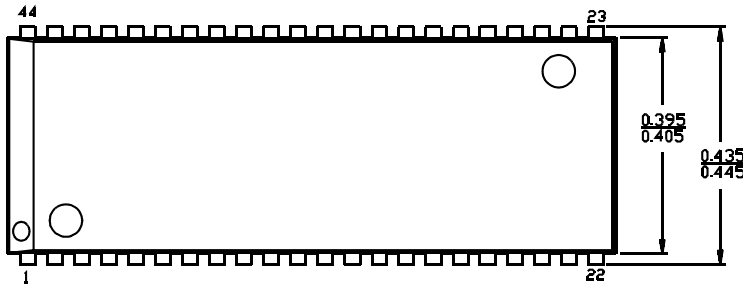


**Ordering Information**

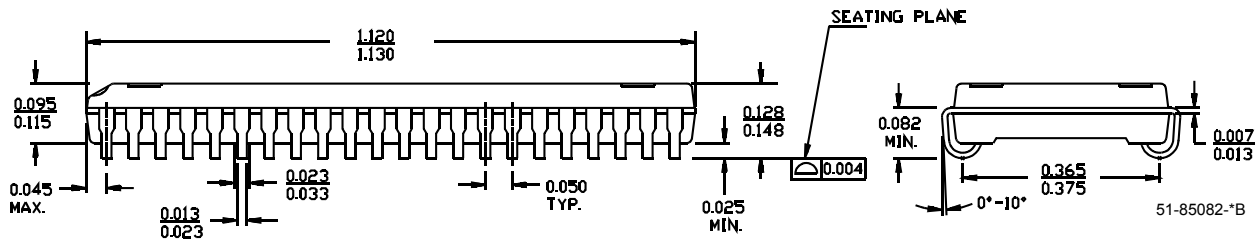
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1041B-12VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1041B-12VXC	V34	44-Lead (400-Mil) Molded SOJ (Pb-free)	
	CY7C1041B-12ZC	Z44	44-Lead TSOP Type II	
	CY7C1041B-12ZXC	Z44	44-Lead TSOP Type II (Pb-free)	
15	CY7C1041B-15VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1041B-15VXC	V34	44-Lead (400-Mil) Molded SOJ (Pb-free)	
	CY7C1041BL-15VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1041B-15ZC	Z44	44-Lead TSOP Type II	
	CY7C1041B-15ZXC	Z44	44-Lead TSOP Type II (Pb-free)	
	CY7C1041BL-15ZC	Z44	44-Lead TSOP Type II	
17	CY7C1041B-17VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1041BL-17VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1041B-17ZC	Z44	44-Lead TSOP Type II	
	CY7C1041BL-17ZC	Z44	44-Lead TSOP Type II	
20	CY7C1041B-20VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1041B-20VXC	V34	44-Lead (400-Mil) Molded SOJ (Pb-free)	
	CY7C1041BL-20VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1041BL-20VXC	V34	44-Lead (400-Mil) Molded SOJ (Pb-free)	
	CY7C1041B-20ZC	Z44	44-Lead TSOP Type II	
	CY7C1041B-20ZXC	Z44	44-Lead TSOP Type II (Pb-free)	
25	CY7C1041B-25VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1041BL-25VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1041B-25ZC	Z44	44-Lead TSOP Type II	
	CY7C1041BL-25ZC	Z44	44-Lead TSOP Type II	
15	CY7C1041B-15ZI	Z44	44-Lead TSOP Type II	Industrial
	CY7C1041B-15ZXI	Z44	44-Lead TSOP Type II (Pb-free)	
	CY7C1041B-15VI	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1041B-15VXI	V34	44-Lead (400-Mil) Molded SOJ (Pb-free)	
17	CY7C1041B-17ZI	V34	44-Lead TSOP Type II	
	CY7C1041B-17VI	Z44	44-Lead (400-Mil) Molded SOJ	
20	CY7C1041B-20ZI	Z44	44-Lead TSOP Type II	
	CY7C1041B-20ZXI	Z44	44-Lead TSOP Type II (Pb-free)	
	CY7C1041B-20VI	Z44	44-Lead (400-Mil) Molded SOJ	
	CY7C1041B-20VXI	Z44	44-Lead (400-Mil) Molded SOJ (Pb-free)	
25	CY7C1041B-25ZI	Z44	44-Lead TSOP Type II	
	CY7C1041B-25VI	Z44	44-Lead (400-Mil) Molded SOJ	

Package Diagrams

44-Lead (400-Mil) Molded SOJ V34

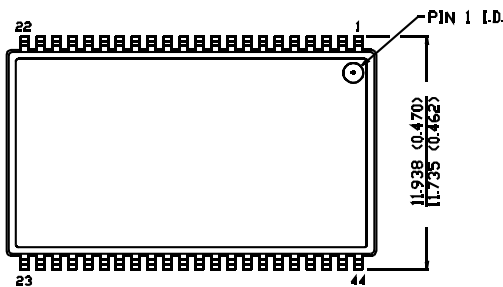


DIMENSIONS IN INCHES MIN. MAX.

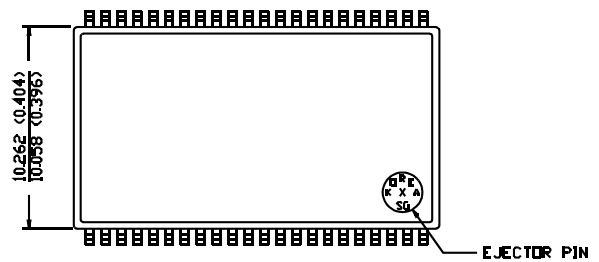


44-Pin TSOP II Z44

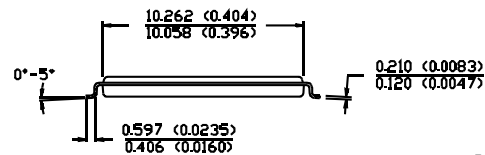
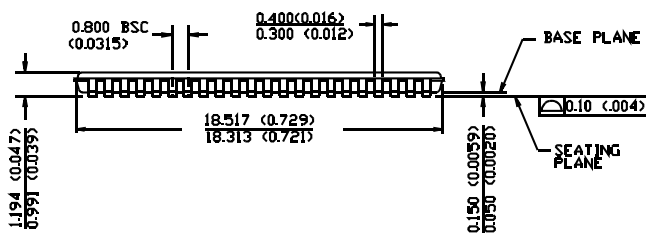
DIMENSION IN MM (INCH) MAX MIN.



TOP VIEW



BOTTOM VIEW



51-85087-A

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**Document History Page**

<b>Document Title: CY7C1041B 256K x 16 Static RAM</b> <b>Document Number: 38-05142</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	109886	09/15/01	SZV	Change from Spec number: 38-00938 to 38-05142
*A	341401	See ECN	AJU	Added Pb-free ordering information