

# MC100ELT23

## 5 V Dual Differential PECL to TTL Translator

### Description

The MC100ELT23 is a dual differential PECL to TTL translator. Because PECL (Positive ECL) levels are used, only +5 V and ground are required. The small outline 8-lead package and the dual gate design of the ELT23 makes it ideal for applications which require the translation of a clock and a data signal.

The PECL inputs are differential; therefore, the MC100ELT23 can accept any standard differential PECL input referenced from a  $V_{CC}$  of 5.0 V.

### Features

- 3.5 ns Typical Propagation Delay
- 24 mA TTL Outputs
- Flow Through Pinouts
- The 100 Series Contains Temperature Compensation
- Operating Range  $V_{CC} = 4.75$  V to 5.25 V with  $GND = 0$  V
- Internal Input 50 K $\Omega$  Pulldown Resistors
- Pb-Free Packages are Available



**ON Semiconductor®**

<http://onsemi.com>

### MARKING DIAGRAMS\*



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
M = Date Code  
▪ = Pb-Free Package

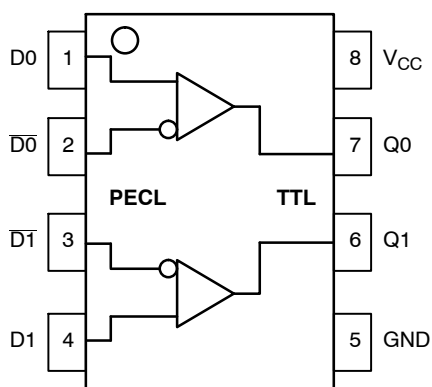
(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

# MC100ELT23



**Table 1. PIN DESCRIPTION**

Pin	Function
Qn	TTL Outputs
Dn, $\bar{D}n$	PECL Differential Inputs
V <sub>CC</sub>	Positive Supply
GND	Ground
EP	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

**Figure 1.8—Lead Pinout (Top View) and Logic Diagram**

**Table 2. ATTRIBUTES**

Characteristics	Value	
Internal Input Pulldown Resistor	50 k $\Omega$	
Internal Input Pullup Resistor	N/A	
ESD Protection	Human Body Model	> 2 kV
	Machine Model	> 400 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb Pkg	Pb-Free Pkg
	SOIC-8	Level 1
	TSSOP-8	Level 1
	DFN8	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	91 Devices	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

**Table 3. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	Power Supply	GND = 0 V		7	V
V <sub>I</sub>	Input Voltage	GND = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub>	0 to 6	V
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm	SOIC-8	190	°C/W
		500 lfpm	SOIC-8	130	°C/W
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-8	41 to 44	°C/W
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm	TSSOP-8	185	°C/W
		500 lfpm	TSSOP-8	140	°C/W
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44 ± 5%	°C/W
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm	DFN8	129	°C/W
		500 lfpm	DFN8	84	°C/W
T <sub>sol</sub>	Wave Solder	Pb	<2 to 3 sec @ 248°C	265	°C
		Pb-Free	<2 to 3 sec @ 260°C	265	°C
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	(Note 2)	DFN8	35 to 40	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

# MC100ELT23

**Table 4. PECL INPUT DC CHARACTERISTICS**  $V_{CC} = 5.0\text{ V}$ ;  $GND = 0.0\text{ V}$  (Note 3)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{IH}$	Input HIGH Voltage (Single-Ended) (Note 4)	3835		4120	3835		4120	3835		4120	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	3190		3525	3190		3525	3190		3525	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 5)	2.2		5.0	2.2		5.0	2.2		5.0	V
$I_{IH}$	Input HIGH Current			255			175			175	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Input parameters vary 1:1 with  $V_{CC}$ .  $V_{CC}$  can vary  $\pm 0.25\text{ V}$ .

4. TTL output  $R_L = 500\ \Omega$  to GND.

5.  $V_{IHCMR}$  min varies 1:1 with GND,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$

**Table 5. TTL OUTPUT DC CHARACTERISTICS**  $V_{CC} = 4.75\text{ V}$  to  $5.25\text{ V}$ ;  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -3.0\text{ mA}$	2.4		(Note 6)	V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 24\text{ mA}$			0.5	V
$I_{CCH}$	Power Supply Current			23	33	mA
$I_{CCL}$	Power Supply Current			26	36	mA
$I_{OS}$	Output Short Circuit Current		-150		-60	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6. Max level is  $V_{CC} - 0.7\text{ V}$  by design.

**Table 6. AC CHARACTERISTICS**  $V_{CC} = 5.0\text{ V}$ ;  $GND = 0.0\text{ V}$  (Note 7 and Note 8)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Toggle Frequency					100					MHz
$t_{JITTER}$	Random Clock Jitter (RMS)					35					ps
$t_{PLH}$	Propagation Delay @ 1.5 V	2.0		5.5	2.0		5.5	2.0		5.5	ns
$t_{PHL}$	Propagation Delay @ 1.5 V	2.0		5.5	2.0		5.5	2.0		5.5	ns
$V_{PP}$	Input Swing (Note 9)	200		1000	200		1000	200		1000	mV
$t_r/t_f$	Output Rise Time (10–90%) Output Fall Time (10–90%)					1.6 1.1					ns ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7.  $V_{CC}$  can vary  $\pm 0.25\text{ V}$ .

8. TTL output  $R_L = 500\ \Omega$  to GND, and  $C_L = 20\text{ pF}$  to GND. Refer to Figure 2.

9.  $V_{PP}(\text{min})$  is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of  $\approx 40$ .

## MC100ELT23

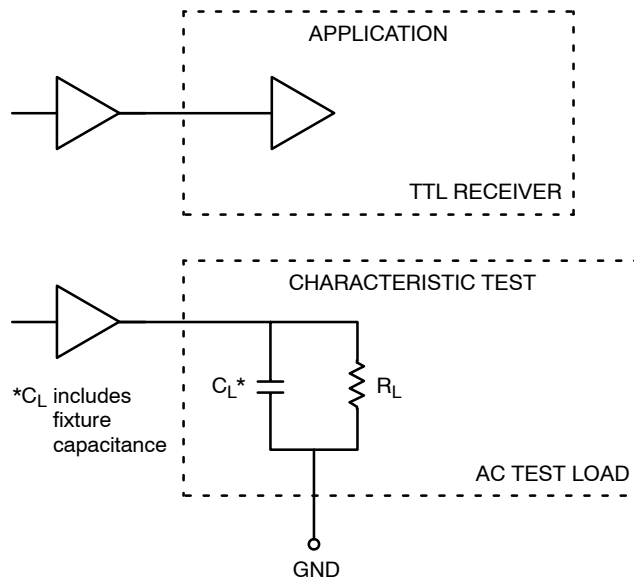


Figure 2. TTL Output Loading Used for Device Evaluation

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC100ELT23D	SOIC-8	98 Units / Rail
MC100ELT23DG	SOIC-8 (Pb-Free)	98 Units / Rail
MC100ELT23DR2	SOIC-8	2500 / Tape & Reel
MC100ELT23DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC100ELT23DT	TSSOP-8	100 Units / Rail
MC100ELT23DTG	TSSOP-8 (Pb-Free)	100 Units / Rail
MC100ELT23DTR2	TSSOP-8	2500 / Tape & Reel
MC100ELT23DTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel
MC100ELT23MNR4	DFN8	1000 / Tape & Reel
MC100ELT23MNR4G	DFN8 (Pb-Free)	1000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## MC100ELT23

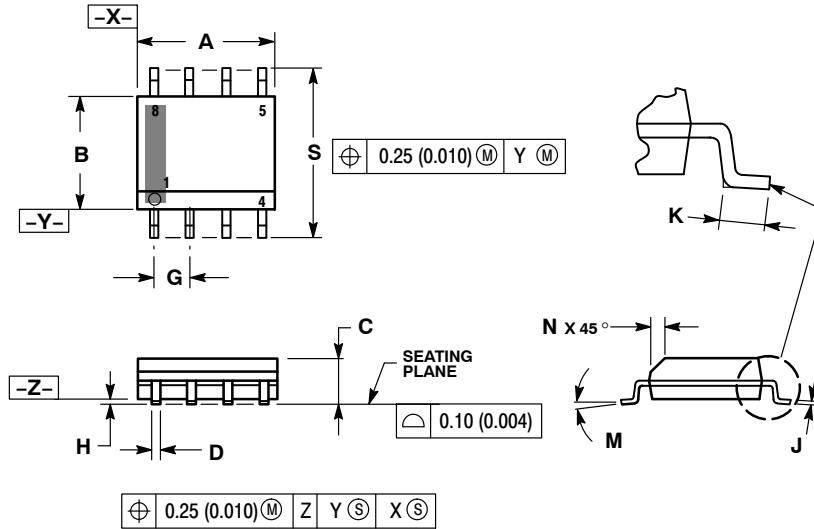
### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

# MC100ELT23

## PACKAGE DIMENSIONS

SOIC-8 NB  
CASE 751-07  
ISSUE AH

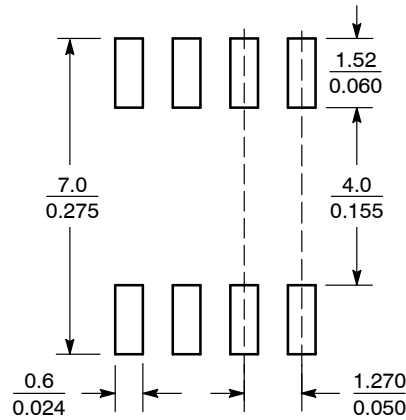


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



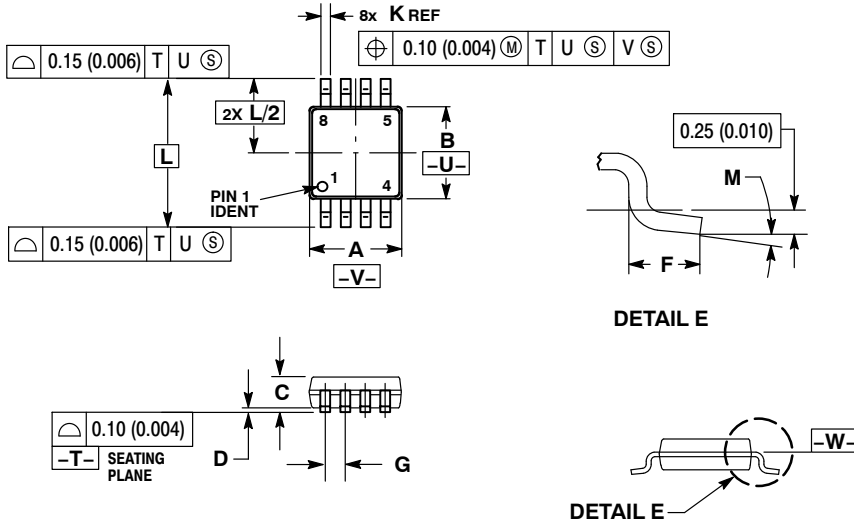
SCALE 6:1  $\left(\frac{\text{mm}}{\text{inches}}\right)$

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC100ELT23

## PACKAGE DIMENSIONS

TSSOP-8  
DT SUFFIX  
PLASTIC TSSOP PACKAGE  
CASE 948R-02  
ISSUE A



### NOTES:

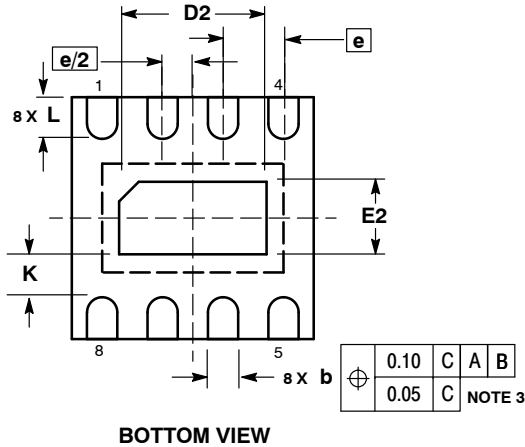
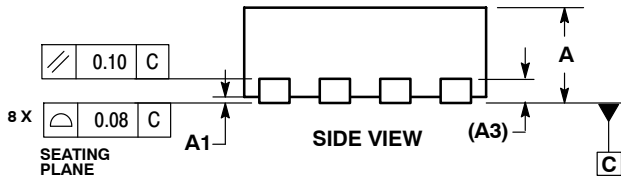
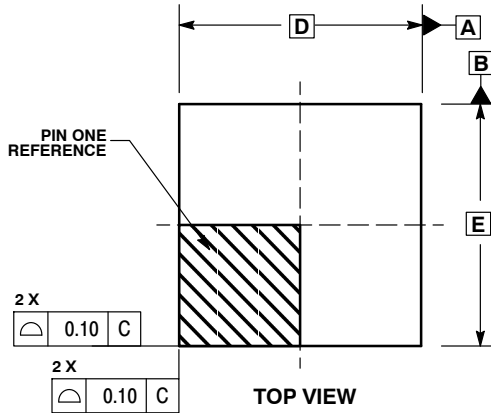
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

# MC100ELT23

## PACKAGE DIMENSIONS

DFN8  
CASE 506AA-01  
ISSUE D



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.00 BSC	
E2	0.70	0.90
e	0.50 BSC	
K	0.20	---
L	0.25	0.35

ECLinPS is a trademark of Semiconductor Components Industries, LLC (SCILLC).

**ON Semiconductor** and **ON** are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local Sales Representative

MC100ELT23/D