Winbond
ACPI Controller
W83304D
W83304G
For AMD Claw Hammer ™ CPU

W83304D
Data Sheet Revision History

	PAGES	DATES	VERSION	VERSION ON WEB	MAIN CONTENTS
1		June/04	0.50	N/A	Preliminary Version
2		April/06	0.51	N/A	Add Pb-free part no of W83304G
3					
4					
5					
6					
7					
8					

LIFE SUPPORT APPLICATIONS

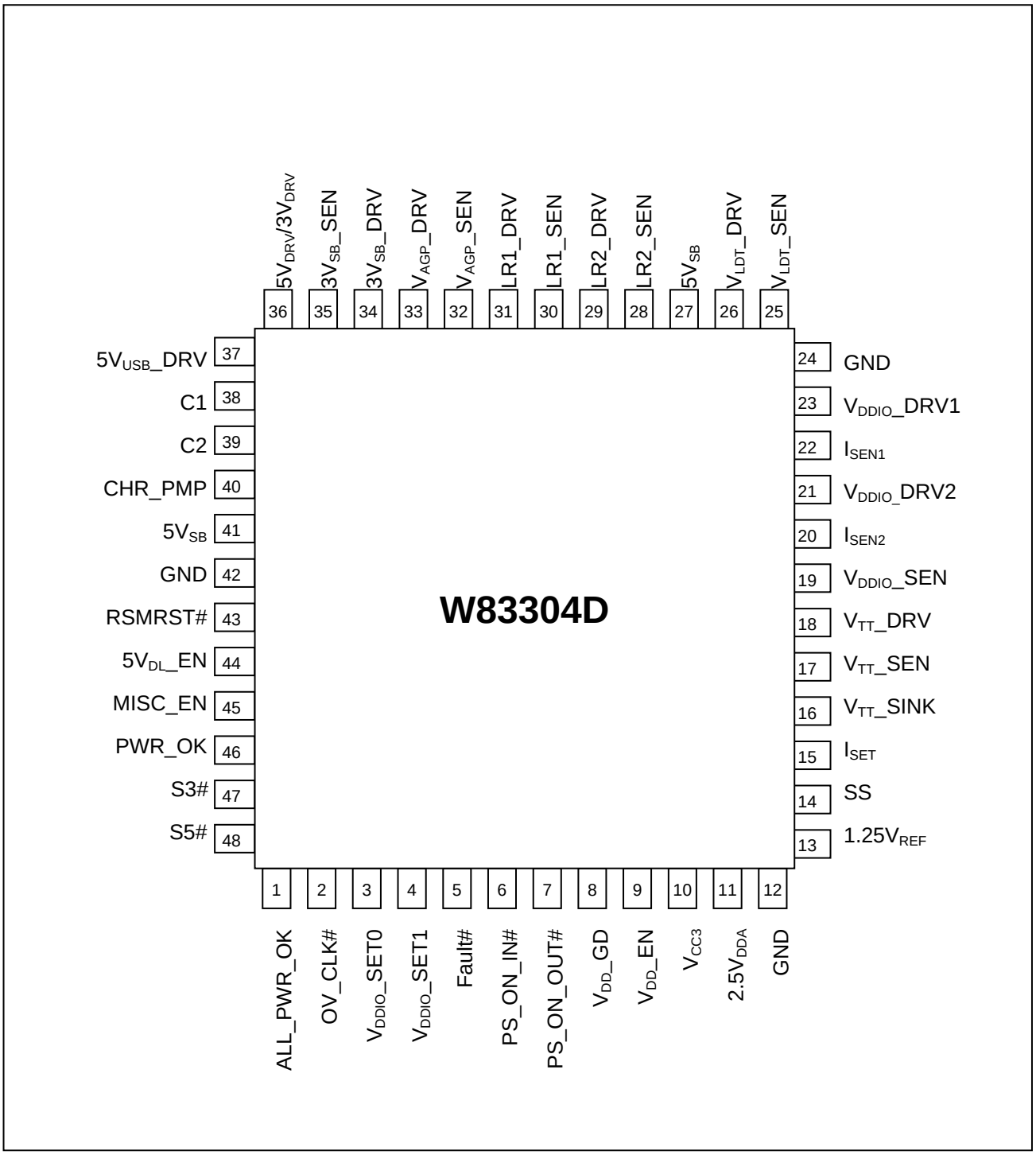
These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

Table of Content-

1. GENERAL FUNCTION DESCRIPTION

- Provides Powers
  - 5V Active/Sleep ($5V_{DL}$)
  - Provide a switch $5V_{DLEN}$ pin to enable/disable $5V_{DL}$ output in S5 state for USB application.
  - 3.3V Active/Sleep (3.3VDUAL)
  - Dual-Channel 2.5V Active/Sleep (2.5VSTR) for DDR
  - 1.5V for AGP 4X/8X Voltage
  - Two 1.25V~5V Linear Voltage Regulators Support VCC/VSTR/VDL/VSB Voltages
  - 1.25V DDR Bus Termination Regulated Voltage
  - 1.2V VLDT for AMD_K8 CPU Hyper transport.
  - 2.5VDDA for AMD_K8 PLL.
  - 1.25VREF for AMD_K8 reference.
  - Up to 0.3V/0.1V incremental voltage on DDR RAM for over-clocking application.
- Provides Signals for ATX Power Supply PS_ON# Control
- Support AMD K8 Claw Hammer Specific Power Up/Down Sequence
- Provides fault signal control.
- Internal Charge Pump Support Up to 9.5VSB
- Drive All N-Channel MOSFET
- Soft Start
- Under-Voltage Monitoring for VAGP, VRAM, VLDT, 3.3VDUAL Channels

2. PIN-OUT


W83304D
1 ALL_PWR_OK
2 OV_CLK#
3 VDDIO_SET0
4 VDDIO_SET1
5 Fault#
6 PS_ON_IN#
7 PS_ON_OUT#
8 VDD_GD
9 VDD_EN
10 VCC3
11 2.5VDDA
12 GND
13 1.25VREF
14 SS
15 ISET
16 VTT_SINK
17 VTT_SEN
18 VTT_DRV
19 VDDIO_SEN
20 ISEN2
21 VDDIO_DRV2
22 ISEN1
23 VDDIO_DRV1
24 GND
25 VLDT_SEN
26 VLDT_DRV
27 5VSB
28 LR2_SEN
29 LR2_DRV
30 LR1_SEN
31 LR1_DRV
32 VAGP_SEN
33 VAGP_DRV
34 3VSB_DRV
35 3VSB_SEN
36 5VDRV/3VDRV
37 5VUSB_DRV
38 C1
39 C2
40 CHR_PMP
41 5VSB
42 GND
43 RSMRST#
44 5VDL_EN
45 MISC_EN
46 PWR_OK
47 S3#
48 S5#

3. PIN DESCRIPTIONS

I/O_{12t} - TTL level bi-directional pin with 12 mA source-sink capability,open drain output
I/O_{12ts} - TTL level and schmitt trigger
O_{12} - Output pin with 12 mA source-sink capability
AO_{12} - Output pin(Analog) with 12mA capability
OD_{12} - Open-drain output pin with 12 mA sink capability
IN_t - TTL level input pin
IN_{ts} - TTL level input pin and schmitt trigger
AIN - Input pin(Analog)

<table>
<tr><th>NO</th><th>NAME</th><th>I/O</th><th>POWER SOURCE</th><th>FUNCTION DESCRIPTION</th></tr>
<tr><td>1</td><td>ALL_PWR_OK</td><td>OD_{24}</td><td>5VSB</td><td>Power OK Signal. The signal is drove high to indicate all power ready.</td></tr>
<tr><td>2</td><td>OV_CLK#</td><td>I</td><td>5VSB</td><td>H/W Trapping Pin for Over-Clocking Application.
1: Normal
0: +50mV is added on All regulated powers (V_{DDIO}, V_{DDA}, V_{AGP}, V_{LDT}, $1.25V_{REF}$).</td></tr>
<tr><td>3</td><td>V_{DDIO}_SET0</td><td>I_{ts}</td><td>5VSB</td><td rowspan="2">VDDIO Output Voltage Setting Pin.
V_{DDIO} output with OV_CLK# = High
<table>
<tr><th></th><th>V_{DDIO}_SET1</th><th>V_{DDIO}_SET0</th></tr>
<tr><td>2.5V</td><td>0</td><td>0</td></tr>
<tr><td>2.6V</td><td>0</td><td>1</td></tr>
<tr><td>2.7V</td><td>1</td><td>0</td></tr>
<tr><td>2.8V</td><td>1</td><td>1</td></tr>
</table>
V_{DDIO} output with OV_CLK# = Low
<table>
<tr><th></th><th>VRAMSET1</th><th>VRAMSET0</th></tr>
<tr><td>2.55V</td><td>0</td><td>0</td></tr>
<tr><td>2.65V</td><td>0</td><td>1</td></tr>
<tr><td>2.75V</td><td>1</td><td>0</td></tr>
<tr><td>2.85V</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>4</td><td>V_{DDIO}_SET1</td><td>I_{ts}</td><td>5VSB</td></tr>
<tr><td>5</td><td>Fault#</td><td>I_{ts}</td><td></td><td>System Fault Input Signal.
Pull the pin low when any critical event alerted; the chip will shut the system down when the signal pulled low.</td></tr>
<tr><td>6</td><td>PS_ON_IN#</td><td>I_{ts}</td><td></td><td rowspan="2">ATX PS_ON# Signal Input.
The PS_ON# signal of ATX power supply is routed through the chip for power fault control.</td></tr>
<tr><td>7</td><td>PS_ON_OUT#</td><td>OD_{12}</td><td></td></tr>
</table>

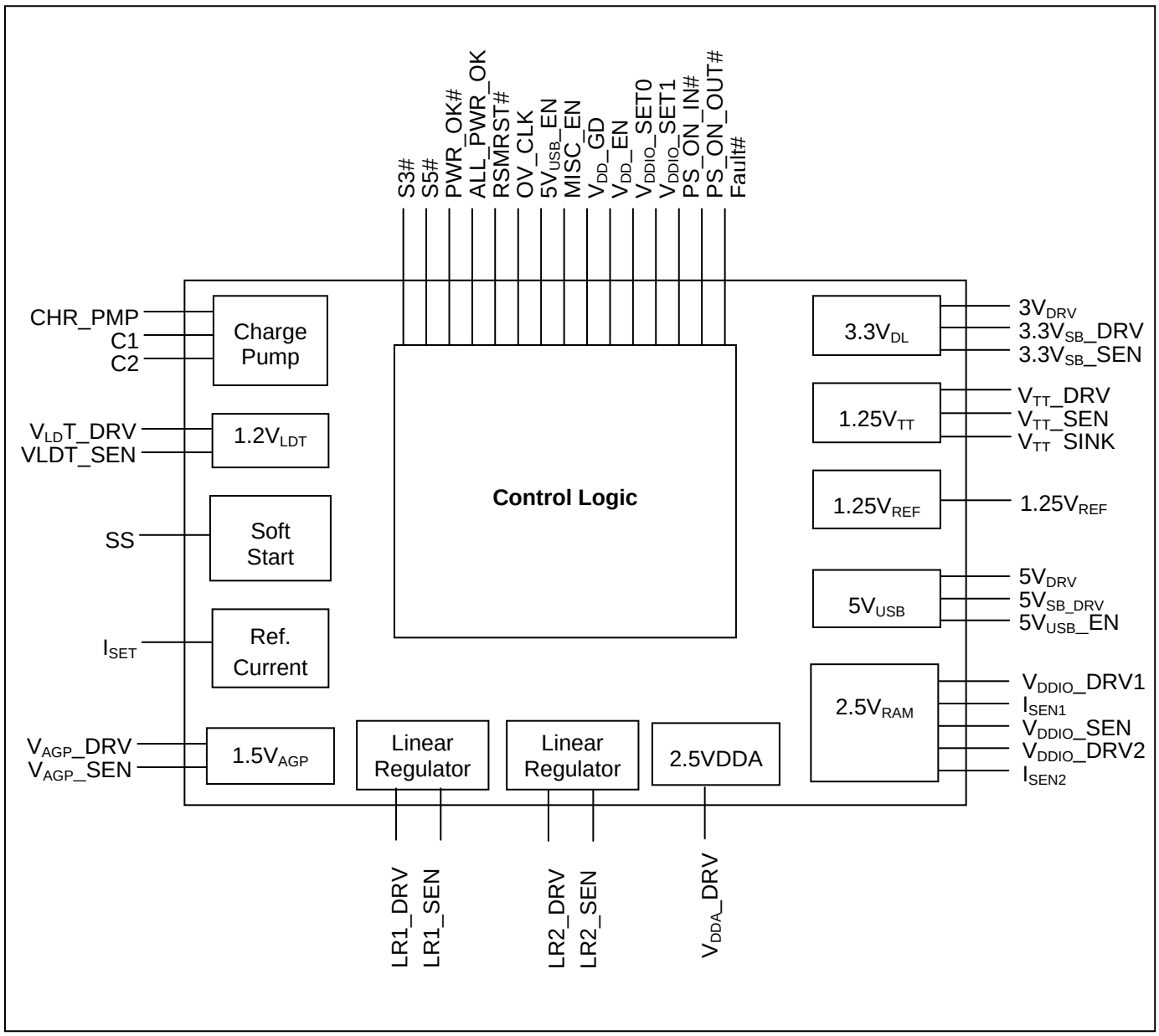
Pin Descriptions, continued

NO	NAME	I/O	POWER SOURCE	FUNCTION DESCRIPTION
8	V_{DD}_GD	I	5VSB	**CPU Power Good Signal.** The signal is inputted for power sequence control.
9	V_{DD}_EN	OD_{24}	5VSB	**Signal Output to Enable CPU Power.** The signal output to enable CPU power for sequence control.
10	V_{CC3}	P		**Power V_{CC}.**
11	$2.5V_{DDA}$	AO_{200mA}	VCC3	**2.5V Power for CPU PLL Core.**
12	GND	P		**Power Ground.**
13	$1.25V_{REF}$	AO_{5mA}	3VSB	**1.25V Reference Voltage.**
14	SS	AI/AO	5VSB	**Soft-Start Pin.** A capacitor (0.1u) is attached in this pin for soft-start slope rate adjustment.
15	I_{SET}	AI/AO	5VSB	**Reference Current Input.** An input current for internal circuit reference.
16	V_{TT}_SINK	AO	5VSB	**Power V_{TT}.** A bi-direction linear regulator is provided to regulate voltage for DDR bus terminator.
17	V_{TT}_SEN	AI	5VSB	
18	V_{TT}_DRV	AO	9VSB	
19	V_{DDIO}_SEN	AI	9VSB	**Power V_{DDIO}.** A dual-channels linear regulator with current balancing architecture is provided for higher current DDR SDRAM application.
20	I_{SEN2}	AI		
21	V_{DDIO}_DRV2	AO		
22	I_{SEN1}	AI		
23	V_{DDIO}_DRV1	AO		
24	GND	P		**Power Ground.**
25	V_{LDT}_SEN	AI	5VSB	**Power V_{LDT}.** 1.2V power for LDT bus.
26	V_{LDT}_DRV	AO	9VSB	
27	$5V_{SB}$	P		**Standby Power Pin.**
28	LR2_SEN	AI	5VSB	**Linear Regulator 1.** A general purpose linear regulator is provided to generate 1.2V~5.0V power for specific device.
29	LR2_DRV	AO	9VSB	
30	LR1_SEN	AI	5VSB	**Linear Regulator 2.** A general purpose linear regulator is provided to generate 1.2V~5.0V power for specific device.
31	LR1_DRV	AO	9VSB	

Pin Descriptions, continued

NO	NAME	I/O	POWER SOURCE	FUNCTION DESCRIPTION
32	V_{AGP}_SEN	AI	5VSB	**Power for AGP Core.** 1.5V power is regulated for AGP core.
33	V_{AGP}_DRV	AO	9VSB	
34	$3V_{SB}$_DRV	AO	9VSB	**Power 3.3V_{DL}.** A linear regulator and switch is combined to generate 3V dual power.
35	$3V_{SB}$_SEN	AI	5VSB	
36	$5V_{DRV}/3V_{DRV}$	AO	9VSB	
36	$5V_{DRV}/3V_{DRV}$	AO	9VSB	**Power for USB Device.** A 5V switch power is provided for USB device and can be programmed for various USB application with configuration of pin 44.
37	$5V_{USB}$_DRV	AO	9VSB	
38	C1	I	5VSB	**Charge Pump Pins.** It supports achieve 10mA driving current and insures output voltage 9.5V or above.
39	C2	I	5VSB	
40	CHR_PMP	P	5VSB	
41	$5V_{SB}$	P		**Standby Power Pin.**
42	GND			**Power Ground.**
43	RSMRST#	OD_{12}		**Signal to Indicate Status of Standby Power.** The signal will be pulled high to indicate the standby power stable.
44	$5V_{DL}$_EN	I	5VSB	**5VUSB Power Type Setting Pin.** $5V_{USB}$_EN=Low, support power for USB device in S0, S3 state. $5V_{USB}$_EN =High, support power for USB device in S0, S3, S5 state.
45	MISC_EN	OD_{24}	5VSB	**Signal to Enable Miscellaneous Power.**
46	PWR_OK	I_{ts}	5VSB	**Power OK Signal form ATX Power Supply.**
47	S3#	I		**ACPI Control Signals.**
48	S5#	I		

4. BLOCK DIAGRAM



5. ELECTRICAL SPECIFICATION

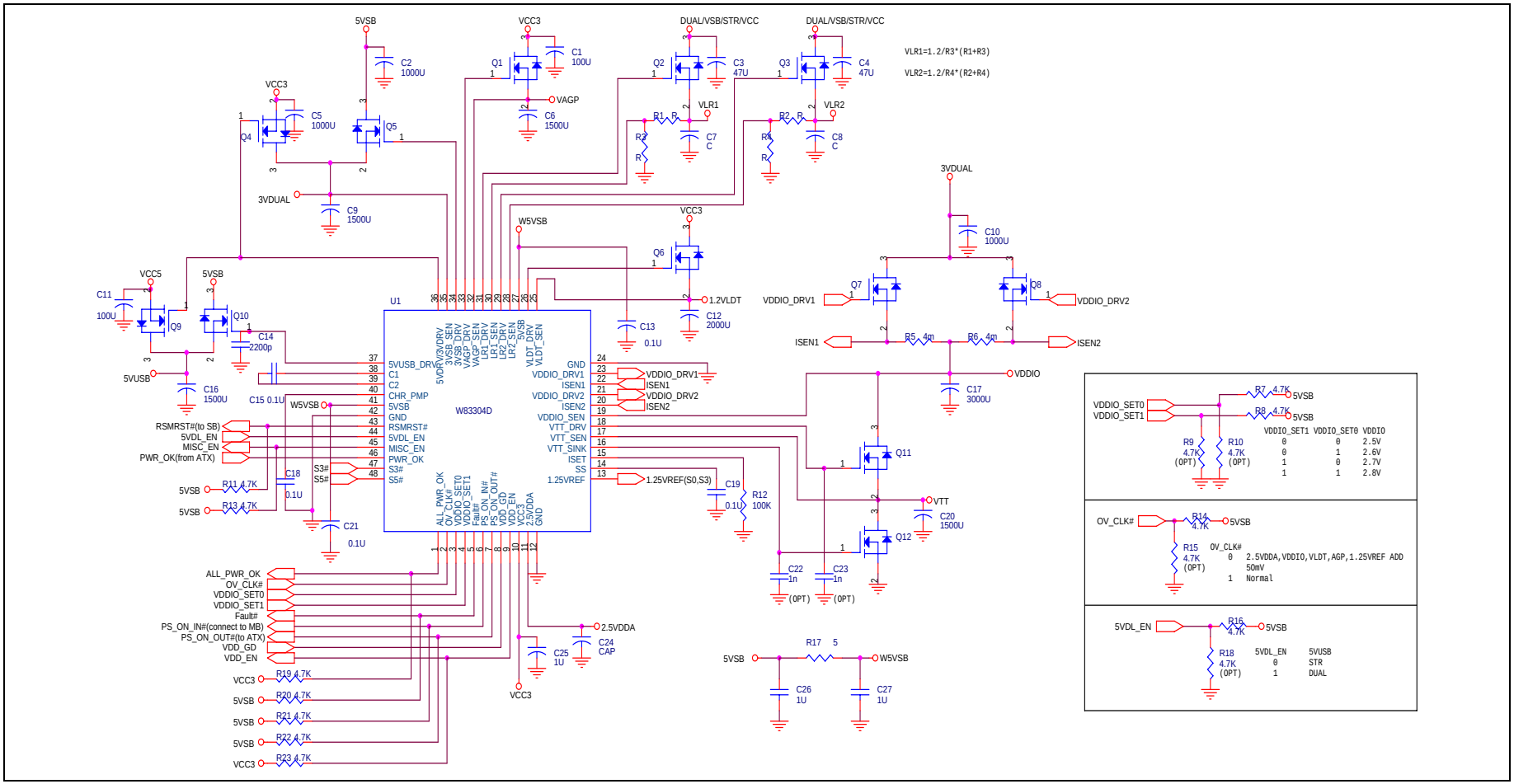
5.1 AC CHARACTERISTICS

<table>
<tr><td colspan="7">Vcc=5V ±5 %, T_A = 0℃ to +70℃</td></tr>
<tr><th>PARAMETER</th><th>SYMBOL</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNITS</th><th>TEST CONDITIONS</th></tr>
<tr><td colspan="7">VAGP Linear Regulator</td></tr>
<tr><td>Nominal Output Voltage</td><td></td><td></td><td>1.5</td><td></td><td>V</td><td>OVA#=1</td></tr>
<tr><td>Nominal Output Voltage</td><td></td><td></td><td>1.55</td><td></td><td>V</td><td>OVA#=0</td></tr>
<tr><td>Regulation</td><td></td><td></td><td></td><td>5</td><td>%</td><td></td></tr>
<tr><td>Under-Voltage Falling Threshold</td><td></td><td></td><td>86.67</td><td></td><td>%</td><td></td></tr>
<tr><td colspan="7">1.25VREF</td></tr>
<tr><td>Nominal Output Voltage</td><td></td><td></td><td>1.25</td><td></td><td></td><td>I_{load} < 5mA; OVA#=1</td></tr>
<tr><td>Nominal Output Voltage</td><td></td><td></td><td>1.3</td><td></td><td></td><td>I_{load} < 5mA; OVA#=0</td></tr>
<tr><td colspan="7">1.2VLDT Linear Regulator</td></tr>
<tr><td>Nominal Output Voltage</td><td></td><td></td><td>1.2</td><td></td><td>V</td><td>OVA#=1</td></tr>
<tr><td>Nominal Output Voltage</td><td></td><td></td><td>1.25</td><td></td><td>V</td><td>OVA#=0</td></tr>
<tr><td>Regulation</td><td></td><td></td><td></td><td>5</td><td>%</td><td></td></tr>
<tr><td>Under-Voltage Falling Threshold</td><td></td><td></td><td>87.5</td><td></td><td>%</td><td></td></tr>
<tr><td colspan="7">VDDIO Regulator</td></tr>
<tr><td>VRAMSET0</td><td colspan="6" rowspan="2">VDDIO VOLTAGE SETTING OVA#=1
<table><tr><th></th><th>VRAMSET1</th><th>VRAMSET0</th></tr><tr><td>2.5V</td><td>0</td><td>0</td></tr><tr><td>2.6V</td><td>0</td><td>1</td></tr><tr><td>2.7V</td><td>1</td><td>0</td></tr><tr><td>2.8V</td><td>1</td><td>1</td></tr></table></td></tr>
<tr><td>VRAMSET1</td></tr>
<tr><td colspan="6">VDDIO VOLTAGE SETTING OVA#=0
<table><tr><th></th><th>VRAMSET1</th><th>VRAMSET0</th></tr><tr><td>2.55V</td><td>0</td><td>0</td></tr><tr><td>2.65V</td><td>0</td><td>1</td></tr><tr><td>2.75V</td><td>1</td><td>0</td></tr><tr><td>2.85V</td><td>1</td><td>1</td></tr></table></td></tr>
<tr><td>Under-Voltage Falling Threshold</td><td></td><td></td><td>84</td><td></td><td>%</td><td></td></tr>
<tr><td>Regulation</td><td></td><td></td><td></td><td>5</td><td>%</td><td></td></tr>
</table>

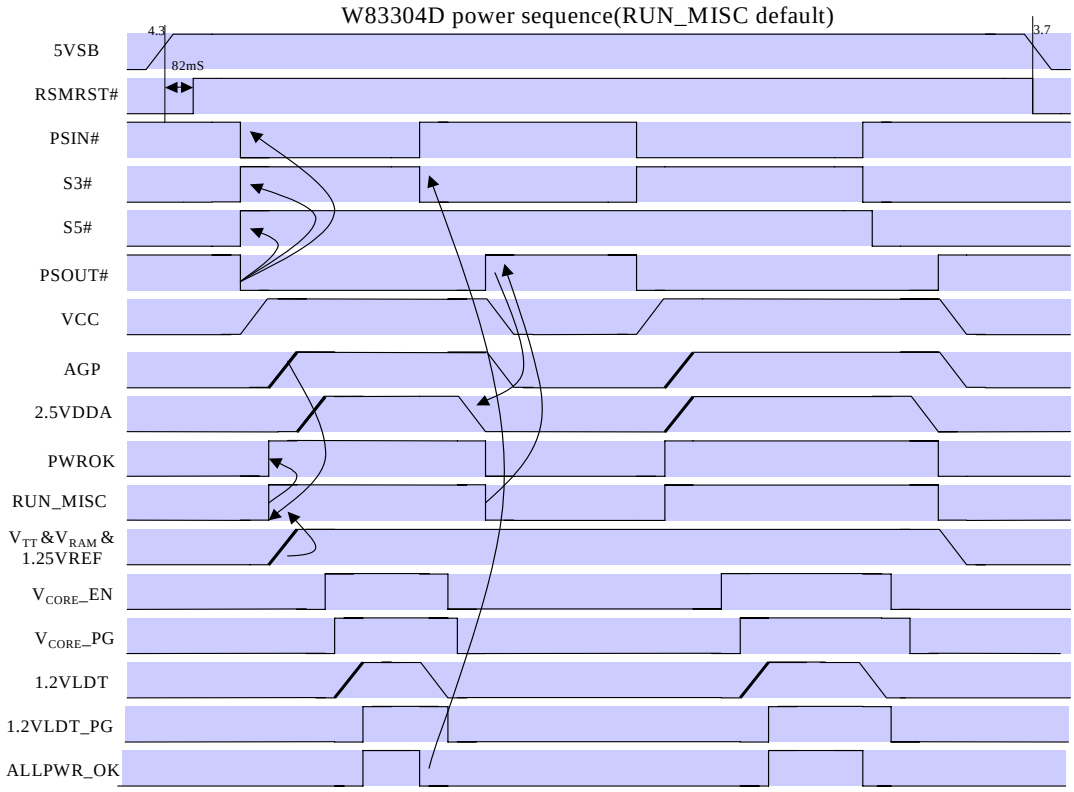
AC CHARACTERISTICS, continued

Vcc=5V ±5 %, T_A = 0℃ to +70℃						
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**TEST CONDITIONS**
2.5VDDA						
Nominal Output Voltage			2.5			I_{load} < 200mA; OVA#=1
Nominal Output Voltage			2.55			I_{load} < 200mA; OVA#=0
Bus Terminator						
Nominal Output Voltage / V(VRAM2.5_SEN)			50		%	Regulate a 1.25V for DDR bus termination Half of VDDIO voltage
Nominal Output Voltage			1.25		V	
5VDUAL Switch Controller						
5VDRV Output High Voltage		9				Cap Loading
5VSBDRV Output High Voltage		9				Cap Loading
5VUSB SS Sourcing Current			2.5		uA	@ Soft-start
3.3VDual						
Under-Voltage Falling Threshold			78.79		%	
5VDRV Output High Voltage		9			V	
3VSBDRV		3.3				Regulation
Charge Pump						
Charge Pump Frequency			180		KHz	
Charge Pump Voltage		9.5				
Two linear regulator						
Nominal Output Voltage	Linear regulator from1.2V~5V					

6. APPLICATION CIRCUIT



7. POWER SEQUENCE



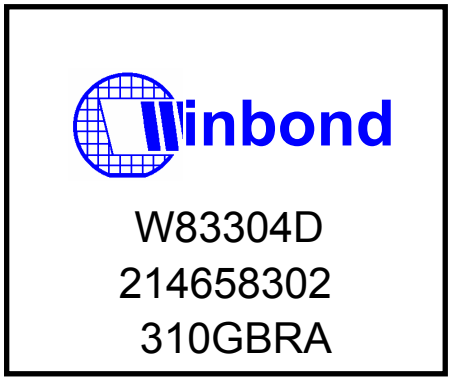
Note:

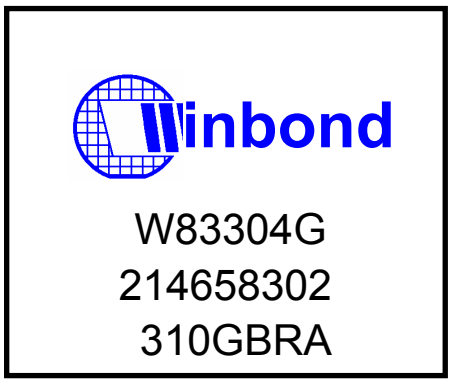
1. When at power up sequence, the delay time between adjacent power planes is 5ms after the previous power plane is power-good.
2. When at power down sequence, the delay time between adjacent power planes is 20ms after the previous power plane is power-down.
3. After 1.2VLDT_PG=H and delay 20ms, the ALLPWR_OK will be High(ALLPWR_OK=H).
4. All “LUV” detect is enabled after the power plane have power-good.

8. ORDERING INSTRUCTION

PART NO.	PACKAGE	REMARKS
W83304D	48-pin LQFP	
W83304G	48-pin LQFP	Pb-free package

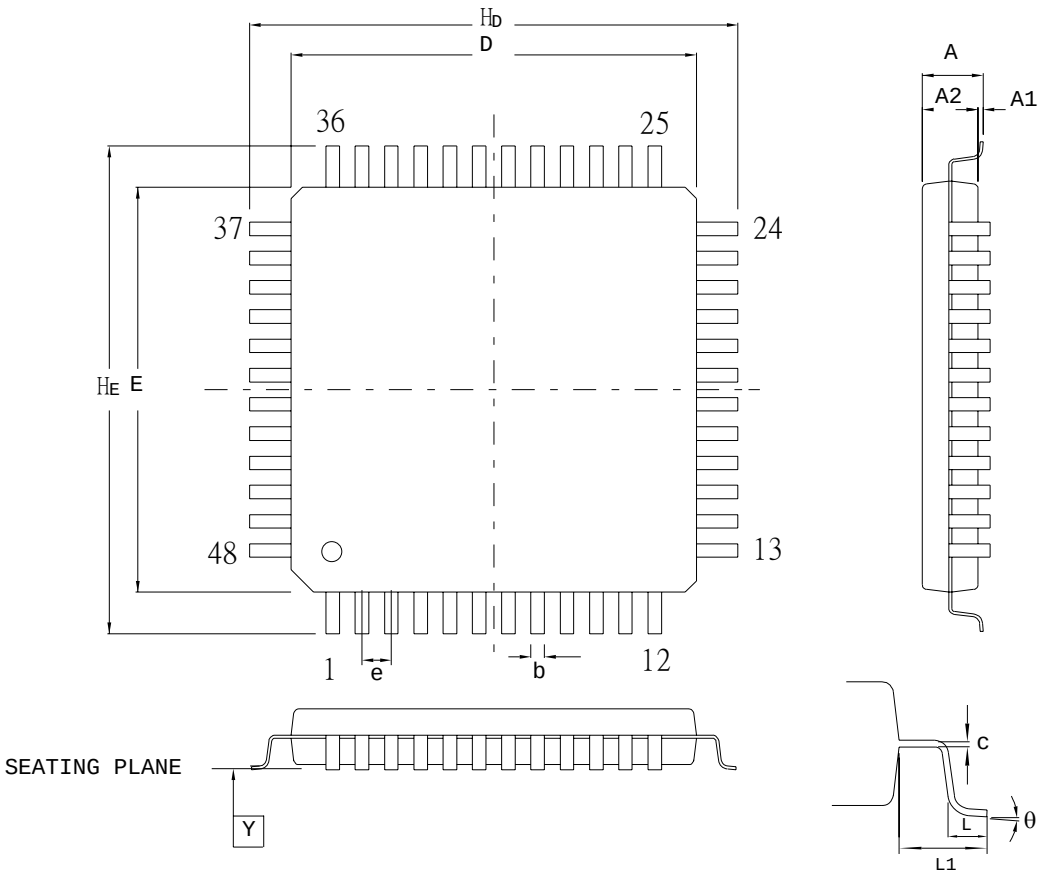
9. HOW TO READ THE TOP MARKING





1st Line: Winbond Logo
2nd Line: Part_No W83304D, W83304G (Pb-free package)
3rd Line: lot no
4th Line: tracking code 310GBRA
310：date code,310 means package was made in '03 week 10
G：Assembly ID, G means GR, A means ASE…etc.
B：Chip Version, A means version A, B means version B
RA：Winbond internal use

10. PACKAGE DIMENSION



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7 °	0°	—	7 °

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