SC2614
Complete DDR Power Solution With BF_CUT and PGOOD

POWER MANAGEMENT

Description

The SC2614 is a fully integrated DDR power solution providing power for the VDDQ and the VTT rails. The SC2614 also completely adheres to the ACPI sleep state power requirements. A synchronous buck controller provides the high current of the VDDQ at high efficiency, while a linear sink/source regulator provides the termination voltage with 2 Amp Source/Sink capability . This approach makes the best trade-off between cost and performance. Additional logic and UVLOs complete the functionality of this single chip DDR power solution in compliance with S3 and S5 motherboard signals. A **BF_CUT output signal** prevents Back Feeding Input Rail during S3 while a **PGOOD output** signals correct voltage Rails.

The SC2614 is capable of sourcing up to 20A at the switcher output, and 2A at the VTT output. The MLP package provides excellent thermal impedance while keeping small footprint. VDDQ current limit as well as 3 independent thermal shutdown circuits assure safe operation under all fault conditions.

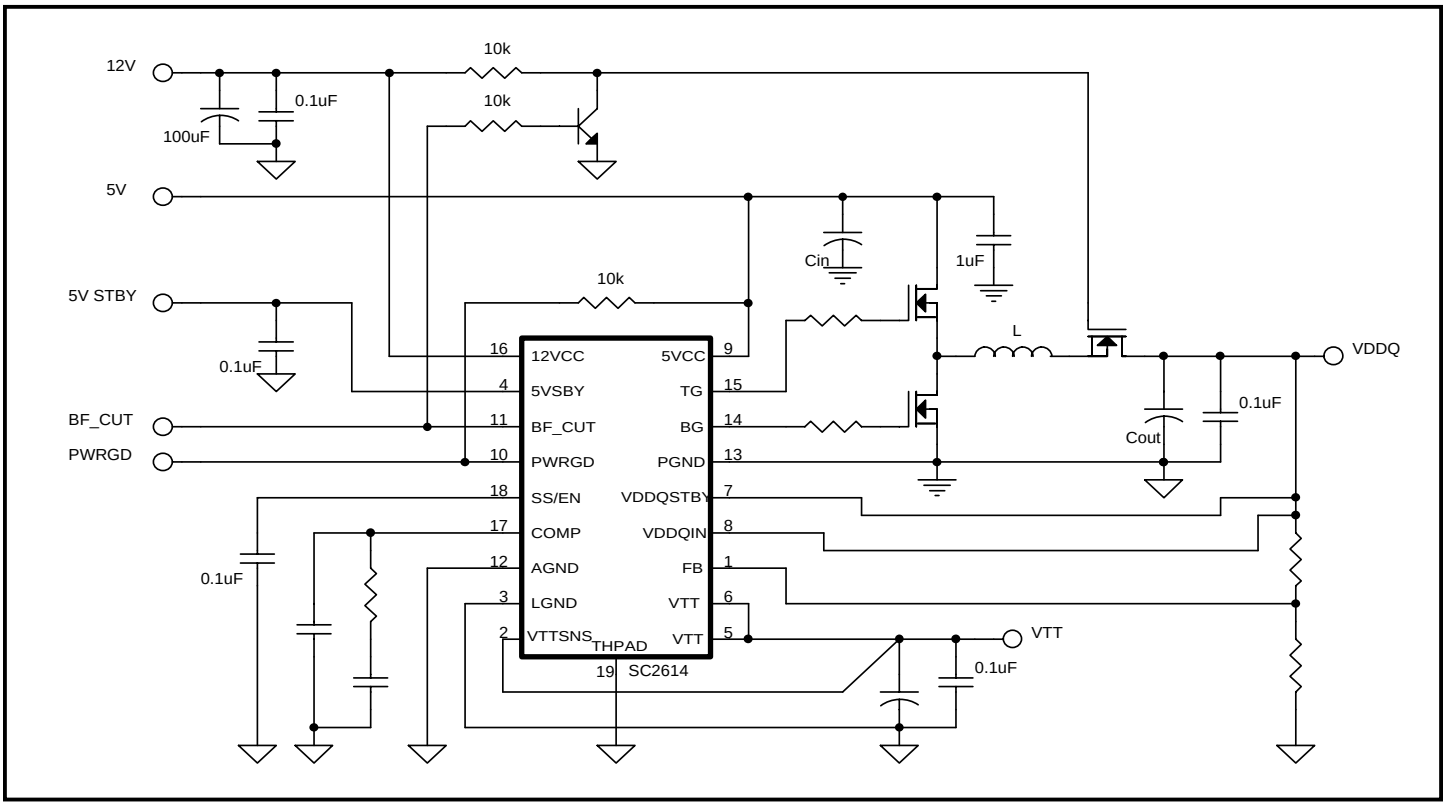
Features

- **Uses Latched BF_Cut from Glue Chip to sequence the three regulators**
- High efficiency (90%) switcher for **VDDQ supplies 20 Amps**
- Single chip solution complies fully with ACPI power sequencing Specifications
- **2 Amp VTT** Source/Sink Capability
- High current gate drives
- **Internal S3 state LDO for VDDQ**
- UVLO on 5V and 12V
- Independent Thermal Shutdown for VDDQ and VTT
- Fast transient response
- 18 pin MLP package

Applications

- Power Solution for DDR memory per Intel ® motherboard specification
- High speed data line termination

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
Supply Voltage, 5VCC to AGND	V_{5VCC}	7	V
Supply Voltage, 12VCC to AGND	V_{12VCC}	15	V
Standby Input Voltage	V_{5VSBY}	7	V
Inputs	I/O	5VSTBY +0.3, AGND -0.3	V
AGND to PGND or LGND		0.3	V
VTT Output Current	$I_{O(VTT)}$	+/- 2	A
Operating Ambient Temperature Range	T_A	0 to 70	°C
Operating Junction Temperature	T_J	125	°C
Thermal Resistance Junction to Ambient *	θ_{JA}	25	°C/W
Thermal Resistance Junction to Case *	θ_{JC}	4	°C/W
Storage Temperature Range	T_{STG}	-65 to 150	°C
TG/BG DC Voltage		12Vcc + 0.3, AGND -0.5	V
TG/BG AC Voltage		12Vcc + 1.0, AGND -1.0	V
ESD Rating (Human Body Model)	ESD	2	kV

* See Mounting Considerations.

Electrical Characteristics

Unless specified: T_A = 25°C, 12VCC = 12V, 5VCC = 5V, 5VSBY = 5V.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
5V Supply Voltage	V_{5VCC}		4.5	5	5.5	V
12V Supply Voltage	V_{12VCC}		10.8	12	13.2	V
5V Standby Voltage	V_{5VSBY}		4.5	5	5.5	V
Quiescent Current	$I_{Q(5VSBY)}$	BF_CUT low		1.8	2.5	mA
		BF_CUT High		3.5	5.0	
BF_CUT Threshold				TTL		V
12VCC Under Voltage Lockout	$UVLO_{12VCC}$		7	8.2	10	V
5VCC Under Voltage Lockout	$UVLO_{5VCC}$		3.5	3.7	4	V
Feedback Reference	V_{REF}			1.25		V
Feedback Current	I_{FB}	V_{FB} = 1.25V			2	uA
SS/EN Shutdown Threshold	$V_{EN(TH)}$			0.3		V

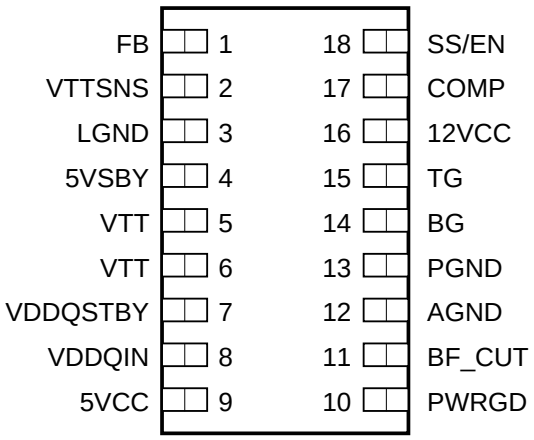
Electrical Characteristics (Cont.)

Unless specified: T_A = 25°C, 12VCC = 12V, 5VCC = 5V, 5VSBY = 5V.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Thermal Shutdown	T_{J-SHDN}			150		°C
Thermal Shutdown Hysteresis	T_{J-HYST}			10		°C
Switcher						
Load Regulation		I_{VDDQ} = 0A to 10A		0.2		%
Oscillator Frequency	f_{OSC}		225	250	275	KHz
Soft Start Current	I_{SS}			25		uA
Duty Cycle			0		80	%
Overcurrent Trip Voltage	V_{TRIP}	% of VDDQ Setpoint	50	60	70	%
Top Gate Rise Time	TG_R	Gate capacitance = 4000pF		25		nS
Top Gate Fall Time	TG_F	Gate capacitance = 4000pF		25		nS
Bottom Gate Rise Time	BG_R	Gate capacitance = 4000pF		35		nS
Bottom Gate Fall Time	BG_F	Gate capacitance = 4000pF		35		nS
Dead Time	t_d		20	50		nS
Error Amplifier Transconductance	gm			0.8		mS
Error Amplifier Gain @ DC	A_{EA}	R_{COMP} = open		38		dB
Error Amplifier Bandwidth	G_{BW}			5		MHz
Error Amplifier Source/Sink Current				+/-60		uA
Modulator Gain	A_M	V_{IN} = 5V		19		dB
Power Good Low		I_{PWRGD} = 1mA, sink		50	400	mV
Power Good High Leakage		V_{PWRGD} = 5V; BF_CUT = 0		0.1	2	uA
STBY LDO						
Output Current	$I_{VDDQSTBY}$		750			mA
Load Regulation	$\Delta V/\Delta I$	I_{VDDQ} = 0A to 650mA		0.5		%
Current Limit	I_{LIM}	BF_CUT = high, VTT floating		1		A
VTT LDO						
Output Voltage	VTT	V_{VDDQ} = 2.500V	1.235	1.250	1.265	V
Source and Sink Currents	I_{VTT}		+/-1.8			A
Load Regulation	$\Delta VTT/\ \Delta I$	I_{VTT} =+1.8A to -1.8A			+/- 1	%
Error Amplifier Gain	A_{EA_VTT}			75		dB
Current Limit	VTT_{ILIM}	BF_CUT = low		3		A

Pin Configuration

TOP VIEW



(18 Pin MLP)

Note: Pin19 is the thermal Pad on the bottom of the device

Ordering Information

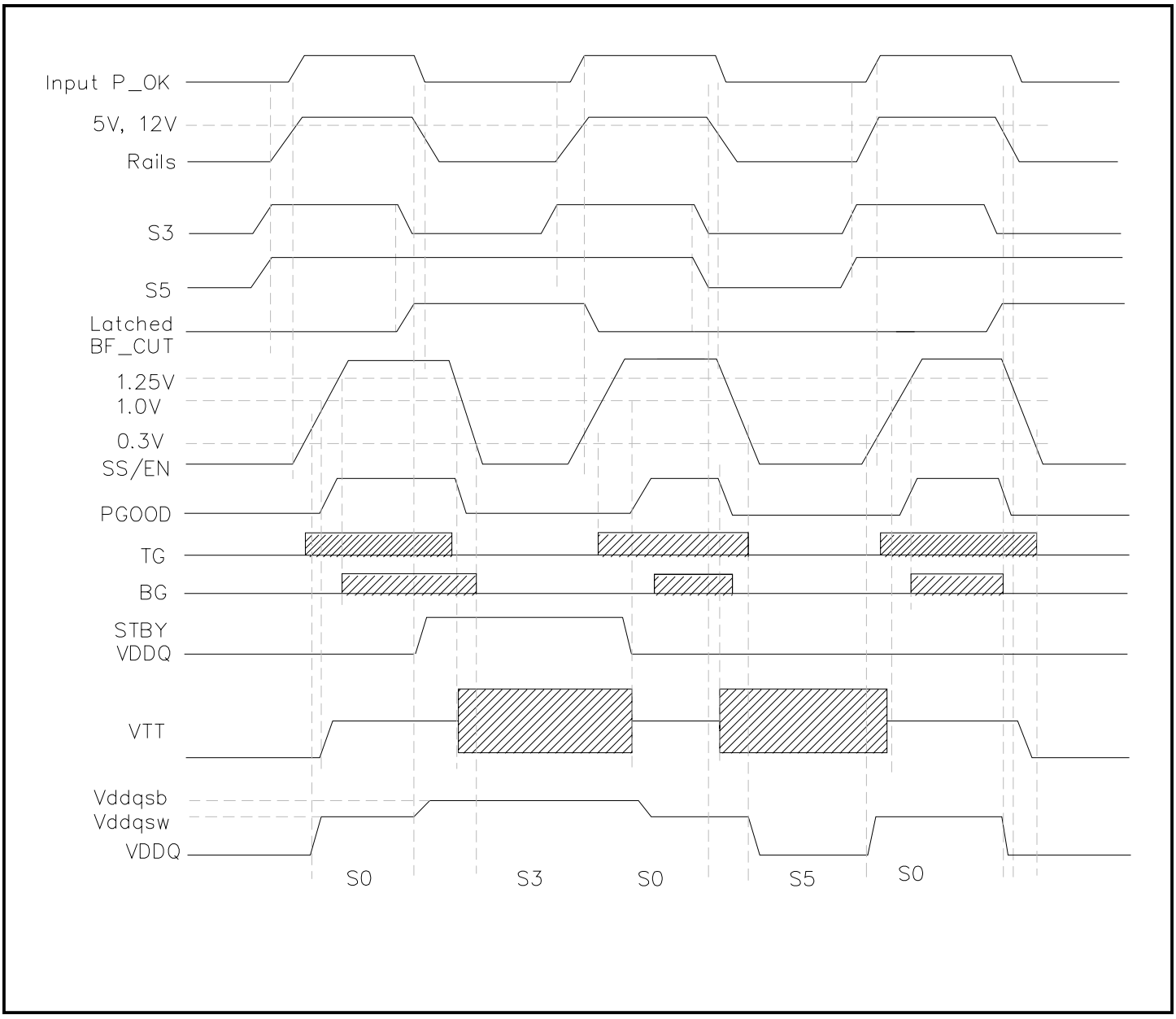
Part Numbers	Package
SC2614MLTR(1)	MLP-18

Notes:
(1) Only available in tape and reel packaging. A reel contains 3000 devices.

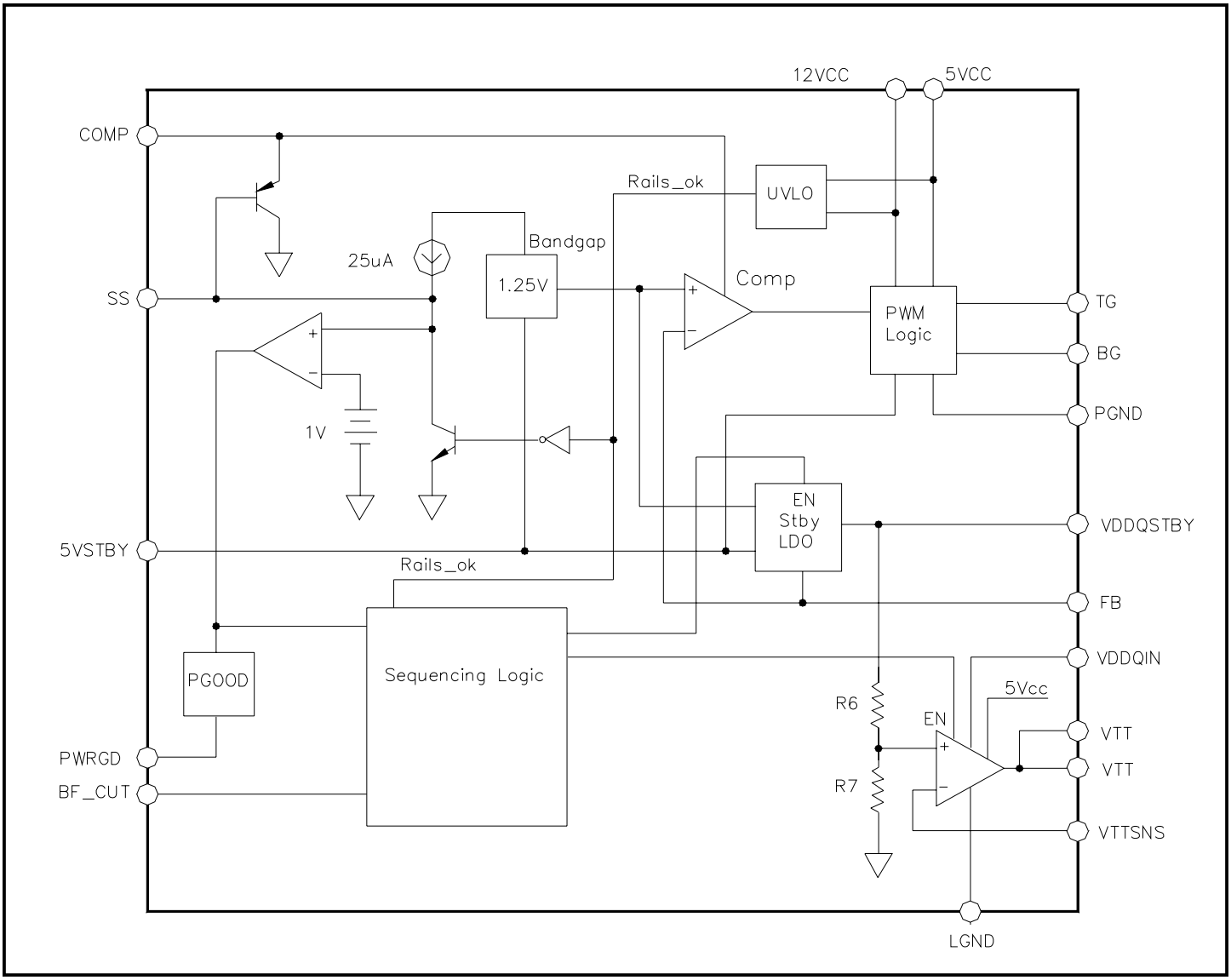
Pin Descriptions

Pin #	Pin Name	Pin Function
1	FB	Feedback for the STBY LDO and the switcher for VDDQ.
2	VTTSNS	VTT LDO feedback and remote sense input.
3	LGND	VTT return. Connect to point of load return. The trace connecting to this pin must be able to carry 2 Amps.
4	5VSBY	Bias supply for the chip. Connect to 5V standby.
5, 6	VTT	Regulator output. Regulates to 1/2 VDDQ. Sources or sinks current. 2 Amp source capability.
7	VDDQSTBY	S3 VDDQ output.
8	VDDQIN	VDDQ power input to VTT LDO. Must carry 2 Amps.
9	5VCC	Supply to the lower gate drive.
10	PWRGD	Switcher powergood and internal enable to VTT LDO.
11	BF_CUT	This pin will enable the STBY LDO in S3.
12	AGND	Analog ground.
13	PGND	Gate drive return. Keep this pin close to bottom FET source.
14	BG	Bottom gate drive.
15	TG	Top gate drive.
16	12VCC	Supply to the upper and lower gate drives.
17	COMP	Compensation pin for the PWM transconductance amplifier.
18	SS/EN	Soft start capacitor to GND. Pull low to disable.
19	TH_PAD	Internally Connected to AGND.

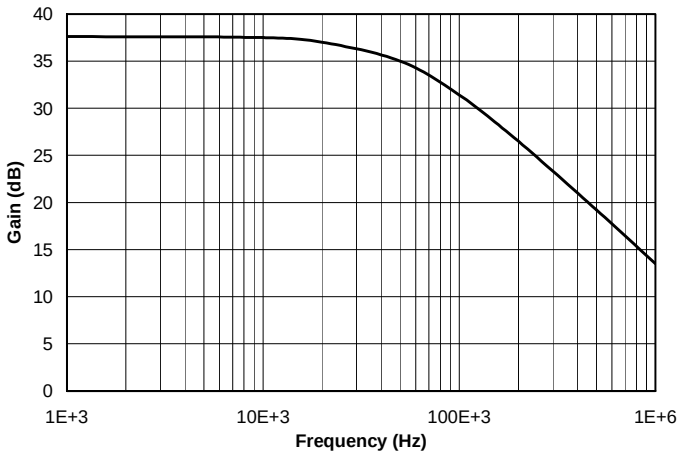
Timing Diagram



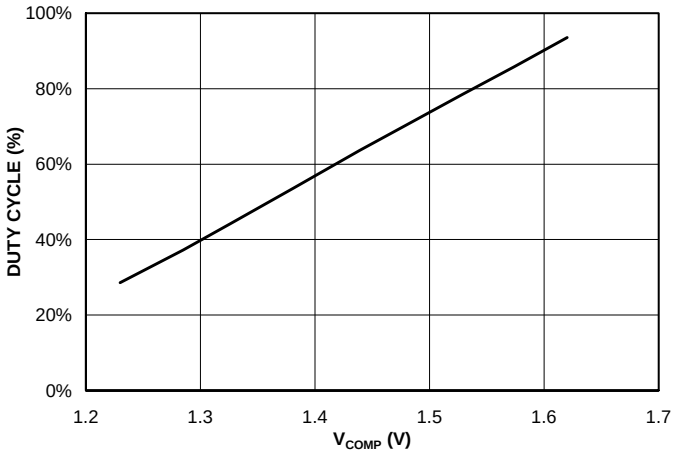
Block Diagram



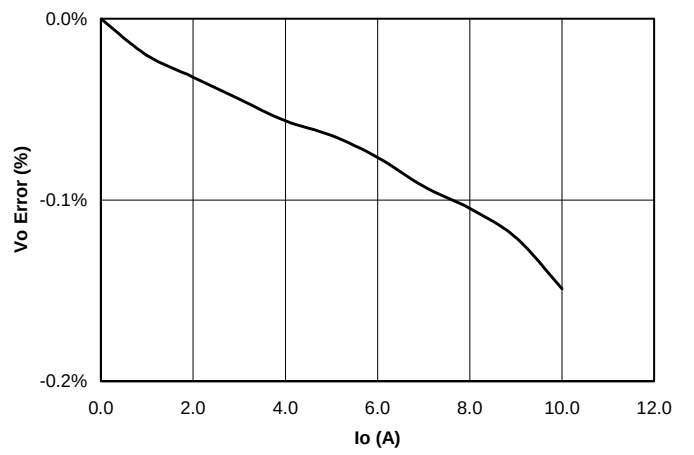
Typical Characteristics



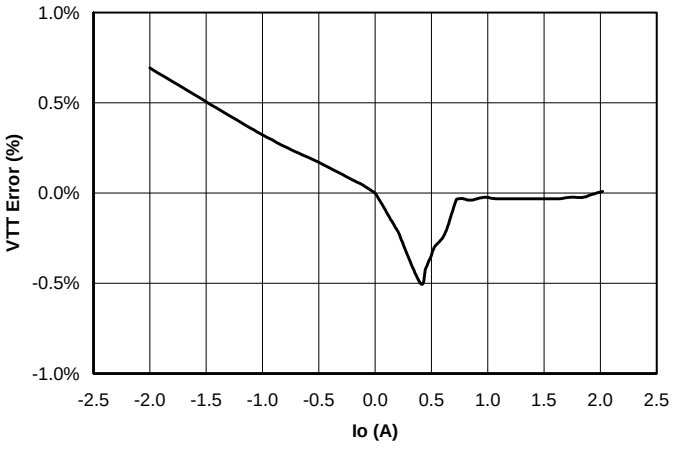
Switching Section Error Amplifier Gain



VCOMP vs Duty Cycle



VDDQ Load Regulation



VTT Load Regulation, Source and Sink

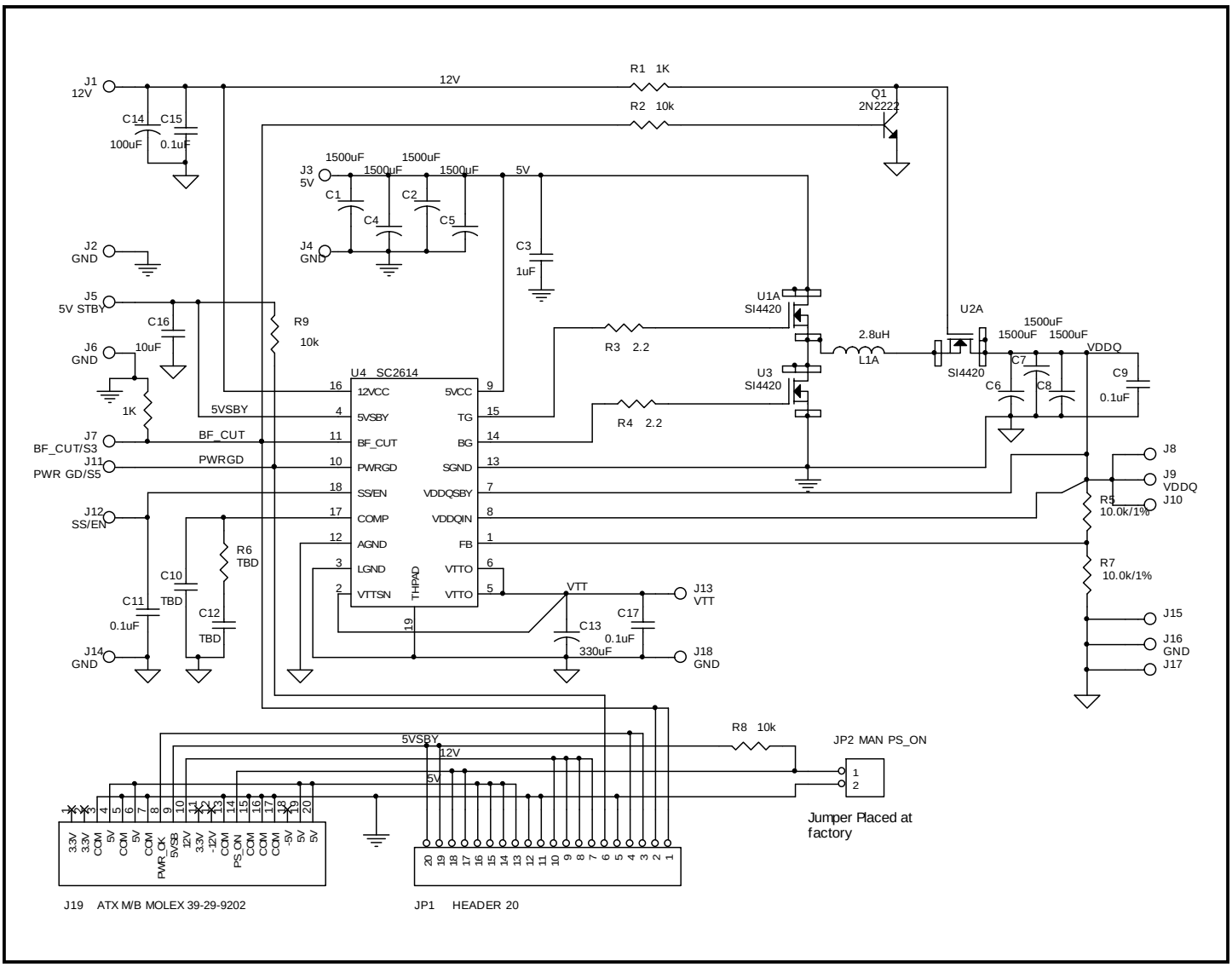


Figure 2: Evaluation Board Schematic

Applications Information

Description

The Semtech SC2614 DDR power supply controller is the latest and most complete, three in one, switching and linear regulator, providing the necessary functions to comply with S3 and S5 sleep state signals generated by the Desktop Computer Motherboards. The SC2614 uses the **BF_CUT** input signal which is generated externally on Intel P4 Motherboard glue chip to comply with the power sequencing requirements.
Logically, the BF_CUT signal can be represented as:

BF_CUT=S0 .NAND.P_OK

Where S0 is the state of the operation, S0=high for S0 and Low for S3. P_OK is a signal generated by the Silverbox supply, indicating that all rails are within specification .

The BF_CUT signal is inverted to drive a **Back_Feed_Cut** MOSFET. The **Back_Feed_Cut** MOSFET prevents current flow from the VDDq supply back to the 5V supply during S3 state (when BF_CUT is high). VDDQ supply and the VTT termination voltages are supplied to the Memory bus during S0 (normal operation).
During S0, VDDQ is supplied via the Switching regulator, sourcing high output currents to the VDD bus which in turn sources the termination supply current. The SC2614 is capable of driving a 4000pf capacitor in 25ns (typical, top gate). This drive capability allows 15-20A DC load on the VDDQ supply.
The VTT termination voltage is an internal sink/source linear regulator, which during S0 state receives its power from the VDDQ bus. It is capable of sourcing and sinking 2 Amps (max). The current limit on this pin is set to 3 Amps (typical). The current handling capacity of this pin depends upon the amount of heat the PC board can sink from the SC2614 thermal pad. (See mounting instructions). The PC board layout must take into consideration the high current paths, and ground returns for both the VDDQ and VTT supply pins. VTT, LGND, VDDQ, 5VCC and PGND traces must also be routed using wide traces to minimize power loss and heat in these traces, based on the current handling requirements.

S3 and S5 States

During S3 and S5 sleep states, The BF_CUT signal is pulled high (see the timing diagram). The operation of the VDDQ and VTT supplies is governed by the internal sequencing logic in strict adherence with intel™ specifications with regards to the BF_CUT sgnal. The timing diagram demonstrates the state of the controller, and each of the VDDQ and VTT supplies during S3 and S5 transitions. When S3 is low, the VDDQ supplies the "Suspend To RAM" current of 650 mA (max) to maintain the information in memory while in standby mode. The VTT termination voltage is not needed during this state, and is thus tri-stated. Once BF_CUT goes low, the VDDQ switcher recovers and takes control of the VDDQ supply voltage.
The SS/EN pin must be pulled low and high again to restart the SC2614. This can be achieved by cycling the input supplies, 5V or 12V.

Initial Conditions

With the S5 and S3 go high (BF_CUT goes low) for the first time, the VDDQ is supplied by the Switcher, thus removing the burden of charging the output capacitors via the linear VDDQ regulator.

Back-feeding the Input Supply

When in S3 state, VDDQ is supplied by the linear regulator and current can flow back from the VDDQ supply through the body diode of the Top switching MOSFET to the 5V supply in the Silver Box. Since the 5VCC is off during this state, this back flow of current in effect shorts out the VDDQ supply and is not desirable.

The blocking MOSFET is driven from the inverted BF_CUT signal, as shown in figure 2 (Evaluation Board Schematic). When the gate voltage for this series MOSFET is low, the current can not flow from the VDDQ supply back into the input power source.

Current Limit

Current limit is implemented by sensing the VDDQ voltage If it falls to 60% off its nominal voltage, as sensed by the FB pin, the TG and BG pins are latched off and the switcher and the linear controllers are shutdown. To

recover from the current limit condition, either the power rails, 5VCC /12VCC have to be recycled, or the SS/EN pin must be pulled low and released to restart switcher operation.

Thermal Shutdown

There are three independent Thermal Shutdown protection circuits in the SC2614: The VDDQ linear regulator, the VTT source regulator, and the VTT sink regulator. If any of the three regulators' temperature rises above the threshold, that regulator will turn off independently, until the temperature falls below the thermal shutdown limit.

Power Good

An open collector output provides indication that the VDDq switcher is in regulation. This is accomplished by monitoring the SS/EN pin. When the voltage on this pin has risen above 1.0V, PGOOD goes high (open). When BF_CUT goes high (standby), the 5V and 12V rails go low, and the SS/EN also goes low. Subsequsntly, PWRGD will also go low, and stays low until the 5V and 12V rails are recycled and rise above their respective UVLO thresholds.

Compensation Components -

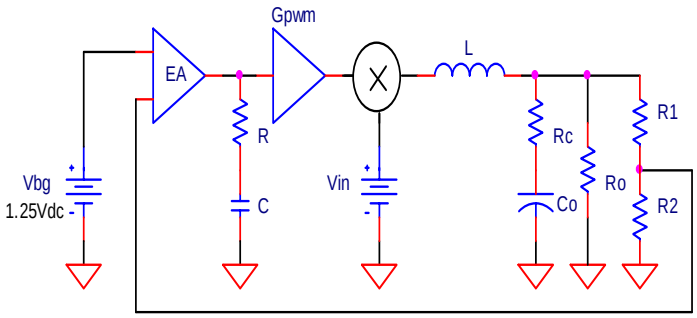


Fig. 1. SC2614 control model.

The control model of SC2614 can be depicted in Fig. 1. This model can also be used in Spice kind of simulator to generate loop gain Bode plots. The bandgap reference is 1.25 V and trimmed to +/-1% accuracy. The desired output voltage can be achieved by setting the resistive divider network, R1 and R2.

The error amplifier is transconductance type with fixed gain of:

$$G_m := \frac{0.0008\,A}{V}$$

The compensation network includes a resistor and a capacitor in series, which terminates from the output of the error amplifier to the ground.

This device uses voltage mode control with input voltage feed forward. The peak-to-peak ramp voltage is proportional to the input voltage, which results in an excellent performance to reject input voltage variation. The PWM gain is inversion of the ramp amplitude, and this gain is given by:

$$G_{pwm} := \frac{1}{V_{ramp}}$$

where the ramp amplitude (peak-to-peak) is 0.55 volts when input voltage is 5 volts.

The total control loop-gain can then be derived as follows:

$$T(s) = T_o \cdot \left(\frac{1 + s \cdot R \cdot C}{s \cdot R \cdot C}\right) \cdot \frac{1 + s \cdot R_c \cdot C_o}{1 + s \cdot \left(R_c \cdot C_o + \frac{L}{R_o}\right) + s^2 \cdot L \cdot C_o \cdot \left(1 + \frac{R_c}{R_o}\right)}$$

where

$$T_o := G_m \cdot G_{pwm} \cdot V_{in} \cdot R \cdot \left(\frac{V_{bg}}{V_o}\right)$$

The task here is to properly choose the compensation network for a nicely shaped loop-gain Bode plot. The following design procedures are recommended to accomplish the goal:

(1) Calculate the corner frequency of the output filter:

$$F_o := \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C_o}}$$

(2) Calculate the ESR zero frequency of the output filter capacitor:

$$F_{esr} := \frac{1}{2 \cdot \pi \cdot R_c \cdot C_o}$$

(3) Check that the ESR zero frequency is not too high.

$$F_{esr} < \frac{F_{sw}}{5}$$

If this condition is not met, the compensation structure may not provide loop stability. The solution is to add some electrolytic capacitors to the output capacitor bank

Applications Information (Cont.)

to correct the output filter corner frequency and the ESR zero frequency. In some cases, the filter inductance may also need to be adjusted to shift the filter corner frequency. It is not recommended to use only high frequency multi-layer ceramic capacitors for output filter.

(4) Choose the loop gain cross over frequency (0 dB frequency). It is recommended that the crossover frequency is always less than one fifth of the switching frequency :

$$F_{x\_over} \le \frac{F_{sw}}{5}$$

If the transient specification is not stringent, it is better to choose a crossover frequency that is less than one tenth of the switching frequency for good noise immunity. The resistor in the compensation network can then be calculated as:

$$R := \frac{1}{G_{pwm} \cdot V_{in} \cdot G_m} \cdot \left(\frac{F_{esr}}{F_o}\right)^2 \cdot \left(\frac{F_{x\_over}}{F_{esr}}\right) \cdot \left(\frac{V_o}{V_{bg}}\right)$$

when

$$F_o < F_{esr} < F_{x\_over}$$

or

$$R := \frac{1}{G_{pwm} \cdot V_{in} \cdot G_m} \cdot \left(\frac{F_o}{F_{esr}}\right)^2 \cdot \left(\frac{F_{x\_over}}{F_o}\right) \cdot \left(\frac{V_o}{V_{bg}}\right)$$

when

$$F_{esr} < F_o < F_{x\_over}$$

(5) The compensation capacitor is determined by choosing the compensator zero to be about one fifth of the output filter corner frequency:

$$F_{zero} := \frac{F_o}{5}$$

$$C := \frac{1}{2 \cdot \pi \cdot R \cdot F_{zero}}$$

(6) The final step is to generate the Bode plot, either by using the simulation model in Fig. 1 or using the equations provided here with Mathcad. The phase margin can then be checked using the Bode plot. Usually, this design procedure ensures a healthy phase margin.

An example is given below to demonstrate the procedure introduced above. The parameters of the power supply are given as:

$V_{in} := 5\ V$

$V_o := 2.5\ V$

$I_o := 20\ A$

$F_{sw} := 250\ KHz$

$L := 3\ \mu H$

$C_o := 6600\ \mu F$

$R_c := 0.006\ \Omega$

$R_1 := 1.0\ K\Omega$

$R_2 := 1.0\ K\Omega$

Step 1. Output filter corner frequency

$F_o = 1.13\ KHz$

Step 2. ESR zero frequency:

$F_{esr} = 4.019\ KHz$

Step 3. Check the following condition:

$$F_{esr} < \frac{F_{sw}}{5}$$

Which is satisfied in this case.

Step 4. Choose crossover frequency and calculate compensator R:

$F_{x\_over} = 50\ KHz$

$R = 43.197\ K\Omega$

Step 5. Calculate the compensator C:

$C = 16.287\ nF$

Step 6. Generate Bode plot and check the phase margin. In this case, the phase margin is about 85°C that ensures the loop stability. Fig. 2 shows the Bode plot of the loop.

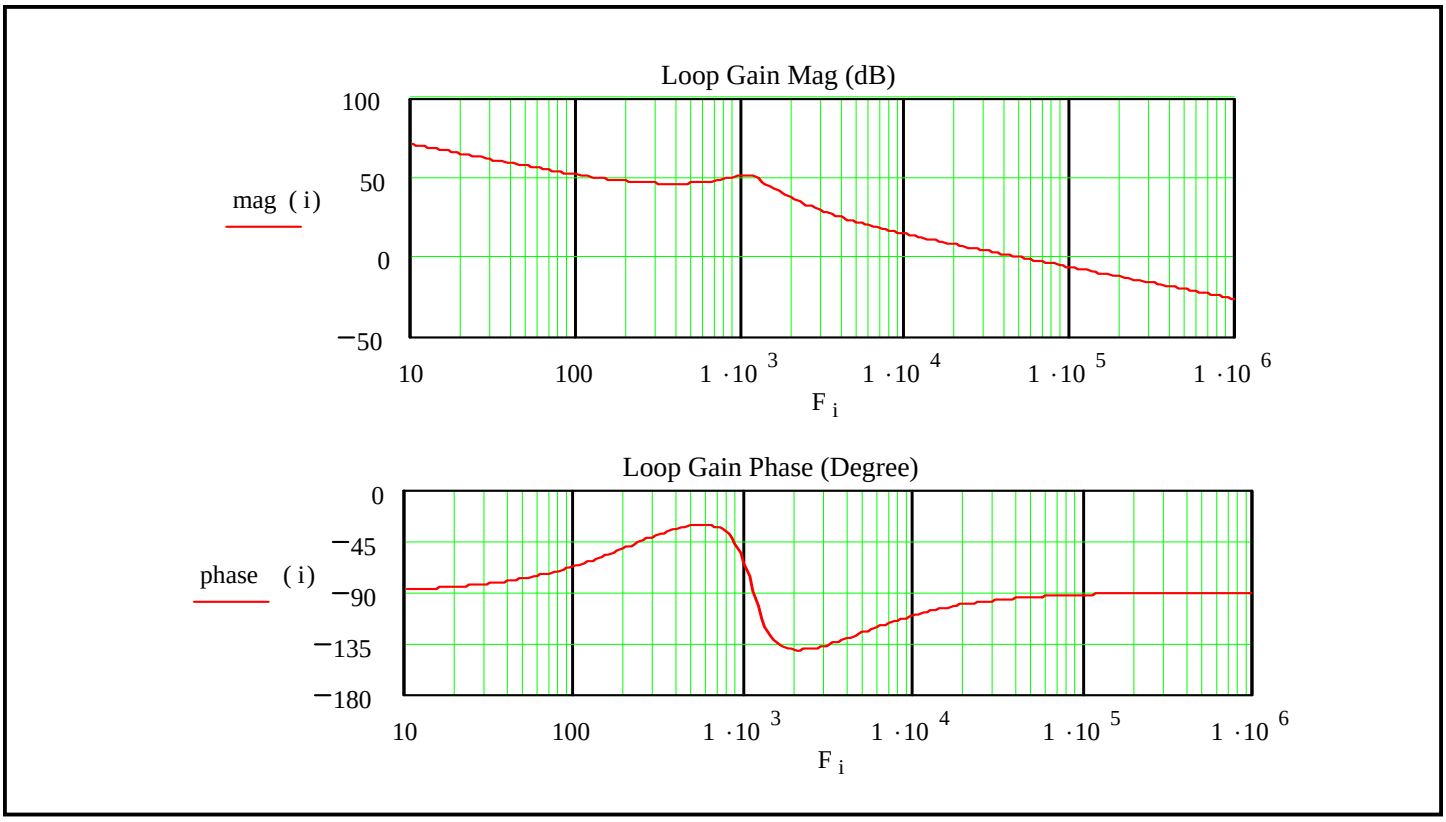


Fig. 2. Bode plot of the loop

Mounting Considerations

Description

The MLP18 is a leadless package whose electrical connections are made by lands on the bottom surface of the component. These lands are soldered directly to the PC board. The MLP has an exposed die attach pad, which enhances the thermal and electrical characteristics enabling high power applications. Power handling capability of the MLP package is typically >2x the power of other common SMT packages, such as the TSSOP and SOIC packages. In order to take full advantage of this feature the exposed pad must be physically connected to the PCB substrate with solder.

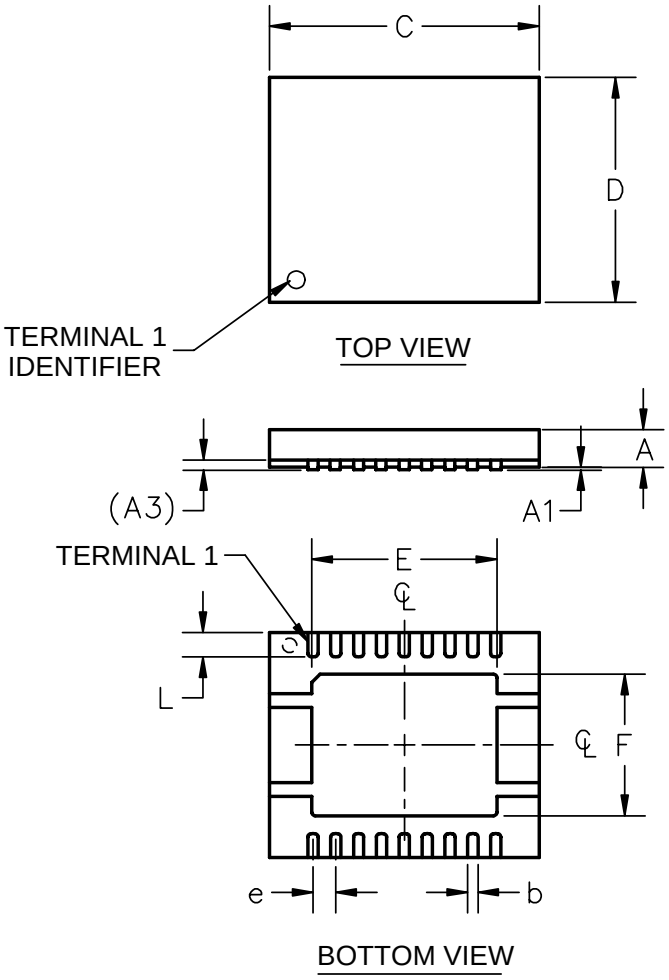
Thermal Pad Via Design

Thermal data for the MLP18 is based on a 4 layer PCB incorporating vias which act as the thermal path to other layers. (Ref: Jedec Specification JESD 51-5). Based on thermal performance, four-layer PCB's with vias are recommended to effectively remove heat from the device. Vias should be 0.3mm diameter on a 1.2mm pitch, and should be plugged to prevent voids being formed between the exposed pad and PCB thermal pad due to solder escaping by capillary action. Plugging can be accomplished by "tenting" the via during the solder mask process. The via solder mask diameter should be 100µm larger than the via diameter.
Two layer boards have less copper and thus typically require an increase in the PC board area for effective heatsinking. The copper area immdiately surrounding the thermal pad connection must not be interupted by routing traces.

Exposed Pad Stencil Design

It is good practice to minimize the presence of voids within the exposed pad inter-connection. Total elimination is difficult but the design of the exposed pad stencil is important, a single slotted rectangular pattern is recommended. (If large exposed pads are screened with excessive solder, the device may "float", thus causing a gap between the MLP terminal and the PCB land metalization.) The proposed stencil designs enables out-gassing of the solder paste during reflow as well as controlling the finished solder thickness.

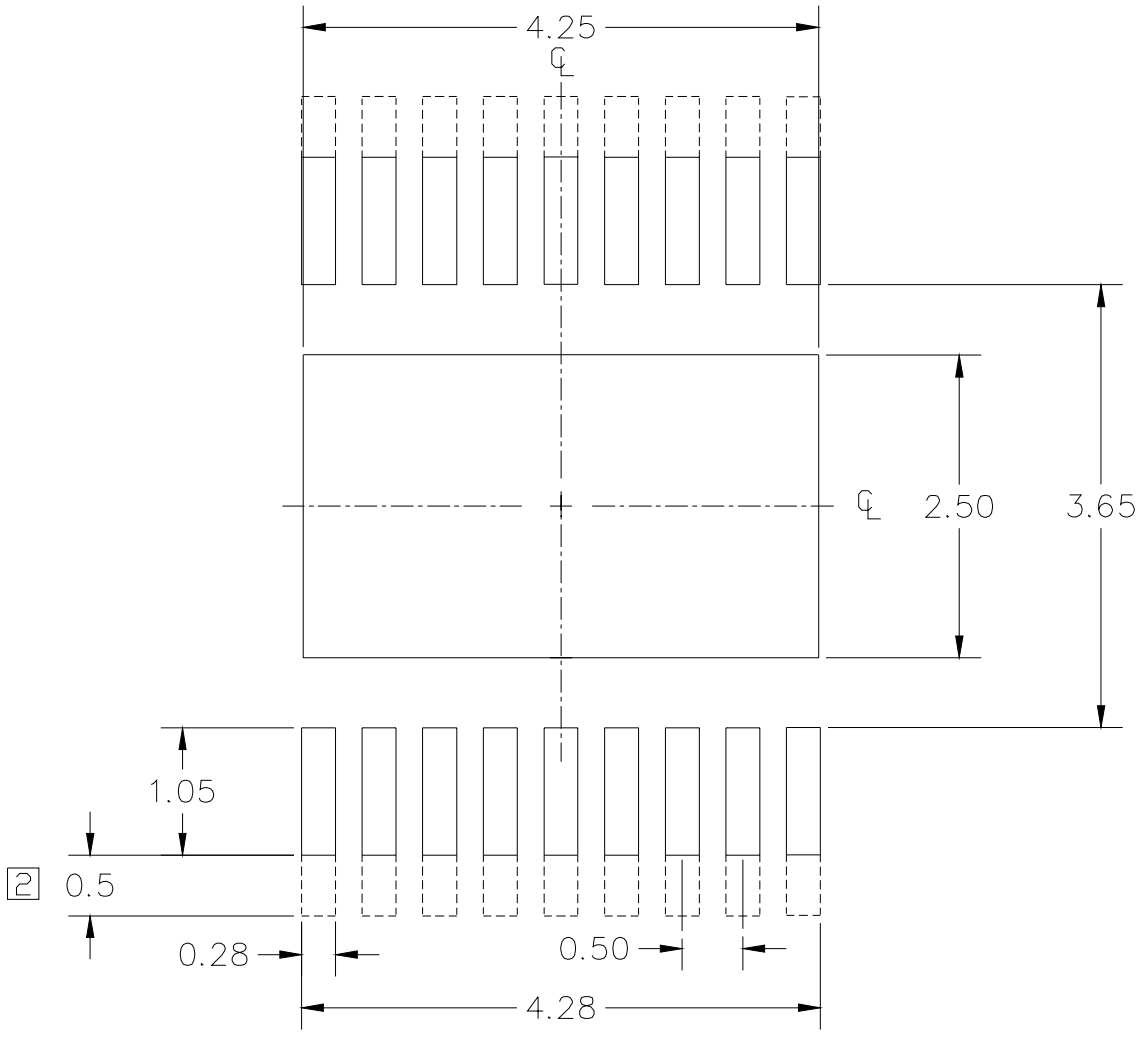
Outline Drawing - MLP-18



DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.032	.039	0.80	1.00	–
A1	0	.002	0	0.05	–
A3	–	.008	–	0.20	REF
b	.007	.012	0.18	0.30	–
C	.236		6.00		NOM
D	.197		5.00		NOM
E	.157	.167	4.00	4.25	–
F	.118	.128	3.00	3.25	–
e	.020 BSC		0.50 BSC		–
L	.017	.026	0.45	0.65	–

[1] CONTROLLING DIMENSIONS: MILLIMETERS

Land Pattern - MLP-18



2 PAD LENGTHS MAY BE EXTENDED BY DASHED LINE DIMENSIONS FOR EASE OF REWORK.

1 CONTROLLING DIMENSIONS: MILLIMETERS.

Contact Information

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